Microelectronic Products Data Book

Issue 3

MITEL® SEMICONDUCTOR

Table of Contents

Table of Contents

Table of Contents (cont'd)

4.0 Analog Telecom Components

5.0 ST-BUS™ Family of ISDN Components

Table of Contents (cont'd)

General Information

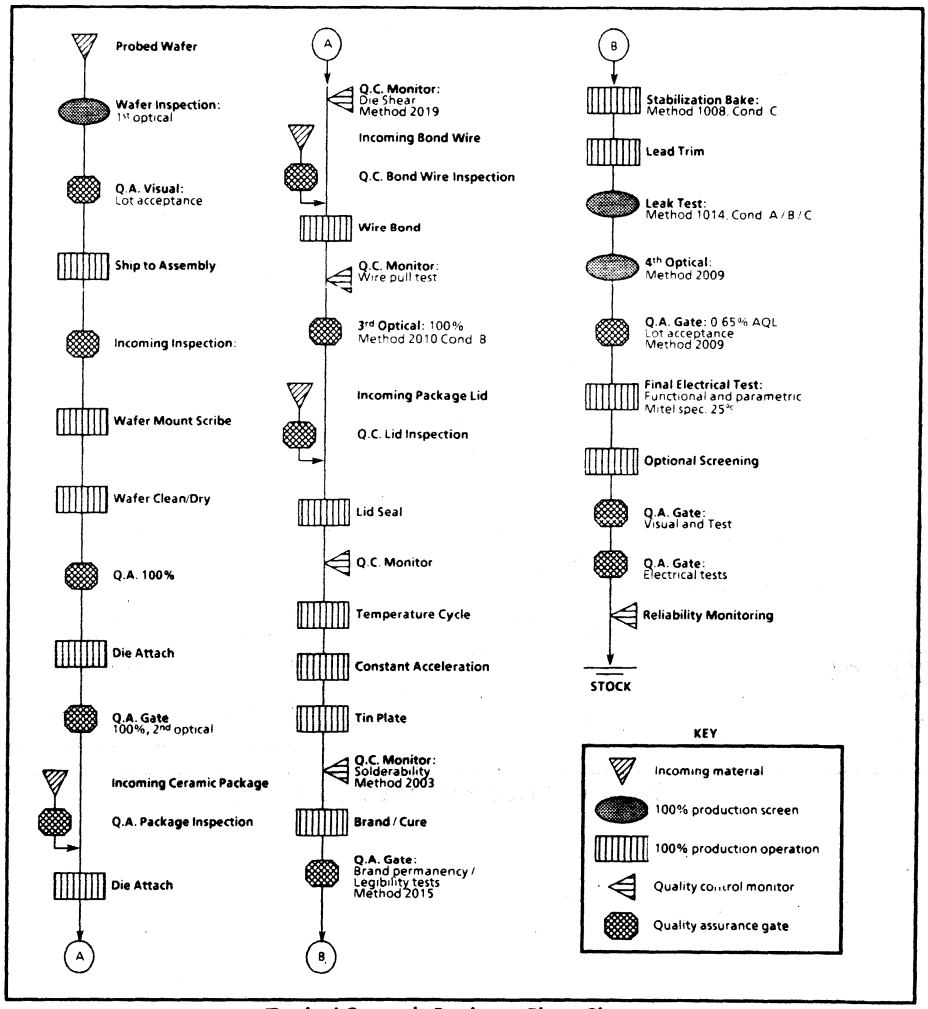
Quality and Reliability

Quality Control in Action

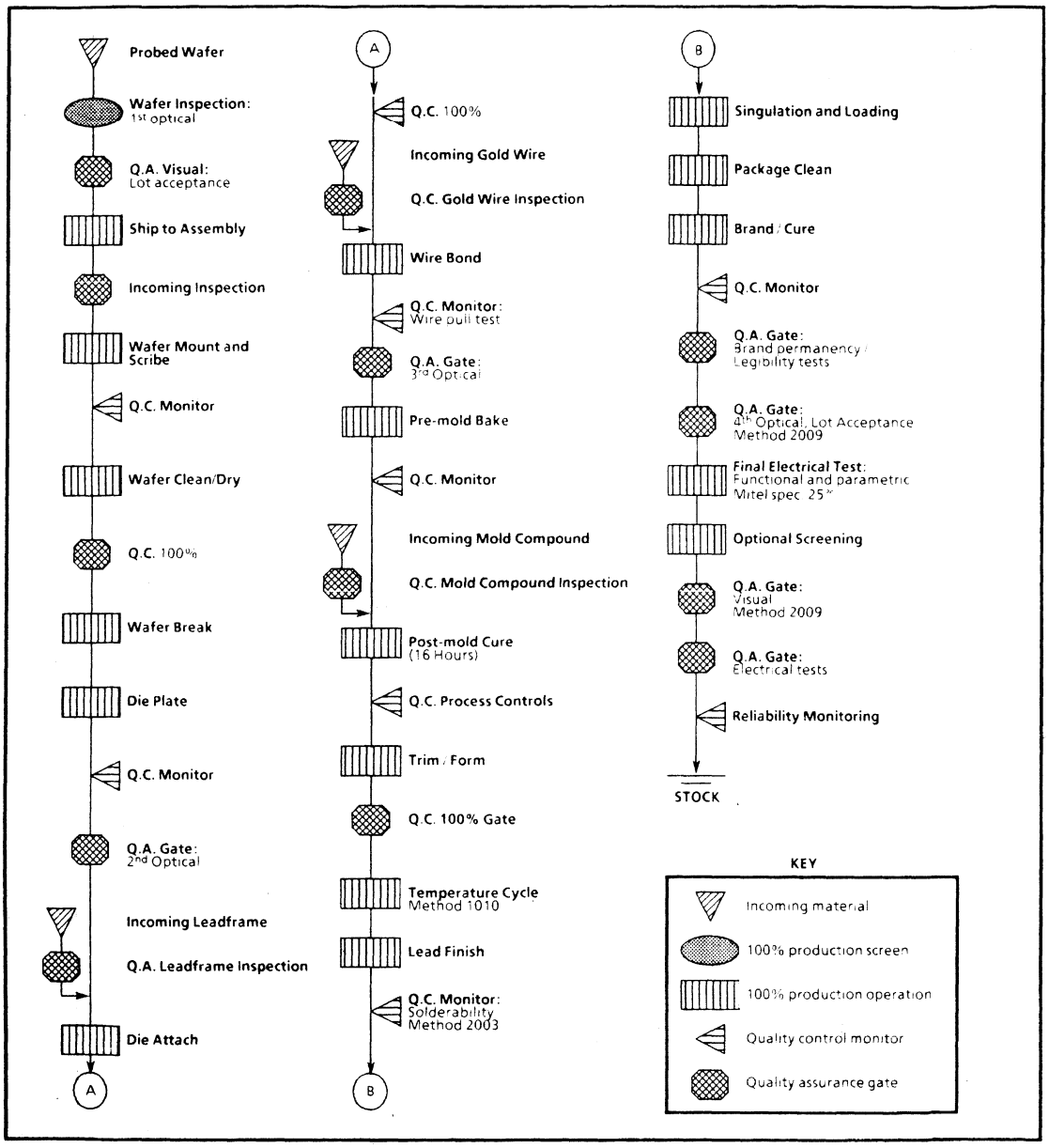
The final quality and reliability of Mitel Semiconductor products are governed by strict production controls and quality assurance monitors which are exercised during the manufacturing process. International standards are used for production methods, test methods and quality screening procedures.

Devices are 100% electrically tested and released for shipmant after outgoing quality control tests have been preformed.

Detailed documentation enables batch traceability from the finished tested device back to the raw material.A reliability assurance program includes life and enviromental testing and detailed failure analysis to provide further ongoing monitors of production quality as well as the data essential for lifetime prediction. The following two flowcharts illustrate the production process and location of QC gates for ceramic and plastic packages.



Typical Ceramic Package Flow Chart



Typical Plastic Package Flow Chart

MITEL SEMICONDUCTOR

During the last decade, Mitel has participated in virtually all aspects of the semiconductor industry: as an innovative designer of telecommunications components and digital devices, as a pioneer of the ISO-CMOS process, and as a participant in the merchant components market. Increasingly, companies need to obtain custom and semi-custom devices to survive in today's highly competitive market. Mitel offers the following range of services and facilities to design engneers for co-operative production of custom and semi-custom devices.

Design

The Mitel wafer foundry accepts customer's designs in the form of a database tape, Pattern Generation (PG) tape, or a set of photo-masks.

Mitel Semiconductor supplies design rules and electrical parameters to customers who have the resources to produce their own design tooling.

Full design services are available through design houses such as Pacific Microcircuits Limited, a Mitel-affiliated design house. Complete information about this service is available upon request.

Wafer Foundry

This state-of-the-art facility comprises:

- A 9500 square foot production area consisting of class 100 clean room modules.
- A 5000 square foot process development area.

The foundry currently processes silicon gate, P-well CMOS wafers in 5-, 4-, and 3-micron geometries, and is compatible with a number of other major foundries. Double layer polysilicon is available on all processes, and there are a number of processes that can support double level metalizations.

A 2-micron process using direct step-on wafer technology is available for prototyping. Process options include two poltsilicon layers and two metalization layers.

A 9-micron metal gate CMOS process is offered for high voltage alppications.

Fabrication equipment includes medium and high current implanters, plasma etching equipment, sputterers and projection alignment. The foundry maintains tight parametric control and consistantly acheives high yields.

Mask Making

In order to acheive optimum yields, and simplify the interface to the foundry, many customers find it convenient to have the Mitel photomask shop prepare their photomasks for their production requirements. The Mitel photomask shop uses optical pattern generation techniques to create high-quality projection master plates from GDS-1 ar GDS-2 database tapes or Mann 3000, Mann 3600 and Emask 2000 PG tapes.

Device Testing

Mitel has available the following equipment for wafer probe and final testing of devices:

- LTX with DX89 or 90 and full DSP capibility
- Fairchild Sentinel and Sentry VII
- Megatest Q2/62

Prototype Packaging

Mitel Semiconductor offers rapid turn-around on prototype packaging and offers a complete choice of hermetic packages.

Packages available are Cerdip, Side-brazed DIP and Leadless chip carrier.

Mitel qualified subcontractors perform plastic packaging for prototyping or high volume assembly.

Customer Service

At Mitel Semiconductor customer service is viewed as one of the major advantages. The throughput commitment that Mitel measures itself against is 4 weeks turnaround in wafer fabrication. Should photomask making be required, or wafer probing, an additional week would be required for each step.

Beyond this, the customer service group in Bromont, Quebec prides itself on the ease of availability of timely information about the position and forcasted due-out date of foundry wafers. Whether by telephone or electronic mail, customers are kept well informed about the progress of their wafers as they move through the fabrication process.

CMOS Process Options

Several process options are available to customers at Mitel depending upon their needs. The process options listed in the following tables are given for guidance only. Many of the parameters can be adjusted to suit customer requirements. For full process specifications, contact a Mitel Sales Office or representative.

CMOS OPTION PROCESS Gate Size: 3 micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.6 - 1.0	0.6 - 1.0
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>10	>10
K'	($\mu A/Volt^2$)	43.5	16.0
Body Effect Coefficient	($Volt^{\frac{1}{2}}$)	0.43	0.53
Effective Channel Length	(μm)	2.4	2.2
Gate Oxide Thickness	(Å)	480	480
Sheet Resistivity	(Ohms/square)	20 - 35	80 - 120
Polysilicon I Gate Resistivity	(Ohms/square)	15 - 30	15 - 30
Polysilicon II Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly I to Poly II Capacitance	($10\text{-}4\ pF/\mu m^2$)	4.8	
Metal Width/Spacing	(μm)	3/3	
Second Layer Metal Option		Yes	
Process Compatibility		GTE, IMP	

CMOS OPTION PROCESS Gate Size: 2.5 micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.6 - 1.0	0.6 - 1.0
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>10	>10
K'	($\mu A/Volt^2$)	47.5	12.4
Body Effect Coefficient	($Volt^{\frac{1}{2}}$)	0.44	0.47
Effective Channel Length	(μm)	1.9	1.9
Gate Oxide Thickness	(Å)	400	400
Sheet Resistivity	(Ohms/square)	20 - 35	80 - 120
Polysilicon I Gate Resistivity	(Ohms/square)	15 - 30	15 - 30
Polysilicon II Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly I to Poly II Capacitance	($10\text{-}4\ pF/\mu m^2$)	5.3	
Metal Width/Spacing	(μm)	3/3	
Second Layer Metal Option		Yes	
Process Compatibility		None	

CMOS OPTION PROCESS Gate Size: 2 micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.5 - 0.9	0.5 - 0.9
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>10	>10
K'	($\mu A/Volt^2$)	53.9	15.7
Body Effect Coefficient	($Volt^{\frac{1}{2}}$)	0.33	0.37
Effective Channel Length	(μm)	1.5	1.3
Gate Oxide Thickness	(Å)	325	325
Sheet Resistivity	(Ohms/square)	70 - 90	150 - 200
Polysilicon I Gate Resistivity	(Ohms/square)	15 - 30	15 - 30
Polysilicon II Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly I to Poly II Capacitance	($10\text{-}4\ pF/\mu m^2$)	6.9	
Metal Width/Spacing	(μm)	2/2.5	
Second Layer Metal Option		Yes	
Process Compatibility		None	

CMOS OPTION PROCESS Gate Size: 5 micron, High Threshold

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.6 - 1.2	0.6 - 1.2
Field Threshold	(Volts)	>18	>18
Breakdown Voltage BV_{dss}	(Volts)	>18	>18
K'	($\mu A/Volt^2$)	26.0	10.0
Body Effect Coefficient	($Volt^{\frac{1}{2}}$)	1.10	0.55
Effective Channel Length	(μm)	3.0	3.4
Gate Oxide Thickness	(Å)	800	800
Sheet Resistivity	(Ohms/square)	18 - 38	40 - 90
Polysilicon I Gate Resistivity	(Ohms/square)	14 - 26	14 - 26
Polysilicon II Resistivity	(Ohms/square)	30 - 80	30 - 80
Poly I to Poly II Capacitance	($10\text{-}4\ pF/\mu m^2$)	6.0	
Metal Width/Spacing	(μm)	5/5	
Second Layer Metal Option		None	
Process Compatibility		AMI	

CMOS OPTION PROCESS Gate Size: 5 micron, Low Threshold

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.4 - 0.9	0.4 - 0.9
Field Threshold	(Volts)	>18	>18
Breakdown Voltage BV_{dss}	(Volts)	>18	>18
K'	($\mu A/Volt^2$)	26.0	10.0
Body Effect Coefficient	($Volt^{\frac{1}{2}}$)	1.10	0.55
Effective Channel Length	(μm)	1.8	2.8
Gate Oxide Thickness	(Å)	800	800
Sheet Resistivity	(Ohms/square)	6 - 14	70 - 110
Polysilicon I Gate Resistivity	(Ohms/square)	14 - 26	14 - 26
Polysilicon II Resistivity	(Ohms/square)	30 - 80	30 - 80
Poly I to Poly II Capacitance	($10\text{-}4\ pF/\mu m^2$)	4.8	
Metal Width/Spacing	(μm)	5/5	
Second Layer Metal Option		None	
Process Compatibility		GTE, Plessey	

CMOS OPTION PROCESS Gate Size: 4 micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.4 - 0.9	0.4 - 0.9
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>15	>15
K'	($\mu A/Volt^2$)	32.0	13.0
Body Effect Coefficient	($Volt^{\frac{1}{2}}$)	0.90	0.45
Effective Channel Length	(μm)	1.6	2.6
Gate Oxide Thickness	(Å)	640	640
Sheet Resistivity	(Ohms/square)	6 - 14	70 - 110
Polysilicon I Gate Resistivity	(Ohms/square)	14 - 26	14 - 26
Polysilicon II Resistivity	(Ohms/square)	30 - 80	30 - 80
Poly I to Poly II Capacitance	($10\text{-}4\ pF/\mu m^2$)	4.8	
Metal Width/Spacing	(μm)	4/4	
Second Layer Metal Option		None	
Process Compatibility		GTE, Plessey	

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1 Oldfield Drive
East Irvine, CA 92718-9208
(714) 768-4444

Anthem Electronics
1040 E. Brokaw Road
San Jose, CA 95131
(408) 295-4200

Anthem Electronics
9369 Carroll Park Drive
San Diego, CA 92121
(619) 453-4871/9005
TWX: 910-335-1515

Pacesetter Electronics
543 Weddell Drive
Sunnyvale, CA 94089
(408) 734-5470
TWX: 910-328-6161

Pacesetter Electronics
5417 East La Palma
Anaheim, CA 92807
(714) 779-5855
TWX: 910-595-1704

Time Electronics
19210 South Van Ness Ave.
Torrance, CA 90501
(213) 320-0880

Northern California

Time Electronics
1339 Moffett Park Drive
Sunnyvale, CA 94086
(408) 734-9888

Counties in California

(Los Angeles & Kern)
Time Electronics
9751 Independence Street
Chatsworth, CA 91311
(818) 998-7200

(San Diego & Imperial)
Time Electronics
8525 Arjons Drive, Suite A
San Diego, CA 92126
(619) 586-1331

(Orange)
Time Electronics
2410 East Cerritos Avenue
Anaheim, CA 92806
(714) 937-0911

Colorado

("Ship to" Address)
Anthem Electronics
373 Inverness Drive, South
Englewood, CO 80112
(303) 790-4500

Time Electronics
7300 South Alton Way
Englewood, CO 80012
(303) 799-8851

North American Distributors (cont'd)

Connecticut

Time Electronics
1701 Milldale Road
Cheshire, CT 06410
(203) 271-3200

Delaware

Mid-Atlantic Electronics
Interstate Industrial Park
Kor-Center East H-1
Bellmawr, NJ 08030
(609) 931-5305

Time Electronics
600 Clark Avenue
King of Prussia, PA 19406
(215) 337-0900

District of Columbia

Time Electronics
9051 Red Branch Road
Columbia, MD 21045
(301) 964-3090

Florida South

Time Electronics
6610 N.W. 21st Avenue
Ft. Lauderdale, FL 33309
(305) 974-4800

Florida North

Time Electronics
4405 Vineland Road
Suite C-15
Orlando, FL 32811
(305) 841-6565

Georgia

QC Southeast, Inc.
6145 B Northbelt Pkwy.
Norcross, GA 30071
(404) 449-9508
1-800-241-0037

Time Electronics
5555 Oakbrook Pkwy.
Suite 535
Norcross, GA 30093
(404) 448-4448

Idaho

Anthem Electronics
5020 148th Avenue N.E.
Redmond, WA 98052
(206) 881-0850

Time Electronics
8601 Willows Road, N.E.
Redmond, WA 98052
(206)882-1600

Illinois

Classic Components
3336 Commercial
Northbrook, IL 60062
(312) 272-9650
TWX: 910-686-4783

Time Electronics
945 Edgewood Drive
Suite G
Wooddale, IL 60191
(312) 350-0610

Illinois (South)

Time Electronics
330 Sovereign Court
St. Louis, MI 63011
(314) 391-6444

L-Comp Inc.
2211 Riverfront Drive
Kansas City, MO 64120-1476
(816) 221-2400

L-Comp Inc.
2550 Harley Drive
Maryland Heights, MO
63043-3563
(314) 291-6200

Indiana

Graham Electronics
133 South Pennsylvania
Indianapolis, IN 46204
(317) 634-8208

Iowa

Industrial Components
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
TWX: 910-576-3135

L-Comp Inc.
2211 Riverfront Drive
Kansas City, MO 64120-1476
(816) 221-2400

L-Comp Inc.
2550 Harley Drive
Maryland Heights, MO
63043-3563
(314) 291-6200

Kansas

L-Comp Inc.
2111 West Harry
Wichita, KS 67213-3253
(316) 265-5100

L-Comp Inc.
2211 Riverfront Drive
Kansas City, MO 64120-1476
(816) 221-2400

Time Electronics
330 Sovereign Court
St. Louis, MI 63011
(314) 391-6444

L-Comp Inc.
2550 Harley Drive
Maryland Heights, MO
63043-3563
(314) 291-6200

Kentucky

Graham Electronics
133 South Pennsylvania
Indianapolis, IN 46204
(317) 634-8208

Louisiana

Quality Components
1005 Industrial Blvd
Sugarland, TX 77478
(713) 240-2255

Time Electronics
2210 Hutton Drive, Suite 101
Carrolton, TX 75006
(214) 241-7411

Time Electronics
10450 Stancliff Blvd.
Suite 110
Houston, TX 77099
(713) 530-0800

Maine

R.C. Components
222 Andover Street (Billing)
3 Upton Street (Shipping)
Wilmington, MA 01887
(617) 657-4310
TWX: 710-347-1743

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(617) 532-6200

Maryland

Time Electronics
9051 Red Branch Road
Columbia, MD 21045
(301) 964-3090

Massachusetts

R.C. Components
222 Andover Street
Wilmington, MA 01887
(617) 273-1860
TWX: 710-347-1743

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(617) 532-6200

Michigan

Time Electronics
945 North Edgewood Drive
Suite G
Wooddale, IL 60191
(312) 350-0610

Graham Electronics
3981 Varsity Drive
Ann Arbor, MI 48106
(313) 971-9093

Minnesota

Industrial Components
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
TWX: 910-576-3135

Time Electronics
7488 West 78th Street
Bloomington, MN 55434
(612) 944-9192

Northern, Inc. (Classic)
6405 Cecilia Circle
Minneapolis, MN 55435
(612) 944-1167

Mississippi

QC Southeast, Inc.
4900 University Square
Huntsville, AL 35805
(205) 830-1881

Time Electronics
5555 Oakbrook Parkway
Suite 535
Norcross, GA 30093
(404) 448-4448

Missouri

L-Comp Inc.
2550 Harley Drive
Maryland Heights, MO
63043
(314) 291-6200
1-800-325-1393

L-Comp Inc.
2211 Riverfront Drive
Kansas City, MO 64120
(816) 221-2400

Time Electronics
330 Sovereign Court
St. Louis, MO 63011
(314) 391-6444

Montana

Time Electronics
7300 South Alton Way
Englewood, CO 80012
(303) 799-8851

Nevada

Anthem Electronics
1727 East Weber Drive
Tempe, AZ 85281
(602) 244-0900
TWX: 910-950-0110

Sterling Electronics Inc.
3501 East Broadway Road
Phoenix, AZ 85040
(602) 268-2121

Nevada (North)

Time Electronics
1339 Moffet Park Drive
Sunnyvale, CA 94086
(408) 734-9888

New Hampshire

R.C. Components
222 Andover Street (Billing)
3 Upton Street (Shipping)
Wilmington, MA 01887
(617) 657-4310
TWX: 710-347-1743

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(617) 532-6200

New Jersey

Mid-Atlantic Electronics
Interstate Industrial Park
Kor Center East H1
Bellmawr, NJ 08030
(609) 931-5305

New Jersey (South)

Time Electronics
600 Clark Avenue
King of Prussia, PA 19406
(215) 337-0900

North American Distributors (cont'd)

New Jersey (North)

Time Electronics
70 Marcus Blvd
Hauppauge, NY 11788
(516) 273-0100

New Mexico

Sterling Electronics Inc.
3540 De Panamerican Hwy.
Albuquerque, NM 87107
(505) 884-1900

Time Electronics
1203 West Geneva Drive
Tempe, AZ 85282
(602) 967-2000

New York

ACI Electronics
200 Newtown Road
Plainview, NY 11803
(516) 293-6630
TWX: 510-224-6550

ADD Electronics
7 Adler Drive
East Syracuse, NY 13057
(315) 437-0300

(Metropolitan & Long Island)

Time Electronics
70 Marcus Blvd.
Hauppauge, NY 11788
(516) 273-0100

Upstate New York

Time Electronics
6075 Corporate Drive
East Syracuse, NY 13057
(315) 432-0355

North Carolina

QC Southeast, Inc.
2940-15 Trawicks Road
Raleigh, NC 27604
(919) 876-7767

Time Electronics
9800-L Southern Pine Blvd.
Charlotte, NC 28210
(704) 522-7600

North Dakota

Industrial Components
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
TWX: 910-576-3135

Time Electronics
7488 West 78th Street
Bloomington, MN 55434
(612) 944-9192

Ohio

Graham Electronics
444 Windsor Park Drive
Dayton, OH 45459
(513) 435-8660

Time Electronics
6175H Shamrock Court
Dublin, OH 43017
(614) 761-1100

Oklahoma

Quality Components Inc.
9934 East 21st Street South
Tulsa, OK 74129
(918) 664-8812

Time Electronics
330 Sovereign Court
St. Louis, MO 63011-4491
(314) 391-6444

Oregon

Anthem Electronics
15812 S.W. Upper Boones
Ferry Road
Lake Oswego, OR 97034
(503) 684-2661

Time Electronics
16125 S.W. 72nd Avenue
Building 2
Portland, OR 97224
(503) 684-3780

Pennsylvania (East)

Time Electronics
600 Clark Avenue
King of Prussia, PA 19406
(215) 337-0900

Mid-Atlantic Electronics
Interstate Industrial Park
Kor-Center East-H-1
Bellmawr, NJ 08030
(609) 931-5305

Rhode Island

R.C. Components
222 Andover Street (Billing)
3 Upton Street (Shipping)
Wilmington, MA 01887
(617) 657-4310
TWX: 710-347-1743

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(617) 532-6200

South Carolina

QC Southeast, Inc.
2940-15 Trawicks Road
Raleigh, NC 27604
(919) 876-7767

Time Electronics
9800-L Southern Pine Blvd.
Charlotte, NC 28210
(704) 522-7600

South Dakota

Industrial Components
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
TWX: 910-576-3135

Time Electronics
7488 West 78th Street
Bloomington, MN 55434
(612) 944-9192

Tennessee

Time Electronics
5555 Oakbrook Parkway,
Suite 535
Norcross, GA 30093
(404) 448-4448

Texas

Quality Components Inc.
4257 Kellway Circle
Addison, TX 75001
(214) 733-4300

Quality Components Inc.
2120M West Braker Lane
Austin, TX 78758
(512) 835-0220

Quality Components Inc.
1005 Industrial Blvd.
Sugarland, TX 77478
(713) 240-2255

Time Electronics
2210 Hutton Drive, Suite 101
Carrolton, TX 75006
(214) 241-7441

Time Electronics
10450 Stancliff Blvd.
Suite 110
Houston, TX 77099
(713) 530-0800

Utah

Anthem Electronics
1615 W. 2200 South, Suite A
Salt Lake City, UT 84119
(801) 973-8555

Time Electronics
7300 South Alton Way
Englewood, CO 80012
(303) 799-8851

Vermont

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(617) 532-6200

Virginia

Time Electronics
9051 Red Branch Road
Columbia, MD 21045
(301) 964-3090

Washington

Anthem Electronics
5020 148th Avenue, N.E.
Redmond, WA 98052
(206) 881-0850

Time Electronics
8601 Willows Road, N.E.
Redmond, WA 98052-3411
(206) 882-1600

Wisconsin

Classic Components
2925 S. 160th Street
New Berlin, WI 53151
(414) 786-5300

Wyoming

Time Electronics
7300 South Alton Way
Englewood, CO 80012
(303) 799-8851

CANADA

Alberta

Zentronics
3300-14th Avenue N.E.
Bay #1
Calgary, Alberta
T2A 6J4
(403) 272-1021
1-800-372-9504

Deskin Sales
3504 78th Avenue
Edmonton, Alberta
T6B 2X9
(403) 466-2106
TWX: 610-831-1660

Deskin Sales
339-10th Avenue S.E.
Calgary, Alberta
1-800-661-1935
T2G 0W2
TWX: 610-821-7394

British Columbia

Zentronics
11400 Bridgeport Road
Unit 108
Richmond, British Columbia
V6X 1T2
(604) 273-5575
TELEX: 04-507789

Deskin Sales
105-3830 Jacombs Road
Richmond, British Columbia
V6V 1Y6
(604) 273-4963
TWX: 610-922-5036

Manitoba

Zentronics
590 Berry Street
Winnipeg, Manitoba
R3H 0S1
(204) 775-8661

Deskin Sales
P.O. Box 173
Transcona, Manitoba
R2C 2Z9
(0) Zenith 06009
(403) 466-2106
TWX: 610-641-9508

North American Distributors (cont'd)

Nova Scotia

Deskin Sales
East Mountain Road
R.R. #2 Truro, Nova Scotia
B2N 5B1
(902) 893-9228

Ontario

Zentronics
8 Tilbury Court
Brampton, Ontario
L6T 3T4
(416) 451-8445
TELEX: 06-97678

Zentronics
564/10 Weber Street
Waterloo, Ontario
N2L 5C6
(519) 884-5700

Zentronics
155 Colonnade Road, South
Unit 17 & 18
Nepean, Ontario
K2E 7K1
(613) 226-8840

Deskin Sales
155 Clayton Drive
Markham, Ontario
L3R 5T9
(416) 475-1412
TELEX: 06-966559
TWX: 610-492-5113

Deskin Sales
880 Lady Ellen Place
Suite 106
Ottawa, Ontario
K1Z 5L9
(613) 729-1099
TWX: 610-421-3793

Deskin Sales
519 Westheights Drive
Kitchener, Ontario
N2N 1M6
(519) 743-1702

Quebec

Zentronics
817 McCaffrey Street
Ville St. Laurent, Quebec
H4T 1N3
(514) 737-9700
TELEX: 05-824826

Deskin Sales
290 Benjamin Hudon
Montreal, Quebec
H4N 1J4
(514) 331-2860
TWX: 610-421-3793
TELEX: 05-827584

International Distributors/Representatives

Argentina

YEL S.R.L.
Cangallo 1454, Piso 8 of.41
(1037) Buenos Aires,
Argentina
Phone: 46 2211
Telex: 18605

Australia

Benmar International
Pty. Ltd.
Level 59, MLC Centre CNR
King and Castlereagh Streets
Sydney N.S.W. 2000 Australia
G.P.O. Box 4048
Sydney N.S.W. 2001 Australia
Phone: (02) 233-7939

China

Chinam Associates Ltd.
Block C-1, 12th Floor
Hong Kong Industrial Centre
491 Castle Peak Road
Kowloon, Hong Kong
Phone: 3 7441186
Telex: 37644 SPSHK HX
Cable: SPEEDYHKG

Hong Kong

Draco International Ltd.
Rm. 2609 Shun Tak Centre
Office Tower, 200
Connaught Re.
Central, Hong Kong
Phone: 5-594591
Fax: 5-493405
Telex: 80539 DRACO HX

India

Balcorp (India) Pvt. Ltd.
921 Maker Chambers V
Nariman Point
Bombay 40002, India
Phone: 23-03-19
Telex: 81-112009 BIPL-IN

Indonesia

P.T. Centronix
26 Jalan Matraman Jakarta
13150
Indonesia
Phone: 884187
Telex: 48421

Israel

Vectronics
60 Medinat Hayehudim St.
P.O.B. 2024 Herzlia B 46120
Israel
Phone: 972 52 556070
Telex: 342579
Fax: 972-52-556508

Japan

Tokyo Electron Limited
Shinjuku Nomura Bldg.
1-26-2 Nishi-Shinjuku
Shinjuku-ku, Tokyo 160,
Japan
Phone: 03 343 4411
Telex: 720232220
Fax: 03-344-6094 "or"
03-343-6778

Korea

Duksung Trading Company
Room 301, Jinwon Bldg.
507-30 Sinrim Dong,
Gwanak-Ku,
Seoul, Korea
Phone: 854-5047, 854-5831
862-6713
Telex: K23459 DUKSUNG
Fax: 02-862-1985

Mexico

Mitel do Mexico
Av. Oleoducto #2810
Parque Industrial El Alamo
44490 Guadaljara
Jalisco, Mexico
ADPO. Postal 91-081
Phone: 397520-356834-
356876

New Zealand

G.T.S. Engineering Ltd.
52 Broadway Newmarket
P.O. Box 9613
Auckland, New Zealand
Phone: 456-745, 543, 214
Telex: 60430

Singapore

DOS Electronis Pte Ltd.
80 Genting Lane
#02-09 Genting Block
Ruby Industrial Complex
Singapore 1334
Republic of Singapore
Phone: 743312-3
Telex: RS35382
Fax: 7447653

Taiwan

Fairply Enterprises Inc.
P.O. Box 8-199, Taipei
Rm 602, 6th Floor, No. 63,
Sec. 2
Chang An East Road
Taipei, Taiwan
Republic of China
Phone: 541-6135, 541-6133
537-4802
Telex: 24685 FAIRWOOD
Cable: FAIRWOOD TAIPEI

European Distributors/Representatives

Austria

Codico GMBH & Co. KG
Aspettenstrasse 48
A-2380 Perchtoldsdorf bei Wien
Nat: 0222 86 24 28
Int: + 48 222 86 24 28
Telex: 134413 CODI A
Fax: + 43 222 86 32 5

Belgium

Betea Sa
Chausee de Louvain 775
B 1140 Bruxelles
Nat: 02 736 80 50
Int: + 32 2 736 80 50
Telex: 23188 BETEA B

Denmark

Advanced Electronic of Denmark
Mariendalsvej 55
DK 2000 Copenhagen
Nat: 01 19 44 33
Int: + 45 1 19 44 33
Telex: 22431 ADVEL DK

Finland

Komdel Oy
Ph 52, Meteorinkadu No 3
02211 Espoo 21
Nat: 90 885 011
Int: + 358 0 885 011
Telex: 121926 KOMDL SF
Fax: + 358 0 885 327

France

Miel Sarl
60 rue de Wattignies
75012 Paris
Nat: 01 43 42 92 07
Int: + 33 1 43 42 92 07
Telex: 213005 MADAX F

Germany

Atlantik Electronik GMBH
Fraunhoferstrasse 11A
D 8033 Martinsried
Munich
Nat: 089 85 72 086
Int: + 49 89 85 72 086
Telex: 5215111 ALEC D
Fax: + 49 89 85 3702

Beka Electronic GMBH
Bahnhofstr 42
D-2000 Wedel
Nat: 041 038 4061
Int: + 49 41 038 4061
Telex: 2189582 BEKA D

Fest & Pohl Elektronik GMBH
Dominicusstrasse 32
D-1000 Berlin 62
Nat: 030 784 1078
Int: + 49 30 784 1078
Telex: 186232 FEPO D

Holland

Benco Telecomponents
Benelux BV
Kievietslaan 13
2243 GB Wassenaar
Netherlands
Nat: 01751 77 338
Int: + 31 1751 77 338
Telex: 8950511 ONEONE G
(UK) Attn 14681001 (Relay)

Ireland

Electronics 2000 Ltd.
Pye Complex
Dundrum
Dublin 16
(see also UK)
Nat: 01 98 62 40
Int: 0001 98 62 40 (from UK)
Telex: 93654 PYE EI

Italy

Celte Srl
via Teodosio 13
20131 Milano
Nat: 02 29 62 95
Int: + 39 2 29 62 95
Telex: 334360 ELECOM I

Claitron S p A
via gallarate
211-20151 Milano
Nat: 02 30 10 091
Int: + 39 2 30 10 091
Telex: 313843

Norway

Elektronix A/S
Odinsgate 21
0266 Oslo 2
Nat: 02 55 90 50
Int: + 47 2 55 90 50
Telex: 72738 ELNIX N

Portugal

Teleprinta
Comercio e Tecnologia Electronica Lda
Rua Ferreira Lapa, 35, r/c
100 LISBOA
Nat: 19 548 423
Int: + 351 19 548 423
Telex: 14899 PRINTA P

South Africa

Promilect (Pty) Ltd.
P.O. Box 56310
Pinegowrie
2123 South Africa
Nat: 011 789 14 00
Int: + 27 11 789 14 00
Telex: 420452 RADIOKOM SA

Spain

Compania Electronica di Technicas Applicodas SA
Emilio Munoz 41,
Nave 1-1-2
28037 Madrid
Nat: 01 754 30 01
Int: + 34 1 754 30 01
Telex: 42007 CETA E

Sweden

Lagercrantz Elektronik ab
Box 716
S-194 27 Upplands Vasby
Nat: 0760 861 20
Int: + 46 760 861 20
Telex: 11275
Fax: + 46 760 318 40

Switzerland

Egli Fischer & Company Ltd.
Gotthardstrasse 6
8022 Zurich
Nat: 01 209 81 11
Int: + 41 1 209 81 11
Telex: 815535 EFZ CH
Fax: + 41 1 209 22 75

Turkey

Barkey
Sanayi Malzemelevi
Buyukdere CAD., No. 20/5
P.K. 667 Sisli
Istanbul
Nat: 01 148 91 47
Int: + 90 1 148 91 47
Telex: 27843 HEN TR
Fax: + 90 1 131 11 29

United Kingdom

Pronto Electronic Systems Ltd.
City Gate House
399-425 Eastern Avenue
Gants Hill
Ilford
Essex IG2 6LK
Nat: 01 554 6222
Int: + 44 1 554 6222
Telex: 8954213 PRONTO G
Fax: 01 518 3222

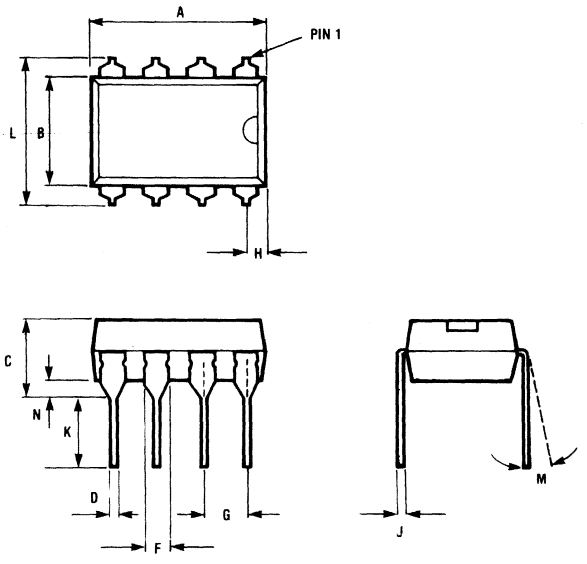
Online Distribution Ltd.
Melbourne House
Kingsway
Bedford MK42 9AZ
Nat: 0234 217 915
Int: + 44 234 217 915
Telex: 827665 ONDIST G
Fax: 0234 216631

Electronics 2000 Ltd.
Grafton House
Grafton Street
High Wycombe
Bucks HP12 3AJ
(see also Ireland)
Nat: 0494 44 40 44
Int: + 44 494 44 40 44
Telex: 838808 TRONIC G

Alternate Source Guide to MITEL Components

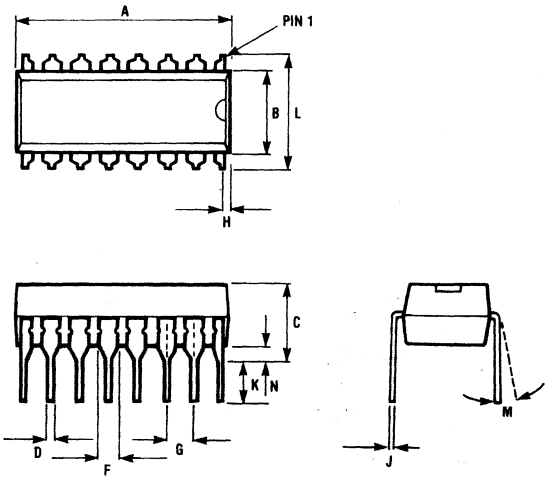
MITEL PART NUMBER	ALTERNATE SOURCE	ALTERNATE PART NUMBER
MD4332	Mostek Plessey Sanyo	MK4332 MV4332 STK4332
MD65SC22	GTE Rockwell UMC VTI Gen Micro Intech	G65SC22 *R6522 *UM6522 *VL6522 *GMS6522 *SY6522
MD65SC51B	AMI GTE AMI Hitachi Motorola Panasonic Rockwell UMC VTI	S65SC51 G65SC51 *S6551 *HM6551 *AN6551 *R6551 *UM6551 *UM6551 *VL6551
MD68SC21	AMI Hitachi Motorola MCR Systems Thompson	*S6821 *HD6821 *MC8621 *MBK6821 *EF6821
MD68SC40	AMI Hitachi Motorola Thompson	*S6840 *HD8640 *MC8640 *EF6840
MD68SC49B	AMI	S68SC49B
MT4320	Plessey	MV4320
MT4325	Plessey	MV4325
MT3530B	AMI Harris	S3530 HC3530
MT35212A	AMI Reticon Sierra Exar	S35212A RM5632A SC11004 XR2120
MT35213	AMI	S35213
MT8804	Plessey	MV8804
MT8812	SGS	M093
MT8860	GTE Plessey	G8860X MV8860
MT8865	GTE Plessey	G8865X MV8865
MT8975	AMI	S8975
MT8978	AMI	S8978
MT8940	AMI	S8940
MT8970	AMI	S8970
MT8980	AMI	S8980
MT8981	AMI	S8981

* These devices are fully compatible, but are not CMOS versions.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.91	0.350	0.390
B	6.10	6.60	0.240	0.260
C	4.19	5.21	0.165	0.205
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	1.27	0.010	0.050
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

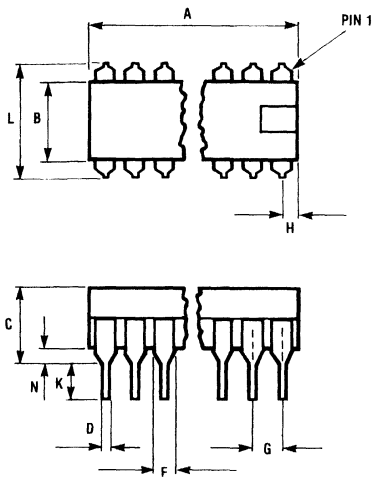
8-Lead Dual-In-Line Plastic (E Suffix)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.34	22.10	0.840	0.870
B	6.10	6.60	0.240	0.260
C	4.19	5.21	0.165	0.205
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	2.29	0.010	0.090
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

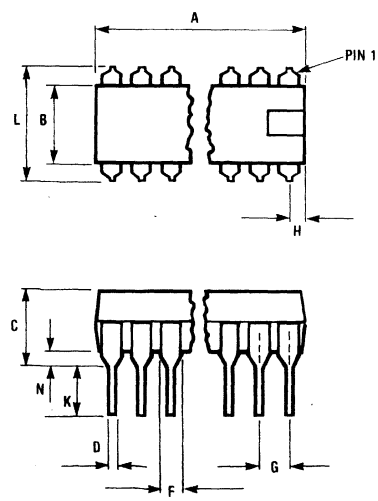
16-Lead Dual-In-Line Plastic (E Suffix)

Package Outlines



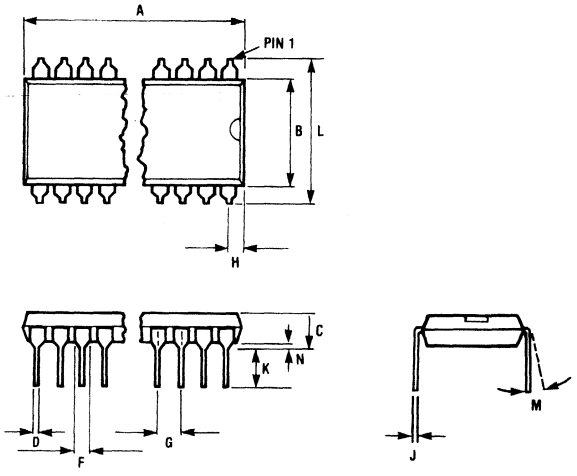
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.23	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	4.19	5.08	0.165	0.200
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	2.29	0.010	0.090
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

18-Lead Dual-In-Line Plastic (E Suffix)



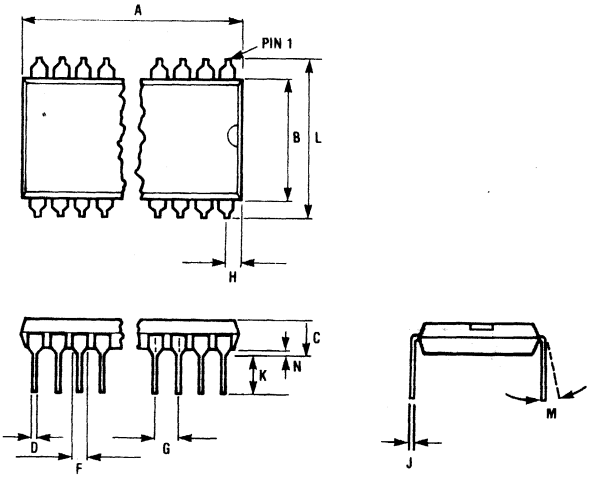
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.42	26.92	1.040	1.060
B	6.10	6.60	0.240	0.260
C	4.19	5.21	0.165	0.205
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	2.29	0.010	0.090
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 TYP		0.300 TYP	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

20-Lead Dual-In-Line Plastic (E Suffix)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	4.19	5.21	0.165	0.205
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	2.29	0.010	0.090
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

22-Lead Dual-In-Line Plastic (E Suffix)

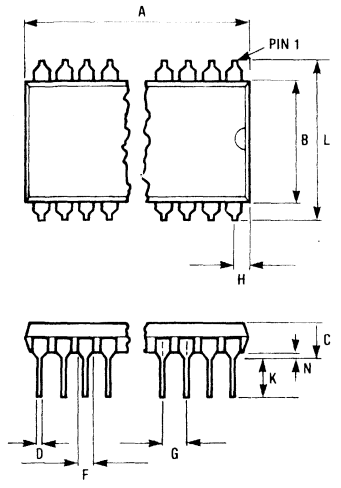


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.19	5.21	0.165	0.205
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	2.29	0.010	0.090
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

5300

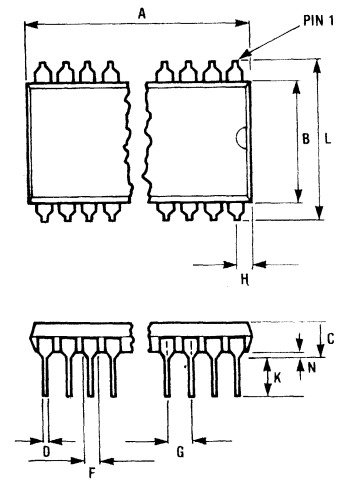
24-Lead Dual-In-Line Plastic (E Suffix)

Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	4.19	5.21	0.165	0.205
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	2.29	0.010	0.090
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

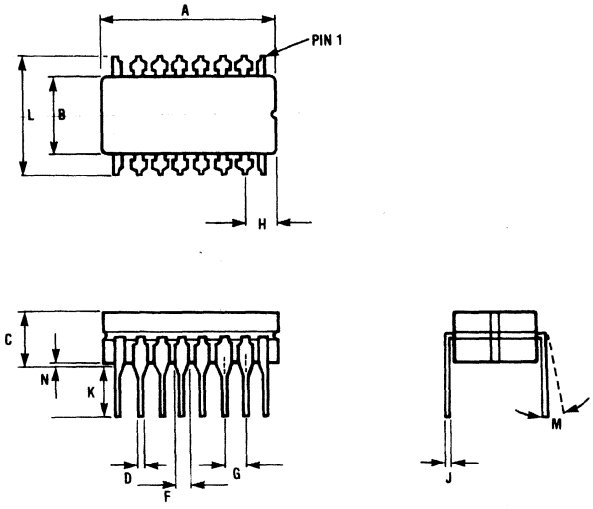
28-Lead Dual-In-Line Plastic (E Suffix)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	4.19	5.21	0.165	0.205
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	0.25	2.29	0.010	0.090
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

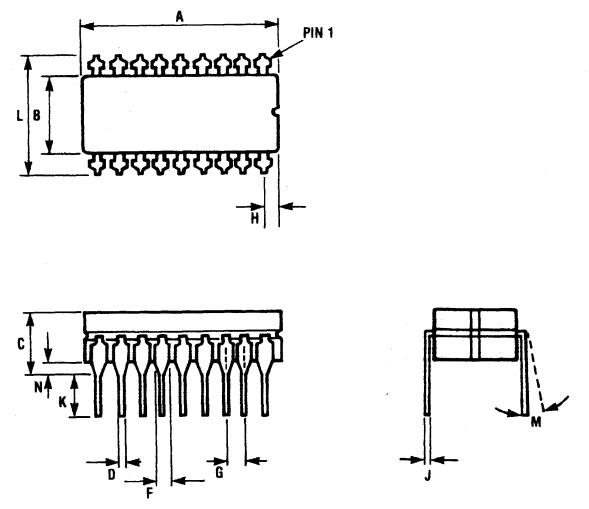
5299

40-Lead Dual-In-Line Plastic (E Suffix)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.13	20.00	0.753	0.787
B	6.73	7.39	0.265	0.291
C	4.17	5.74	0.164	0.226
D	0.41	0.51	0.016	0.020
F	1.14	1.78	0.045	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	1.65	0.015	0.065
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.64	1.60	0.025	0.063

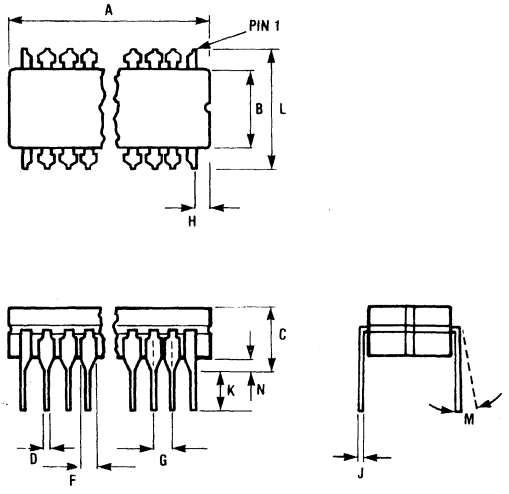
16-lead CERDIP (C Suffix)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.41	23.32	0.882	0.918
B	7.24	7.39	0.285	0.291
C	4.17	5.69	0.164	0.224
D	0.41	0.51	0.016	0.020
F	1.14	1.78	0.045	0.070
G	2.54 BSC		0.100 BSC	
H	0.64	2.41	0.025	0.095
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.64	1.60	0.025	0.063

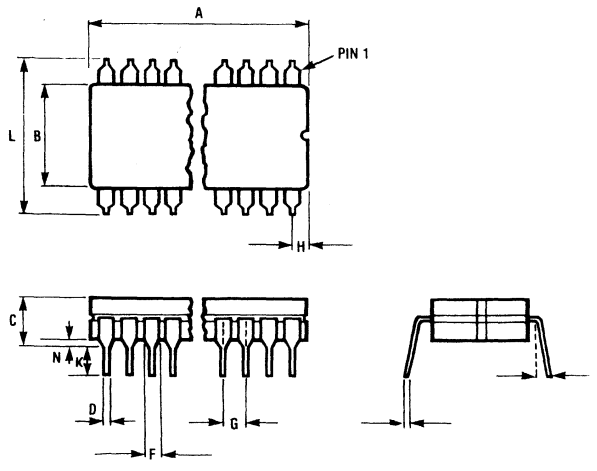
18-Lead CERDIP (C Suffix)

Package Outlines



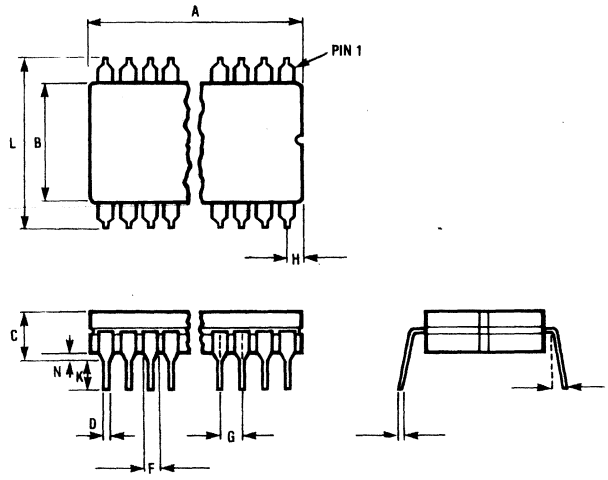
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.93	25.35	0.942	0.998
B	6.91	7.39	0.272	0.291
C	4.17	5.82	0.164	0.229
D	0.41	0.51	0.016	0.020
F	1.14	1.78	0.045	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.16	0.015	0.085
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.64	1.60	0.025	0.063

20-Lead CERDIP (C Suffix)



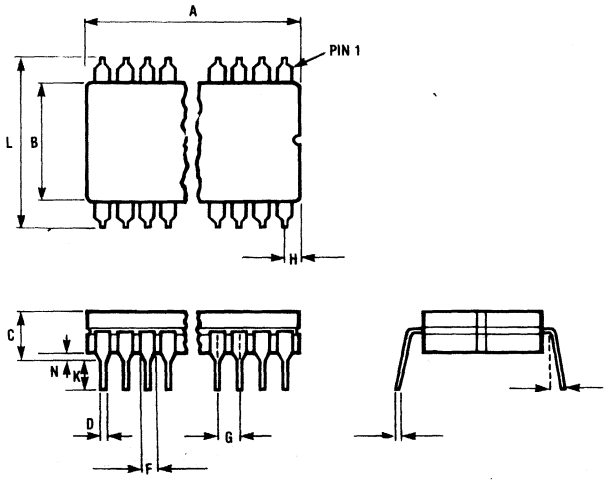
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.92	27.94	1.060	1.100
B	9.27	10.16	0.365	0.400
C	4.22	5.77	0.166	0.227
D	0.41	0.51	0.016	0.020
F	1.14	1.78	0.045	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	2.41	0.040	0.095
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.64	1.60	0.025	0.063

22-Lead CERDIP (C Suffix)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.52	32.54	1.241	1.281
B	13.06	15.06	0.514	0.593
C	4.22	5.77	0.166	0.227
D	0.41	0.51	0.016	0.020
F	1.14	1.78	0.045	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	2.41	0.040	0.095
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.64	1.60	0.025	0.063

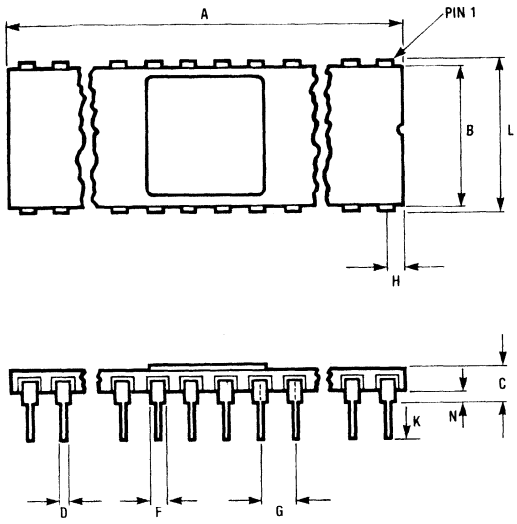
24-Lead CERDIP (C Suffix)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.20	37.47	1.425	1.475
B	13.06	15.06	0.514	0.593
C	4.22	5.77	0.166	0.227
D	0.41	0.51	0.016	0.020
F	1.14	1.78	0.045	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	2.41	0.040	0.095
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.64	1.60	0.025	0.063

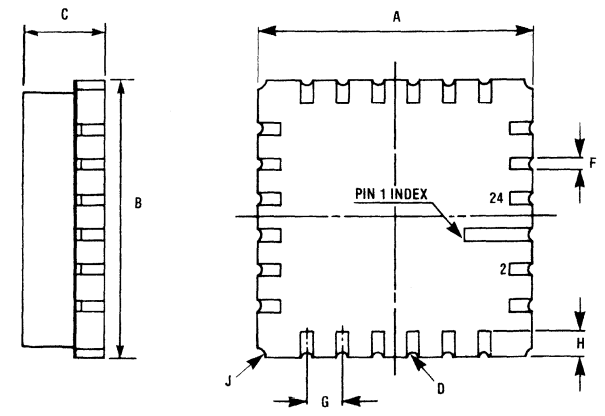
28-Lead CERDIP (C Suffix)

Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.61	15.37	0.575	0.605
C	2.84	3.91	0.112	0.154
D	0.41	0.51	0.016	0.020
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.40	0.030	0.055
J	0.23	0.30	0.009	0.012
K	2.29	3.81	0.090	0.150
L	15.24 BSC		0.600 BSC	
M	−5°	5°	−5°	+5°
N	1.02	1.52	0.040	0.060

40-Lead Dual-In-Line Ceramic (D Suffix)

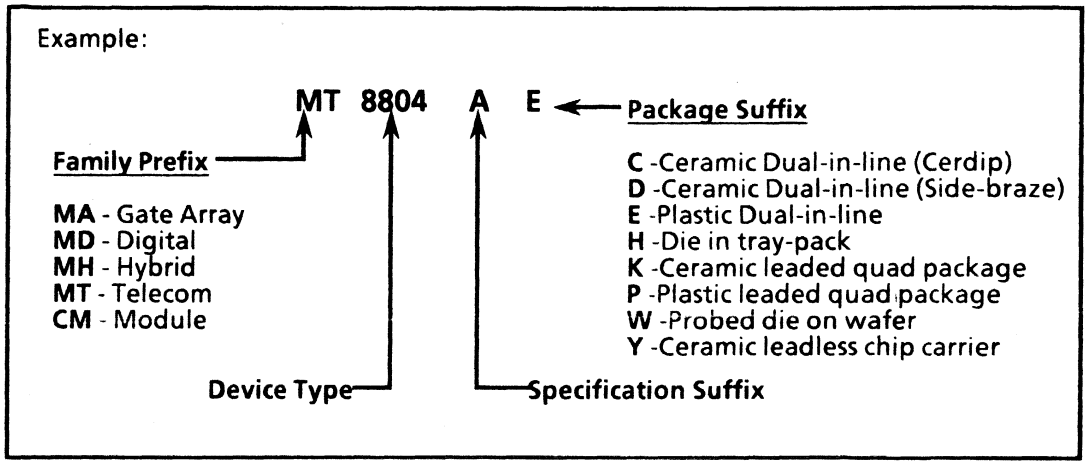


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.03	10.41	0.395	0.410
B	10.03	10.41	0.395	0.410
C	1.27	3.33	0.050	0.131
D	0.020 R (TYP)		0.008 R (TYP)	
F	0.38	0.64	0.015	0.025
G	1.27 BSC		0.050 BSC	
H	0.76	1.02	0.030	0.040
J	0.030 R (TYP)		0.012 R (TYP)	

24-Pad Leadless Chip-Carrier (Y Suffix)

Part Number Identification

Mitel Semiconductor products are identified by a prefix defining the product family, a device type designation number, a specification suffix, and a package suffix. The specification suffix defines variants of a particular device-type and its significance is described in the data sheet of the device concerned. The package suffix, which defines the packge type, refers to drawings in the databook section "Package Outlines". The first page of each data sheet carries a section named "Ordering Information". This shows the full part number for each of the variants and package styles available for the device, and should be consulted to determine the correct part number for ordering purposes. A breakdown of a typical part number is shown below for reference.



Advance and Preliminary Data

Some data sheets carry the designation "Advance" or "Preliminary". Advance information represents the design objective for a device type in development and may be devised without notice before the device reaches production. Preliminary information is intended for design guidance purposes and refers to a device type in early production where device characterization is ongoing and information is still subject to change without notice. Current information on the status of Advance or Preliminary programs may be obtained from Mitel Sales Offices, Representatives, or Distributors.

Modems

ISO²-CMOS MT35212A
BELL 212A/CCITT V.22 Modem Filter

9161-002-038-NA ISSUE 2 JUNE 1986

Features

- Bell 212A and CCITT V.22 compatible
- Usable for Bell 103 and V.22 bis Applications
- Guard tone notch filters for V.22 Application
- High and low band filters with compromise group delay equalizers and smoothing filters
- Answer/originate operating modes
- Detection of call progress tones
- Choice of clocking frequencies: 2.4576 MHz, 1.2288 MHz, or 153.6 kHz
- Analog loopback test capability
- Two uncommitted operational amplifiers
- Pin compatible with AMI S35212A

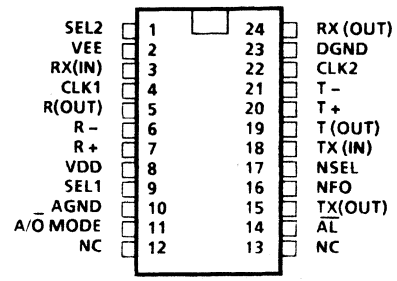
Applications

- Modem filter/equalizer for 1200 bps full duplex modem implementation
- Detection of tones in the call progress band by selecting filters

Description

The MT35212A is an ISO²-CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 modems.

Pin Connections



Ordering Information

MT35212AE	Plastic Dual-in-Line Package
MT35212AC	CERDIP

The MT35212A includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection. In addition, half-channel compromise amplitude and group delay equalizers are included. Provision is made for the receive smoothing filter to switch between the Call Progress mode and the normal data transmission mode.

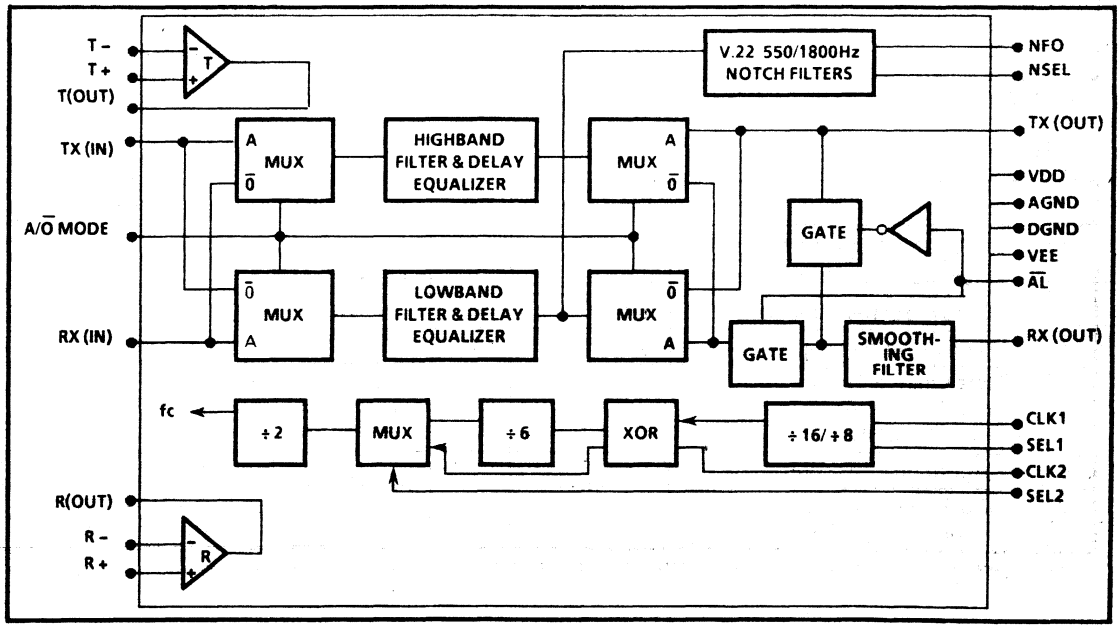


Figure 1- Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Positive Supply Voltage	V_{DD}		6.75	V
2	Negative Supply Voltage	V_{EE}		- 6.75	V
3	Storage Temperature Range	T_{STG}	- 55	+ 125	°C
4	Analog Input	V	V_{EE} - 0.3	V_{DD} + 0.3	V

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Positive Supply Voltage	V_{DD}	4.75	5	5.25	V	DGND = AGND = 0 V
2		Negative Supply Voltage	V_{EE}	- 4.75	- 5	- 5.25	V	DGND = AGND = 0 V
3		Operating Temperature Range	T_O	0	25	70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Operating Conditions - T_O = 0°C to 70°C

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Positive Supply Voltage	V_{DD}	+ 4.75	5.0	5.25	V	
2		Negative Supply Voltage	V_{EE}	- 4.75	- 5.0	- 5.25	V	
3		Power Consumption	P_C		75	150	mW	V_{DD} = 5.25V; V_{EE} = - 5.25V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD} = + 5 V ± 5%, V_{EE} = - 5 V ± 5%, AGND = DGND = 0 V, T_O = 0°C to 70°C

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	I	High Level Logic	V_{IH}	4		V_{DD}	V	Pins 1, 9, 11,14, 17.
2	N	High Level Logic	V_{IH}	2.0		V_{DD}	V	Pins 4, 22.
3	P	Low Level Logic	V_{IL}	V_{EE}		0.8	V	Pins 1, 4, 9, 11,14, 17,22.
4	U	Resistance	R_{IN}		5		MΩ	Pins 3, 18.
5	T S	Capacitance	C_{IN}		10		pF	Pins 3, 18.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - V_{DD} = + 5 V ± 5%, V_{EE} = -5 V ± 5%, AGND = DGND = 0 V, T_O = 0°C to 70°C

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Reference Signal Level Input	V_{REF}		1		V_{RMS}	
2	Maximum Signal Level Input	V_{MAX}			1.4125	V_{RMS}	
3	Bandwidth (both bands)	BW		960		Hz	
4	Gain at Center Frequencies	A_{FO}	- 1.0	0	+ 1.0	dB	
5	Idle Channel Noise - Low Band Filter High Band Filter			 23 22	 33 33	 dBrnC0 dBrnC0	No load.
6	Harmonic Distortion	THD		- 55		dB	
7	Clock Feed Through with respect to signal level	CLK_{FT}		- 23 - 60		dB dB	T_X (clock feedthrough R_X frequency is 76.8 kHz)

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

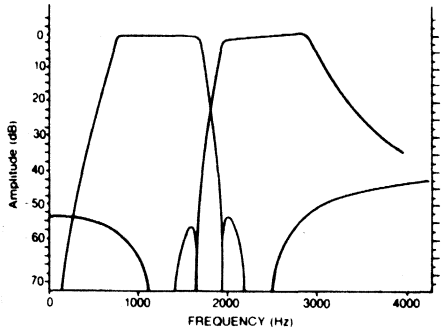


Figure 2 – Typical Amplitude vs. Frequency Plot

Frequency (Hz)		Relative Gain (dB)	
		Min.	Max.
Low Band	400		−35
	800	−1	+1
	1200	−1	+1
	1600	−1.5	+1
	1800		−18
	2000		−48
	2400		−55
	2800		−50
High Band	800		−50
	1200		−53
	1600		−50
	2000	−2.5	+0.5
	2400	−1	+1
	2800	0	+2.5
	3200		−10
	3500		−20

Table 1 – Amplitude vs. Frequency Response

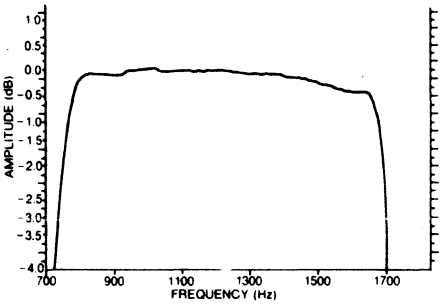


Figure 3 – Typical Low-Band Amplitude vs. Frequency Plot

Figure 5 – Typical High-Band Amplitude vs. Frequency Plot

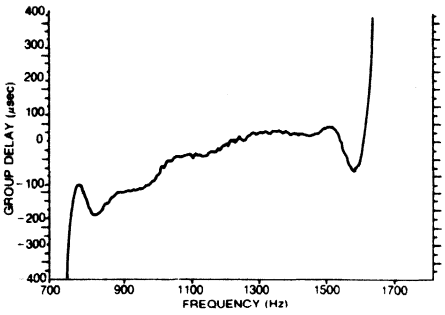


Figure 4 – Typical Low-Band Group Delay vs. Frequency Plot

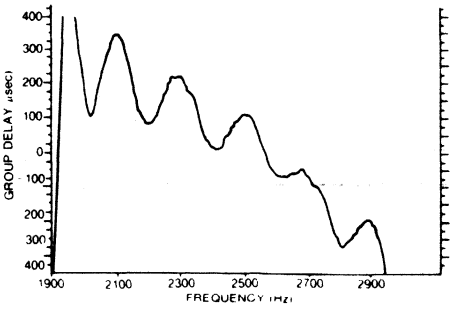


Figure 6 – Typical High-Band Group Delay vs. Frequency Plot

Pin Description

Pin #	Name	Description
1	SEL2	**Select 2.** A logic '0' selects normal operation. A logic '1' scales the filter frequency response by a factor of six for Call Progress Tone Detection with the high group filter.
2	V_{EE}	Negative supply voltage (typically – 5 V) .
3	RX(IN)	**Receive signal input.**
4	CLK1	**Digital Clock 1.** TTL/CMOS input clock at 2.4576 or 1.2288 MHz. If CLK2 is used, CLK1 should be left unconnected.
5	R(OUT)	Receive uncommitted Op Amp Output.
6	R –	Receive uncommitted Op Amp Input. Inverting input.
7	R +	Receive uncommitted Op Amp Input. Non-inverting input.
8	V_{DD}	Positive supply voltage (typically + 5 V).
9	SEL1	**Select 1.** Logic '0' permits operation at 1.2288 MHz; Logic '1' permits operation at 2.4576 MHz.
10	AGND	**Analog ground.**
11	A/$\overline{O}$ MODE	**Mode Answer/Originate.** A logic '0' sets the device in originate mode - the transmit signal in the low band, and the receive signal in the high band. A logic '1' sets the device in the answer mode (the opposite bands to the originate mode).
12	NC	No Connection.
13	NC	No Connection.
14	$\overline{AL}$	**Analog Loopback** control input. A logic '0' sets the device in loopback mode. A logic "1" sets the device in normal mode.
15	TX(OUT)	**Transmit Signal Output.** Filtered transmit signal. This output will drive a 20 kΩ load.
16	NFO	**Notch Filter Output.** This output is capable of driving 20 kΩ.
17	NSEL	**Notch Select.** A logic '0' on this input will select the notch filter to reject 550 Hz. A logic '1' selects a notch at 1800 Hz.
18	TX(IN)	**Transmit/Signal Input.** Unfiltered signal input.
19	T(OUT)	Transmit uncommitted op amp output.
20	T +	Transmit uncommitted op amp non-inverting input.
21	T –	Transmit uncommitted op amp inverting input.
22	CLK2	**Digital Clock 2.** TTL/CMOS input clock at 153.6 kHz. If CLK1 is used, CLK2 should be left unconnected.
23	DGND	**Digital Ground.**
24	RX(OUT)	**Receive Signal Output.** This output is capable of driving a 20 kΩ load.

Functional Description

The MT35212A modem filter implements both the filtering and equalizing functions required in Bell 212A and CCITT V.22 Modems. For CCITT V.22 applications a notch filter is included. The MT35212A includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection. In addition, half-channel compromise amplitude and group delay equalizers are included giving full compromise equalization through the transmit and receive filter pair. For the Call Progress Mode provision is made to select the R_X (OUT) smoothing filter. See Call Progress Mode for details

Figure 1 illustrates the functionality of the MT35212A modem filter. Selection between the call progress tone detection mode and the normal data transmission mode is made via Pin 1 (SEL2). For CCITT V.22 applications the notch filter can be programmed to provide rejection at 1800 Hz or 550 Hz via Pin 17 (NSEL). For maximum flexibility the MT35212A may be operated from a 2.4576 MHz, 1.2288 MHz, or 153.6 kHz clock. Refer to Table 2 for input clock selection.

CLOCK INPUT	SEL1	CLK1	CLK2
153.6 kHz	Don't care	Open	Input
1.2288 MHz	logic '0'	Input	Open
2.4576 MHz	logic '1'	Input	Open

Table 2 - Input Clock Selection

Two uncommitted operational amplifers are provided which can be used for gain control or anti-aliasing filters.

Call Progress Mode Operation

A logic '1' on Pin 1 (SEL2) selects this mode. This will insert a divide by six factor in the clock frequency (fc) causing the center frequencies of the filters to shift down to one-sixth of their original values. As a result, the 1200 Hz filter will be centered around 200 Hz and the 2400 Hz filter will be centred around 400 Hz. Refer to figure 2.

With the high group filter centered at 400 Hz, its passband will be approximately 300 Hz to 480 Hz. This allows the precision dial tone of 350/440 Hz to pass, as well as audible ringing at 440/480 Hz. Half of the busy or reorder tone of 480/620 Hz will also pass through the high group filter in this mode.

By using a suitable detector circuit combined with a method of timing determination it is possible to build a more intelligent modem that can communicate back to its terminal or computer the status of the phone call.

Diagnositc Mode

The MT35212A has Analog Loopback capability. A logic '0' on $\overline{AL}$ pin switches the transmit carrier output back through the receive smoothing filter for testing. For normal operation the $\overline{AL}$ pin should be connected to a High voltage level (+ 5 V) .

ISO²-CMOS MT35213
BELL 212A 1200/300 BPS Modem

Preliminary Information

9161-002-039-NA ISSUE 3 JUNE 1986

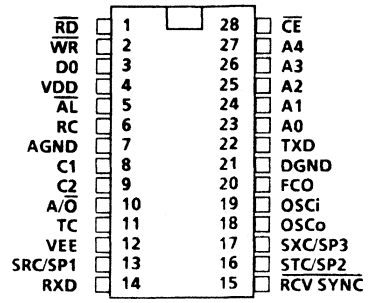
Features

- Bell 212A compatible
- Single chip 1200 bps, full duplex DPSK modem with 300 bps FSK fallback mode
- On-chip scrambler/descrambler
- On-chip async/sync and sync/async conversion
- Full analog and digital loopback test capability
- Carrier detect and automatic gain control
- Selectable for operation with int. or ext. clock
- 2.4576 MHz crystal controlled with filter clock (153.6 kHz) output available
- 48 dB (0 to – 48 dBm) dynamic input range
- Selectable character length (8, 9, 10 or 11 bits)
- Microprocessor bus interface
- CMOS with TTL compatible inputs/outputs
- Pin compatible with AMI S35213

Applications

- Stand alone RS-232C interface modem
- Board level µP bus interface modems
- "Smart Modems"
- Data telemetry systems

Pin Connections



Ordering Information

MT35213AE	Plastic Dual-in-Line Package
MT35213AC	CERDIP
	0 °C to 70 °C

Description

The MT35213 is a single chip modulator/demodulator circuit fully compatible with the Bell 212A standard. It contains a 1200 bps DPSK modulator/demodulator and a fallback 300 bps FSK modulator/demodulator. The MT35213 has on chip scrambler and descrambler, asynchronous to synchronous and synchronous to asynchronous conversion circuitry. Full digital and analog loopback test capability are also provided. When used with the MT35212A modem filter, all the modulation/demodulation and filtering functions required to realize a Bell 212A modem are in place.

The MT35213 and the MT35212A are both fabricated in Mitel's ISO²-CMOS technology.

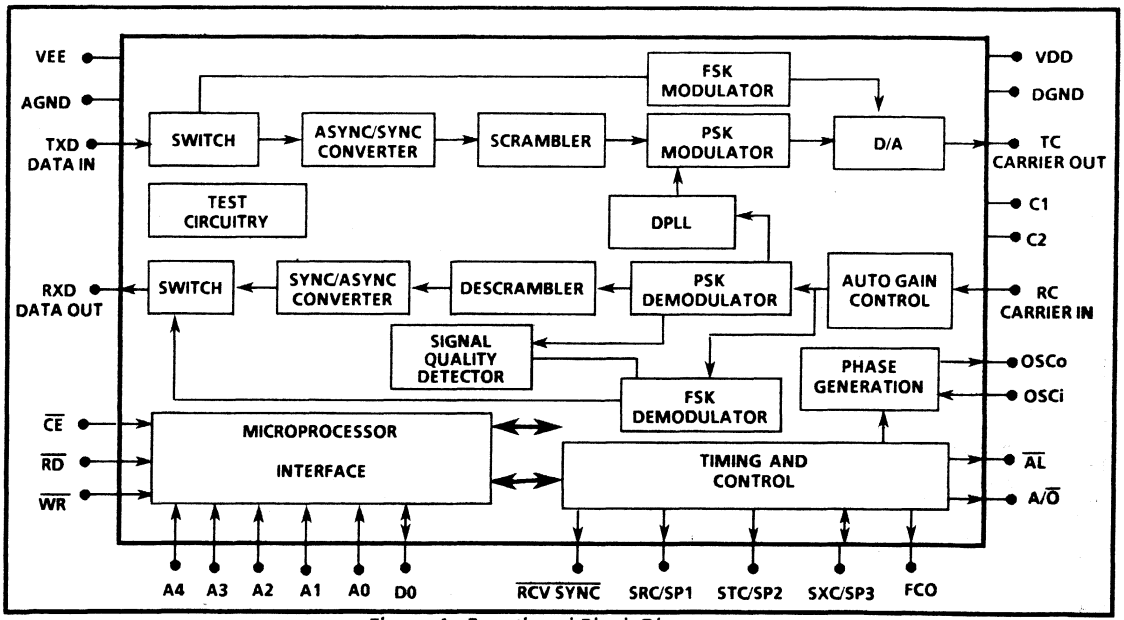


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	$V_{DD} - V_{EE}$		+ 13.5	V
2	Storage Temperature Range	T_{ST}	- 55	+ 125	°C
3	Analog Input/Digital Input	V_{IN}	V_{EE} - 0.3	V_{DD} + 0.3	V

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typical‡	Max	Units	Test Conditions
1	Positive Power Supply	V_{DD}		+ 5		V	$D_{GND} = A_{GND} = 0V$
2	Negative Power Supply	V_{EE}		- 5		V	$D_{GND} = A_{GND} = 0V$
3	Oscillator Clock Frequency	f_{OSC}		2.4576		MHz	
4	Oscillator Freq. Tolerance	Δf_{OSC}		± 0.005		%	
5	Operating Temperature Range	T_O	0		+ 70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

D.C. Electrical Operating Conditions - T_O = 0°C to + 70°C

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive Power Supply	V_{DD}	+ 4.5	+ 5	+ 5.5	V	$D_{GND} = A_{GND} = 0V$
2	Negative Power Supply	V_{EE}	- 4.5	- 5	- 5.5	V	$D_{GND} = A_{GND} = 0V$
3	Power Consumption	P_C		90		mW	V_{DD} = + 5.5V; V_{EE} = - 5.5V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics - T_O = 0°C to + 70°C; V_{DD} = + 5 V (± 10%); V_{EE} = - 5 V (± 10%) unless otherwise specified

	Characteristics	Sym	Min	Max	Units	Test Conditions
1	High Level Logic Input	V_{IH}	2.0	V_{DD}	V	Pins 1-3, 17, 22-28
2	Low Level Logic Inputs	V_{IL}	V_{EE}	+ 0.8	V	Pins 1-3, 17, 22-28
3	High Level Logic Outputs	V_{OH}	2.4	V_{DD}	V	Pins 3, 13-17, 20 (I_{OH} = 100 µA)
4	Low Level Logic Outputs	V_{OL}	0	0.4	V	Pins 3, 13-17, 20 (I_{OL} = 1.6 mA)
5	High Level Logic Outputs	V_{OH}	V_{DD}-0.3 (V_{DD}-V_{EE})	V_{DD}	V	Pins 5, 10
6	Low Level Logic Outputs	V_{OL}	V_{EE}	V_{EE} + 0.3(V_{DD}-V_{EE})	V	Pins 5, 10

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

A.C. System Specifications - T_O = 25°C; V_{DD} = + 5 V; V_{EE} = - 5 V unless otherwise specified

	Parameter	Sym	Min	Typical‡	Max	Units	Test Conditions
1	Oscillator Frequency	f_{OSC}		2.4576		MHz	
2	Clock Signal Output	f_{CO}		153.6		kHz	
3	Transmit Carrier Output Level	T_{OUT}	- 9.0	- 7.5	- 6.0	dBm	200 kΩ load
4	Receive Carrier Input Level	R_{SENS}	- 48		0	dBm	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Microprocessor Interface Timing - Read Cycle (Refer to Figure 2)

	Parameters	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Enable Set-up	t_{ESR}	70			ns	
2	Pulse Width	t_{PWR}	250			ns	
3	Enable Hold	t_{EHR}	0			ns	
4	Data Access	t_{DAR}			120	ns	
5	Data Hold	t_{DHR}	20			ns	
6	Address Setup	t_{AS}	0			ns	

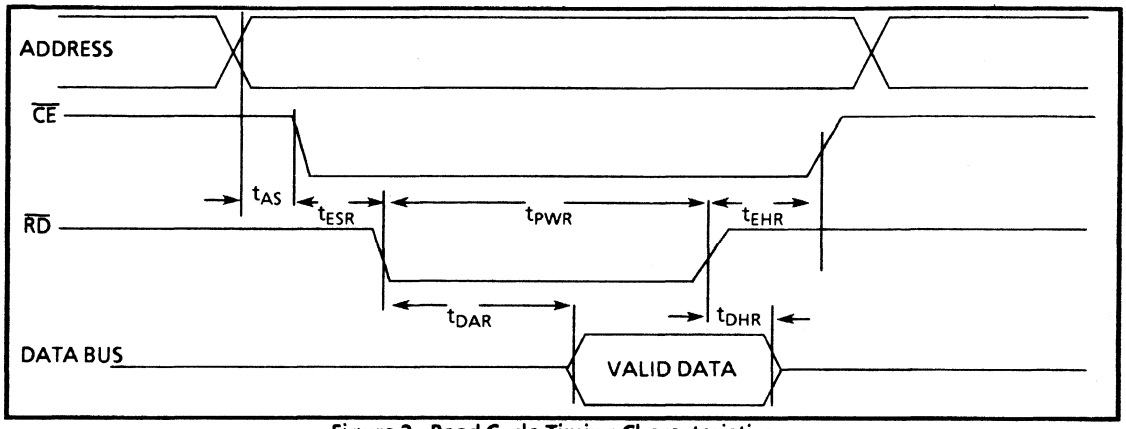


Figure 2 - Read Cycle Timing Characteristics

Microprocessor Interface Timing - Write Cycle (Refer to Figure 3)

	Parameters	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Enable Set-up	t_{ESW}	70			ns	
2	Pulse Width	t_{PWW}	250			ns	
3	Enable Hold	t_{EHW}	0			ns	
4	Data Set-up	t_{DSW}	60			ns	
5	Data Hold	t_{DHW}	20			ns	
6	Address Setup	t_{AS}	0			ns	

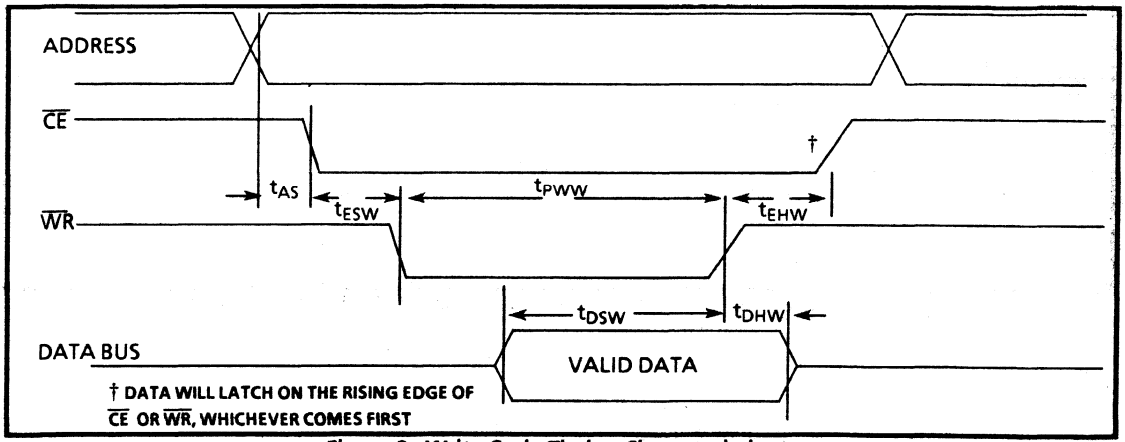
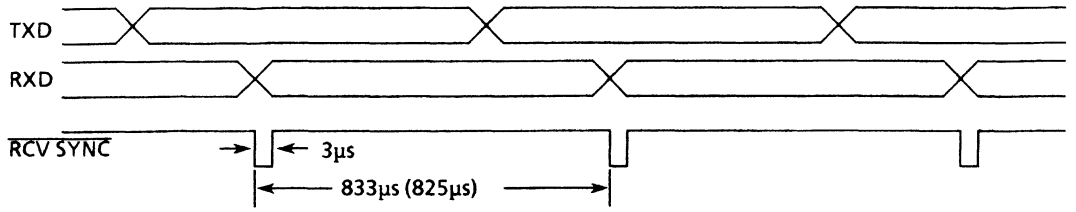


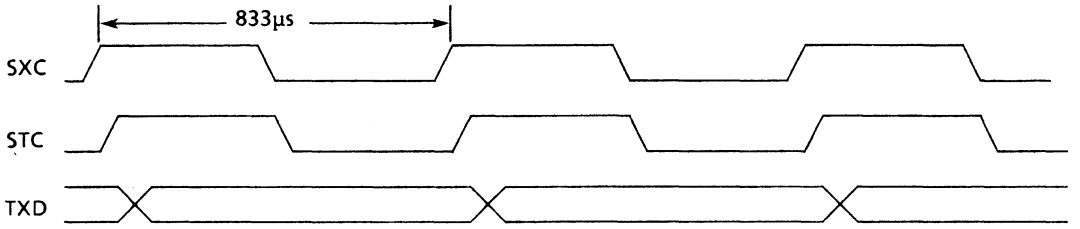
Figure 3 - Write Cycle Timing Characteristics

ASYNCHRONOUS MODE

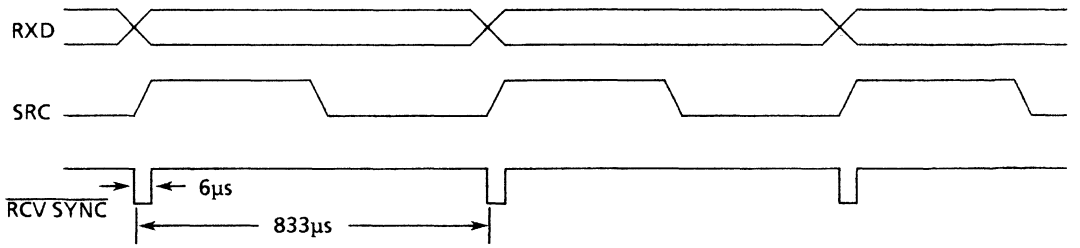


IN THE ASYNCHRONOUS MODE SRC, STC ARE NOT VALID.
IN LOW SPEED MODE $\overline{\text{RCV SYNC}}$ FREE RUNS AND IS NOT RELATED TO RECEIVE DATA.

SYNCHRONOUS MODE



IN THE EXTERNAL MODEs STC IS DERIVED FROM SXC WHICH IS THE EXTERNAL SYNCHRONOUS SIGNAL. THE DATA SHOULD BE CHANGING ON THE POSITIVE EDGES OF STC. IT IS SAMPLED ON THE NEGATIVE EDGE OF STC.



SRC IS DERIVED FROM THE TRANSITIONS OF THE INCOMING DATA STREAM. THE POSITIVE TRANSITIONS OF SRC COINCIDE WITH THE BIT CHANGES IN RXD. RCV SYNC IS A NEGATIVE GOING PULSE COINCIDING WITH THE POSITIVE EDGES OF SRC.

Figure 4 - MT35213 Signal Relationships, Serial Data Path, High Speed Mode

Pin Description

Pin #	Name	Description
1	$\overline{RD}$	**Read** Enable (TTL input).
2	$\overline{WR}$	**Write** Enable (TTL input).
3	D_O	**Data I/O** (TTL) - high impedance when not selected.
4	V_{DD}	**Positive Supply Pin** - typically + 5 V.
5	$\overline{AL}$	**Analog Loopback** (CMOS output) - signal to the filter chip (MT35212A).
6	R_C	**Receive Carrier** - analog input signal.
7	A_{GND}	**Analog Ground Pin** - (0 V).
8 & 9	C_1 & C_2	External 0.1µF capacitor for offset compensation connected across these pins.
10	$A/\overline{O}$	**Answer or Originate Mode** (CMOS output) - signal to the filter chip (MT35212A).
11	T_C	**Transmit Carrier** - output signal.
12	V_{EE}	**Negative Supply Pin** - typically – 5V
13	SRC/SP1	**Synchronous Receive Clock** (TTL Output) - received 1200 Hz clock (recovered) - The data bit transitions are synchronous with positive edge of SRC. Alternatively, under async. mode, this pin can be used as a spare line, SP1 (addresses 18, 19).
14	RXD	**Received Digital Data** to terminal (TTL output) - will be synchronous with SRC in the synchronous mode.
15	$\overline{RCV\ SYNC}$	Provides a negative pulse 3 µs or 6 µs wide on the leading edge of each received data bit (TTL output).
16	STC/SP2	**Synchronous Transmit Clock** (TTL output) - transmitted 1200 Hz clock. Its rising edge indicates time to change T_D data. Alternatively, SP2 (addresses 20, 21).
17	SXC/SP3	**Synchronous External Clock** (TTL) - external transmit clock from data terminal for sync. in the external sync. mode. Alternatively, SP3 output (addresses 22, 23).
18	OSC_O	**Crystal Oscillator Output Pin** (CMOS output) - A 2.4576 MHz crystal is connected across the OSC_O and OSC_i pins. Also, connect a 20 pF capacitor to V_{EE}.
19	OSC_i	**Crystal Oscillator Input Pin** (CMOS input) - A 2.4576 MHz crystal is connected across the OSC_O and OSC_i pins. Also, connect a 20 pF capacitor to V_{EE}.
20	FCO	153.6 kHz clock signal to the filter chip (MT35212A) - (TTL output)
21	D_{GND}	**Digital Ground Pin.**
22	TXD	**Transmit Digital Data** (TTL input) - from terminal must be synchronized to STC or SXC when in synchronous mode.
23	A_0	**Address** line (TTL input).
24	A_1	**Address** line (TTL input).
25	A_2	**Address** line (TTL input).
26	A_3	**Address** line (TTL input).
27	A_4	**Address** line (TTL input).
28	$\overline{CE}$	**Chip Enable** (TTL input).

MT35213 Command Locations [x] - Refer to Figure 5

Note: There is no power-on reset. The microprocessor or controller must perform an initialization.

Location	Address A4	A3	A2	A1	A0	Write Commands (All positive true unless otherwise stated)
0	0	0	0	0	0	Transmit Squelch Control
1	0	0	0	0	1	Scramble Disable (for Remote Digital Loopback)
2	0	0	0	1	0	Force RXD to a Mark
3	0	0	0	1	1	Receive Sync Disable (sets pin 15 to a "1")
4	0	0	1	0	0	Signal Quality Detector Enable
5	0	0	1	0	1	PLL Control; High Speed/$\overline{\text{Low Speed}}$
6	0	0	1	1	0	WL1 Data Word Length Control 1
7	0	0	1	1	1	WL0 Data Word Length Control 0 Bits Per Word: 8 / 9 / 10 / 11 WL1: 0 / 0 / 1 / 1 WL0: 0 / 1 / 0 / 1
8	0	1	0	0	0	Async Mode/$\overline{\text{Sync Mode}}$
9	0	1	0	0	1	High Speed/$\overline{\text{Low Speed}}$
10	0	1	0	1	0	Slave Mode/$\overline{\text{External Mode}}$ (DTE Clock) [Sync Mode Only]
11	0	1	0	1	1	Local Clock/$\overline{\text{External Timing}}$ (Local if Async)
12	0	1	1	0	0	Answer/$\overline{\text{Originate}}$
13	0	1	1	0	1	Analog Loopback/$\overline{\text{Normal}}$
14	0	1	1	1	0	Digital Loopback/$\overline{\text{Normal}}$
15	0	1	1	1	1	Connect Modulator to Dotting Pattern Generator
16	1	0	0	0	0	Connect Modulator to Mark Generator
17	1	0	0	0	1	Connect Modulator to Space Generator
18	1	0	0	1	0	SRC/$\overline{\text{SP1}}$ Selection of Pin 13 Function
19	1	0	0	1	1	SP1 High/$\overline{\text{Low}}$
20	1	0	1	0	0	STC/SP2 Selection of Pin 16 Function
21	1	0	1	0	1	SP2 High/$\overline{\text{Low}}$
22	1	0	1	1	0	SXC/SP3 Selection of Pin 17 Function
23	1	0	1	1	1	SP3 High/$\overline{\text{Low}}$
24	1	1	0	0	0	Enter Test Mode 0
25	1	1	0	0	1	Enter Test Mode 1
26	1	1	0	1	0	Enter Test Mode 2
27	1	1	0	1	1	Enter Test Mode 3
28	1	1	1	0	0	Force RXD Open (This is a higher priority than location 2 command to force a Mark out)
29	1	1	1	0	1	Carrier Valid-Sets Energy Detect Threshold from – 41 dBm to – 46 dBm
30	1	1	1	1	0	Reserved
31	1	1	1	1	1	Reserved

MT35213 Read Locations (y) - Refer to Figure 5

Location	Address A4	A3	A2	A1	A0	Read Information
0	0	0	0	0	0	Energy Detect (1 = True, 0 = False) 5 ms Time Constant
1	0	0	0	0	1	PSK Demodulator Output*
2	0	0	0	1	0	PSK Unscrambled Output
3	0	0	0	1	1	FSK Demodulator Output*
4	0	0	1	0	0	Signal Quality Indicator (1 = Good, 0 = Bad)

*Note: When operating in one speed (mode) the opposite output may have random data. See MT35213 Demodulator State Table 1 for more details

REGISTER	INCOMING CARRIER CONDITION			
	No Carrier	FSK Mark	PSK Scram Mark	PSK Unscram Mark
FSK DEM ANS	Random	Mark	Random	Space
PSK DEM ANS	Random	Random	Random	Mark
PSK UNSCRAM	Random	Random	Mark	Mark
FSK DEM ORIG	Random	Mark	Random	Mark
PSK DEM ORIG	Random	Mark	Random	Mark
PSK UNSCRAM	Random	Mark	Mark	Mark

Table 1 - MT35213 Demodulator State

Table 1 indicates the state of the three output data registers (FSK Demodulator Output, PSK Demodulator Output, and PSK Unscrambled Output) in both the Answer and Originate modes.

The suggested method of detection is to sample each register for a specified amount of time looking for the Mark state; if a predetermined amount of Spaces are detected within that time period then the desired signal is not present and the search should continue for a valid output from either FSK or PSK.

It is important to note that for some carrier conditions there will be a Mark present at more than one output. This means that the detection routine will have to compare against a table of expected conditions for each mode.

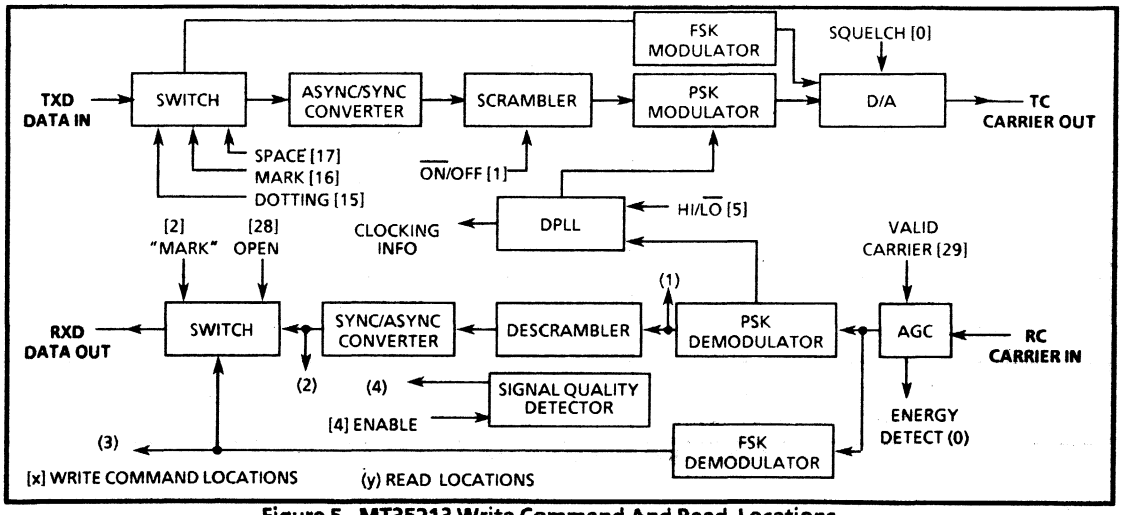


Figure 5 - MT35213 Write Command And Read Locations

Functional Description

The MT35213 will do 1200 bps asynchronous or synchronous data transmission in a duplex mode over the switched telephone network using differential phase-shift keying (DPSK) signal. Each phase shift represents two bits of data (called "di-bit" encoding). For a 1200 bps data stream this results in a 600 baud rate. In order to provide a relatively uniform energy level and to maintain synchronization the data signals are scrambled before modulation and descrambled after demodulation.

The MT35213 contains the PSK modulator/demodulators, the scrambler/de-scrambler and the synchronous/asynchronous converters mentioned above. Included is a "fallback" mode, in case a slow modem or a bad telephone line is encountered. The MT35213 can indicate reception of FSK signals and can be operated in the 0 to 300 bps FSK mode as a Bell 103 type modem.

Private line protocols as well as the common Bell 212A protocol are available through a flexible command structure. Timing and procedures can be programmed and tailored for specific applications in the controller. An example of that would be the initialization routine performed each time the modem is powered on.

When the reset command initiates the controller, it has to write into locations 0,2,6,7,8,9,10 etc. of the MT35213 to set all the proper functions.

When the RI line indicates ringing the DTE would decide whether to answer immediately or after so many rings. After causing OH to go Low the controller has to turn on the Answer Tone (a high band FSK Mark) by changing locations 0, 9, 12, 16, and others to accomplish the goal of answering. Then location 0 is polled to see if there is carrier detect. As soon as carrier detect is determined the controller will sample locations 2 and 3 to see if the incoming signal is FSK or PSK.

Comprehensive diagnosis functions including Analog Loopback (AL), Digital Loopback (DL) and Remote Digital Loopback (RDL) are incorporated.

Frequency Assignment (See Table 2)

Standard conventions such as Bell 212A are established to guarantee compatible communications. For full duplex operation, modems must be able to transmit and receive simultaneously in the voice frequency channel. For both 300 and 1200 bps operation the voice band is separated into high and low band segments. The answering modem transmits in the high band and the originating modem transmits in the low band. The use of high performance filters such as the Mitel MT35212A allows the receive signals to be separated from the transmit signals and demodulated accurately.

Applications

The MT35213 modem chip is designed to be used with the MT35212A filter, a controller chip, and a dialer chip.It can be either a RS-232 stand alone modem or a bus-interfaced modem card for direct plug-in to personal computers.

With any off-the-shelf 8-bit microcomputer, such as the 6805, a compact and cost-effective Bell 212A modem can be realized. Figure 6 shows how such a modem might be configured to provide 1200/300 bps asynchronous operations with auto-answer and auto-dialing (DTMF & Pulse) with a minimum number of chips. Note that this modem would be able to communicate over the RS-232C link to the DTE (computer) for control functions such as dialing, on-hook/off-hook, speed control (perhaps eliminating CH and CI in the cable) and ring indicate (eliminating CE). Since the functions are all available it becomes an exercise in software to

Mode		Transmit Frequency (Hz)		Receive Frequency (Hz)	
		Mark	Space	Mark	Space
Bell 103 Originate	0-300 bps	1270	1070	2225	2025
Bell 103 Answer	0-300 bps	2225	2025	1270	1070
Bell 212A Originate	1200 bps	1200		2400	
Bell 212A Answer	1200 bps	2400		1200	

Table 2 - Bell 212A Frequency Assignment

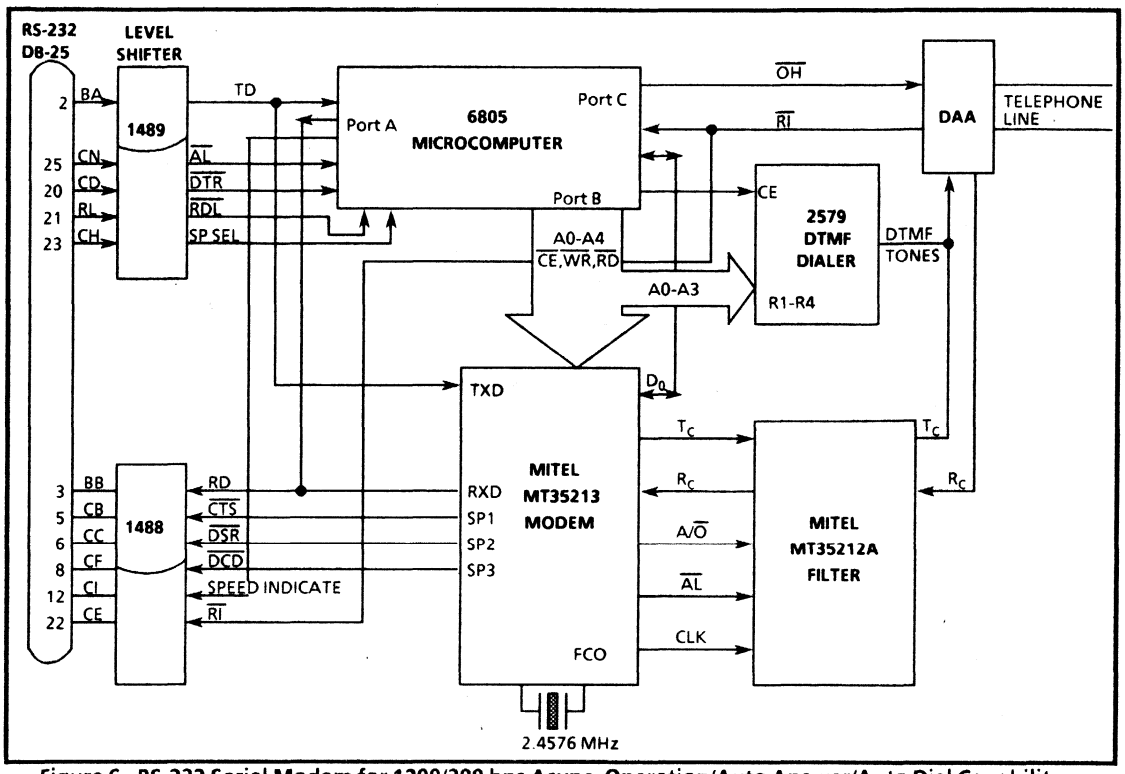


Figure 6 - RS-232 Serial Modem for 1200/300 bps Async. Operation/Auto Answer/Auto Dial Capability

implement the desired features for a particular application.

Figure 7 shows an implementation of an intelligent Bell 212A modem with auto-dial, auto-answer, and call progress tone detection capability. The 2579 does the tone dialing function and the controller

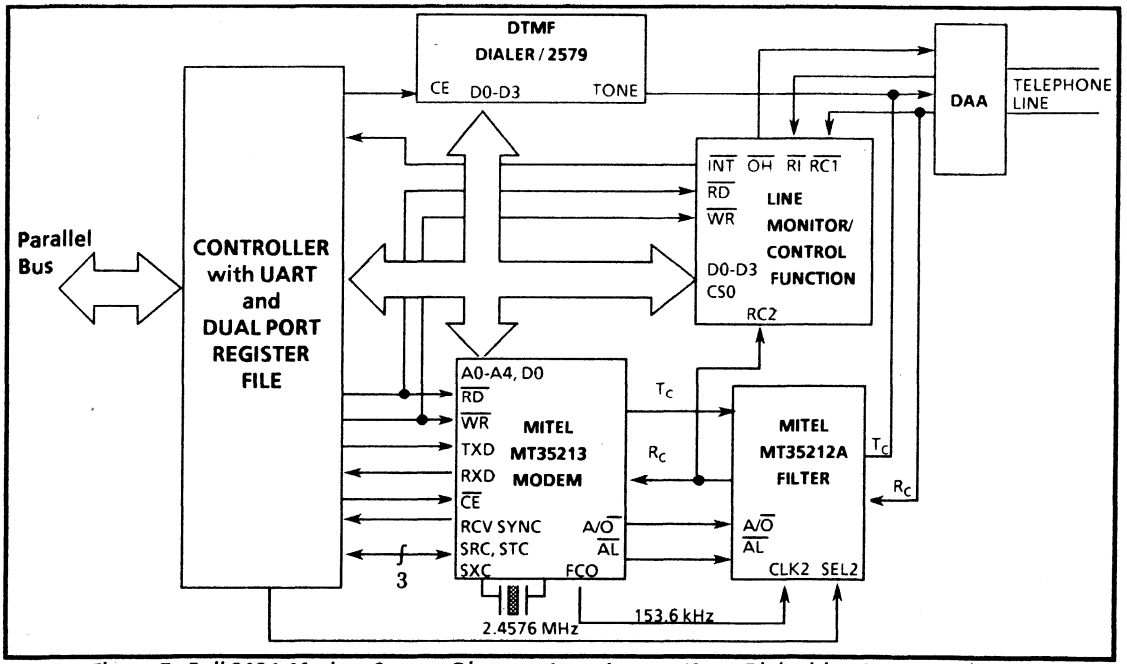


Figure 7 - Bell 212A Modem System Diagram Auto Answer/Auto Dial with µP Bus Interface

does the pulse dialing function through the control circuitry, switching the OH (off-hook) relay line. When RI is received from the ring detector circuit in the DAA (Data Access Arrangement) the logic sends an interrupt to the controller to initiate the auto-answer sequence.

During the auto-dial or origination sequence the call progress tones (dial tone, busy, ringing, etc.) can be monitored. The MT35212A filter will change center frequencies when SEL2 is switched. The high group filter will shift from 2400 Hz to 400 Hz center frequencies, thus passing the 350, 440, 480 Hz tones. By using the energy detector in the MT35213, the microcontroller will be able to examine the cadence of the tones to determine status or progress of the call. The microcomputer (controller) is programmed to handle the modem protocol, perform loopback testing and monitor call progress. It can convert specific terminal controls to appropriate control signals.

This figure illustrates how a parallel interface modem designed to plug directly into an option slot in a personal computer might be arranged. To convert serial data to parallel data for microprocessor bus interface the controller must be able to perform the UART/USRT functions as well as control dual port register files for bus I/O. A variety of controllers such as the Intel 8051 can perform these functions.

Notes

ISO²-CMOS MT3530
BELL 103/V.21 Single Chip Modem

9161-002-037-NA ISSUE 2 JUNE 1986

Features

- Single chip 300 bps, full duplex, asynchronous FSK modem
- Bell 103/113 and CCITT V.21 selectable
- Auto Answer/Originate operating modes
- Manual mode
- Phase continuous transmit carrier switching
- Digital and Analog Loopback modes
- CCITT V.25 tone generation
- UART clock output
- Passthru mode for protocol independence
- No external filtering required
- DTE Interface - Functionally: RS-232C Compatible (CCITT V.24)
  Electrically: TTL level Compatible

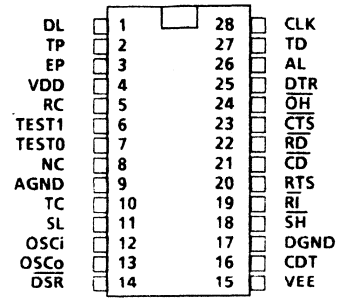
Applications

- Stand alone RS-232C interface modem
- Add on modem for personal computers and microprocessor systems

Description

The MT3530 is a ISO²-CMOS single chip full duplex FSK modem. It is intended for use in Bell 103/113 and CCITT V.21 type applications. The MT3530 features on-chip transmit and receive filters; Answer/Originate mode selection; RS-232C control interface; Digital and Analog Loopback test modes; and generation of both 4.8 kHz UART clock and V.25 Answer Tone. The device uses a 3.579545 MHz NTSC color T.V. crystal.

Pin Connections



Ordering Information

MT3530BE	Plastic Dual-in-Line Package
MT3530BC	CERDIP

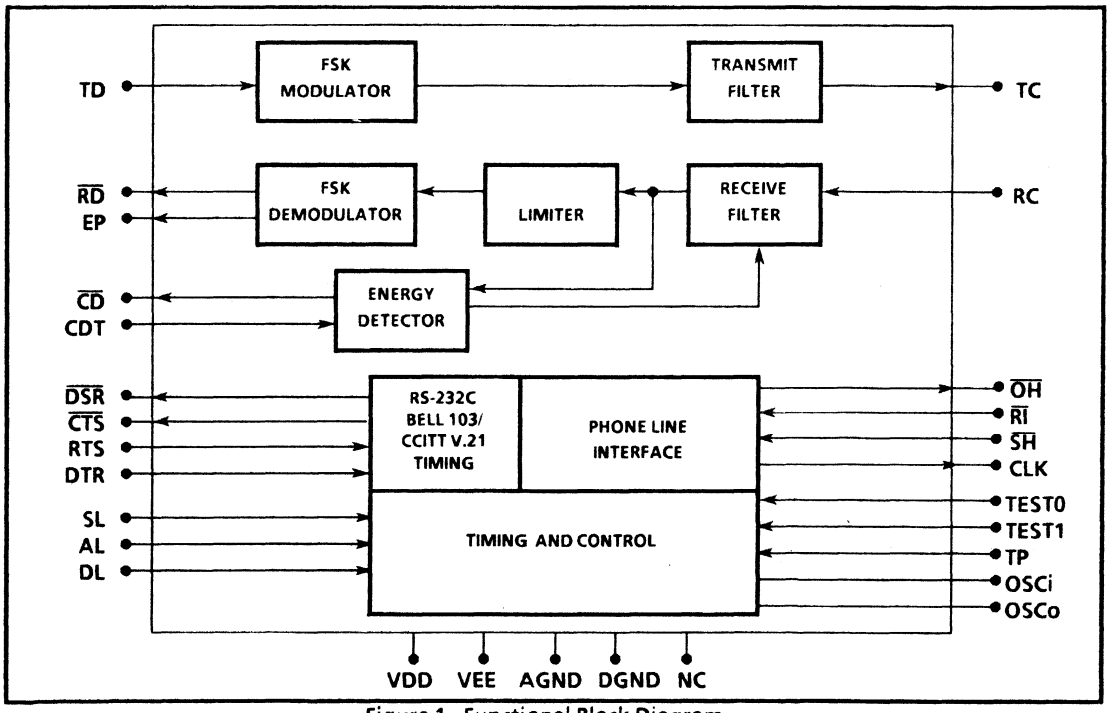


Figure 1- Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{DD}-V_{EE}		+ 12.0	V
2	Storage Temperature Range	T_{STG}	- 65	+ 150	°C
3	Input Voltage, All Pins	V_{IN}	V_{EE} - 0.3	V_{DD} + 0.3	V

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

D.C. Electrical Operating Conditions - T_O = 0°C to + 70°C;

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Positive Supply Voltage	V_{DD}	+ 4.75	+ 5.0	+ 5.25	V	DGND = AGND = 0 Volt
2		Negative Supply Voltage	V_{EE}	- 4.75	- 5.0	- 5.25	V	DGND = AGND = 0 Volt
3		Power Consumption	P_C		110	200	mW	V_{DD} = 5.0 V; V_{EE} = - 5.0 V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Recommended Operating Conditions - Voltages are with respect to ground unless otherwise stated

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	I	Positive Supply Voltage	V_{DD}		+ 5		V	DGND = AGND = 0 Volt
2	N	Negative Supply Voltage	V_{EE}		- 5		V	DGND = AGND = 0 Volt
3	P	Oscillator Clock Frequency	fosc		3.579545		MHz	
4	U	Oscillator Frequency Tolerance	Δfosc		± 0.02		%	
5	T S	Operating Temperature Range	T_O	0		70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Analog Signal Parameters T_O = 0°C to + 70°C, ± 5 Vdc, fosc = 3.579545 MHz

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Oscillator Clock Frequency Oscillator Frequency Tolerance Transmit Frequency Tolerance	fosc Δfosc Δft		3.579545 ± 0.02 ± 1.2	 ± 3	MHz % Hz	
2		Transmit 2nd Harmonic Attenuation with respect to carrier level	T_{HD}		50		dB	
3		Transmit Output Level	T_{OUT}	- 9	- 8	- 7	dBm	Load 10 kΩ 25 pF Max.
4		Carrier Input Range		- 50		0	dBm	CDT open
5		Dynamic Range	DNR		50		dB	CDT open
6		Carrier Detect: On Level Off Level On/Off level Hysterisis	CD_{ON} CD_{OFF} CD_H	 - 50 2.5	- 43 - 48 5	- 41	dBm dBm dB	
7		Bit Jitter Bit Bias (Mark and Space) Bias Distortion			100 1 3		µs % %	Input = - 30dBm

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD} = 5 ± 5% Vdc, V_{EE} = −5 ± 5% Vdc, AGND = DGND = 0V, T_O = 0°C to 70°C

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	CMOS Inputs Voltage High	V_{IH}	3			V	Note 1
		Voltage Low	V_{IL}			−3	V	
2		TTL Inputs Voltage High	V_{IH}	2			V	Note 2
		Voltage Low	VIL			0.8	V	
3		Input Resistance	R_{IN}	8			MΩ	All Inputs
4		Input Capacitance	C_{IN}			15	pF	All Inputs
1	OUTPUTS	LSTTL Outputs						Note 3
		Voltage High	V_{OH}	2.4			V	
		Voltage Low	V_{OL}			0.4	V	I_{OL} = 0.4mA
2		TTL Output						Note 4
		Voltage High	V_{OH}	2.4			V	
		Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6mA

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

Modem Timing† Parameter for CCITT V.21 Operating Mode. See Figures 2 and 4a

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ORIG	Answer Detect	t_{AD}	332	450	564	ms	Note 5
2		Receive Carrier Low	t_{RCL}	172	205	236	ms	Note 5
3		Transmit Carrier	t_{TXC}	592	632	688	ms	Note 5
4		Receive Carrier to $\overline{CD}$ Delay	t_{RCD}	20	50	80	ms	Note 5
5		$\overline{CD}$ to Off-Hook Delay	t_{COH}	180	200	232	ms	Note 5
1	ANS	Billing Delay	t_{BD}	2.0	2.1	2.3	s	Note 5
2		Answer Tone	t_{AT}		3.4		s	Note 5
3		Transmit Carrier Delay	t_{TCD}		80		ms	Note 5
4		Clear-To-Send	t_{CTS}	332	450	564	ms	Note 5

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Modem Timing† Parameters for Bell 103 Operating Mode. See Figures 3 and 4a

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ORIG	Receive Dial Tone	t_{DT}	70			ms	Note 5
2		Answer Tone Detect	t_{ATD}	100	120	200	ms	Note 5
3		Receive Carrier Low	t_{RCL}	172	200	236	ms	Note 5
4		Transmit Carrier	t_{TXC}	592	632	688	ms	Note 5
5		Receive Carrier to $\overline{CD}$ Delay	t_{RCD}	10	20	32	ms	Note 5
6		$\overline{CD}$ to Off-Hook Delay	t_{COH}	180	200	232	ms	Note 5
1	ANS	Billing Delay	t_{BD}	2.0	2.1	2.2	s	Note 5
2		Clear-To-Send Low	t_{CTS}	100	120	200	ms	Note 5

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 1. Include $\overline{SH}$, $\overline{RI}$, TEST0 , TEST1
Note 2. Include RTS, TD, DTR, AL, DL, SL
Note 3. Include $\overline{OH}$,$\overline{CLK}$, $\overline{CD}$, $\overline{DSR}$
Note 4. Include $\overline{RD}$, $\overline{CTS}$
Note 5. Test conducted using Passthru mode

Modem Timing† Parameters for Bell 103/CCITT V.21. See Figures 2, 3, 4b & 5

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ORIG	Data Terminal Low	t_{DTL}	15			ms	Note 5
2	ORIG	Request to Send On Delay	t_{RTS}	1			ms	Note 5
3	ORIG	Switch Hook Low	t_{SHL}	54			ms	
1	ANS	Ring Indicator to $\overline{OH}$ Delay	t_{RIO}		80		ms	Note 5
2	ANS	Data Terminal Low to $\overline{OH}$ Delay	t_{TOH}		10		ms	Note 5
3	ANS	Switch Hook to Off Hook Delay	t_{SOH}		40		ms	Note 5
4	ANS	Ring Indicator Low	t_{RIL}	107			ms	

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 5: Test conducted using Passthru Mode.

Pin Name	Pin No.	Input	Output	Voltage Level Low	Voltage Level High	Logic Family	I_{OL} mA
$\overline{SH}$	18	X		−3	+3	CMOS	
$\overline{RI}$	19	X		−3	+3	CMOS	
TEST0	7	X		−3	+3	CMOS	
TEST1	6	X		−3	+3	CMOS	
$\overline{OH}$	24		X	+0.4	+2.4	LSTTL	0.4
CLK	28		X	+0.4	+2.4	LSTTL	0.4
$\overline{CD}$	21		X	+0.4	+2.4	LSTTL	0.4
$\overline{RD}$	22		X	+0.4	+2.4	TTL	1.6
$\overline{CTS}$	23		X	+0.4	+2.4	TTL	1.6
$\overline{DSR}$	14		X	+0.4	+2.4	LSTTL	0.4
RTS	20	X		+0.8	+2.0	TTL	
TD	27	X		+0.8	+2.0	TTL	
DTR	25	X		+0.8	+2.0	TTL	
AL	26	X		+0.8	+2.0	TTL	
DL	1	X		+0.8	+2.0	TTL	
SL	11	X		+0.8	+2.0	TTL	

Table 1 - Signal Input and Output Compatibility

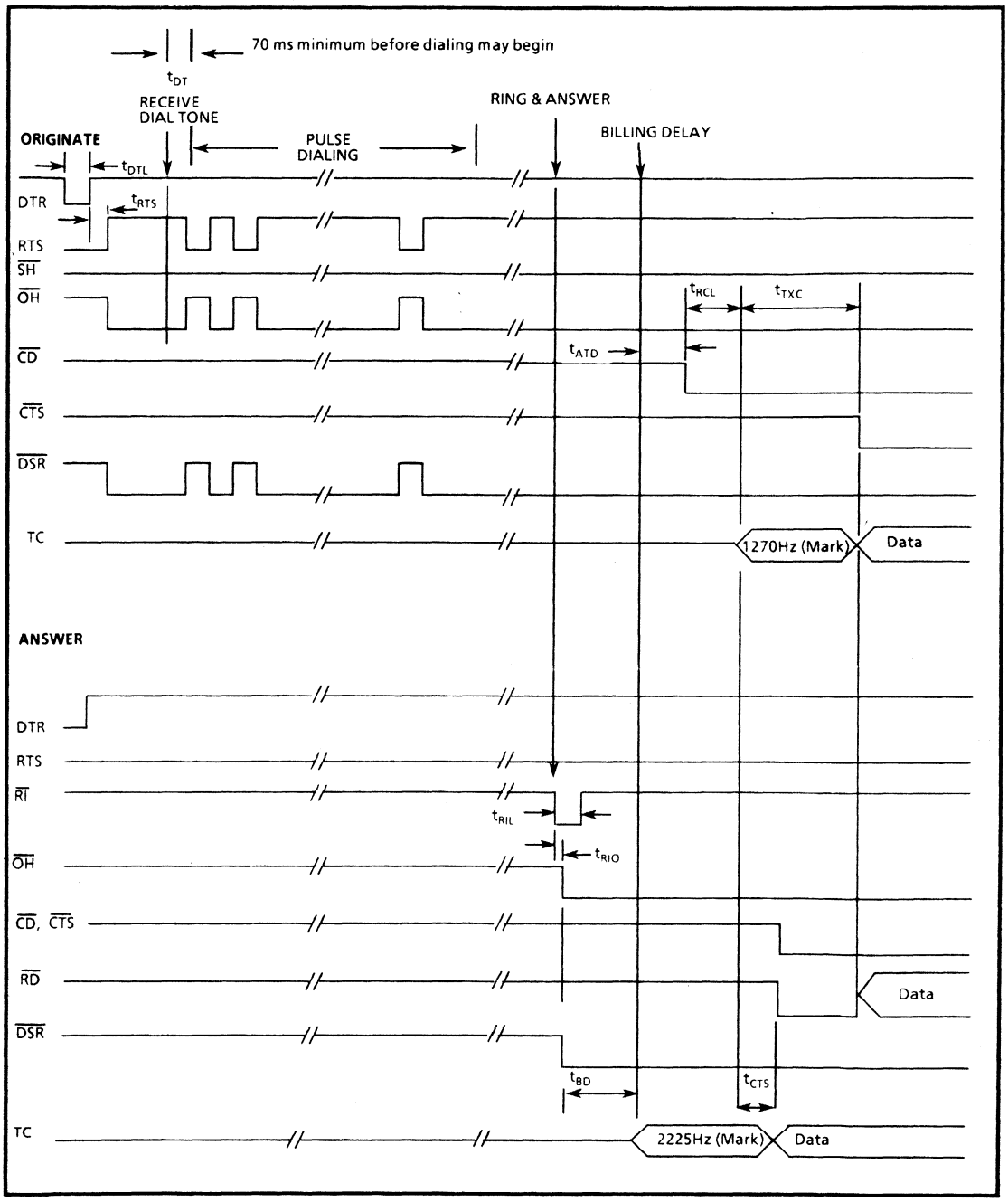


Figure 2 - MT3530 Modem Timing Chart for Bell 103 Operating Mode

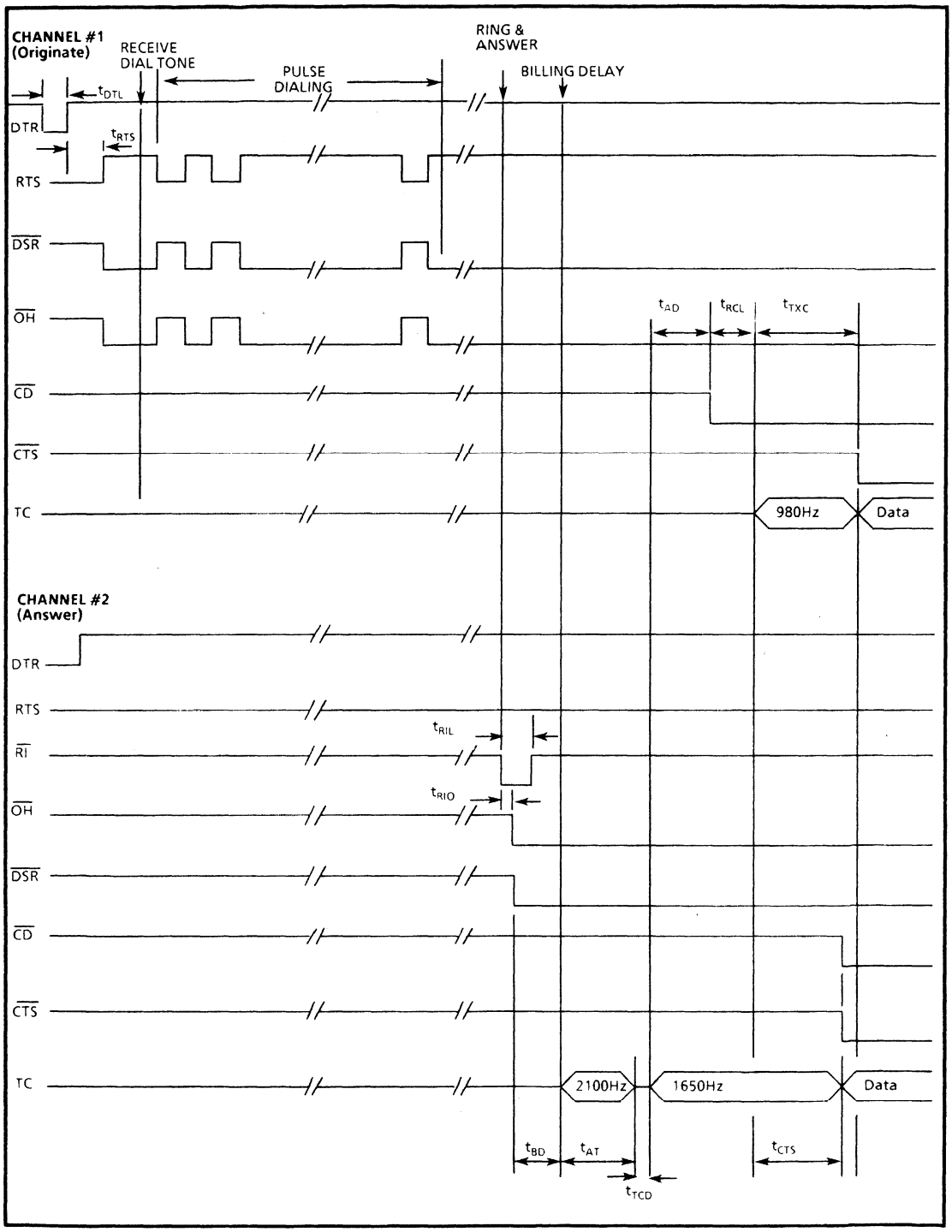


Figure 3 - MT3530 Modem Timing Chart for CCITT V.21 Operating Mode

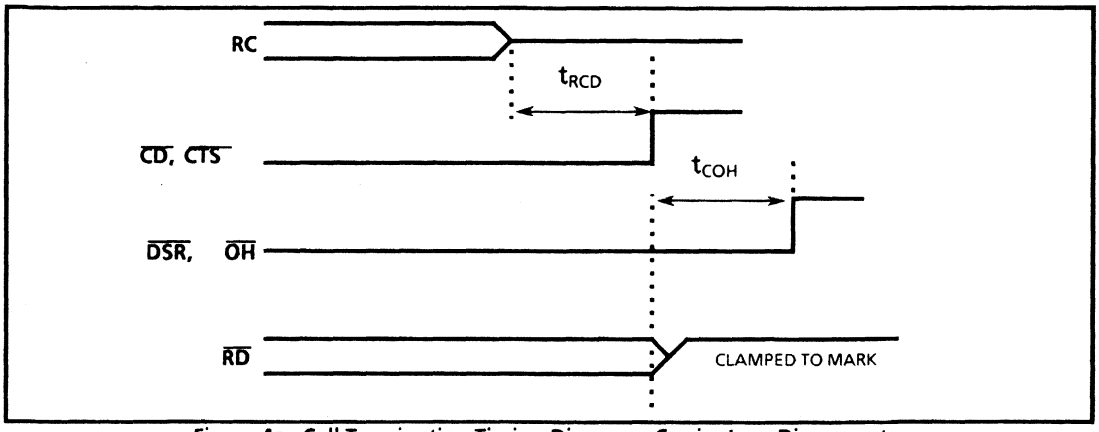


Figure 4a - Call Termination Timing Diagram - Carrier Loss Disconnect

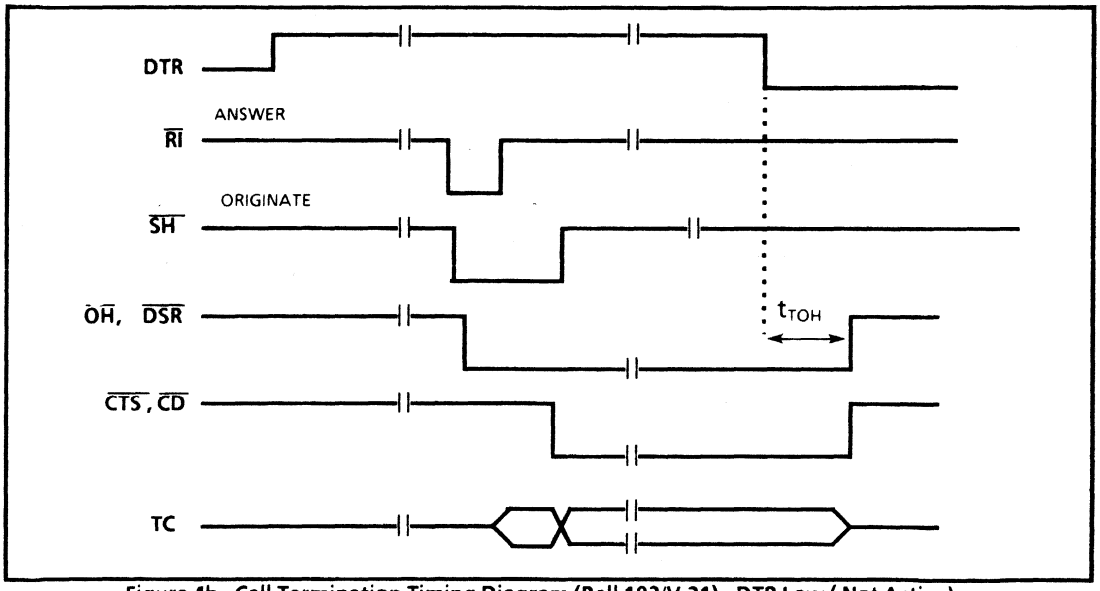


Figure 4b - Call Termination Timing Diagram (Bell 103/V.21) - DTR Low (Not Active)

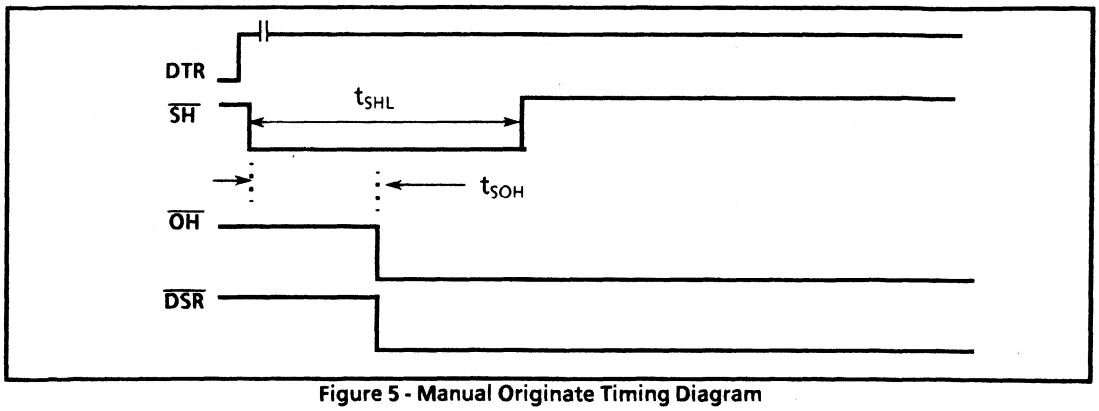


Figure 5 - Manual Originate Timing Diagram

Pin Description

Pin #	Name	Description
1	DL	**Digital Loopback** (TTL Input) - A High level on this input causes the device to enter the Digital Loopback mode. In this mode, the received data from the remote end is internally looped back to TD and $\overline{DSR}$ is forced High to signal to the DTE that the modem is not ready for transmission. The received data is not available on $\overline{RD}$ pin during the DL mode.
2	TP	**Test Point** - Test pin must be connected to either VEE or VDD for normal operations.
3	EP	**Eye Pattern** - Output (analog) of the demodulator prior to slicing. Do not load.
4	VDD	Positive power pin (+ 5 V).
5	RC	**Receive Carrier** - This analog input is the data carrier received by the Data Access Arrangement from the line. The modem demodulates this signal to generate the receive data bits.
6 7	TEST1 TEST0	These are test inputs and must be tied to VEE for normal applications. See Table 3 under Passthru mode.
8	NC	**No Connect**
9	AGND	**Analog Ground** - (0 Volt).
10	TC	**Transmit Carrier** - This analog output is the modulated transmit data carrier. Its frequency depends upon whether the modem is in the Answer or Originate mode and if a Mark or Space condition is being sent (Table 2).
11	SL	**Select** - A High on this input selects the CCITT V.21 data transmission format. Applying a Low selects the Bell 103 data transmission format.
12	OSCi	**Oscillator Input** - A 3.579545 MHz crystal can be connected between OSCi and OSCo. All internal clock signals are derived from this time base. Additional 20 pF caps to V_{EE} from each pin are required. An external clock signal may instead be applied at the OSCi input.
13	OSCo	**Oscillator Output** - This is not connected when external clock is applied at at the OSCi input.
14	$\overline{DSR}$	**Data Set Ready** - This output, when Low, indicates to the data terminal that the modem is ready to transmit data.
15	VEE	Negative power input pin (- 5 V).
16	CDT	**Carrier Detect Threshold** - Applying a variable voltage between 0 and - 5 V_{DC} at this input pin allows control of the receiver carrier detection threshold. This will override the internally determined threshold. If CDT is set to a voltage between + 1.5 V and + 2.0 V the AGC will be disabled during the test modes of pins 6 and 7.
17	DGND	**Digital Ground** - (0 Volt).
18	$\overline{SH}$	**Switchhook** - This input is used to manually place the device in the Originate mode. The device will make the $\overline{OH}$ output Low and start the Originate sequence if $\overline{SH}$ is Low and DTR is High. This can be a level or a momentary low-going pulse input (min. 54 ms). A pulse duration of less than 27 ms will not be detected. $\overline{RI}$ should be High if $\overline{SH}$ is to be exercised. Once $\overline{RI}$ has been activated then RTS has no effect.
19	$\overline{RI}$	**Ring Indicator** - This input when High permits auto answer capability. The Data Access Arrangement should apply a Low level to $\overline{RI}$ when a ringing signal is detected. The level should be Low for at least 107 ms. The input can remain Low until reset by DTR or loss of carrier. Similarly, in Manual mode, the Answer Mode is entered by applying a Low to this input, unless RTS is High.

Pin Description (continued)

Pin #	Name	Description
20	RTS	**Request To Send** - This controls data transmission from the modulator. A High on this input with the DTR input High (in the On condition) causes the device to enter the Originate mode. $\overline{OH}$ will go Low to seize the phone line. Auto dialing can be performed by turning the RTS input High and Low to effect dial pulsing. This input must remain High for the duration of data transmission. (Auto and manual answer will not function if RTS is High).
21	$\overline{CD}$	**Carrier Detect** - The output goes Low (On) to indicate that the receive data carrier has been received. It goes High (Off) if the received data carrier falls below the carrier detection threshold.
22	$\overline{RD}$	**Received Data** - The device presents data bits demodulated from the received data carrier at this output. This output is forced High if DTR is Low or Carrier Detect is High (Off).
23	$\overline{CTS}$	**Clear To Send** - This output goes Low at the completion of the handshaking sequence and goes High when the modem disconnects. It is always High if the device is in the Digital Loopback mode. Data to be transmitted should not be applied at the TD input until this output goes Low (active).
24	$\overline{OH}$	**Off-Hook** - This output goes to Low when either the RTS or $\overline{SH}$ input is active in the Originate mode and when a valid ring signal is detected on the $\overline{RI}$ input in the Answer mode.This outputis High if DTR is Low or if the disconnect sequence has been completed.
25	DTR	**Data Terminal Ready** - A High on this input enables all the other inputs and outputs and must be present before the device will enter the data mode either manually or automatically. The device will enter an irreversible disconnect sequence if the input goes Low for more than 14 ms during a data call. A pulse duration of less than 6 ms will not be detected.
26	AL	**Analog Loopback**- This input allows the data terminal to make the telephone line busy (Off-Hook) and implement the Analog Loopback mode. A High at this input while DTR is High causes the device to make the OH output Low and to enter the Analog Loopback mode. The receive filter center frequency is switched to correspond to the transmit filter center frequency and the transmit data carrier output is internally connected to the receive data carrier input, as well as being available at TC.
27	TD	**Transmit Data** - Data bits to be transmitted are presented to this input serially by the data terminal. A High is considered a binary '1' or Mark and a Low is considered a binary '0' or Space. The data terminal should hold this input in the Mark state when data is not being transmitted. During handshaking this input is ignored.
28	CLK	**Clock** - A 4.8 kHz LSTTL compatible square wave output is provided for supplying the 16 times clock signal required by a UART for 300 bps data rate. This output facilitates the integration of the modem function in the data terminal.

Introduction

The MT3530 is a low-speed full duplex modem designed for use in stand-alone modem applications and applications in which the modem function is designed directly into the Data Terminal Equipment (DTE). The MT3530 contains on-chip FSK modulator and demodulator, transmit and receive filters and a supervisory control section. The modem can be used in many different modes. These include Answer/Originate modes, automatic/manual modes, automatic abort, automatic disconnect and Passthru.

Functional Description

Figure 1 illustrates the functionality of the MT3530 modem. The modulator section converts input serial digital data into a square wave of the frequency corresponding to the Mark/Space being sent. The transmit filter outputs a Frequency Shift Keying signal at the TC (Transmit Carrier) output. The frequency of the FSK signal corresponds to the fundamental frequency of the square wave at the input of the filter. The incoming analog signal from the telephone network is bandlimited (filtered) and limited (amplified/clipped) prior to the demodulator carrier input to remove adjacent channel interference and system noise. The output at the receive data pin is a digital logic "1" or "0". The supervisory control and timing section contains the necessary logic to provide initial inter-modem handshaking as well as operational protocol, such as automatic Answer, Originate only and automatic disconnect. Two diagnostic modes, analog and Digital Loopbacks, allow for system tests. In addition, Passthru mode is available whereby the protocol handshake is disabled. The modem I.C. may be operated in Bell 103/113 or CCITT V.21 type applications. The select (SL) pin defines the operating mode. See Table 2.

Operation of MT3530 Modem Chip

A. Bell 103/113

Answer Mode

In the answer mode the MT3530 is idle waiting for an incoming call. As long as DTR is High, when a Low from the ring detector is presented to $\overline{RI}$ the MT3530 sets $\overline{OH}$ and $\overline{DSR}$ Low. This enables the hook-switch relay. This connects the modem to the phone line in the Answer mode. The MT3530 waits 2.0 s (min.), then sends carrier at 2225 Hz (Mark) to the originating modem. When the originating modem returns with 1270 Hz (Mark) the carrier detect circuit turns on within 120 ms and sets $\overline{CD}$ and $\overline{CTS}$ Low, indicating the handshaking sequence is completed. Data can now be sent and received.

Originate Mode

In the Originate mode a call is initiated, if DTR is High, by applying a High to the RTS input in auto mode or a negative pulse or Low to $\overline{SH}$ in manual mode. This will cause $\overline{OH}$ to go Low pulling in the hook-switch relay to connect the telephone line, and putting the MT3530 in the Originate mode.

After a suitable time, or when dial tone is detected, RTS can be pulsed Low/High to provide dial pulses. (N.B $\overline{OH}$ only follows RTS. The proper timing for dialing must come from the terminal on the RTS line.) The $\overline{OH}$ will go Low and High, pulsing the line with desired digits. When the answering modem comes on line it will wait 2.0 s minimum ("billing delay") and then send the 2225 Hz Answer Tone. 120 ms later the $\overline{CD}$ output goes Low indicating received carrier. 200 ms later it will respond with 592 ms (min.) of 1270 Hz carrier. At the end of that time $\overline{CTS}$ (Clear-to-Send) will go Low indicating to the terminal side that the communications link has been established.

SL (Select)	Mode	Transmit Frequency (Hz)*		Receive Frequency (Hz)*	
		Mark	Space	Mark	Space
0	Bell 103 Originate Bell 103 Answer	1270 2225	1070 2025	2225 1270	2025 1070
1	CCITT V.21 Channel 1 (Originate) CCITT V.21 Channel 2 (Answer)	980 1650	1180 1850	1650 980	1850 1180
	CCITT V.25 Answer Tone	2100			

Table 2 - Bell 103/CCITT V.21 Operating Modes

Space = Binary 0, Mark = Binary 1, Crystal Frequency = 3.579545 MHz, *Frequency drift = ± 3 Hz

Abort Mode

There is an automatic abort feature in the MT3530 to avoid tying up a system should there be difficulty in establishing the link. If no carrier is detected within 14 seconds after the device has been put into the Answer or Originate mode it will abort the call by setting High $\overline{OH}$ and disconnecting the telephone line. $\overline{DSR}$ will, also, go High. This abort time can be extended by pulsing RTS Low for 1 ms minimum before the 14 seconds have elapsed. This will reset the abort timer. If it does time out DTR will need to be pulsed High to reset the MT3530. After Abort mode it resorts to Originate mode.

Shutdown Mode

Should the received carrier fall below – 50 dBm during data exchange for more than 190 ms the MT3530 will terminate the call and go on-hook, disconnecting the telephone line. (See Figure 4a.)

Manual Operation

The MT3530 can be operated manually as well as automatically. To put it in the Answer mode apply a negative pulse (– 5V) on $\overline{RI}$ of greater than 107 ms. If $\overline{RI}$ is tied Low then the device will go into the Answer mode whenever DTR is set High.

Similarly, to put it into the Originate mode, $\overline{SH}$ can be pulled Low for more than 54 ms. By tying $\overline{SH}$ Low, the MT3530 will go into the Originate mode whenever DTR is set High.

Passthru Mode

With the control of "TEST0" and "TEST1" pins the MT3530 can be put into the Passthru mode. See Table 3 for setup. In this mode the modem stands idle in the Originate mode and the transmit and receive functions become independent of each other. In this mode the timing and handshake protocol can be suspended, depending on the status of DTR.

With DTR set Low, the transmit and receive functions become independent of the timing and handshake protocol. All the events on Switch-Hook, Ring Indicator and Request-To-Send input pins are ignored.

With DTR High, Answer or Originate mode is selected in the same manner as in the normal mode. The transmit and receive functions are dependent on the timing and handshake protocol. Carrier Detect operates as in the normal mode. Auto Shutdown applies but Auto Abort does not apply. After call termination the modem is placed in the Originate mode.

TEST0 PIN 7	TEST1 PIN 6	MT3530 STATUS	H = + 5 V (V_{DD}) L = – 5 V (V_{EE})
L	L	Normal	
H	L	Passthru	

Table 3 - Passthru Mode Control Inputs

B. CCITT V.21 Mode

The MT3530 will perform the same operations described above in the CCITT V.21 mode if the SL pin is tied High. The basic principle is the same but the frequencies and the timings are switched to conform to V.21 specifications. See the timing charts (Figures 3 and 4) and Table 2 for additional details. When in V.21 mode the V.25 Answer Tone of 2100 Hz will be generated upon answering.

External Clock Requirements

To use an external 3.579545 MHz clock a TTL level, 50 % duty cycle, square wave can be applied to pin 12, OSCi, through a 0.1 μF capacitor.

Diagnostic Modes

The MT3530 has two diagnostic modes available to the operator. By putting the AL pin High while DTR is High, the device enters the Analog Loopback Mode. $\overline{OH}$ goes Low to busy out the phone line.

The receive filter center frequency moves to the transmit center frequency and TC signal is internally connected to the RC input. The transmit signal also remains available on the TC pin. Thus, any digital input at TD is coded and sent out via TC, and at the same time back through the analog input, decoded, and out on the $\overline{RD}$ pin.

By putting the DL pin High the MT3530 enters Digital Loopback mode. In this mode any data received from the remote end of the telephone line is retransmitted back to its source and $\overline{DSR}$ is forced High. Note that the digital data is not available at the $\overline{RD}$ output in this mode. See Table 4.

Test Mode	Status Lines†						
	DTR	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RD}$
AL	H	H	L	L	L	L	L
DL	H	H	H	L	H	H	H

Table 4 - Control Status During Diagnostic Modes

† (L = Low, H = High)

Application

Two typical MT3530 system configurations are illustrated. Figure 6 shows a stand-alone RS-232 interface modem to be used as a peripheral accessory to a communications terminal or computer.

Figure 7 shows an add-on modem for building into a computer and connecting to the internal parallel bus structure. The ACIA or UART does the parallel-to-serial and serial-to-parallel conversion required.

Both configurations are intended for direct connection to the telephone line. This requires meeting FCC Part 68 for network protection.

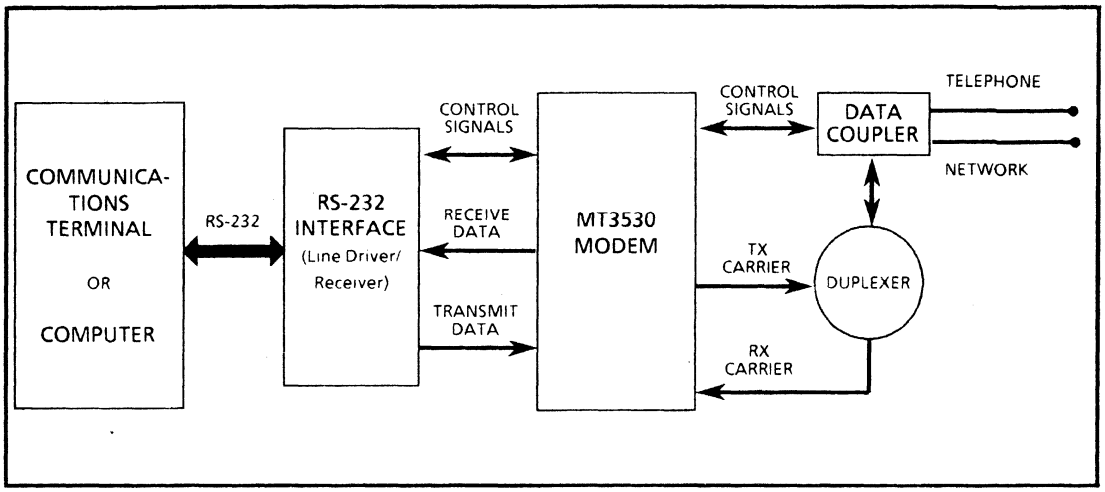


Figure 6 - Serial Interface System Configuration for MT3530

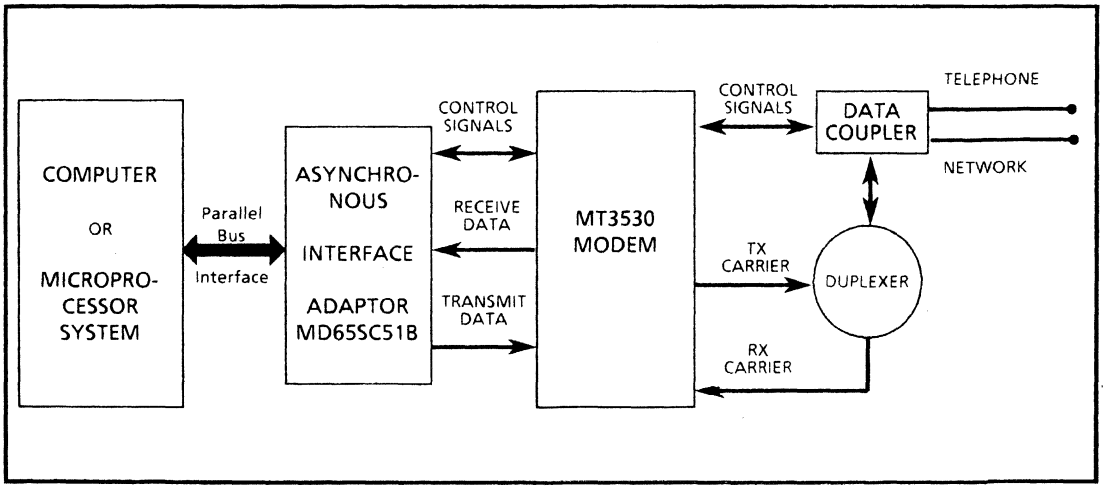


Figure 7 - Parallel Interface System Configuration for MT3530

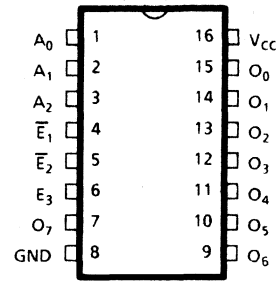
Microprocessor Peripherals and Logic Circuits

MD54/74HCT138R
1 of 8 Octal Decoder/Demultiplexer
February '85

Features

- High latch-up immunity
- High current outputs can drive 15 LSTTL loads
- Low power ISO-CMOS technology
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS138 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



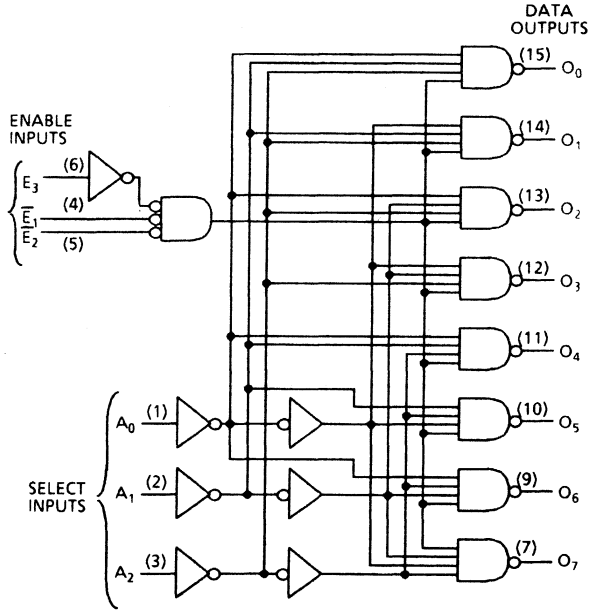
Description

This ISO-CMOS, MSI circuit is designed for use in high speed memory and peripheral address decoding systems. The MD54/74HCT138 will decode 3 binary inputs (A_0, A_1,A_2) to select one of eight mutually exclusive outputs (O_0 - O_7). Three enable inputs, two active LOW ($\overline{E_1}$, $\overline{E_2}$) and one active HIGH (E_3), reduce the need for external gates in an expanded system. A 1 of 32 decoder requires only four of these devices and one external inverter. The enable inputs can be used as the data input for demultiplexing applications.

Ordering Information

MD54HCT138RC, Cerdip
-55°C to 125°C

MD74HCT138RE, Plastic Dip
-40°C to 85°C



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
E_3	$\overline{E_1}$	$\overline{E_2}$	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = logic "1", L = logic "0", X = don't care

MD54/74HCT139R

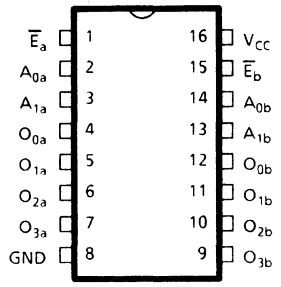
Dual 1 of 4 Decoder/Demultiplexer

February '85

Features

- High latch-up immunity
- High current outputs can drive 15 LSTTL loads
- Low power ISO-CMOS technology
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS139 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



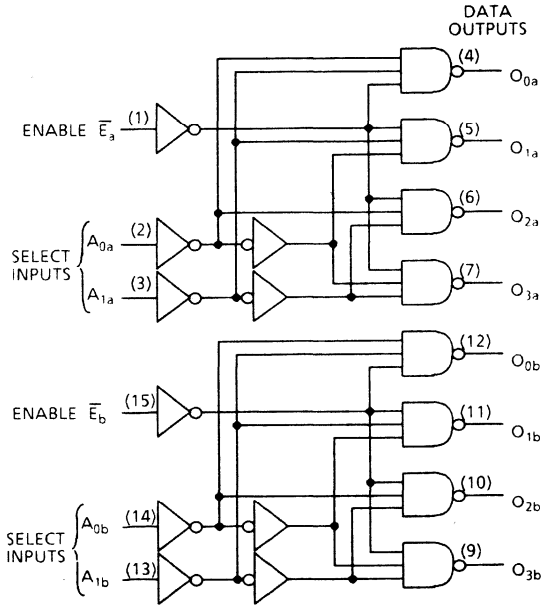
Ordering Information

MD54HCT139RC, Cerdip
-55°C to 125°C

MD74HCT139RE, Plastic Dip
-40°C to 85°C

Description

This ISO-CMOS, MSI circuit is designed for use in high speed memory and peripheral, address decoding systems. The MD54/74HCT139 will decode 2 binary inputs (A_0, A_1) to select one of four mutually exclusive outputs (O_0 - O_3). The enable inputs, active LOW ($\overline{E}_a$, $\overline{E}_b$) independantly control the two separate 1 of 4 decoder/demultiplexers.



FUNCTION TABLE

(each decoder/demultiplexer)

INPUTS		OUTPUTS
ENABLE	SELECT	
$\overline{E}$	A_1 A_0	O_0 O_1 O_2 O_3
H	X X	H H H H
L	L L	L H H H
L	L H	H L H H
L	H L	H H L H
L	H H	H H H L

H = logic "1", L = logic "0", X = don't care

TABLE 1. **Absolute Maximum Ratings①, Standard Output Devices**

	PARAMETER	SYMBOL	VALUE	UNIT
1	Supply Voltage	V_{CC}	-0.5 to 7.5	V
2	Input Voltage	V_{IN}	-0.9 to V_{CC} + 0.9	V
3	Output Voltage	V_{OUT}	-0.9 to V_{CC} + 0.9	V
4	Clamp Diode Current, Per Pin	I_K②	± 60	mA
5	DC Output Current, Per Output Pin	I_{OUT}	± 80	mA
6	DC V_{CC} or Ground Current	I_{CC}	± 80	mA
7	Storage Temperature	T_S	-65 to + 150	°C
8	Package Power Dissipation DIP CERDIP	P P	450 1000	mW mW

① Exceeding these ratings may cause permanent damage . Functional operation under these conditions is not implied.
② I_K is the current required to initiate latch-up.

TABLE 2. **Recommended Operating Conditions, Standard Output Devices**

	PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
1	Supply Voltage	V_{CC}	1.5	7.0	V
2	Input Voltage	V_{IN}	0.0	V_{CC}	V
3	Output Voltage	V_{OUT}	0.0	V_{CC}	V
4	Operating Temperature 74HCT 54HCT	T_A T_A	-40 -55	+85 +125	°C °C
5	Input Rise and Fall Time	t_r, t_f	0	500	ns

TABLE 3. **D.C. Characteristics, Standard Output Devices** V_{CC} = 5V ± 10%, V_{SS}/GND = 0V

	CHARACTERISTICS	SYM	V_{CC}	25°C		74HCT -40 to 85°C		54HCT -55 to 125°C		UNIT	TEST CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
1	Input High Level	V_{IH}	4.5 to 5.5	2.0		2.0		2.0		V	
2	Input Low Level	V_{IL}	4.5 to 5.5		0.8		0.8		0.8	V	
	Output High Level	V_{OH}	4.5								V_{IN} = V_{IH} or V_{IL}
3				4.40		4.40		4.40		V	I_{OH} = -20μA
4				3.98		3.84		3.70		V	I_{OH} = -4 mA
5				2.60		2.50		2.40		V	I_{OH} = -7 mA
	Output Low Level	V_{OL}	4.5								V_{IN} = V_{IH} or V_{IL}
6					0.10		0.10		0.10	V	I_{OL} = 20μA
7					0.32		0.37		0.40	V	I_{OL} = 6 mA
8	Input Leakage	I_I	5.5		0.1		1.0		1.0	μA	V_{IN} = V_{CC} or GND
9	Quiescent Current	I_{CC}	5.5		4		80		160	μA	V_{IN} = V_{CC} or GND Outputs unloaded

MD54/74HCT138R ***TABLE 4.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 1, Recommended operating conditions Table 2, D.C. characteristics Table 3,Timing waveforms Figure 1, Test load Figure 2.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	TYP	MAX	TYP	MAX		
1	Address to Output	t_{PLH}	18	32		35		38	ns	
2	Address to Output	t_{PHL}	20	35		39		41	ns	
3	E to Output	t_{PLH}	22	36		40		43	ns	
4	E to Output	t_{PHL}	22	36		40		43	ns	
5	Input Capacitance	C_I	3	8					pF	V_{IN} = V_{CC} or GND

MD54/74HCT139R ***TABLE 5.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 1, Recommended operating conditions Table 2, D.C. characteristics Table 3,Timing waveforms Figure 1, Test load Figure 2.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	TYP	MAX	TYP	MAX		
1	Address to Output	t_{PLH}	17	30		34		36	ns	
2	Address to Output	t_{PHL}	18	32		35		38	ns	
3	E to Output	t_{PLH}	20	30		34		36	ns	
4	E to Output	t_{PHL}	21	32		35		38	ns	
5	Input Capacitance	C_I	3	8					pF	V_{IN} = V_{CC} or GND

Figure 1. **Timing Diagrams for Standard Output Devices**

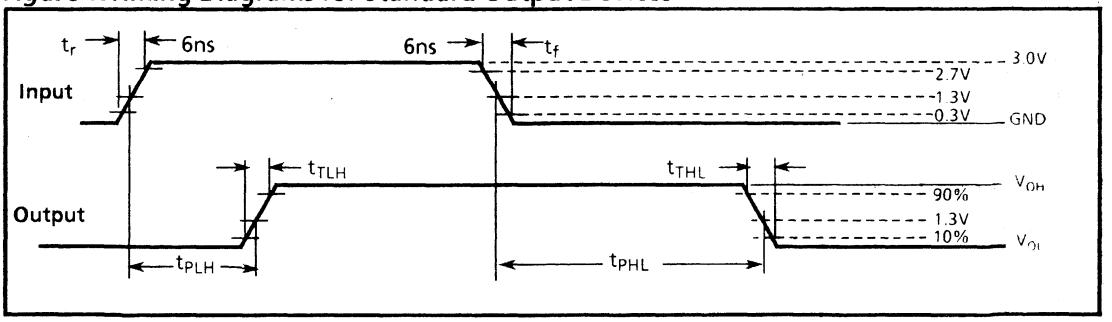
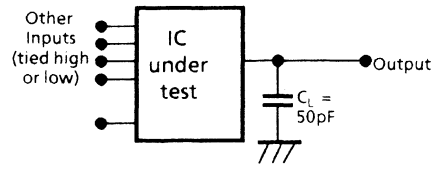


Figure 2. **Test Load Circuit for Standard Output Devices**

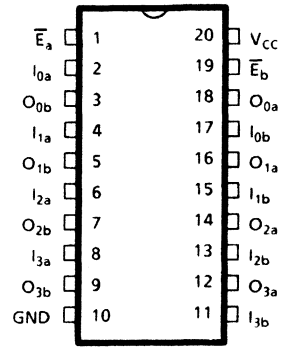


MD54/74HCT240R
Inverting Octal Line Driver/Buffer
February '85

Features

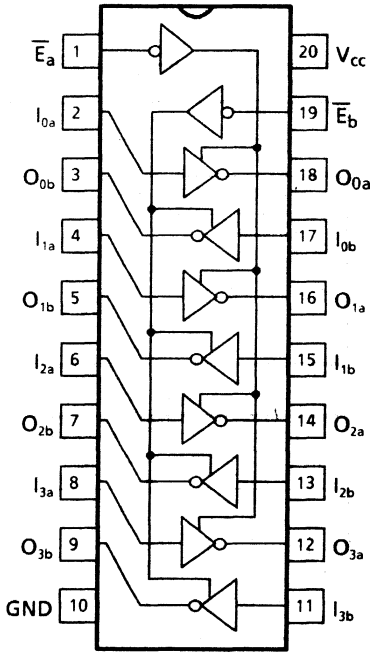
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS240 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed to improve P.C. board density and performance in three-state memory address drivers, clock drivers, and bus oriented receivers/transmitters. The MD54/74HCT240R offers inverting three-state buffers controlled by two complementary enable pins. The '240R is functionally identical to the '540R but has a non-bus-oriented pin-out.



Ordering Information

MD54HCT240RC, Cerdip
-55°C to 125°C

MD74HCT240RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
$\overline{E}_a$, $\overline{E}_b$	Data Output Enable
I_{0a} to I_{3a}	Data Inputs (a)
I_{0b} to I_{3b}	Data Inputs (b)
O_{0a} to O_{3a}	Data Outputs (a)
O_{0b} to O_{3b}	Data Outputs (b)
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE (A or B buffers)

INPUTS		OUTPUTS
$\overline{E}$	I_{0-3}	O_{0-3}
L	L	H
L	H	L
H	X	Z

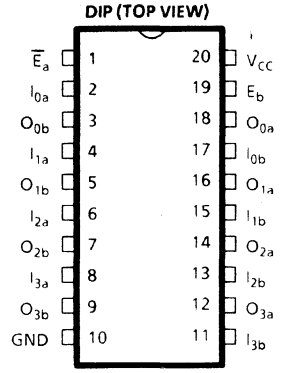
H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MD54/74HCT241R
Octal Line Driver/Buffer
February '85

Features

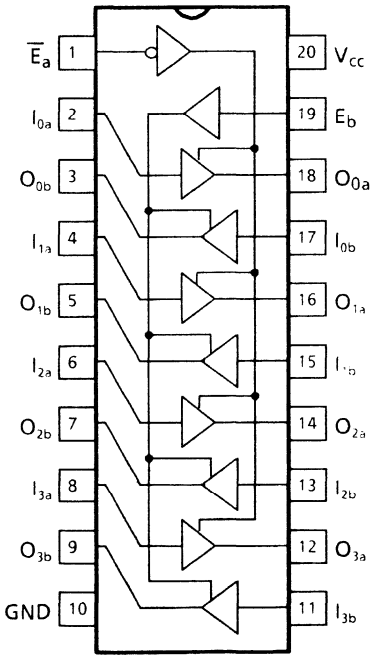
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS241 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed to improve P.C. board density and performance in three-state memory address drivers, clock drivers, and bus oriented receivers/transmitters. The MD54/74HCT241R offers non-inverting three-state buffers controlled by two complementary enable pins. The '241R is functionally identical to the '541R but has a non-bus-oriented pin-out.



Ordering Information

MD54HCT241RC, Cerdip
-55°C to 125°C

MD74HCT241RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
$\overline{E}_a$, E_b	Data Output Enable
I_{0a} to I_{3a}	Data Inputs (a)
I_{0b} to I_{3b}	Data Inputs (b)
O_{0a} to O_{3a}	Data Outputs (a)
O_{0b} to O_{3b}	Data Outputs (b)
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE

a BUFFERS			b BUFFERS		
INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_a$	I_{0-3}	O_{0-3}	E_b	I_{0-3}	O_{0-3}
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

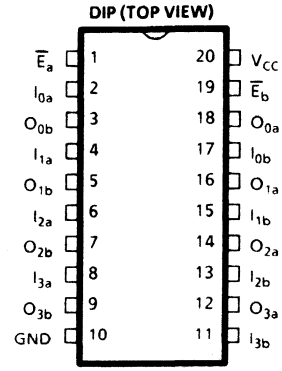
H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MD54/74HCT244R
Octal Line Driver/Buffer
February '85

Features

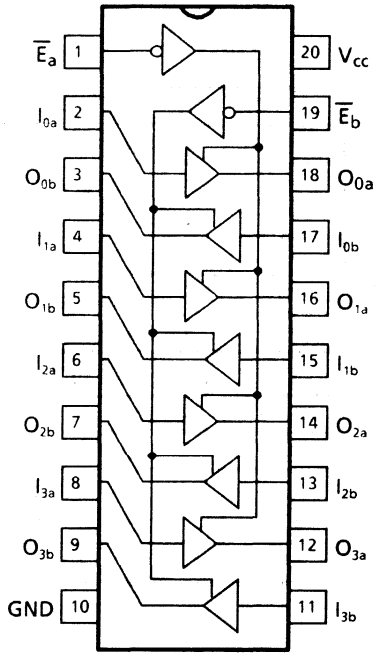
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS244 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

The ISO-CMOS Octal line driver/buffers are designed to improve P.C. board layout and performance in three-state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The MD54/74HCT244R offers non-inverting three-state buffers controlled by two active low enable pins.



Ordering Information

MD54HCT244RC, Cerdip
-55°C to 125°C

MD74HCT244RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
$\overline{E}_a$, $\overline{E}_b$	Data Output Enable
I_{0a} to I_{3a}	Data Inputs (a)
I_{0b} to I_{3b}	Data Inputs (b)
O_{0a} to O_{3a}	Data Outputs (a)
O_{0b} to O_{3b}	Data Outputs (b)
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE (a or b buffers)

INPUTS		OUTPUTS
$\overline{E}$	I_{0-3}	O_{0-3}
L	L	L
L	H	H
H	X	Z

H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MD54/74HCT245R

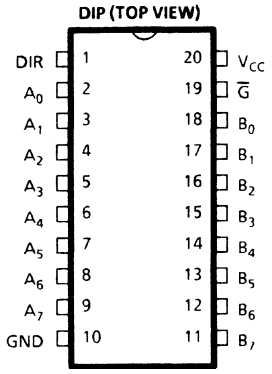
Octal Bus Transceiver with 3-State Buffered Outputs

February '85

Features

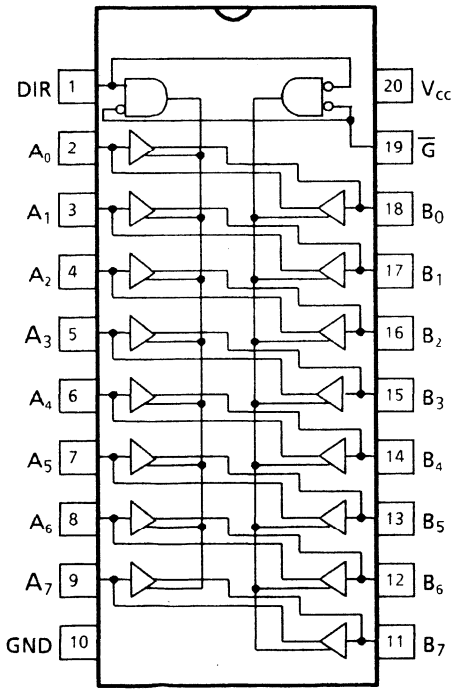
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS245 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed for high speed asynchronous two-way communication between data buses. The control inputs minimize external timing requirements. Data transmission from the A bus to the B bus, or from the B bus to the A bus, is provided depending upon the logic level at the direction control input (DIR) pin. The enable input ($\overline{G}$) pin can be used to disable the device outputs so that the buses are effectively isolated from each other.



Ordering Information

MD54HCT245RC, Cerdip
-55°C to 125°C

MD74HCT245RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
A_0 - A_7	Bus A, Data Inputs/Outputs
B_0 - B_7	Bus B, Data Inputs/Outputs
DIR	Direction Control Pin
$\overline{G}$	Enable Input, Active Low
V_{CC}	Supply Voltage
GND	System Ground

FUNCTION TABLE

INPUT	OUTPUT	
ENABLE ($\overline{G}$)	CONTROL (DIR)	OPERATION
L	L	B to A
L	H	A to B
H	X	ISOLATION

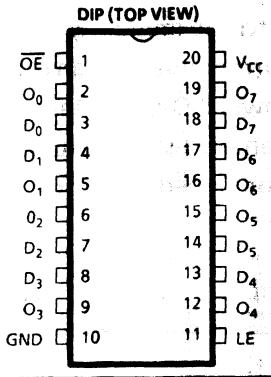
H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MD54/74HCT373R
Octal D-Type Transparent Latch
February '85

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS373 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



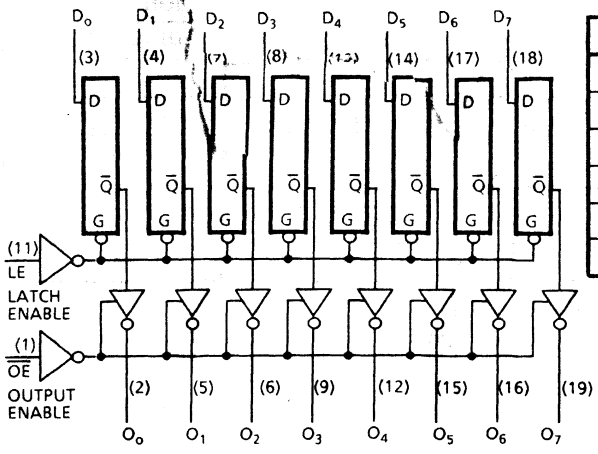
Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The MD54/74HCT373R appears transparent to data (outputs change asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, data meeting the set up times becomes latched. The state of the latches is unaffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance. Data may thus be latched even when the device is deselected. The '373R is functionally identical to the '573R but has a non-bus-oriented pin-out.

Ordering Information

MD54HCT373RC, Cerdip
-55°C to 125°C

MD74HCT373RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

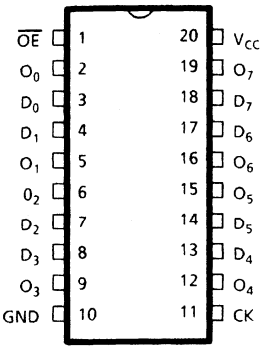
PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
LE	Latch Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

MD54/74HCT374R
Octal D-Type Flip Flop
February '85

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS374 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



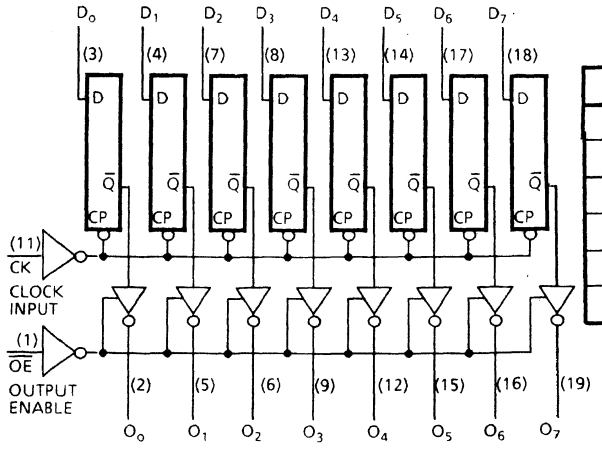
Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The latches hold their individual data when meeting set up times with the clock (CK) LOW to HIGH transition. The state of the latches is unaffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance. Data may thus be latched even when the device is deselected. The '374R is functionally identical to the '574R but has a non-bus-oriented pin-out.

Ordering Information

MD54HCT374RC, Cerdip
-55°C to 125°C

MD74HCT374RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

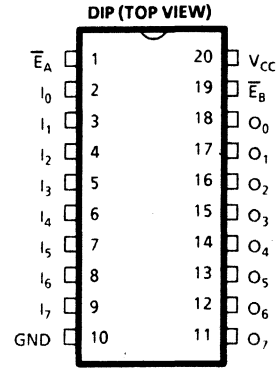
PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
CK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

MD54/74HCT540R
Inverting Octal Line Driver/Buffer
February '85

Features

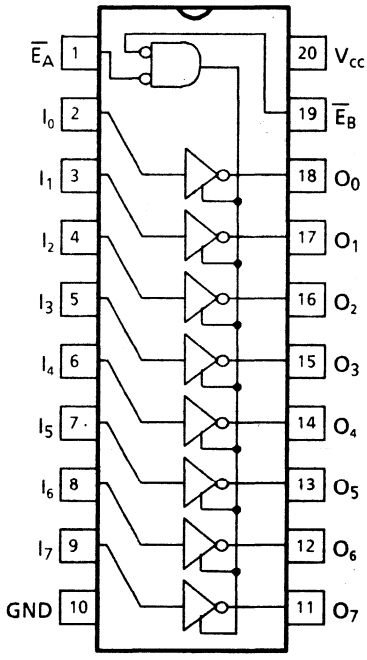
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS540 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed to improve P.C. board density and performance in three-state memory address drivers, clock drivers, and bus oriented receivers/transmitters. The MD54/74HCT540R offers inverting three-state buffers controlled by two active low enable pins. The '540R is functionally identical to the '240R, but has a bus-oriented pin-out.



Ordering Information

MD54HCT540RC, Cerdip
-55°C to 125°C

MD74HCT540RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
$\overline{E}_A$, $\overline{E}_B$	Data Output Enable
I_0 to I_7	Data Inputs
O_0 to O_7	Data Outputs
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{E}_A$	$\overline{E}_B$	I_0 to I_7	O_0 to O_7
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

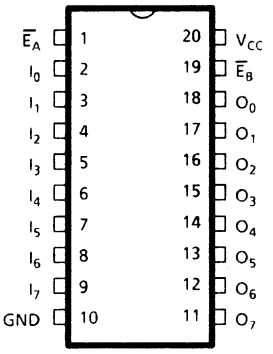
H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MD54/74HCT541R
Octal Line Driver/Buffer
February '85

Features

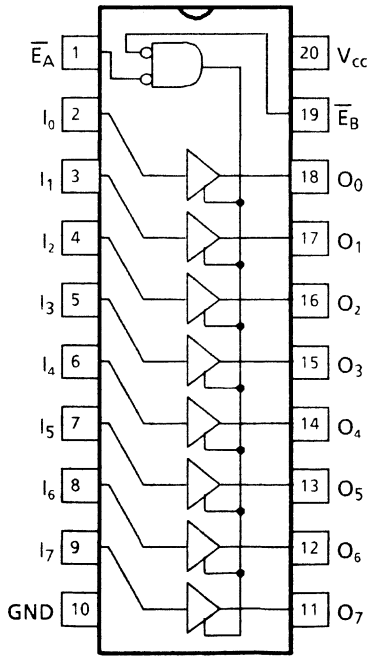
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS541 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed to improve P.C. board density and performance in three-state memory address drivers, clock drivers, and bus oriented receivers/transmitters. The MD54/74HCT541R offers non-inverting three-state buffers controlled by two active low enable pins. The '541R is functionally identical to the '241R, but has a bus-oriented pin-out



Ordering Information

MD54HCT541RC, Cerdip
-55°C to 125°C

MD74HCT541RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
$\overline{E}_A$, $\overline{E}_B$	Data Output Enable
I_0 to I_7	Data Inputs
O_0 to O_7	Data Outputs
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{E}_A$	$\overline{E}_B$	I_0 to I_7	O_0 to O_7
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

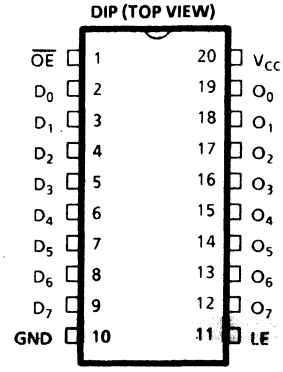
H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MD54/74HCT573R
Octal D-Type Transparent Latch
February '85

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS573 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



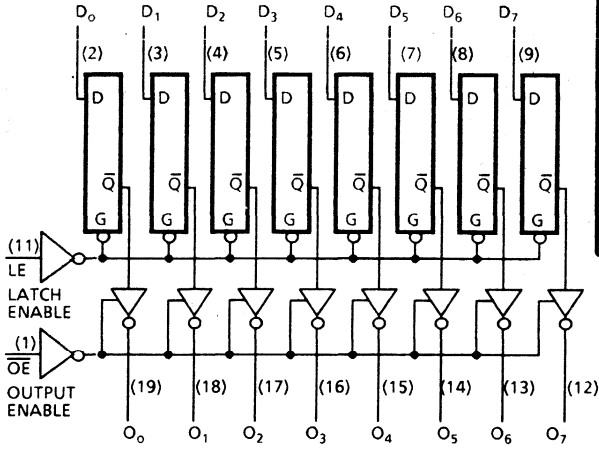
Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The MD54/74HCT573R appears transparent to data (outputs change asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, data meeting the set up times becomes latched. The state of the latches is unaffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance. Data may thus be latched even when the device is deselected. The '573R is functionally identical to the '373R but has a bus-oriented pin-out.

Ordering Information

MD54HCT573RC, Cerdip
-55°C to 125°C

MD74HCT573RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
LE	Latch Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

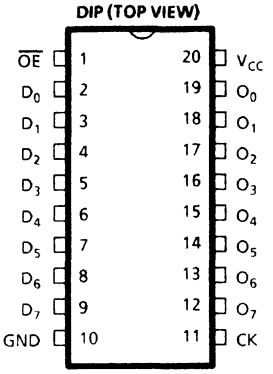
MD54/74HCT574R
Octal D-Type Flip Flop
February '85

MITEL®

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS574 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



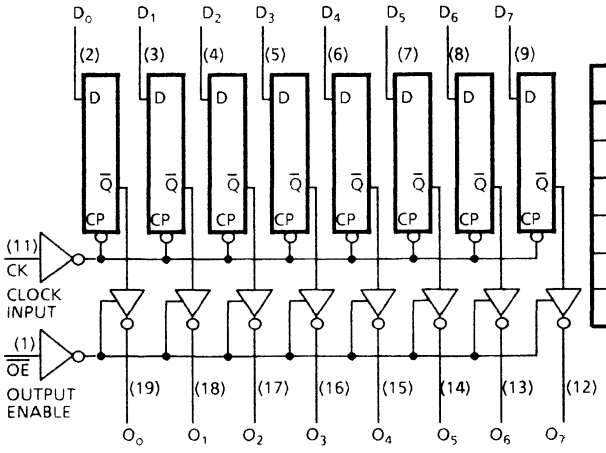
Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The latches hold their individual data when meeting set up times with the clock (CK) LOW to HIGH transition. The state of the latches is uneffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance. Data may thus be latched even when the device is deselected. The '574R is functionally identical to the '374R but has a bus-oriented pin-out.

Ordering Information

MD54HCT574RC, Cerdip
-55°C to 125°C

MD74HCT574RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
CK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

TABLE 6. **Absolute Maximum Ratings① Tri-State Output Devices**

	PARAMETER	SYMBOL	VALUE	UNIT
1	Supply Voltage	V_{CC}	-0.5 to 7.5	V
2	Input Voltage	V_{IN}	-0.9 to V_{CC} + 0.9	V
3	Output Voltage	V_{OUT}	-0.9 to V_{CC} + 0.9	V
4	Clamp Diode Current, Per Pin	I_K②	± 80	mA
5	DC Output Current, Per Output Pin	I_{OUT}	± 160	mA
6	DC V_{CC} or Ground Current	I_{CC}	± 160	mA
7	Storage Temperature	T_S	-65 to + 150	°C
8	Package Power Dissipation DIP CERDIP	P P	450 1000	mW mW

① Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
② I_K is the current required to initiate latch-up.

TABLE 7. **Recommended Operating Conditions Tri-State Output Devices**

	PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
1	Supply Voltage	V_{CC}	1.5	7.0	V
2	Input Voltage	V_{IN}	0.0	V_{CC}	V
3	Output Voltage	V_{OUT}	0.0	V_{CC}	V
4	Operating Temperature 74HCT 54HCT	T_A T_A	-40 -55	+ 85 + 125	°C °C
5	Input Rise and Fall Time	t_r, t_f	0	500	ns

TABLE 8. **D.C. Characteristics Tri-State Output Devices** V_{CC} = 5V ± 10%, V_{SS}/GND = 0V

	CHARACTERISTICS	SYM	V_{CC}	25°C		74HCT -40 to 85°C		54HCT -55 to 125°C		UNIT	TEST CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
1	Input High Level	V_{IH}	4.5 to 5.5	2.0		2.0		2.0		V	
2	Input Low Level	V_{IL}	4.5 to 5.5		0.8		0.8		0.8	V	
3	Output High Level	V_{OH}	4.5	4.40		4.40		4.40		V	V_{IN} = V_{IH} or V_{IL} I_{OH} = -20μA
4				3.98		3.84		3.70		V	I_{OH} = -6 mA
5				2.80		2.70		2.50		V	I_{OH} = -12 mA
6	Output Low Level	V_{OL}	4.5		0.10		0.10		0.10	V	V_{IN} = V_{IH} or V_{IL} I_{OL} = 20μA
7					0.32		0.37		0.40	V	I_{OL} = 12 mA
8	Input Leakage	I_I	5.5		0.1		1.0		1.0	μA	V_{IN} = V_{CC} or GND
9	3 - State Leakage	I_{OZ}	5.5		0.5		5.0		5.0	μA	V_{OUT} = V_{IH} or V_{IL}
10	Quiescent Current	I_{CC}	5.5		4		80		160	μA	V_{IN} = V_{CC} or GND Outputs unloaded

MD54/74HCT240R ***TABLE 9.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 3 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	18	25		30		32	ns	
2	High toLow Output	t_{PHL}	19	25		32		34	ns	
3	Enable to Low	t_{PZL}	23	35		39		41	ns	
4	Enable to High	t_{PZH}	19	29		32		34	ns	
5	Disable from Low	t_{PLZ}	25	35		42		45	ns	
6	Disable from High	t_{PHZ}	23	35		39		41	ns	
7	Input Capacitance	C_I	3	8					pF	V_{IN} = V_{CC} or GND

MD54/74HCT241R ***TABLE 10.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 4 and Figure 5, Test load Figure 5

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	15	24		27		29	ns	
2	High toLow Output	t_{PHL}	16	26		29		31	ns	
3	Enable to Low	t_{PZL}	23	35		39		41	ns	
4	Enable to High	t_{PZH}	23	35		39		41	ns	
5	Disable from Low	t_{PLZ}	25	38		42		45	ns	
6	Disable from High	t_{PHZ}	26	39		44		47	ns	
7	Input Capacitance	C_I	3	8					pF	V_{IN} = V_{CC} or GND

MD54/74HCT244R ***TABLE 11.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 3 and Figure 5, Test load Figure 5

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	15	23		26		28	ns	
2	High to Low Output	t_{PHL}	16	24		27		29	ns	
3	Enable to Low	t_{PZL}	23	35		39		41	ns	
4	Enable to High	t_{PZH}	19	29		32		34	ns	
5	Disable from Low	t_{PLZ}	25	35		42		45	ns	
6	Disable from High	t_{PHZ}	23	35		39		41	ns	
7	Input Capacitance	C_I	3	8					pF	V_{IN} = V_{CC} or GND

MD54/74HCT245R *TABLE 12.* A.C. Characteristics V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 4 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	15	23		26		28	ns	
2	High toLow Output	t_{PHL}	16	24		27		29	ns	
3	Enable to Low	t_{PZL}	24	36		40		43	ns	
4	Enable to High	t_{PZH}	20	30		34		36	ns	
5	Disable from Low	t_{PLZ}	26	39		44		47	ns	
6	Disable from High	t_{PHZ}	24	36		40		49	ns	
7	Input Capacitance	C_I	3	8					pF	$V_{IN} = V_{CC}$ or GND

MD54/74HCT540R *TABLE 13.* A.C. Characteristics V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 3 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	18	25		30		32	ns	
2	High toLow Output	t_{PHL}	19	25		32		34	ns	
3	Enable to Low	t_{PZL}	24	36		40		43	ns	
4	Enable to High	t_{PZH}	20	30		34		36	ns	
5	Disable from Low	t_{PLZ}	26	39		44		47	ns	
6	Disable from High	t_{PHZ}	24	36		40		43	ns	
7	Input Capacitance	C_I	3	8					pF	$V_{IN} = V_{CC}$ or GND

MD54/74HCT541R *TABLE 14.* A.C. Characteristics V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 4 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	15	24		27		29	ns	
2	High toLow Output	t_{PHL}	16	26		29		31	ns	
3	Enable to Low	t_{PZL}	24	36		40		43	ns	
4	Enable to High	t_{PZH}	20	30		34		36	ns	
5	Disable from Low	t_{PLZ}	26	39		44		47	ns	
6	Disable from High	t_{PHZ}	24	36		40		43	ns	
7	Input Capacitance	C_I	3	8					pF	$V_{IN} = V_{CC}$ or GND

MD54/74HCT373R ***TABLE 15.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 6 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	17	26		29		31	ns	
2	High toLow Output	t_{PHL}	17	26		29		31	ns	
3	Enable to Low	t_{PZL}	18	27		30		32	ns	
4	Enable to High	t_{PZH}	20	30		34		36	ns	
5	Disable from Low	t_{PLZ}	19	29		32		34	ns	
6	Disable from High	t_{PHZ}	24	36		40		43	ns	
7	LE to Output	t_{PLE}	23	35		39		41	ns	
8	Set-up Time	t_{SU}			20		20		ns	
9	Hold Time	t_H			0		0		ns	
10	Minimum Pulse Width	t_W			20		20		ns	
11	Input Capacitance	C_I	3	8					pF	$V_{IN} = V_{CC}$ or GND

MD54/74HCT374R ***TABLE 16.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 7 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	CK to High Output	t_{PLH}	20	30		34		36	ns	
2	CK toLow Output	t_{PHL}	22	33		37		40	ns	
3	Enable to Low	t_{PZL}	18	27		30		32	ns	
4	Enable to High	t_{PZH}	20	30		34		36	ns	
5	Disable from Low	t_{PLZ}	19	29		32		34	ns	
6	Disable from High	t_{PHZ}	24	36		40		43	ns	
7	Set-up Time	t_{SU}			20		20		ns	
8	Hold Time	t_H			0		0		ns	
9	Minimum Pulse Width	t_W			20		20		ns	
10	Input Capacitance	C_I	3	8					pF	$V_{IN} = V_{CC}$ or GND

MD54/74HCT573R ***TABLE 17.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 6 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	Low to High Output	t_{PLH}	17	26		29		31	ns	
2	High toLow Output	t_{PHL}	17	26		29		31	ns	
3	Enable to Low	t_{PZL}	18	27		30		32	ns	
4	Enable to High	t_{PZH}	20	30		34		36	ns	
5	Disable from Low	t_{PLZ}	19	29		32		34	ns	
6	Disable from High	t_{PHZ}	24	36		40		43	ns	
7	LE to Output	t_{PLE}	23	35		39		41	ns	
8	Set-up Time	t_{SU}			20		20		ns	
9	Hold Time	t_H			0		0		ns	
10	Minimum Pulse Width	t_W			20		20		ns	
11	Input Capacitance	C_I	3	8					pF	$V_{IN} = V_{CC}$ or GND

MD54/74HCT574R ***TABLE 18.*** **A.C. Characteristics** V_{CC} = 4.5V, Absolute maximum ratings Table 6, Recommended operating conditions Table 7, D.C. characteristics Table 8, Timing waveforms Figure 7 and Figure 5, Test load Figure 5.

	PARAMETER	SYM	25°C		74HCT -40 to +85°C		54HCT -55 to +125°C		UNIT	TEST CONDITIONS
			TYP	MAX	MIN	MAX	MIN	MAX		
1	CK to High Output	t_{PLH}	20	30		34		36	ns	
2	CK toLow Output	t_{PHL}	22	33		37		40	ns	
3	Enable to Low	t_{PZL}	18	27		30		32	ns	
4	Enable to High	t_{PZH}	20	30		34		36	ns	
5	Disable from Low	t_{PLZ}	19	29		32		34	ns	
6	Disable from High	t_{PHZ}	24	36		40		43	ns	
7	Set-up Time	t_{SU}			20		20		ns	
8	Hold Time	t_H			0		0		ns	
9	Minimum Pulse Width	t_W			20		20		ns	
10	Input Capacitance	C_I	3	8					pF	$V_{IN} = V_{CC}$ or GND

FIGURE 3. Timing Diagrams for Inverting Buffer Tri-State Output Devices

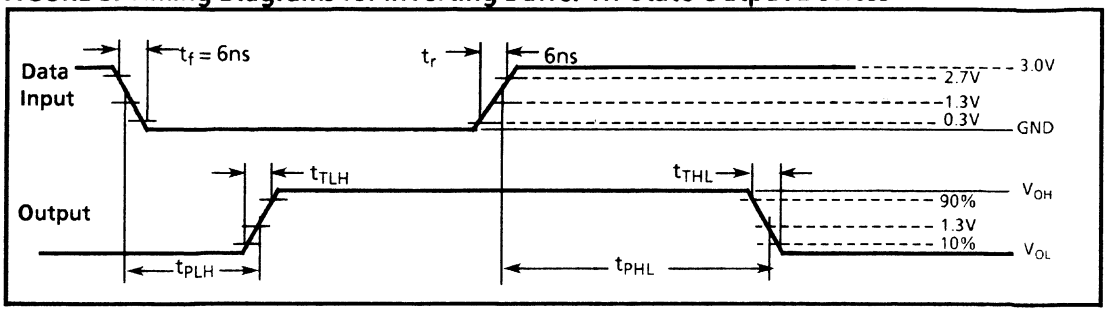


FIGURE 4. Timing Diagrams for Non-inverting Tri-State Output Devices

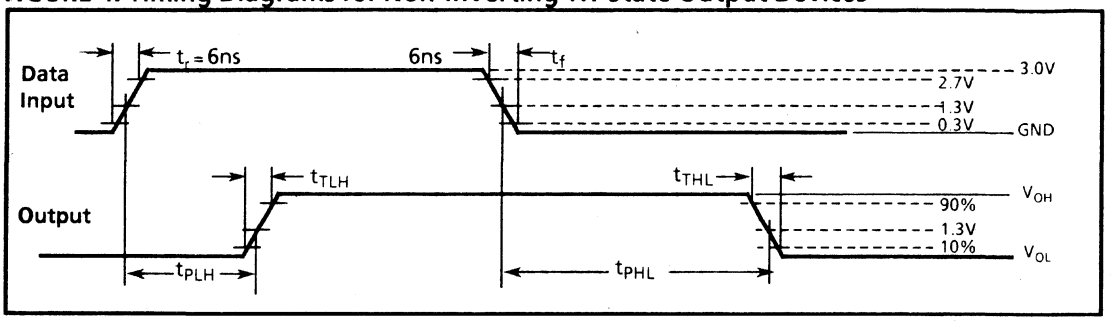


FIGURE 5. Timing Diagrams and Test Load for Tri-State Output Devices

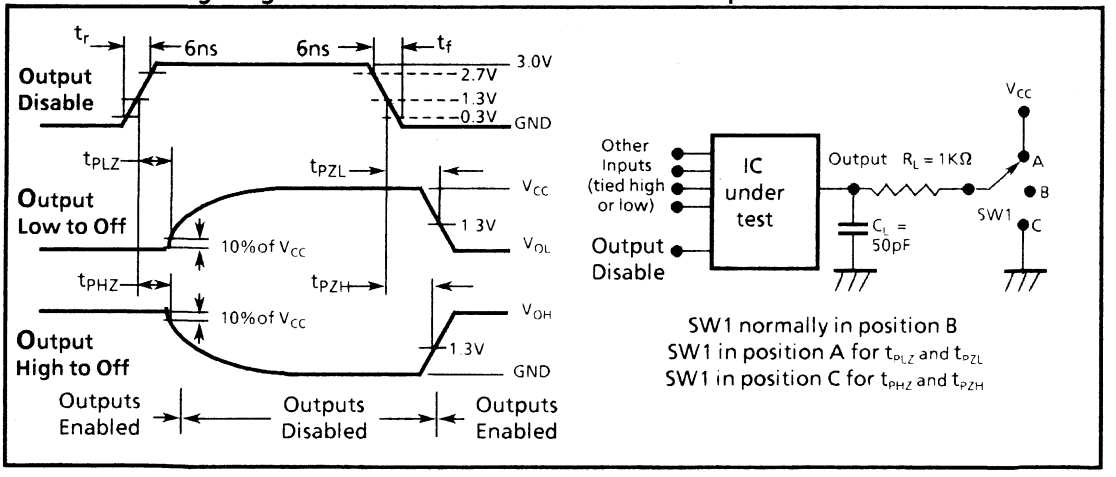


FIGURE 6. **Timing Diagrams for Transparent Latch Tri-State Output Devices**

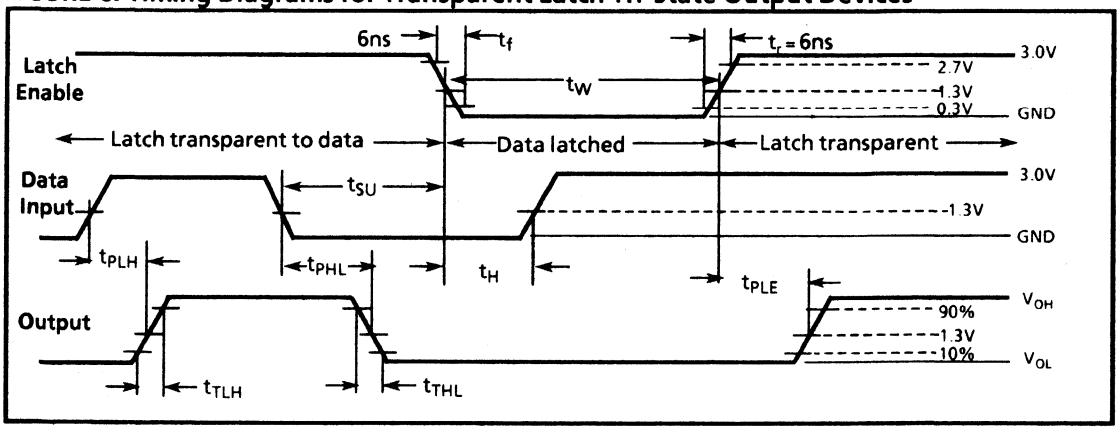
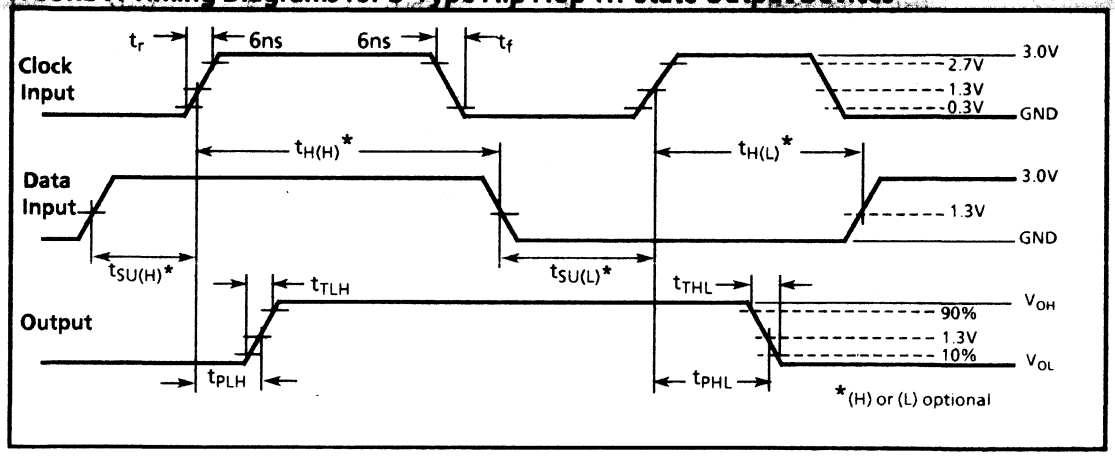


FIGURE 7. **Timing Diagrams for D-Type Flip Flop Tri-State Output Devices**



Compensation Formulae

PROPAGATION DELAY vs. CAPACITIVE LOAD

To calculate changes in propagation delay with changes in capacitve load, use equation 1.

$$t' = t + k(C_L' - 50) \quad \text{.....(1)}$$

where: C_L' = capacitive load (pF)
t = propagation delay with standard 50pF load,from data sheet (ns)
t' = propagation delay with load C_L (ns)
k = appropriate constant from Table 1, below (ns/pF)

Table 1- Propagation delay compensation constants for capacitive loading.

Device Type	Parameter	Constant (*k*) (ns/pF)
Standard Output Devices (HCT138/139)	t_{PHL} t_{PLH}	0.07 0.07
Tri-State Output Devices (HCT240/241/ 244/245/373/374/540/541/573/574)	t_{PHL} t_{PLH}	0.03 0.04

PROPAGATION DELAY vs. TEMPERATURE

Changes in propagation delay with changes in temperature can be calculated using equation 2.

$$t' = t(1 + 0.0021[T - 25]) \quad \text{.....(2)}$$

where: T = temperature (°C)
t = propagation delay at 25°C (from data sheet or equation) (ns)
t' = propagation delay at temperature T (ns)

PROPAGATION DELAY vs. SUPPLY VOLTAGE

Equation 3, below, describes the change in propagation delay with a change in supply voltage.

$$t' = t * c \quad \text{.....(3)}$$

where: c = appropriate constant from Table 2, below
t = propagation delay at 4.5V (from data sheet or equation) (ns)
t' = propagation delay at voltage V_{CC} (ns)

Table 2 - Propagation delay compensation constants for supply voltage varations.

V_{CC} (V)	c	V_{CC} (V)	c
8.0	0.64	4.0	1.10
7.0	0.73	3.0	1.40
6.0	0.85	2.0	2.27
5.0	0.97	1.5	3.70

TRANSITION TIME vs. CAPACITIVE LOAD

Changes in output transition time with changes in capacitive load can be calculated using formula 4.

$$tt' = tt + m(C_L' - 50) \quad \text{.....(4)}$$

where: C_L' = capacitive load (pF)
tt = transition time with 50pF load, from Table 3 below (ns)
tt' = transition time with load C_L' (ns)
m = appropriate constant from Table 3, below (ns/pF)

Table 3 - Transition delay compensation constants for capacitive loading.

Device Type	Parameter	Transition Time (*tt*) at 50pF load (ns)	Constant (*m*) (ns/pF)
Standard Output Devices (HCT138/139)	t_{TLH} t_{THL}	**20.0** 13.5	**0.25** 0.08
Tri-State Output Devices (HCT240/241/ 244/245/373/374/540/541/573/574)	t_{TLH} t_{THL}	11.0 7.0	0.13 0.07

POWER DISSIPATION vs. FREQUENCY OF OPERATION

Power dissipation for MITEL's HCT series of Octal Interface Circuits can be estimated using formula 5.

$$P_{av} = 10 * f \quad \text{.....(5)}$$

where: f = frequency of operation in Megahertz (MHz)
P_{av} = average power dissipated by the device at V_{CC} = 5V (mW)

Due to the nature of CMOS devices, the instantaneous peak power dissipation may be higher than shown by the above formula. This calculation does not include power dissipated by a load on the device outputs. Formula 5 assumes that all devices in a package are in use at the same frequency. If only one-half of the devices in a package are in use (say, 4 out of 8 buffers or latches) then the computed answer for P_{av} should be divided by 2. Below 1KHz power dissipation is approximately 3μW per package (typical).

ISO-CMOS MD65SC22
Versatile Interface Adapter
Preliminary Information

9161-002-046 NA ISSUE 1 AUGUST 1985

Features

- Input/Output Latches.
- Serial data port.
- Two 8-bit bidirectional I/O ports.
- Two 16-bit programmable timers.
- Expanded handshake control.
- Direct replacement for existing NMOS part
- Single 5 volt power supply.
- Low power ISO-CMOS technology.
- Fully TTL compatible.

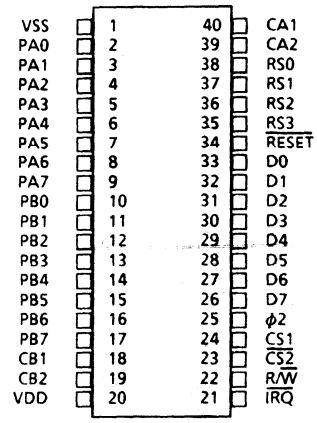
Applications

- General microprocessor I/O port.
- RS232 interface.
- Keyboard controller.
- Peripheral controller.

Description

The MD65SC22 is a Versatile Interface Adapter containing two 8-bit bidirectional latched ports, two 16-bit programmable timers and a serial to parallel/parallel to serial shift register. The device is fabricated in Mitel's ISO-CMOS technology.

Pin Connections



Ordering Information

MD65SC22AC 40 Pin Ceramic Package
MD65SC22AE 40 Pin Plastic Package

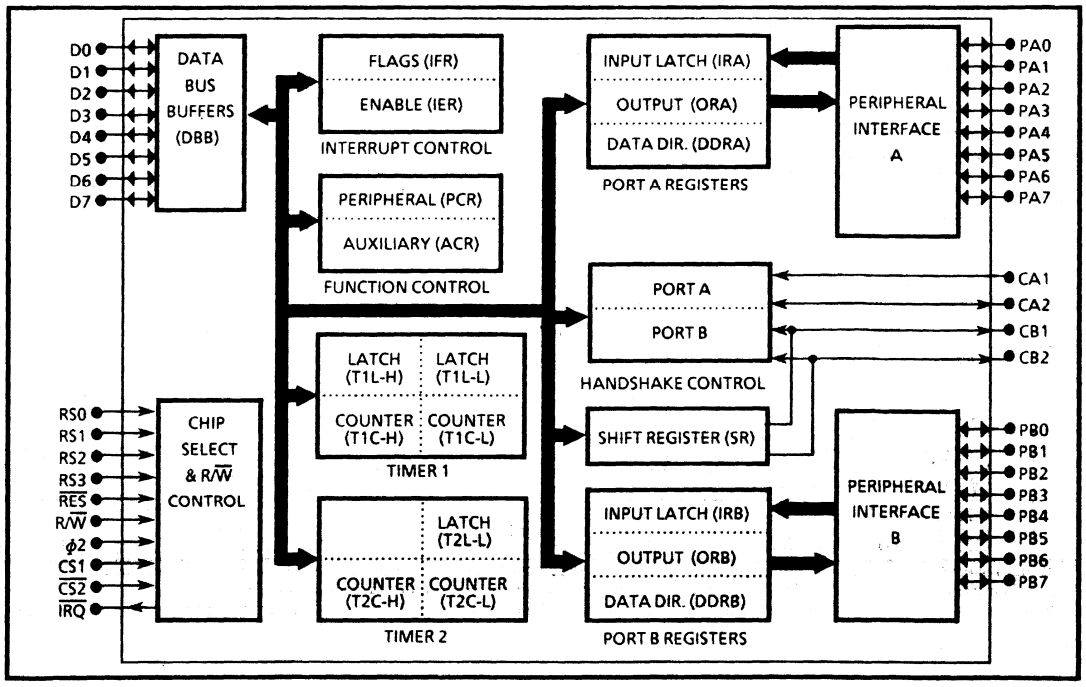


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	7.0	V
2	Voltage on any I/O pin	V_I	V_{SS}-0.3	V_{DD} + 0.3	V
3	Current on any I/O pin	I_I		± 10	mA
4	Operating Temperature	T_A	-40	+ 85	°C
5	Storage Temperature	T_S	-65	+ 150	°C
6	Power Dissipation Plastic	P_D		0.6	W
	Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Input Voltage	V_{IH}	2.4		V_{DD}	V	For a noise margin of 400
		V_{IL}	V_{SS}		0.4	V	mV
3	Operating Temperature	T_A	-40	+ 25	+ 85	°C	
4	Operating Frequency	f	0		2.0	MHz	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD1}		90		μA	Inputs High, $\phi 2$ stopped
2	Operating Supply Current	I_{DD}		0.56		mA	$\phi 2$ = 2 MHz, Inputs High
3	Input High Voltage	V_{IH}	2.0		V_{DD}	V	
4	Input Low Voltage	V_{IL}	V_{SS}		0.8	V	
5	Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0-3, CS1, $\overline{CS2}$, CA1, $\phi 2$	I_{IZ}			± 2.5	μA	$V_I = V_{SS}$ or $V_I = V_{DD}$
6	Input Capacitance	C_{IN}			7.0	pF	T_A = 25°C, f = 1 MHz
7	Output High Voltage	V_{OH}	2.4		V_{DD}	V	V_{DD} = 4.75V, I_{LOAD} = -100μA
	Port B	V_{OH}	1.5		V_{DD}	V	V_{DD} = 4.75V, I_{LOAD} = -1.0mA
8	Output Low Voltage	V_{OL}	V_{SS}		0.4	V	V_{DD} = 4.75V, I_{LOAD} = 1.6mA
9	Output Leakage Current $\overline{IRQ}$	I_{OZ}		0.01	10	μA	Off State
10	Output Capacitance	C_O			10	pF	T_A = 25°C, f = 1 MHz

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\phi 2$ Cycle Period	t_{CYC}	0.5			μs	see Timing Diagram 1
2	$\phi 2$ HIGH Pulse Width	t_C	0.22			μs	see Timing Diagram 1
3	Address Set-up Time	t_{AS}	90	0		ns	see Timing Diagram 2 & 3
4	Address Hold Time	t_{AH}	0			ns	see Timing Diagram 2 & 3
5	$\phi 2$ to Valid Data Delay (Read)	t_{DDR}		54	190	ns	see Timing Diagram 2
6	Data Hold Time (Read)	t_{DHR}	10	20		ns	see Timing Diagram 2
7	Data Set-Up Time (Write)	t_{DSW}	90	42		ns	see Timing Diagram 3

† Timing is over recommended temperature range & recommended power supply voltages. Test loads shown in figures 5 and 6.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note: ① Rise and Fall times (t_R &t_F) are < 10 ns; ② The term *negate* denotes removal of the active signal and *assert* denotes its presence.

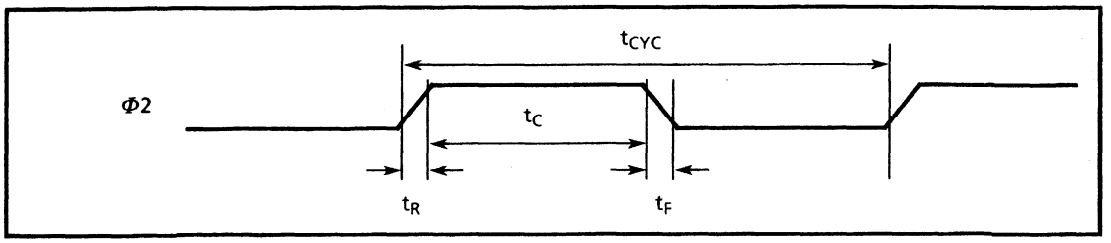
AC Electrical Characteristics[†] (Continued) - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ[‡]	Max	Units	Test Conditions
8		Data Hold Time (Write)	t_{DHW}	10	0		ns	see Timing Diagram 3
9		Read/Write Set-up Time	t_{RWS}	90	10		ns	see Timing Diagram 2 & 3
10		Read/Write Hold Time	t_{RWH}	0			ns	see Timing Diagram 2 & 3
11	PERIPHERAL INTERFACE	Peripheral Data Set up Time	t_{PCR}	150	0		ns	see Timing Diagram 2
12		Peripheral Data Delay Time	t_{CPW}			500	ns	see Timing Diagram 3
13		$\phi 2$ negate to CA2 falling edge (read, handshake-pulse mode)	t_{CA2}		0.20	1.0	μs	see Timing Diagram 4 & 5
14		$\phi 2$ negate to CA2 rising edge (pulse mode)	t_{RS1}		0.10	1.0	μs	see Timing Diagram 4
15		CA1 assert to CA2 rising edge (handshake mode)	t_{RS2}		0.25	2.0	μs	see Timing Diagram 5
16		$\phi 2$ assert to CA2, CB2 falling edge (write handshake)	t_{WHS}	0.05	0.07	1.0	μs	see Timing Diagram 6 & 7
17		Peripheral Data to CB2 falling edge	t_{DS}	0.20	0.30	1.5	μs	see Timing Diagram 6 & 7
18		$\phi 2$ assert to CA2, CB2 rising edge (pulse mode)	t_{RS3}		0.70	1.0	μs	see Timing Diagram 6
19		CA1, CB1 assert to CA2, CB2 rising edge (handshake mode)	t_{RS4}		0.30	2.0	μs	see Timing Diagram 7
20		CA2, CB2 falling edge to CA1, CB1 assert (handshake mode)	t_{21}	400	330		ns	see Timing Diagram 7
21		Peripheral Data Set up Time to CA1, CB1 assert (input latching)	t_{IL}	300	0		ns	see Timing Diagram 8
22		CA1, CB1 negate time before next iatch	t_{AL}	$t_C + 50$	160		ns	see Timing Diagram 8
23		Peripheral Data Hold after CA1, CB1 assert (input latching)	t_{PDH}	150	50		ns	see Timing Diagram 8
24		$\phi 2$ negate to Shift Data Valid	t_{SR1}		40	300	ns	see Timing Diagram 9
25		Shift Data Valid to $\phi 2$ assert	t_{SR2}	300	20		ns	see Timing Diagram 10
26		External Shift to $\phi 2$ negate	t_{SR3}	100	220	t_{CYC}	ns	see Timing Diagram 10
27		Pulse Width, CB1 input pulse	t_{ICW}	$2 \times t_{CYC}$			ns	see Timing Diagram 11
28		Pulse Spacing, CB1 input pulse	t_{ICS}	$2 \times t_{CYC}$			ns	see Timing Diagram 11
29		Pulse Width, PB6 input pulse	t_{IPW}	$2 \times t_{CYC}$			ns	see Timing Diagram 12
30		Pulse Spacing, PB6 input pulse	t_{IPS}	$2 \times t_{CYC}$			ns	see Timing Diagram 12
31		CA1, CB1, CA2, CB2 negate time before next assert	t_{PWI}	$t_C + 50$	170		ns	see Timing Diagram 13
32		$\phi 2$ assert to CB1 rising edge (SR shifted by internal clock)	t_{DPR}		0		ns	see Timing Diagram 14
33		$\phi 2$ assert to CB1 falling edge (SR shifted by internal clock)	t_{DPL}		0		ns	see Timing Diagram 14

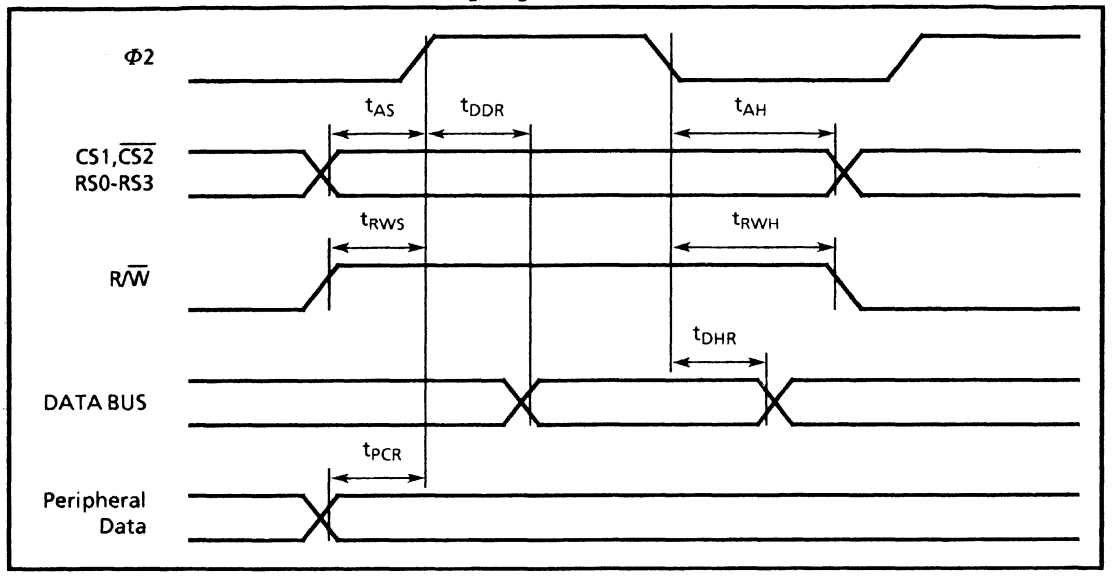
[†] Timing is over recommended temperature range & recommended power supply voltages. Test loads shown in figures 5 and 6.
[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note: ① Rise and Fall times (t_R &t_F) are <10 ns; ② The term *negate* denotes removal of the active signal and *assert* denotes its presence.

Timing Diagrams

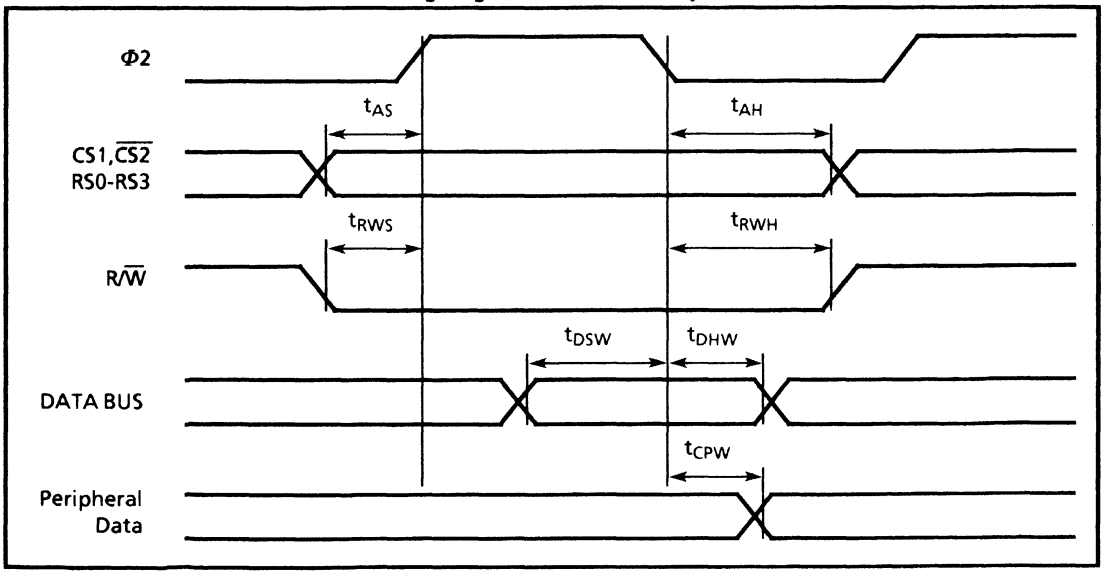
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} and V_{OL} for outputs



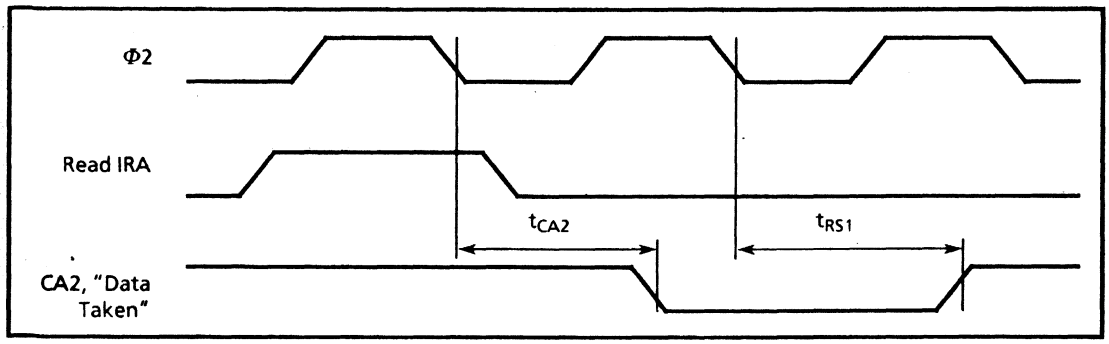
Timing diagram 1. Φ2 Pulse



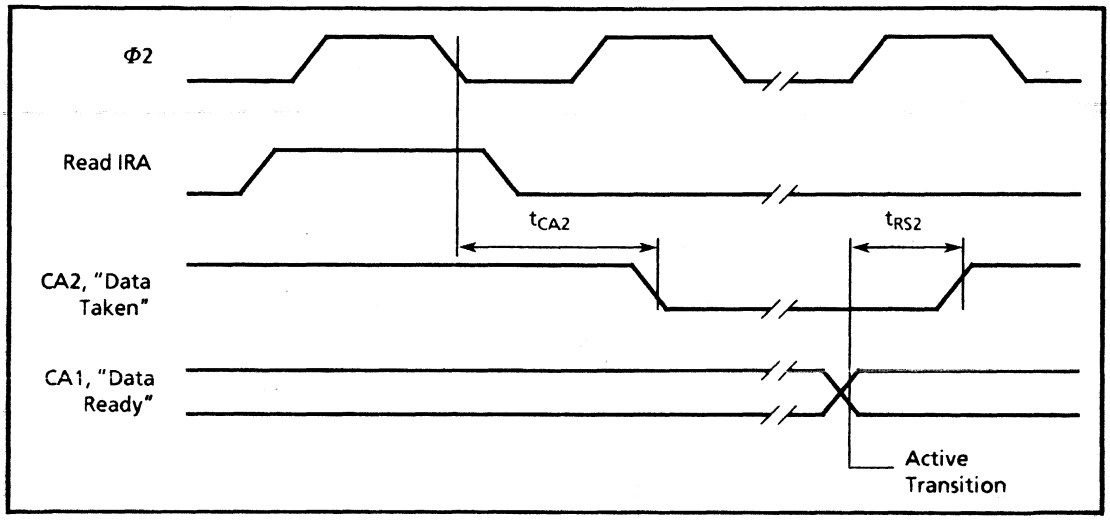
Timing diagram 2. MPU Read Cycle



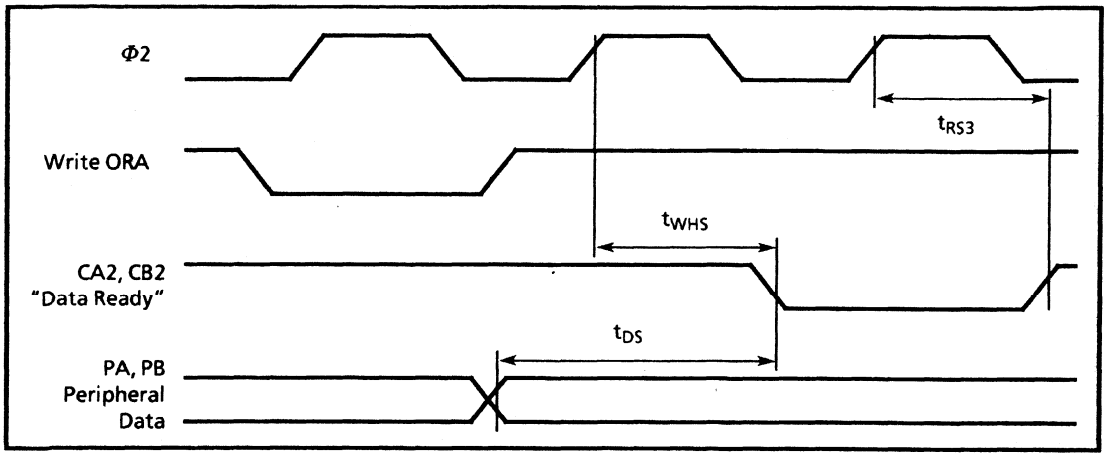
Timing diagram 3. MPU Write Cycle



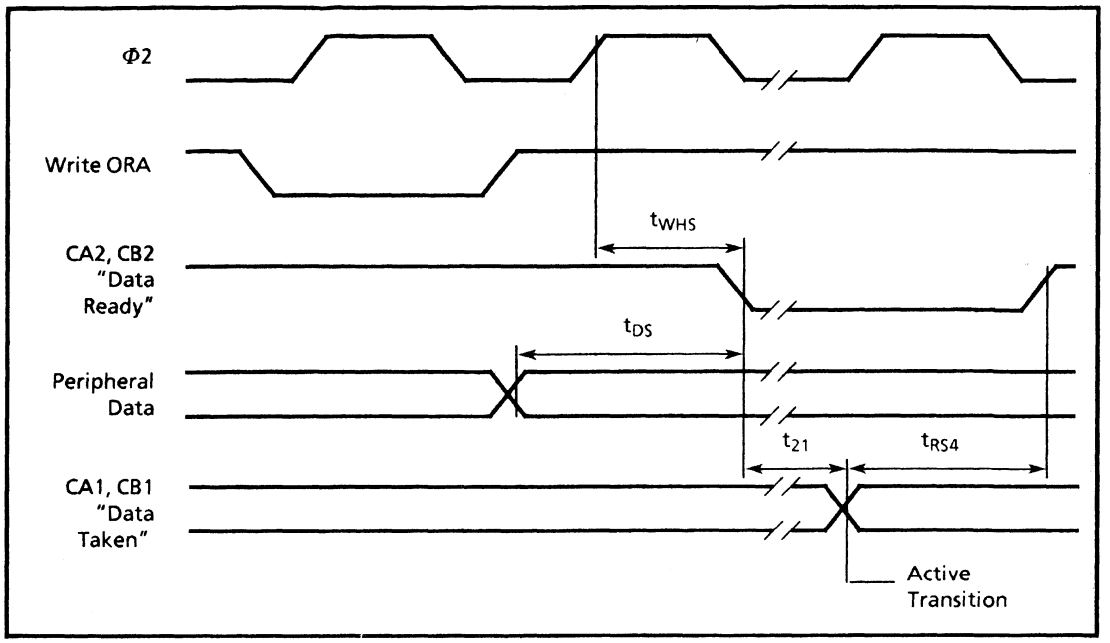
Timing diagram 4. CA2 Timing for Read Handshake, Pulse Mode



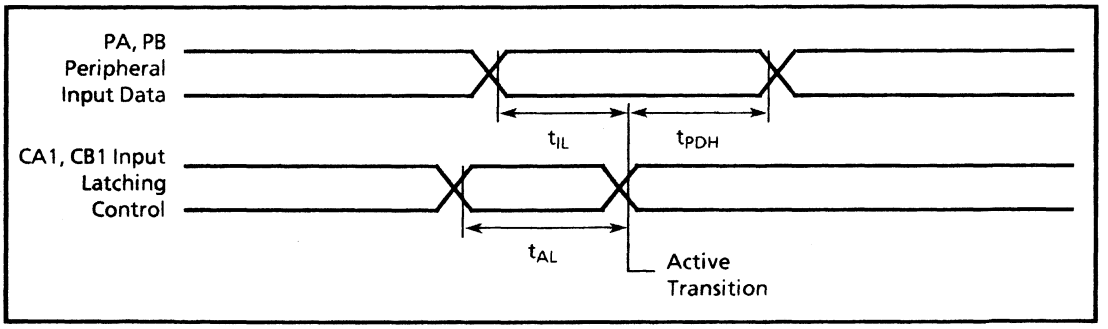
Timing diagram 5. CA2 Timing for Read Handshake, Handshake Mode



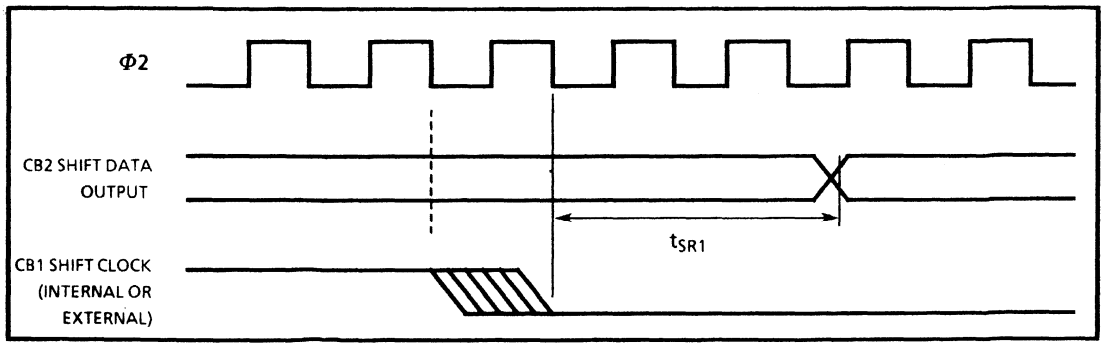
Timing diagram 6. CA2,CB2 Timing for Write Handshake, Pulse Mode



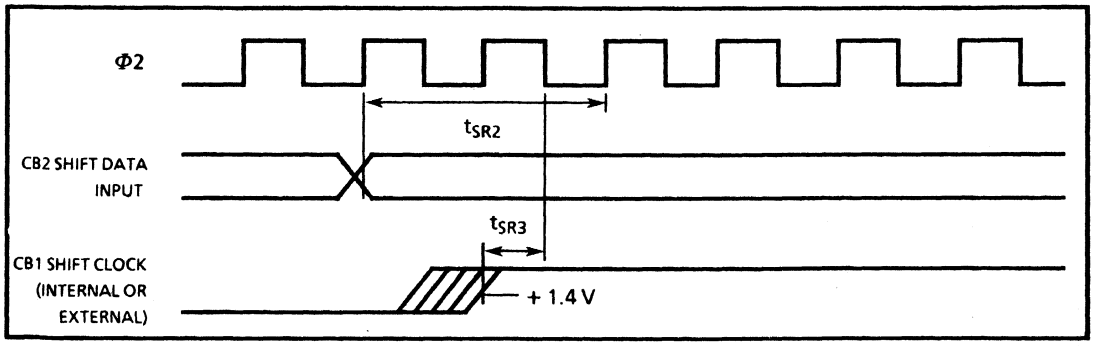
Timing diagram 7. CA2, CB2 Timing for Write Handshake, Handshake Mode



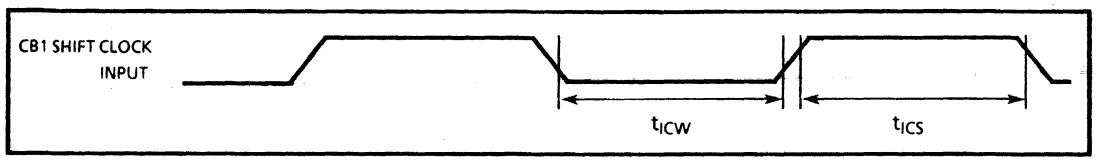
Timing diagram 8. Peripheral Data Input Latch Timing



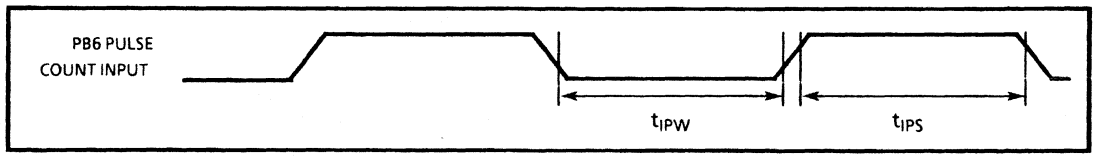
Timing diagram 9. Timing for Shift Out with Internal or External Shift Clocking



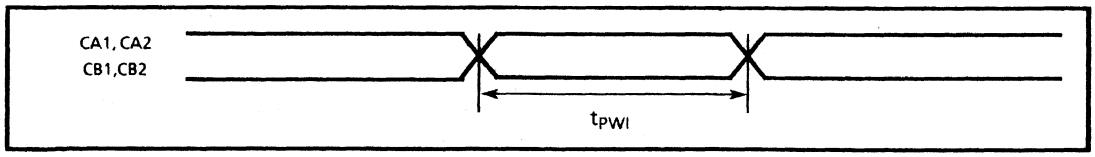
Timing diagram 10. Timing for Shift In with Internal or External Shift Clocking



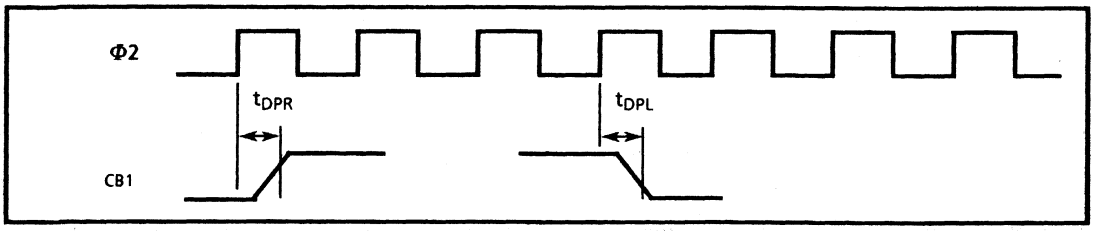
Timing diagram 11. External Shift Clock Timing



Timing diagram 12. Pulse Count Input Timing



Timing diagram 13. Setup Time to Triggering Edge



Timing diagram 14. Shift in/out with Internal Clock - Delay from Φ2

TABLE 1.
Pin Description

Pin #	Name	Description
1	V_{SS}/GND	**LOGIC GROUND**
2-9	PA0-PA7	**PORT A BIDIRECTIONAL DATA INTERFACE.** An 8 line interface whose lines may be configured individually as either inputs or outputs; as programmed in Data Direction Register A (DDRA). The logic level of each pin programmed as an output is controlled by writing to the appropriate bit in Output Register A (ORA), and the status of each pin programmed as an input is reflected by the corresponding bit in Input Register A (IRA). The logic thresholds of the port are TTL compatible and appear as one TTL load when configured as inputs.
10-15	PB0-PB5	**PORT B BIDIRECTIONAL INTERFACE.** These pins operate in the same manner as PA0-PA7, under the control of DDRB, ORB and IRB. Their logic thresholds are TTL compatible except that they can source 10 mA of current at 1.5 volts, in order to drive Darlington transistor pairs. As inputs they appear as one TTL load.
16-17	PB6-PB7	**PORT B BIDIRECTIONAL INTERFACE; TIMER INPUT/OUTPUT.** When the timers are disabled, these pins are the two most significant bits of Port B, identical to PB0-PB5. PB6 also serves as a clock input for Timer 2, and PB7 can be used by Timer 1 to generate waveforms. Control of the timer functions is provided by the Auxiliary Control Register (ACR).
18-19	CB1,CB2	**PORT B CONTROL LINES AND SERIAL PORT.** The port B control lines have various functions, determined by the state of the shift register control bits in the ACR, and the port B control bits in the Peripheral Control Register (PCR). If the shift register is disabled (the use of the shift register preempts the use of these pins by port B), CB1 and CB2 are controlled by the state of the appropriate bits in the PCR. Under PCR control, these pins are used for data transfer handshake control, specifically in the write direction (from the perspective of the microprocessor). As a serial port, serial data is shifted in or out of CB2, and CB1 acts as a clock input or output. Both pins operate as either inputs or outputs, and are TTL compatible.
20	V_{DD}	**POSITIVE POWER SUPPLY.**
21	$\overline{IRQ}$	**INTERRUPT REQUEST.** This open drain output notifies the controlling microprocessor that the MD65SC22 needs to be serviced. It may only go low when the interrupt enable bits in the Interrupt Enable Register (IER) are programmed to acknowledge the source of the interrupt.
22	R/$\overline{W}$	**DATA BUS BUFFER DIRECTION CONTROL.** The direction control input determines whether data is latched into, or read from the MD65SC22.
23,24	$\overline{CS2}$, CS1	**CHIP SELECTS 1 AND 2.** These inputs, when asserted, enable the data bus buffer so data may be transferred into or out of the device. Chip Select 1 is active high, and Chip Select 2 is active low. These inputs are qualified by the system clock ($\phi 2$) so that a transfer may only occur when the system clock is high.
25	$\phi 2$	**SYSTEM CLOCK (OR ENABLE CLOCK).** This input from the microprocessor allows synchronization with the MD65SC22 on data bus transfers. All microprocessor bus set up times and hold times are referenced to the edges of $\phi 2$.
26-33	D7-D0	**MICROPROCESSOR DATA PORT.** This bidirectional port interfaces directly to the host microprocessor, providing a data path between the data bus and the internal registers of the MD65SC22. When not enabled by the Chip Selects and the $\phi 2$ clock, this port appears as a high impedance to the data bus. Whether the port is configured as an input or an output is determined by the state of the R/$\overline{W}$ input. All pins interfacing to the microprocessor bus are TTL threshold compatible but are high impedance inputs.

TABLE 1.
Pin Description (continued)

Pin #	Name	Description
34	$\overline{RES}$	**RESET.** The reset pin allows an external reset of the device. An active level (logic low) on this input will clear all internal registers, except the shift registers and the timer latches. All functions are disabled, including interrupts originating from the device. The parallel ports initialize as inputs after a reset.
35-38	RS3-RS0	**REGISTER SELECTS 0-3.** There are 16 registers inside the MD65SC22, accessible from the controlling microprocessor. When the data port is enabled, the selection of a register for participation in the data transfer is determined by the state of these inputs. RS0 is the least significant bit of the 4 bit register address.
39, 40	CA2,CA1	**PORT A CONTROL LINES.** These pins have a function very similar to the port B control lines, however, CA1 and CA2 can be used for handshaking control in data transfers in both the write and the read directions (from the microprocessor's perspective). These pins are TTL threshold compatible but are high impedance inputs.

TABLE 2.
Register Decode And Designation

RS3	RS2	RS1	RS0	Register Selected	
				Write Operation	Read operation
0	0	0	0	Output Register B (ORB)	Input Register B (IRB)
0	0	0	1	Output Register A (ORA)	Input Register A (IRA)
0	0	1	0	Data Direction Register B (DDRB)	Data Direction Register B (DDRB)
0	0	1	1	Data Direction Register A (DDRA)	Data Direction Register A (DDRA)
0	1	0	0	T1 Low Order Latches (T1C-L)	T1 Low Order Counter (T1C-L)
0	1	0	1	T1 High order Counter (T1C-H)	T1 High Order Counter (T1C-H)
0	1	1	0	T1 Low Order Latches (T1L-L)	T1 Low Order Latches (T1L-L)
0	1	1	1	T1 High Order Latches (T1L-H)	T1 High Order Latches (T1L-H)
1	0	0	0	T2 Low Order Latches (T2C-L)	T2 Low Order Counter (T2C-L)
1	0	0	1	T2 High Order Counter (T2C-H)	T2 High Order Counter (T2C-H)
1	0	1	0	Shift Register (SR)	Shift Register (SR)
1	0	1	1	Auxiliary Control Register (ACR)	Auxiliary Control Register (ACR)
1	1	0	0	Peripheral Control Register (PCR)	Peripheral Control Register (PCR)
1	1	0	1	Interrupt Flag Register (IFR)	Interrupt Flag Register (IFR)
1	1	1	0	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)
1	1	1	1	ORA (without handshaking)	IRA (without handshaking)

TABLE 3.
Port A pin to register map

External Pin	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Data Register bit	ORA_b7 IRA_b7	ORA_b6 IRA_b6	ORA_b5 IRA_b5	ORA_b4 IRA_b4	ORA_b3 IRA_b3	ORA_b2 IRA_b2	ORA_b1 IRA_b1	ORA_b0 IRA_b0
Data Direction Reg. bit	$DDRA_b7$	$DDRA_b6$	$DDRA_b5$	$DDRA_b4$	$DDRA_b3$	$DDRA_b2$	$DDRA_b1$	$DDRA_b0$

TABLE 4.
Port B pin to register map

External Pin	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Data Register bit	ORB_b7 IRB_b7	ORB_b6 IRB_b6	ORB_b5 IRB_b5	ORB_b4 IRB_b4	ORB_b3 IRB_b3	ORB_b2 IRB_b2	ORB_b1 IRB_b1	ORB_b0 IRB_b0
Data Direction Reg. bit	$DDRB_b7$	$DDRB_b6$	$DDRB_b5$	$DDRB_b4$	$DDRB_b3$	$DDRB_b2$	$DDRB_b1$	$DDRB_b0$

TABLE 5.
Data Register A operation

Data Flow	$DDRA_bx$ = 0 (input)		$DDRA_bx$ = 1 (output)	
	ACR_b0 = 0	ACR_b0 = 1	ACR_b0 = 0	ACR_b0 = 1
Read IRA	μP reads logic level of port pin transparently	μP reads logic level of port pin transparently until an active signal is applied on CA1, which latches the state of the port pin until the port is read.	μP reads logic level of port pin transparently	μP reads logic level of port pin transparently until an active signal is applied on CA1, which latches the state of the port pin until the port is read.
Write ORA	logic level of pins not affected until direction of pin is changed*	logic level of pins not affected until direction of pin is changed	logic level of output pins follows logic level written into ORA	logic level of output pins follows logic level written into ORA

*may be continually rewritten, retaining last data written

TABLE 6.
Data Register B operation

Data Flow	$DDRB_bx$ = 0 (input)		$DDRB_bx$ = 1 (output)	
	ACR_b1 = 0	ACR_b1 = 1	ACR_b1 = 0	ACR_b1 = 1
Read IRB	μP reads logic level of port pin transparently	μP reads logic level of port pin transparently until an active signal is applied on CB1, which latches the state of the port pin until the port is read.	μP reads logic level written to the ORB, not what may be on the port pin.	μP reads logic level written to the ORB, not what may be on the port pin.
Write ORB	logic level of pins not affected until direction of pin is changed*	logic level of pins not affected until direction of pin is changed	logic level of output pins follows logic level written into ORB	logic level of output pins follows logic level written into ORB

*may be continually rewritten, retaining last data written

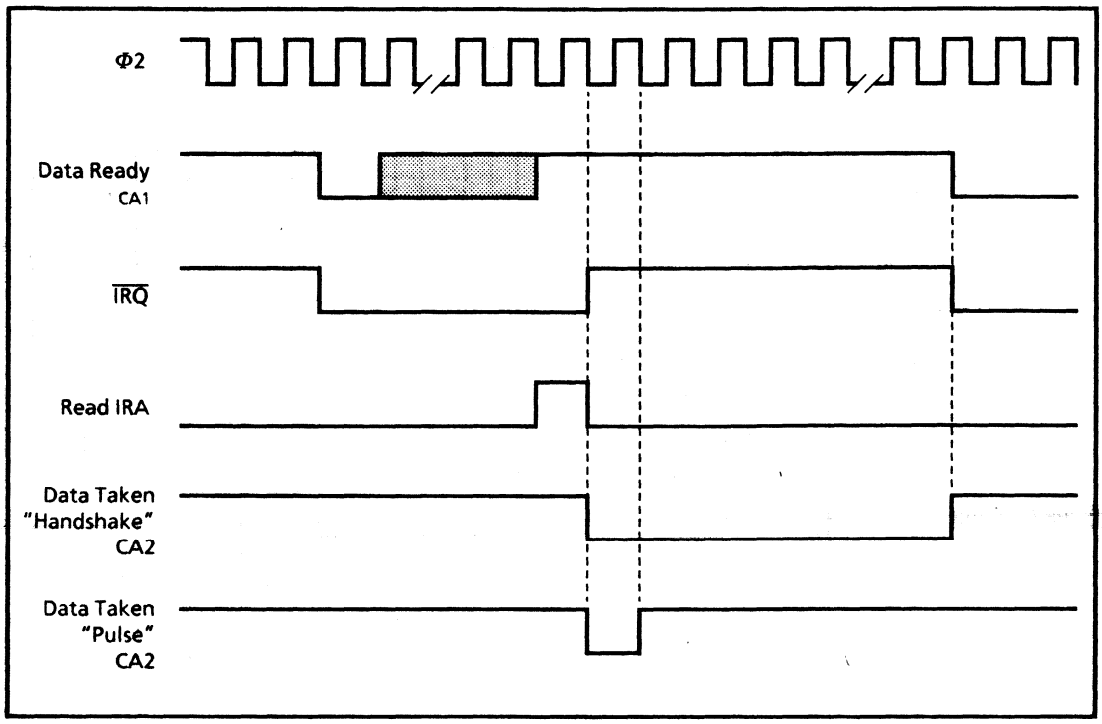


Figure 1. Read Handshake Timing (Port A only)

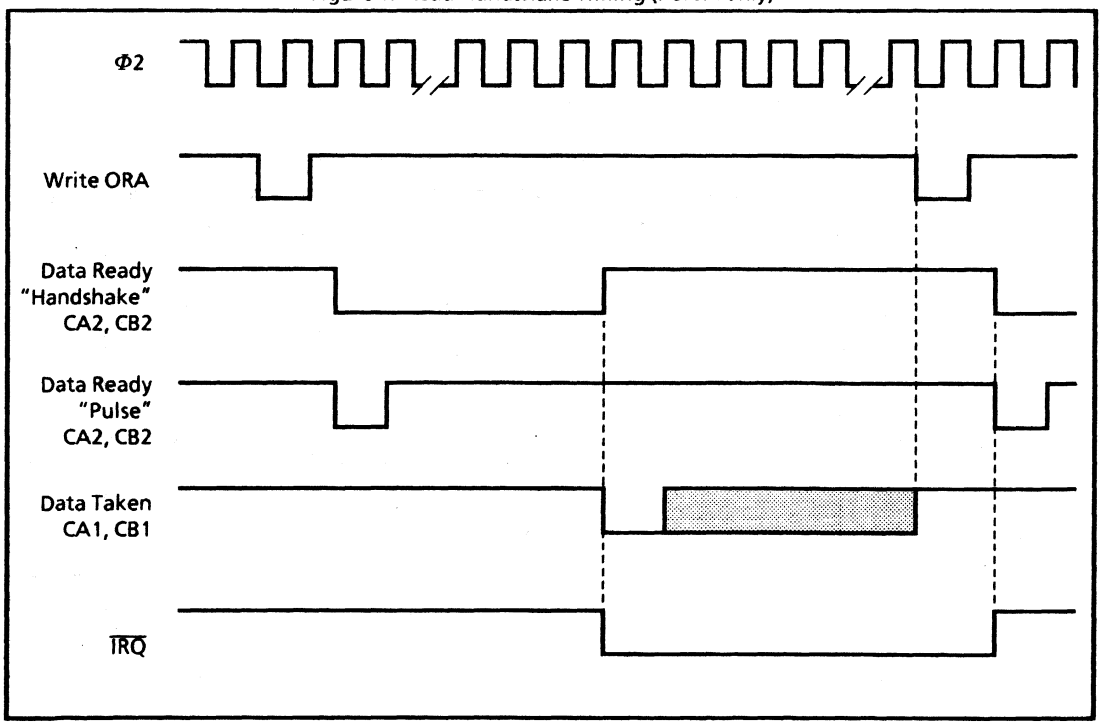


Figure 2. Write Handshake Timing

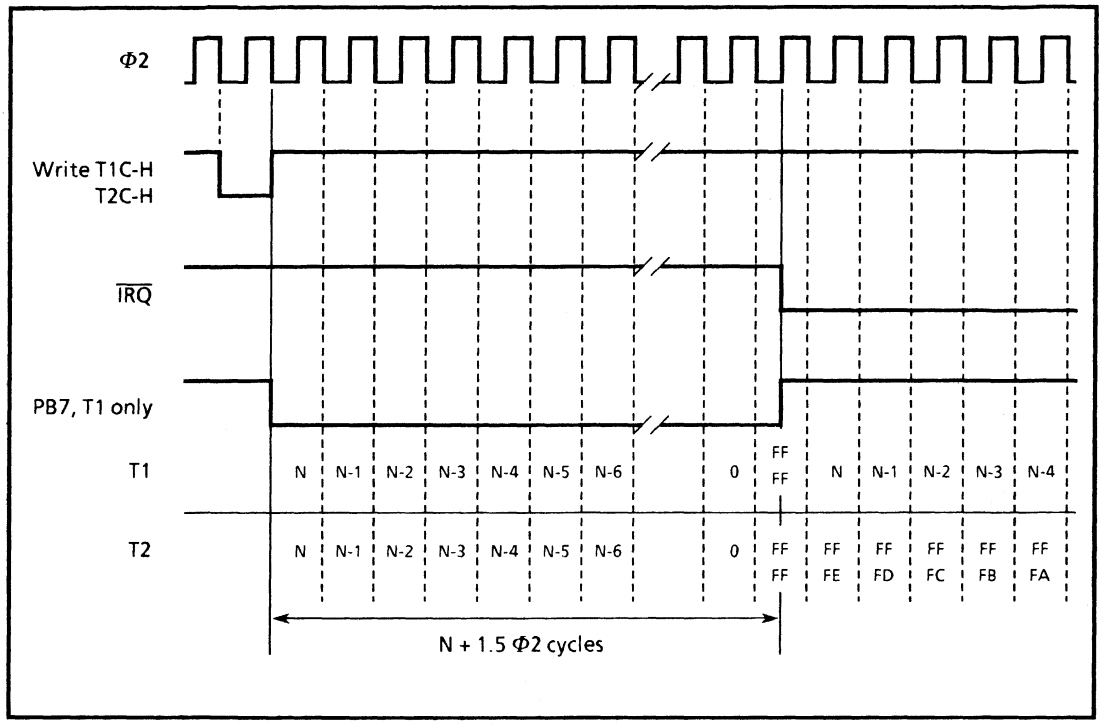


Figure 3. Timer 1 and Timer 2 Single Pass Mode

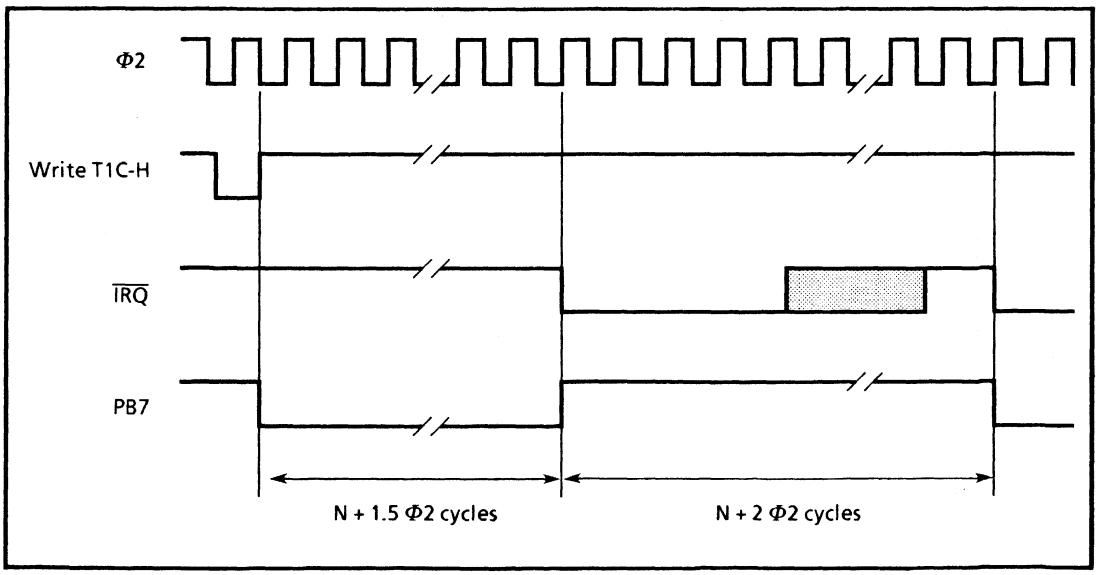


Figure 4. Timer 1 Free Run Mode

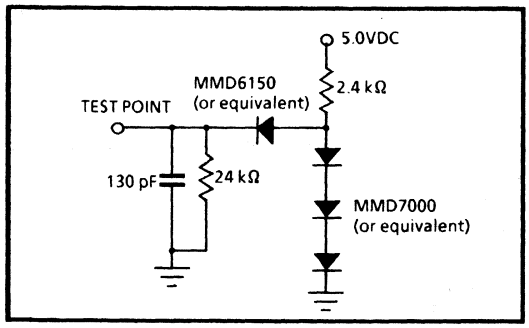


Figure 5. Test load for all pins except $\overline{IRQ}$

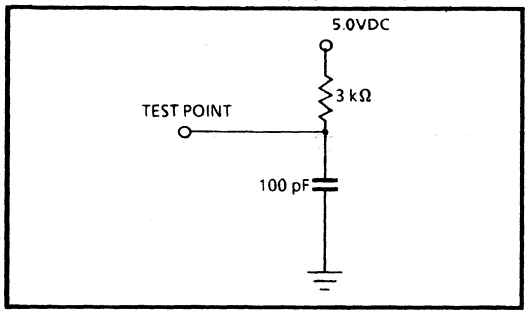


Figure 6. Test load for $\overline{IRQ}$

FUNCTIONAL DESCRIPTION

The MD65SC22 is a system utility device, combining multiple functions into one component. The MD65SC22 provides 2 bidirectional, parallel ports (8 bit); a bidirectional serial port; and 2 timers (16 bits each). Each function is qualified by a number of powerful and flexible user modes. Access and control of the MD65SC22 utility is provided through a microprocessor interface and 16 programmable registers. Complimenting this interface, a maskable interrupt capability may be used to notifiy the microprocessor of real time events. Two registers are provided to qualify the possible sources of an interrupt, and to determine which source originated an interrupt.

Parallel Port Operation (Port A and Port B)

There are 7 registers that control and report the state of parallel ports A and B. The determination of a port pin as an input or an output is performed by the contents of the Data Direction Registers (DDRA and DDRB). Writing a bit in a DDR to a logical '1' defines the corresponding pin of the port as an output. Conversely, writing a logical '0' to the bit causes the port pin to be an input. $DDRA_b0$ (bit 0 in DDRA) controls the direction of pin PA0, $DDRA_b1$ controls the direction of pin PA1, etc., up to $DDRA_b7$ controlling PA7. Port B pins follow the same conventions for mapping to DDRB bits. The contents of the DDRs may be read back by the microprocessor.

The Data Registers (ORA-B and IRA-B) control and monitor the logic level of their respective pins. The bits of these registers are mapped to the pins of the ports in the same manner as the DDRs. If a parallel port pin is defined as an output, the logic level of the pin follows the logic level written into the corresponding bit in the port's OR. When the pin is defined as an input, writing to the OR has no effect, the state of the pin may only be monitored. Changing the pin from an input to an output will cause the logic level of the output to follow the last logic level written to the OR bit.

Read access to individual bits in the OR and the IR is determined by the appropriate bit in the DDR. As well, there are differences between Port A and Port B. Port B pins configured as outputs will only return the last logic level written to them. Port B pins configured as inputs, and Port A pins configured as both inputs and outputs have 2 modes in which they may monitor data: transparent mode and latch mode. In transparent mode, reading an IR bit or ORA bit always returns the actual logic level present on the parallel port pin. In latch mode, an active transition on CA1 or CB1 (CA1 for port A and CB1 for port B) will latch the current logic level of the pin into its respective IR bit or ORA bit, until it is read by the microprocessor. After the bit has been read, and until the next active transition of CA1 or CB1, each bit follows the logic level of its pin as in transparent mode.

Latch mode may be enabled or disabled by 2 bits in the Auxiliary Control Register (ACR): ACR_b0 (Port A) and ACR_b1 (Port B). Writing a logical '0' to these bits disables the latching of the parallel ports, and logical '1' enables latching. Figure 7 shows the input /output circuitry of each of the parallel port pins.

Handshaking

The Control pins (CA1, CA2, CB1 and CB2) have the task of providing handshaking for data transfers (via the MD65SC22) between the controlling microprocessor and another device. The various operating modes of the Control lines are determined by the contents of the Peripheral Control Register (PCR). PCR_b0 and PCR_b4 define the

active edge of the CA1 and CB1 inputs respectively. PCR_b1-3 determine the operation of the CA2 pin, and PCR_b5-7 determine the operation of the CB2 pin.

Port A may be used for handshaking data transfers in both the microprocessor to peripheral device direction (write) and in the peripheral device to microprocessor direction (read). Port B only provides handshaking in the microprocessor to peripheral device direction. It should be made clear that handshaking only occurs in 2 out of a possible 8 modes for the CA2 and the CB2 pins. These are clearly shown in Table 7 as the "Handshake mode" and the "Pulse mode". The setting of the pertinent bits in the PCR for these modes as well as the other modes of the CA2 and CB2 lines are shown.

The protocol for a controlled data transfer in "Handshake" or "Pulse" mode depends on the direction of the transfer. A "write" (supported on Port A and Port B) transfer is initiated by the microprocessor writing data to the OR. In "Pulse" mode, a pulse (one $\phi 2$ cycle in duration) is then output on CA2 or CB2. In Handshake mode, CA2 or CB2 goes low until a response from the peripheral device. This signal on CA2 or CB2 is equivalent to a "Data Ready" signal from the MD65SC22 to the peripheral device. The peripheral device may now read the data on the port's pins, and must acknowledge the receipt of the data by applying an active edge on the CA1 or CB1 line. If the "Handshake" mode is enabled, application of the "Data Taken" signal by the peripheral device will cause the MD65SC22 to remove the "Data Ready" signal. "Data Taken" also sets the interrupt flag for

TABLE 7.
Peripheral Control Register (CA1, CA2, CB1, CB2 control)

b7	b6	b5	b4	b3	b2	b1	b0	Operation
x	x	x	x	x	x	x	0	CA1 Interrupt control, negative active edge
x	x	x	x	x	x	x	1	CA1 Interrupt control, positive active edge
x	x	x	x	0	0	0	x	CA2 control, input, negative active edge
x	x	x	x	0	0	1	x	CA2 control, input, negative active edge, not cleared by read of O/IRA*
x	x	x	x	0	1	0	x	CA2 control, input, positive active edge
x	x	x	x	0	1	1	x	CA2 control, input, positive active edge, not cleared by read of O/IRA*
x	x	x	x	1	0	0	x	CA2 control, output, "Handshake" mode
x	x	x	x	1	0	1	x	CA2 control, output, "Pulse" mode
x	x	x	x	1	1	0	x	CA2 control, output low
x	x	x	x	1	1	1	x	CA2 control, output high
x	x	x	0	x	x	x	x	CB1 Interrupt control, negative active edge
x	x	x	1	x	x	x	x	CB1 Interrupt control, positive active edge
0	0	0	x	x	x	x	x	CB2 control, input, negative active edge
0	0	1	x	x	x	x	x	CB2 control, input, negative active edge, not cleared by read of O/IRB*
0	1	0	x	x	x	x	x	CB2 control, input, positive active edge
0	1	1	x	x	x	x	x	CB2 control, input, positive active edge, not cleared by read of O/IRB*
1	0	0	x	x	x	x	x	CB2 control, output, "Handshake" mode
1	0	1	x	x	x	x	x	CB2 control, output, "Pulse" mode
1	1	0	x	x	x	x	x	CB2 control, output low
1	1	1	x	x	x	x	x	CB2 control, output high

*See section on IFR function

CA1 or CB1, which will cause an interrupt of the microprocessor if that particular interrupt is enabled. The interrupt may be removed by the microprocessor writing to the port.

A "read" data transfer (supported on only Port A) follows a very similar pattern to the "write" protocol. A "read" data transfer is initiated by the peripheral device by presenting an active edge to the CA1 input ("Data Ready") when the data from the peripheral is present on Port A pins. This will set the interrupt flag for CA1, and if this interrupt is enabled, the microprocessor will be interrupted. The microprocessor may read the data at Port A, thereby removing the interrupt and presenting a "Data Taken" signal or pulse (one $\phi 2$ cycle in duration) on CA2. "Data Taken" is cleared by the next active edge of "Data Ready" from the peripheral device.

In Port A operation, the type of handshaken data transfer performed ("read" or "write") depends on what event occurs first after the last data transfer; a write into ORA by the microprocessor, or a "Data Ready" signal from the peripheral device. For data transfers that do not require handshaking, there are 6 modes of CA2, CB2 control that do not follow the previously described protocol. As illustrated in Table 7, the logic level of CA2 or CB2 may be placed high or low, independent of any action from the peripheral device. CA2 and CB2 may also be configured as inputs that trigger an interrupt to the microprocessor. Selection is available between which edge of an input (positive or negative) causes interrupt triggering, and the manner in which the interrupt is cleared is also selectable (Table 7). Interrupts from the CA2 and CB2 inputs may be cleared by reading their respective IRs; or writing

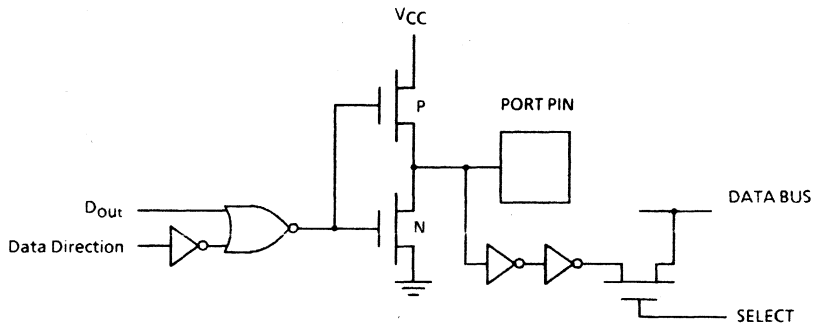


Figure 7a. Port A Equivalent Circuit.

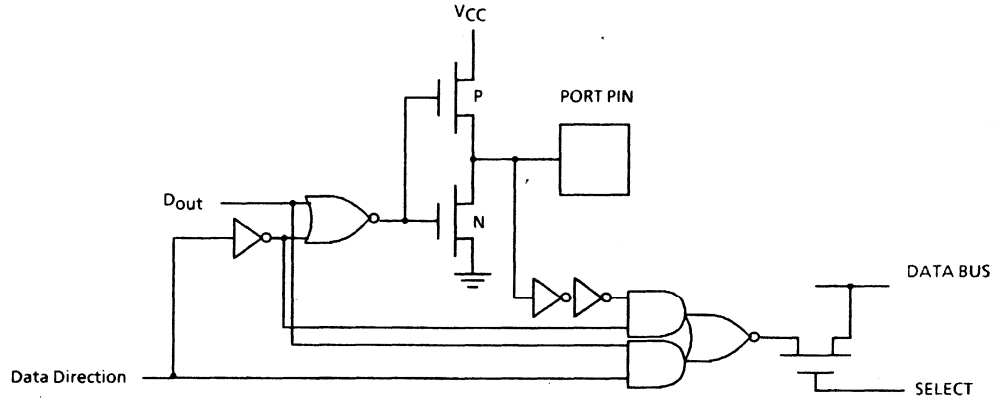


Figure 7b. Port B Equivalent Circuit.

Figure 7. Port A and Port B Equivalent Circuits.

into the Interrupt Flag Register (IFR) may be made mandatory in order to clear the interrupt. This latter method of clearing interrupts is described in the section on the IFR.

A final register is provided for use as a parallel port. This register is equivalent to ORA and IRA, however data transfers performed through this register may not utilize the handshaking protocol (see table 2).

Timer 1 Operation

Timer 1 (T1) is an interval timer, which decrements from a programmable 16-bit count to zero. When the count reaches zero and subsequently rolls over to $FFFF_H$, an interrupt flag in the IFR is set, interrupting the μP if enabled in the Interrupt Enable Register (IER). T1 decrements every full cycle of the $\phi 2$ clock. The timer is divided into a low count and a high count, each of which are separately accessible.

TABLE 8.
Shift register operation

Mode	ACR state			Operation
	b4	b3	b2	
0	0	0	0	**SR DISABLED** - SR interrupt flag disabled, and CB1 and CB2 controlled by contents of PCR.
1	0	0	1	**SHIFT IN UNDER T2 CONTROL** - CB1 is an output and CB2 is an input. CB1 is normally high. A read or a write to the SR initializes shift operation. CB1 changes state on every T2 timeout (N + 2 cycles of $\phi 2$ and coincident with the rising edge of $\phi 2$; note that only the lower byte of the timer is used in the timeout) after the read or write of the SR. Data at CB2 should be stable until the falling edge of $\phi 2$ (which shifts in data) following a rising edge of CB1. After 8 pulses on CB1, the interrupt flag will be set and CB1 will remain high. If enabled in the IER, the interrupt pin will go low on the falling edge of $\phi 2$ following the last rising edge of CB1. This interrupt is cleared by the next initialization of the shift operation (see fig. 8)
2	0	1	0	**SHIFT IN UNDER CONTROL OF $\phi 2$** - Similar to mode 1. CB1 is an output and CB2 is an input. CB1 is toggled on the rising edge of $\phi 2$ after shift initialization, providing a frequency half that of $\phi 2$. All other operation is the same as mode 1 (see fig. 9).
3	0	1	1	**SHIFT IN UNDER CONTROL OF EXTERNAL CB1 CLOCK** - CB1 and CB2 are both inputs. Data is shifted in on each falling edge of the first $\phi 2$ cycle after the rising edge of the signal on CB1. Since CB1 may not be synchronized with $\phi 2$, data must be held at CB2 for at least one full $\phi 2$ cycle after the CB1 rising edge. Initialization and interrupt operation is the same as modes 1 and 2 (see fig. 10).
4	1	0	0	**SHIFT OUT FREE RUN AT T2 RATE** - Same as mode 5 except no interrupt, no initialization. When data is written to the SR, it is shifted out as in mode 5, but is shifted back into the most significant bit. CB1 continues toggling and no interrupt flag is set after 8 T2 timeouts. The same data will continue to be shifted out until new data is writen to the SR (see fig. 11).
5	1	0	1	**SHIFT OUT UNDER CONTROL OF T2** - CB1 and CB2 are both outputs. Similar to mode 1, but CB2 is now an output. Last data is maintained on CB2 until next falling edge of $\phi 2$ after falling edge of CB1. Initialization and interrupt operation is the same as mode 1, but last data remains on CB2 until next initialization (see fig. 12).
6	1	1	0	**SHIFT OUT UNDER CONTROL OF $\phi 2$** - Same as mode 5, but CB1 behaves as in mode 2 (see fig 13).
7	1	1	1	**SHIFT OUT UNDER CONTROL OF EXTERNAL CB1 CLOCK** - CB1 is an input and CB2 is an output. Similar clocking operation as mode 3, data is shifted out on the first falling edge of $\phi 2$ after the falling edge of CB1. Data remains on CB1 until next shift. Initialization and interrupt are the same as the mode 6.

To alleviate the synchronization problem of transferring 16 bits of data to the counter simultaneously, the low order count of T1 is always latched when written by the μP (a write to T1C-L or T1L-L). When the count for the high order byte is written (a write to T1C-H), the low order byte is transferred from its latch to the timer. This write to the high order count initiates a count-down on the next cycle of ϕ2 immediately following.

A latch for the high order count of the timer is also provided (T1L-H), because T1 reinitiates its count automatically in one mode of operation. This causes a requirement for the data to be available repeatedly. Writing to this latch does not transfer the data to the count until the current count decrements to zero. Writing to T1C-L and T1L-L are equivalent operations, however reading T1C-L will return the current state of the low order count, just as reading T1C-H returns the current state of the high order count. Reading T1L-L and T1L-H will merely return the values written to those latches by the μP. Writing to T1C-H and reading from T1C-L both clear the interrupt flag (clearing the interrupt to the μP if it is enabled). Any access of the T1L registers will not affect the operation of the interrupt mechanism. A passive read or write of the timer latches, that doesn't affect the current count of the timer, will prove useful in the "continuous" mode of operation.

T1 allows 2 modes of operation, the "single pass mode" and the "continuous mode", selected by the

TABLE 9.
Interrupt Flag Register

IFR bit	Source	Set by	Cleared by
0	CA2	CA2 active edge	Read or Write of O/IRA* or set IFR bit
1	CA1	CA1 active edge	Read or Write of O/IRA or set IFR bit
2	SHIFT REG	Completion of 8 Shift Register shifts	Read or Write of SR or set IFR bit
3	CB2	CB2 active edge	Read or Write of O/IRB* or set IFR bit
4	CB1	CB1 active edge	Read or Write of O/IRB or set IFR bit
5	TIMER 2	Time out of T2	Read T2 low or Write T2 high, or set IFR bit
6	TIMER 1	Time out of T1	Read T1 low or Write T1 high, or set IFR bit
7	$\overline{IRQ}$	Any enabled interrupt	Clearing all enabled interrupts

*See Table 7. If it is indicated there that the flag will not be cleared by a Read or Write of O/IRAor O/IRB, then the flag must be cleared by writing a logic '1' to the bit position in the IFR occupied by the flag. There are several modes of Port A and Port B operation that require this method of flag clearing.

TABLE 10.
Interrupt Enable Register

IER bit	ENABLE DISABLE	Disabled by	Enabled by
0	CA2	Write 0xxxxxx1_2 to IER, returns 1xxxxxx1_2	Write 1xxxxxx1_2 to IER, returns 1xxxxxx0_2
1	CA1	Write 0xxxxx$1x_2$ to IER, returns 1xxxxx$1x_2$	Write 1xxxxx$1x_2$ to IER, returns 1xxxxx$0x_2$
2	SHIFT REG	Write 0xxxx$1xx_2$ to IER, returns 1xxxx$1xx_2$	Write 1xxxx$1xx_2$ to IER, returns 1xxxx$0xx_2$
3	CB2	Write 0xxx$1xxx_2$ to IER, returns 1xxx$1xxx_2$	Write 1xxx$1xxx_2$ to IER, returns 1xxx$0xxx_2$
4	CB1	Write 0xx$1xxxx_2$ to IER, returns 1xx$1xxxx_2$	Write 1xx$1xxxx_2$ to IER, returns 1xx$0xxxx_2$
5	TIMER 2	Write 0x$1xxxxx_2$ to IER, returns 1x$1xxxxx_2$	Write 1x$1xxxxx_2$ to IER, returns 1x$0xxxxx_2$
6	TIMER 1	Write 01$xxxxxx_2$ to IER, returns 11$xxxxxx_2$	Write 11$xxxxxx_2$ to IER, returns 10$xxxxxx_2$

Note: x is intended to represent don't care in all binary representations, returned data is data read subsequent to enable or disable of an interrupt.

state of ACR_b6. In both modes, if $DDRB_b7$ and ACR_b7 are 1, pin PB7 may be controlled by the timer. Otherwise, control reverts to the parallel port. In "single pass mode", the timer will decrement from the programmed count to zero, set the interrupt flag, and disable further interrupts. The interrupt may be cleared by reading T1C-L or by reading T1C-H, but further interrupts are only made possible by initiating another countdown (a write toT1C-H). Writing to T1C-H also effectively loads register T1L-H with the same data. If $ACR_b7 = 1$, and $DDRB_b7 = 1$, then PB7 will be low for the duration of the single pass countdown (N + 1.5 cycles of $\phi 2$, where N is the contents of the low count and the high count), then go high until the next count is initiated. Time from count initiation to interrupt flag set is the same as the period of the PB7 negative pulse.

In "continuous mode" ($ACR_b6 = 1$), rather than disable interrupts after the zero count is reached, the count is transferred into the counter from the high and low order latches, and the timer starts the count over. PB7 alternates between a high and a low on each timeout. The interrupt on timeout may be cleared without affecting the countdown, by reading T1C-L. Providing the ability to alter the contents of the latches without affecting the current count allows the period of the next timeout to be varied. This provides the facility for generating complex waveforms on PB7. The waveform on PB7 in continuous mode begins with a low going half cycle of N + 1.5 $\phi 2$ cycles duration, where N is the value of the count. Subsequent half cycles will be N + 2 $\phi 2$ cycles in duration. Timeout can be "postponed" by writing to T1C-H before timeout occurs. This effectively starts the count immediately at its new value. The ability to do this is valuable for use in "Watchdog" or "Sanity" timer functions (if the interrupt occurs, a recovery process begins).

TABLE 11.
Auxiliary Control Register

b7	b6	b5	b4	b3	b2	b1	b0	Operation
x	x	x	x	x	x	x	0	Port A latch disable
x	x	x	x	x	x	x	1	Port A latch enable
x	x	x	x	x	x	0	x	Port B latch disable
x	x	x	x	x	x	1	x	Port B latch enable
x	x	x	0	0	0	x	x	Shift register disabled
x	x	x	0	0	1	x	x	Shift register shift in under control of T2
x	x	x	0	1	0	x	x	Shift register shift in under control of $\phi 2$
x	x	x	0	1	1	x	x	Shift register shift in under control of extertnal clock
x	x	x	1	0	0	x	x	Shift register shift out free running at T2 rate
x	x	x	1	0	1	x	x	Shift register shift out under control of T2
x	x	x	1	1	0	x	x	Shift register shift out under control of $\phi 2$
x	x	x	1	1	1	x	x	Shift register shift out under control of external clock
x	x	0	x	x	x	x	x	T2 Timer timed interrupt
x	x	1	x	x	x	x	x	T2 Timer count down with pulses on PB6
0	0	x	x	x	x	x	x	T1 Timer timed interrupt each time T1 is loaded (PB7 disabled)
0	1	x	x	x	x	x	x	T1 Timer continuous interrupts (PB7 disabled)
1	0	x	x	x	x	x	x	T1 Timer timed interrupt each time T1 is loaded, PB7 one shot output
1	1	x	x	x	x	x	x	T1 Timer continuous interrupts, square wave output on PB7

Timer 2 Operation

Timer 2 operates in 2 modes: a single pass mode similar to that of T1 ($ACR_b5 = 0$), and a pulse count mode ($ACR_b5 = 1$). Because there is no "continuous" mode operation, a high order byte latch is not needed to store the value of the high order count for sequential timeouts. Again, the interrupt flag may be cleared by reading the T2C-L and writing to T2C-H reinitializes the timeout as well as clearing the interrupt flag. Reading either T2C-L or T2C-H transfers the contents of the timer onto the data bus. Interrupt occurs N + 1.5 $\phi 2$ cycles after timeout initialization just as in T1 operation, but, although interrupts are disabled until reenabled by writing to T2C-H, the count rolls over to $FFFF_H$ and continues to decrement. The user may use this feature to determine how long it took to service the interrupt. Response time is measured by subtracting the count of the timer from $FFFF_H$.

In Pulse counting mode, the count of the timer is decremented by negative pulses on PB6. PB6 must be configured as an input by $DDRB_b6$, and $ACR_b5 = 1$. The interrupt flag is set by the pulse that rolls the count in T2 over to $FFFF_H$. As in other modes, the interrupt may be cleared by reading T2C-L or T2C-H, but to enable subsequent interrupts T2C-H must be written to.

Shift Register Operation

Parallel /Serial I/O operations are made possible by the provision of an 8-bit serial Shift Register (SR). The serial port uses the 2 port B control pins (CB1 and CB2) when operating. CB1 is used for synchronizing the shifting operation. In some modes it is used as an output, providing shift timing for external circuitry; in other modes it is used by the external circuitry to control the shift operation of the MD65SC22. CB2 is the data stream, and can be configured as either an input or an output.

When being used as an output, data in the SR is shifted from the least significant bit, towards the most significant bit, through the intervening bits. From the most significant bit, the data is shifted out of CB2. This direction of shifting produces a serial data stream starting with the most significant bit of the SR contents and ending with the least significant bit of the SR contents. When CB2 is being used as an input, the same shift direction is followed, so the first bit in the serial stream will become the most significant bit in the SR after 8 shifts.The order of bit transmission and reception should be taken into consideration when trying to use the MD65SC22 to communicate with a device that uses a standard serial communication protocol (MD65SC51 ACIA), as these devices shift the least significant bit out first.

The operating mode of the SR is determined by the state of several bits in the ACR: ACR_b4, ACR_b3 and ACR_b2. For a description of the operating modes of the SR, see Table 8.

Interrupt Registers (IFR and IER)

Control and monitoring of the many different interrupts that may originate from the MD65SC22 is implemented by the Interrupt Flag Register and the Interrupt Enable Register. Specific events have been described that set (logic '1') a bit in the interrupt flag register. Such an event does not necessarily interrupt the microprocessor. To assert the interrupt pin, the bit in the IER that coincides with the set flag must be set (by a write of a logic 1 from the μP). IFR_b7 reflects the state of the interrupt pin. If the interrupt pin is asserted, IFR_b7 will be set (logic '1'), otherwise it will be clear.

The IFR may be read to determine the origin of an interrupt, or it may be written to. Writing to the IFR provides an alternate method of clearing an interrupt flag (modes 1 & 3 - CA2 and CB2). This may be done by writing a logic '1' to the bit intended to be cleared. IFR_b7 may not be cleared in this manner, it may only be cleared if all other flags in the register are cleared, or disabled in the IER.

IER is also a read/write register. As explained, writing to the register enables or disables interrupts to the μP. If IER_b7 is a 0, when writing a byte of information to IER, any other bit in the byte that is a logic '1' clears its corresponding interrupt enable bit. When a 1 is written to IER_b7 , any other bit in the byte that is a logic '1' sets its corresponding interrupt enable (set = enable; clear = disable). Reading the register returns the enabled/disabled information (enabled = logic '1'; disabled = logic '0') written to the register, except for IER_b7. This bit always returns a logic '1'.

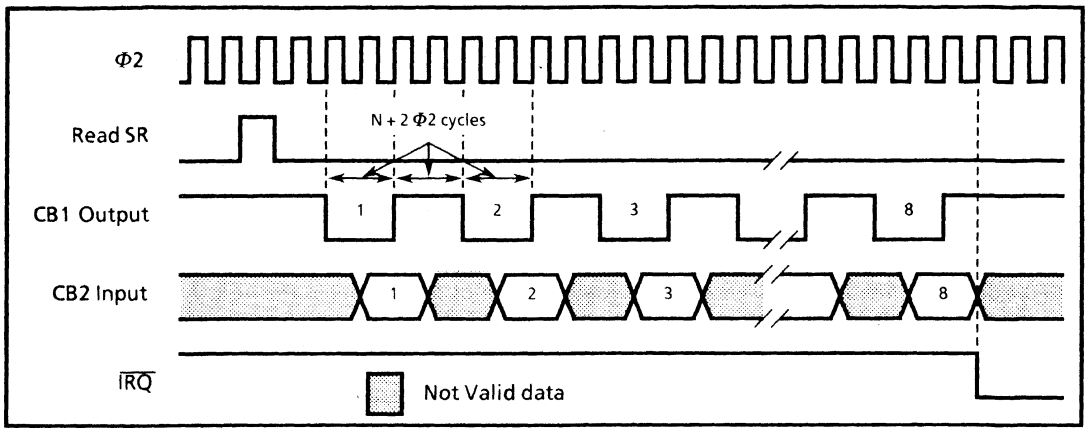


Figure 8. Shift Register timing in mode 1

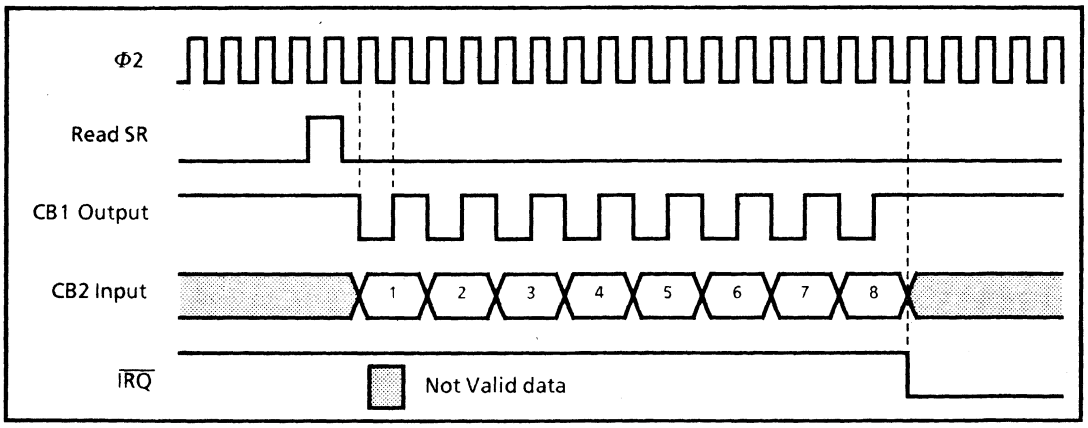


Figure 9. Shift Register timing in mode 2

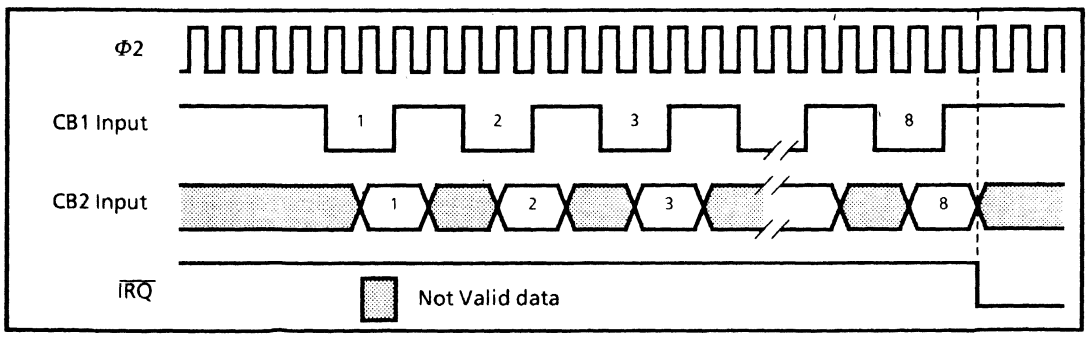


Figure 10. Shift Register timing in mode 3

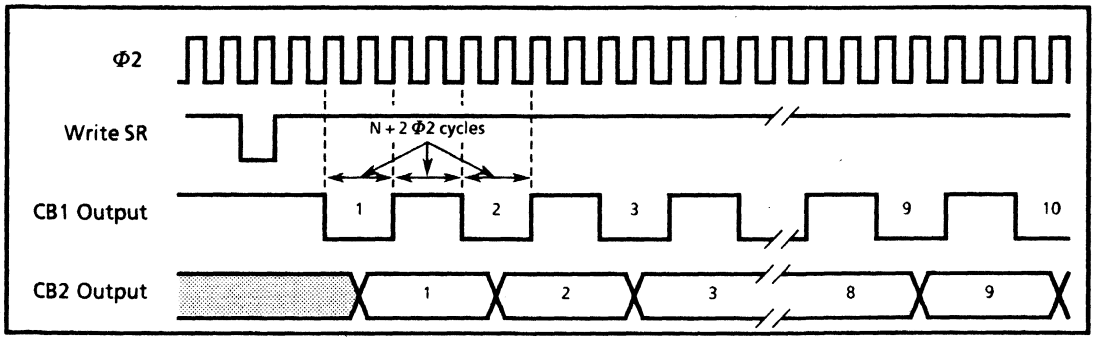


Figure 11. Shift Register timing in mode 4

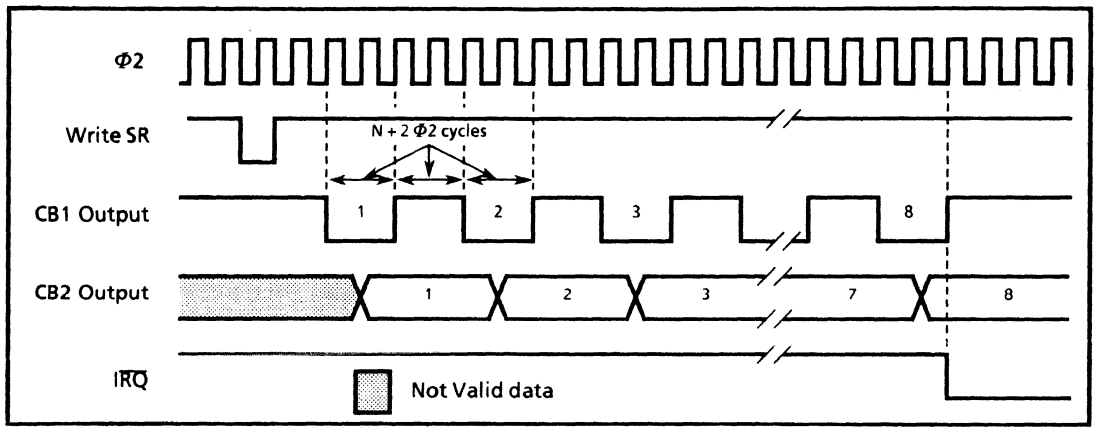


Figure 12. Shift Register timing in mode 5

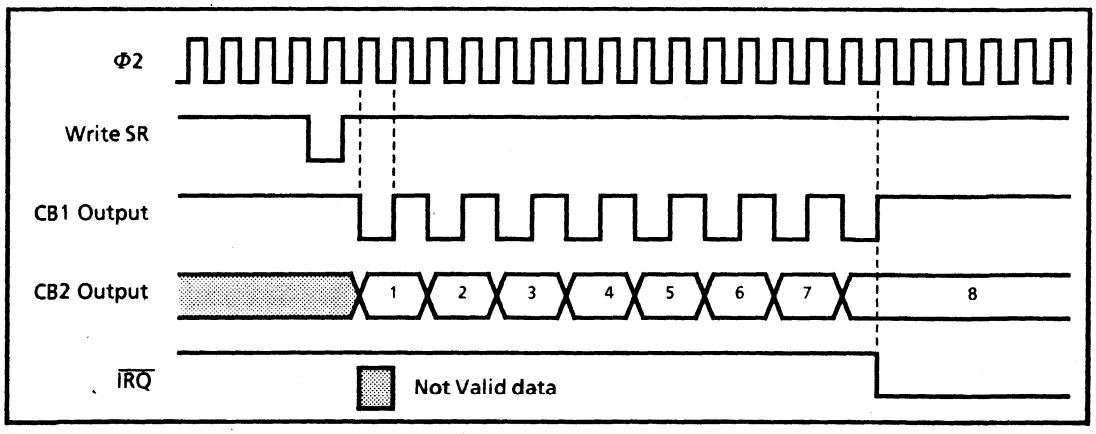


Figure 13. Shift Register timing in mode 6

Note: Shift register mode 7 has similar timing characteristics to mode 6 except CB1 is an input, and is not dependent Φ2. IRQ goes low on the next rising edge of Φ2 after the rising edge of the eighth CB1 Pulse

NOTES:

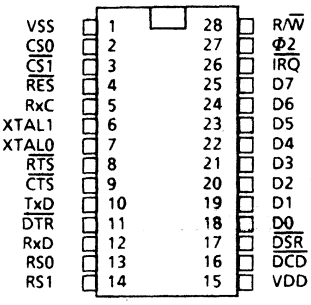
ISO-CMOS MD65SC51B
Asynchronous Communications Interface Adapter
Preliminary Information

9161-002-052 NA ISSUE 2 JUNE 1986

Features

- Replacement for existing NMOS part
- 15 selectable baud rates from 50 bits/s to 19.2 Kbits/s or 1/16th of an external clock rate.
- Selectable word length & number of stop bits.
- Selectable echo mode.
- Full or half duplex operation.
- Data set/modem control functions.
- Parity generation and checking.
- Low power ISO-CMOS technology.
- TTL compatible.
- Single 3-6 volt power supply.

Pin Connections



Ordering Information

MD65SC51BE	Plastic Dual-in-Line Package
MD65SC51BC	Ceramic Dual-in-Line Package

Applications

- Microprocessor to modem bidirectional link.
- Microprocessor (μP) serial data interface.
- Serial Input/Output interface.

Description

The MD65SC51 is an Asynchronous Communication Interface Adapter fabricated in MITEL ISO-CMOS technology. The device provides interfacing between a μP and a modem.

The MD65SC51 will also control all of the interrupt handling between the μP and the modem. An on-board baud rate generator is available to derive one of 15 selectable baud rates or 1/16th of an external clock rate.

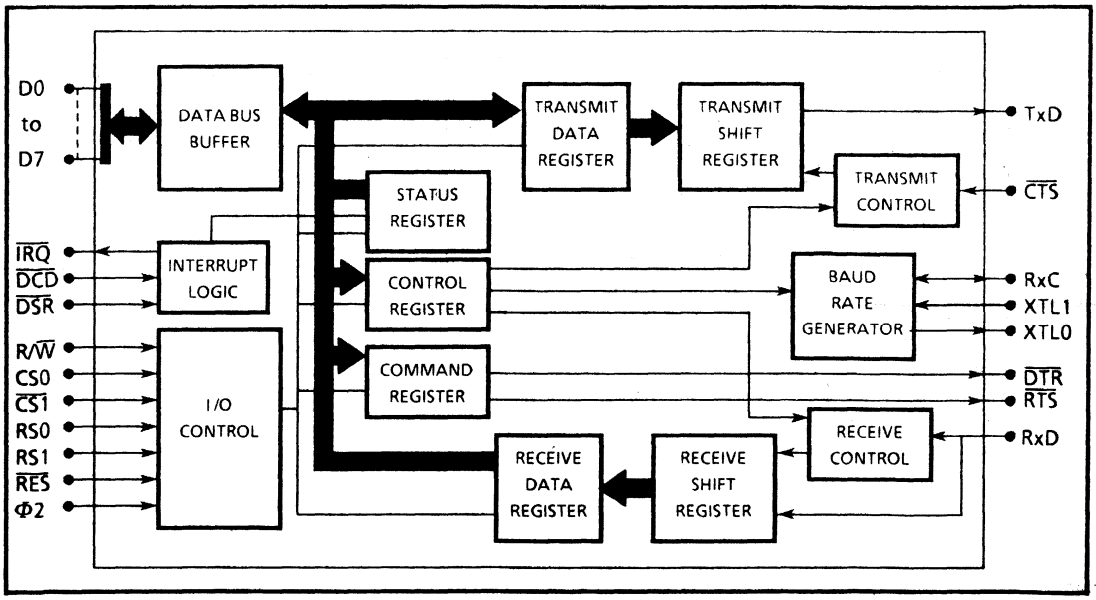


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD} - V_{SS}	- 0.3	7.0	V
2	Voltage on any I/O pin	V_I	V_{SS}-0.3	V_{DD} + 0.3	V
3	Current on any I/O pin	I_I		± 10	mA
4	Storage Temperature	T_S	-65	+ 150	°C
5	Power Dissipation Plastic	P_D		0.6	W
	Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply Voltage	V_{DD}	3.0	5.0	6.0	V	
2		Input Voltage	V_I	0		V_{DD}	V	
3		Operating Temperature	T_A	-40	+ 25	+ 85	°C	
4		Operating Frequency	f	0		2.0	MHz	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent Supply Current	I_{DD1}		2		µA	Outputs Unloaded
2		Operating Supply Current	I_{DD}		2		mA/MHz	Outputs Unloaded
3	I N P U T S	Input High Voltage XTAL1	V_{IH}	3.0		V_{DD}	V	
		OTHER INPUTS	V_{IH}	2.0		V_{DD}	V	
4		Input Low Voltage	V_{IL}	0		0.8	V	
5		Input Leakage Current RxC, (D_0-D_7)	I_{IZ}			10	µA	V_{IN} = 0 to V_{DD}
		Other Inputs (Except XTAL1)	I_{IZ}			2.5	µA	V_{IN} = 0 to V_{DD}
6		Input Capacitance (D_0-D_7)	C_{IN}		5.0		pF	
		Other Inputs (Except XTAL1)	C_{IN}		10.0		pF	
7		Output High Voltage	V_{OH}		V_H①		V	I_{OH} = -20 µA
		(D0-7,TxD, $\overline{RTS}$, $\overline{DTR}$, RxC)	V_{OH}	2.4			V	I_{OH} = -100 µA
8		Output Low Voltage (D0-7,TxD, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$, RxC)	V_{OL}			0.4	V	I_{OL} = 1.6 mA
9		Output Leakage Current $\overline{IRQ}$ (OFF state)	I_{OZ}		10		µA	V_O = V_{SS} to V_{DD}
11		Output Capacitance	C_O		5.0		pF	

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

① V_H = V_{DD} - 0.1 Volts

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes
1	MPU INTERFACE	Φ_2 Cycle Period	t_{CYC}	500	310		ns	See timing diagram 1
2		Φ_2 HIGH Pulse Width	t_C	200			ns	See timing diagram 1
3		Address Set-Up Time	t_{AS}	70			ns	See timing diagram 2, 3
4		Address Hold Time	t_{AH}	0			ns	See timing diagram 2, 3
5		Φ_2 to Valid Data Delay	t_{DDR}			150	ns	See timing diagram 2
6		Data Hold Time (Read)	t_{DHR}	10			ns	See timing diagram 2
7		Data Set-Up Time (Write)	t_{DSW}	60			ns	See timing diagram 3
8		Data Hold Time (Write)	t_{DHW}	10			ns	See timing diagram 3
9		Read/Write Set-up Time	t_{RWS}	70			ns	See timing diagram 2,3
10		Read/Write Hold Time	t_{RWH}	0			ns	See timing diagram 2,3
11	COMMUNICATION INTERFACE	External TxD Clock Cycle Period	t_{ECP}	0.4			μs	See timing diagram 4
12		External TxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 4
13		External TxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 4
14		External Clock to Valid Data Transmitted	t_{TXDD}			500	ns	See timing diagram 4
15		$\overline{RTS}$ and $\overline{DTR}$ Propagation Delay from Φ_2	t_{DLY}			500	ns	See timing diagram 5
16		$\overline{IRQ}$ Propagation Delay from Φ_2 (CLEAR)	t_{IRQD}			500	ns	See timing diagram 5
17		External RxD Clock Cycle Period	t_{ECP}	0.4			μs	See timing diagram 6
18		External RxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 6
19		External RxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 6

† Timing is over recommended temperature range & V_{CC} = 5V ±5%, Test loads shown in Figures 2 and 3.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note : Rise and Fall times (t_R & t_F) are 10 to 30 ns

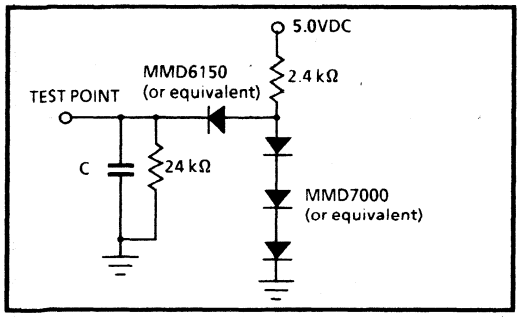


Figure 2. Test load for D_0 - D_7, $\overline{TxD}$, $\overline{DTR}$ $\overline{RTS}$

C = 130 pF for D_0-D_7, C = 30 pF for other outputs

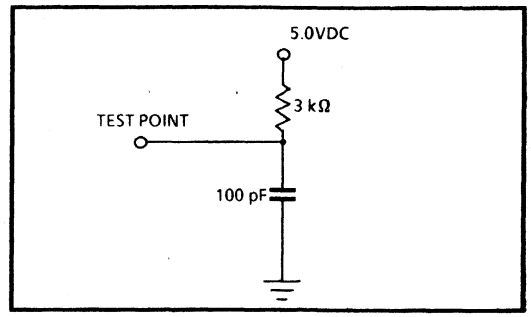
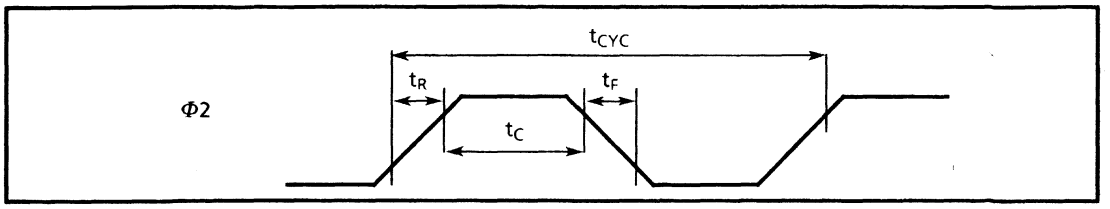


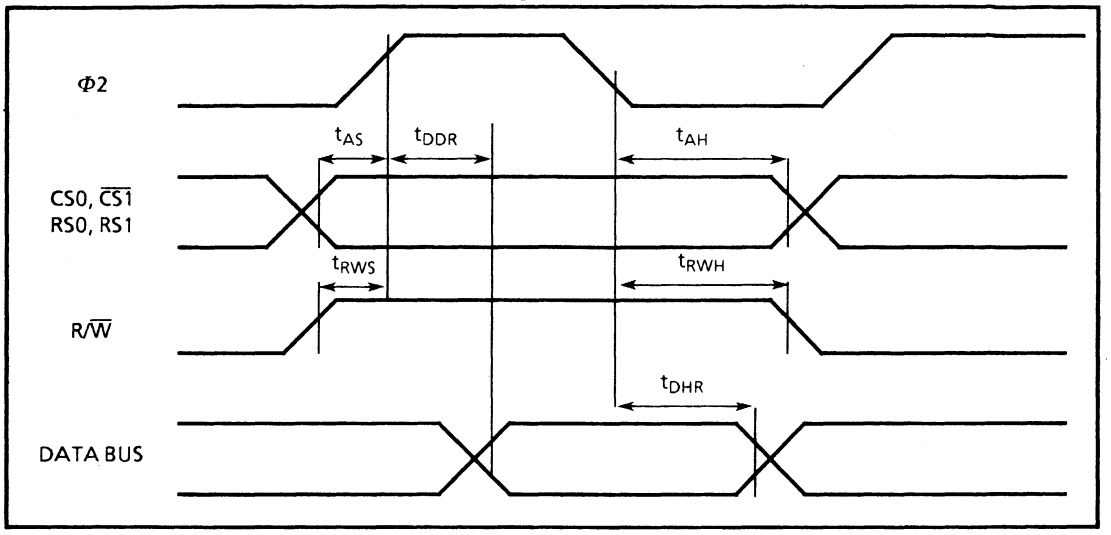
Figure 3. Test load for $\overline{IRQ}$

Timing Diagrams

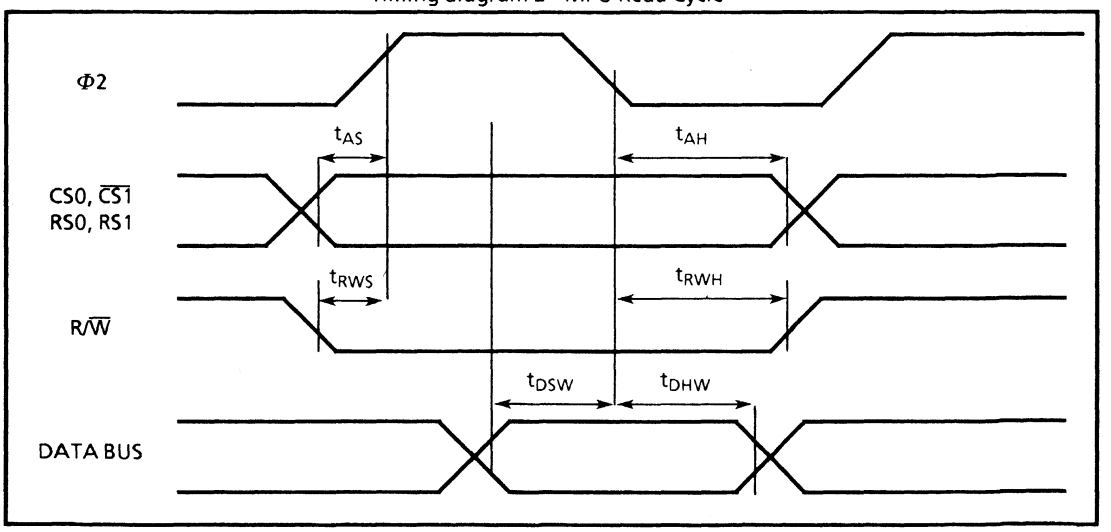
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs



Timing diagram 1 Φ2 clock



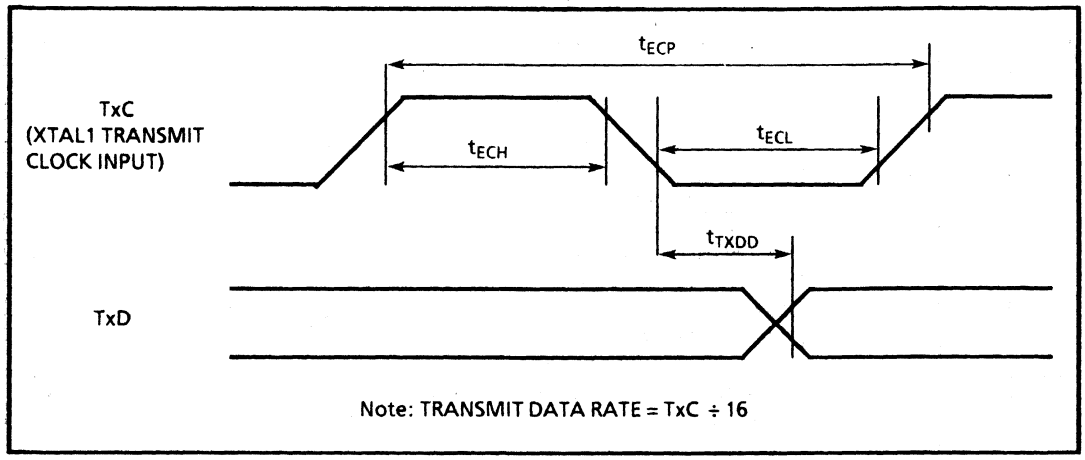
Timing diagram 2 MPU Read Cycle



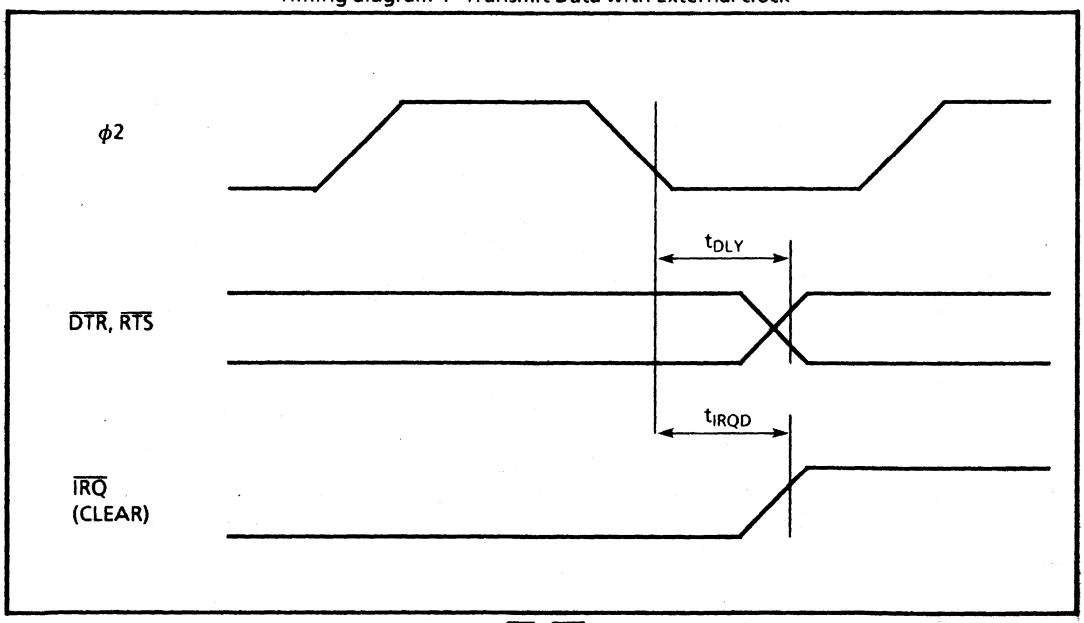
Timing diagram 3 MPU Write Cycle

Timing Diagrams

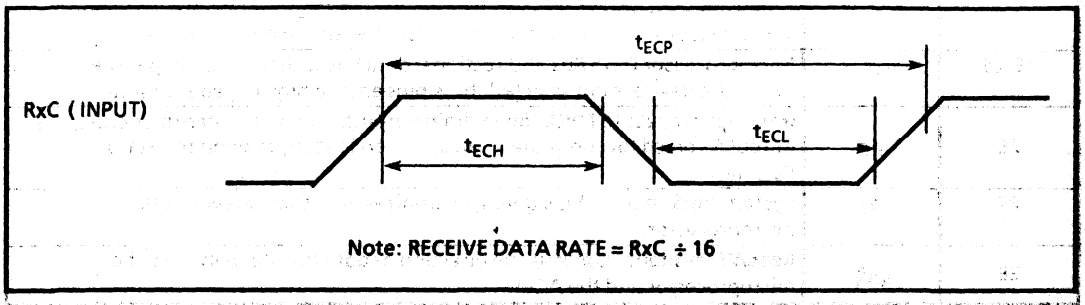
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs



Timing diagram 4 Transmit Data with External clock



Timing diagram 5 $\overline{RTS}$, $\overline{DTR}$ & MPU Interrupt



Timing diagram 6 Receive External clock timing

TABLE 1.
Pin Description

Pin	Name	Description
1	V_{SS}	**Ground Input.** 0 V.
2,3	CS0, $\overline{CS1}$	**Chip Select.** TTL inputs CS0 = 1 & $\overline{CS1}$ = 0 select the chip for data transfer on the microprocessor bus. The direction of the transfer is determined by the state of the R/$\overline{W}$ pin.
4	$\overline{RES}$	**Hardware Reset.** $\overline{RES}$ = 0 to reset the chip. All internal registers will be cleared except bits 4, 5 and 6 in the Status Register (SR_b4, SR_b5 and SR_b6). SR_b4 is set, and SR_b5 and SR_b6 are unaffected.
5	RxC	**Receive Clock.** This is a bidirectional pin which serves as either the receiver 16x clock input or the receiver clock 16x output. The latter mode is selected if the internal baud rate generator is used as the receiver clock source.
6	XTAL1	**Clock Input.** For External Clock or Crystal connection. If clock is stopped, this input must be held high. XTAL1 has CMOS compatible voltage thresholds (See figure 4).
7	XTAL0	**Clock connection.** This pin must be connected to the side of a crystal opposite to XTAL1, or left floating when using an external clock (See figure 4).
8	$\overline{RTS}$	**Request to Send.** Output signal to the modem from the ACIA to control data transfers (see COMMAND REGISTER table 3).
9	$\overline{CTS}$	**Clear to send.** Input signal from the modem to the ACIA to control data transfers. When this input is held high, the transmitter is disabled.
10	TxD	**Transmit Data.** Serial data output in NRZ (Non Return to Zero) format.
11	$\overline{DTR}$	**Data Terminal Ready.** Output to the modem to indicate the ACIA status. $\overline{DTR}$ = 1 if ACIA is disabled (see COMMAND REGISTER table 3).
12	RxD	**Receive Data.** Serial data input NRZ (Non Return to Zero) format.
13,14	RS0,RS1	**Register Select Inputs.** The state of these pins determines which internal register is connected to the data bus when the device is selected (see chip select description and Register Decode Table).
15	V_{DD}	**Positive Supply Input.** + 5 V.
16	$\overline{DCD}$	**Data Carrier Detect Input.** Status of carrier at the modem. [$\overline{DCD}$ = 0 if the carrier is detected]. The state of this pin is reflected by bit 5 of the Status Register (SR). If interrupts are enabled (Command Register (CR) bit 0 = 1), and the logical state $\overline{DCD}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect transmitter function but a logical low must be present for the receiver to operate.
17	$\overline{DSR}$	**Data Set Ready Input.** $\overline{DSR}$ = 0 if the modem is ready to perform a data transfer. The state of this pin is reflected by SR_b6. If interrupts are enabled (CR_b0 = 1), and the logical state of $\overline{DSR}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect the transmitter or the receiver function.
18-25	D_0-D_7	**Microprocessor Data Bus.** Bidirectional data bus which is TTL compatible. When the device is not selected these pins enter a high impedance state.
26	$\overline{IRQ}$	**Interrupt request to MPU.** (open drain output). When an interrupt occurs, this output is forced low until the interrupt is serviced (by reading the Status Register).
27	ϕ_2	**System clock input.** This signal synchronizes data transfers with the microprocessor.
28	R/$\overline{W}$	**Read/Write Input.** Controls the direction of data transfer between the microprocessor and the ACIA.

FUNCTIONAL DESCRIPTION

The MD65SC51 Asynchronous Communications Interface Adaptor provides processor (μP) based systems with a full duplex serial interface. The μP port is directly compatible with 6800/6500 style bus architectures. Coupled with the Status Register, a powerful and flexible interrupt facility is included on the MD65SC51 to allow fast response from the μP to the ACIA.

The serial port provides signals which may be used to control a communication channel compatible to the EIA Standard RS-232C specification. An on-board baud rate generator allows 16 different baud rates, for data transmission and reception timing. All frequencies are derived from an external clock or crystal. The receive frequency may be received separately from the transmit frequency, allowing reception and transmission at independent speeds. Alternatively, the ACIA will produce a signal that is 16 times the baud rate, for use by a remote ACIA (Table 1 - RxC).

The format of the data word is programmable. The word length ranges from 5 to 9 bits (including parity). Parity can be odd, even or deselected altogether. The parity bit may also be forced high

TABLE 2.
Register Address Decoding

RS1	RS0	Internal Register Selected		Reset operation Effect													
				Hardware Reset								Programmed Reset					
		Write	Read	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	Transmit Data Register	Receive Data Register	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	1	Programmed Reset	Status Register	0	-	-	1	0	0	0	0	-	-	-	-	-	0	-	-
1	0	Command Register	Command Register	0	0	0	0	0	0	0	0	-	-	-	0	0	0	0	0
1	1	Control Register	Control Register	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Note: "-" denotes no change from state previous to reset

TABLE 3.
Command Register Description

Command Register Bit								Control Function	Resulting Function
7	6	5	4	3	2	1	0		
x	x	0	x	x	x	x	x	Parity Mode Control	No Parity Bit transmitted or received
0	0	1	x	x	x	x	x		Odd Parity Bit transmitted or received
0	1	1	x	x	x	x	x		Even Parity Bit transmitted or received
1	0	1	x	x	x	x	x		Parity Bit set to MARK (Receive parity check disabled)
1	1	1	x	x	x	x	x		Parity Bit set to SPACE (Receive parity check disabled)
x	x	x	0	x	x	x	x	Echo Mode Enable	Normal Operation
x	x	x	1	0	0	x	x		Echo Mode Enabled (bits 2 and 3 must be 0).
x	x	x	x	0	0	x	x	Transmit Interrupt Control	Transmit interrupt disabled. $\overline{RTS}$ set High (Transmitter off).
x	x	x	x	0	1	x	x		Transmit interrupt enabled. $\overline{RTS}$ set Low (Transmitter on).
x	x	x	x	1	0	x	x		Transmit interrupt disabled. $\overline{RTS}$ set Low (Transmitter on).
x	x	x	x	1	1	x	x		Transmit interrupt disabled. $\overline{RTS}$ set Low (Transmit Break on TxD).
x	x	x	x	x	x	0	x	Receiver Interrupt Enable	Receiver interrupts enabled
x	x	x	x	x	x	1	x		Receiver interrupts disabled
x	x	x	x	x	x	x	0	Data Terminal Ready	Data terminal not ready to transfer data ($\overline{DTR}$ = 1). Receiver and all interrupts disabled.
x	x	x	x	x	x	x	1		Data terminal ready to transfer data ($\overline{DTR}$ = 0). Receiver and all interrupts enabled.

Note: "x" is intended to represent don't care in all binary representations in this and all following tables.

or low. Either 1, 1.5, or 2 stop bits may be added to the end of the serial data stream. For maintenance applications, the received data stream may be looped back onto the transmit data stream using echo mode operation.

SERIAL INTERFACE DESCRIPTION

Transmitted and Received Data

Data is transmitted from the ACIA on the TxD pin, and received on the RxD pin. The inactive state of either data channel (RxD or TxD) is a mark condition (logical high). This type of data code is termed Non-Return to Zero (NRZ). Data transmitted or received by the MD65SC51 is always preceded by a "start bit".

The start bit is a space condition (logical low) which signifies the start of active data on the channel. The receiving ACIA also uses the start bit to optimize its sampling for the middle of the data bits that follow. Between received words, the ACIA samples the channel at 16x Baud rate. When a low is detected, the ACIA waits half a bit period before sampling again. This delay allows subsequent bits (sampled at the same frequency as the baud rate) to be sampled as far from the bit boundaries as possible. Noise or "glitch" immunity is also added by this mechanism. Low going pulses of less than 1/2 a bit period wide will not be mistaken for the start bit (the ACIA resumes the 16x sampling rate).

Data bits following the start bit are in ascending order, with the least significant bit (LSB) first, and the most significant bit (MSB) last. The MSB depends on the number of bits per word selected; the ACIA can be programmed for 5 bit, 6 bit, 7 bit or 8 bit data word transmission/reception. Each bit has a period equal to the reciprocal of the selected baud rate, which in turn is dependent on the clock source frequency (see table 4).

Parity sensing and generation can be chosen for odd parity, even parity or no parity. When parity is

TABLE 4.
Control Register Description

Control Register Bit								Control Function	Resulting Function
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	Stop Bit Control	1 stop bit.
1	x	x	x	x	x	x	x		2 stop bits except in the following cases: a/ 1 stop bit if word length set for 8 bits & parity enabled ② b/ 1.5 stop bits if word length set for 5 bits & parity disabled
x	0	0	x	x	x	x	x	Word Length Setting	8 bits
x	0	1	x	x	x	x	x		7 bits.
x	1	0	x	x	x	x	x		6 bits.
x	1	1	x	x	x	x	x		5 bits.
x	x	x	0	x	x	x	x	Receiver Clock Source	External clock source. (RxC is Input)
x	x	x	1	x	x	x	x		Internal baud rate generator. (RxC is Output)
x	x	x	x	0	0	0	0	Baud Rate Control	115.2 kbaud① or (Frequency) ÷ 16
x	x	x	x	0	0	0	1		50 baud① or (Frequency) ÷ 36,864
x	x	x	x	0	0	1	0		75 baud① or (Frequency) ÷ 25,576
x	x	x	x	0	0	1	1		109.92 baud① or (Frequency) ÷ 16,769
x	x	x	x	0	1	0	0		134.58 baud① or (Frequency) ÷ 13,704
x	x	x	x	0	1	0	1		150 baud① or (Frequency) ÷ 12,288
x	x	x	x	0	1	1	0		300 baud① or (Frequency) ÷ 6,144
x	x	x	x	0	1	1	1		600 baud① or (Frequency) ÷ 3,072
x	x	x	x	1	0	0	0		1200 baud① or (Frequency) ÷ 1,536
x	x	x	x	1	0	0	1		1800 baud① or (Frequency) ÷ 1,024
x	x	x	x	1	0	1	0		2400 baud① or (Frequency) ÷ 768
x	x	x	x	1	0	1	1		3600 baud① or (Frequency) ÷ 512
x	x	x	x	1	1	0	0		4800 baud① or (Frequency) ÷ 384
x	x	x	x	1	1	0	1		7200 baud① or (Frequency) ÷ 256
x	x	x	x	1	1	1	0		9600 baud① or (Frequency) ÷ 192
x	x	x	x	1	1	1	1		19,200 baud① or (Frequency) ÷ 96

notes : ① The preset baud rates given assume a crystal frequency of 1.8432 MHz
② To enable and disable parity, see table 3.

selected, the parity bit follows the MSB of the data word. For even parity, the condition of the parity bit will be such that there are an even number of marks when considering the data word and the parity bit. With odd parity, the condition of the parity bit will be such that there is an odd number of marks when considering the data word and the parity bit (both cases exclude the start and stop bits).

Transmit and Receive Clocks

The signals used by the ACIA for transmit/receive timing are found on 3 pins: XTAL0, XTAL1 and RxC. XTAL1 and XTAL0 are the input and output, respectively, of a crystal oscillator circuit. The crystal can be connected to these pins as seen in figure 4. This oscillator circuit drives the internal baud rate generator, which divides the square wave output of the oscillator by the divisor selected (see table 4). If a crystal is not used, an external clock may drive the oscillator input while the oscillator output is left floating. If the clock is stopped (device still powered), the oscillator input should be held to a logical high.

The clock for the receiver may be taken from 1 of 2 sources: the output of the internal baud rate generator, or from an external clock input on the RxC pin. In the latter case, the baud rate is 1/16th of the external clock. If the source of receiver timing is the internal baud rate generator, RxC becomes an output and sources a clock 16 times (16x) the baud rate (for driving remote ACIAs).

Control Signals

These signals are compatible with the RS-232C modem control circuits. The signals are the Request To Send ($\overline{RTS}$), Data Terminal Ready ($\overline{DTR}$) outputs and the Clear To Send ($\overline{CTS}$), Data Set Ready ($\overline{DSR}$) and Data Carrier Detect ($\overline{DCD}$) inputs. Note that the ACIA is viewed as the Data Termination Equipment (DTE) as opposed to the Data Communication Equipment (DCE) when referencing the RS-232C specification.

Request To Send. $\overline{RTS}$ is used to indicate to the DCE that it should assume the data channel transmit mode. The state of this output is controlled by bits 2 and 3 of the Command Register ($COMR_b2$ and $COMR_b3$, see table 3). When it is high (not asserted, or in other words, "negated") the ACIA's transmitter is disabled.

Data Terminal Ready. The $\overline{DTR}$ signal indicates to the DCE that the ACIA is ready for communication. This output is asserted when $COMR_b0$ is set.

Clear To Send. The $\overline{CTS}$ signal from the DCE tells the ACIA that the DCE is prepared to accept data to pass on to the remote end of the communication channel. When this signal is not asserted, the transmitter of the ACIA is disabled. If the ACIA is in the middle of transmitting a data word when $\overline{CTS}$ is negated, the TxD channel goes immediately to a mark condition. The data word being transmitted at the time is lost, but the character (if any) in the Transmit Data Register (TDR) is not (see register description). As soon as $\overline{CTS}$ is asserted, this data

TABLE 5.
Status Register Description

Status Register bit	Control signal	Status Flag Set by	Status Flag Cleared by
0	PARITY ERROR③	Parity error detected	Cleared Automatically after a read of the Receive Data Register and next error free reception of data.
1	FRAMING ERROR③	Framing error detected	
2	OVERRUN③	Overrun has occurred.	
3	RECEIVE REGISTER	Register full.	Read Receive Data Register
4	TRANSMIT REGISTER	Register empty.	Write Transmit Data Register.
5	$\overline{DCD}$	Carrier not detected (a high on $\overline{DCD}$).④	Carrier detected (a low on $\overline{DCD}$).④
6	$\overline{DSR}$	Data set not ready (a high on $\overline{DSR}$).④	Data set ready (a low on $\overline{DSR}$).④
7	INTERRUPT	Interrupt has occurred. The $\overline{IRQ}$ signal to the microprocessor also goes low.	Read Status Register. This also clears the $\overline{IRQ}$ signal to the microprocessor.

notes ③ No interrupt is generated from these conditions.
④ These bits are not resetable and reflect the state of the input.

TABLE 6.
Crystal Specification

Characteristics	Spec.
Temperature stability @ -45 to +85°C	± 0.01%
Frequency* (MHz)	1.8432
Frequency tolerance* (± %)	0.02
Resonance mode*	parallel
Equivalent resistance* (ohms)	400 max.
Drive level* (mW)	2
Shunt capacitance* (pF)	7 max.
Load capacitance* (pF)	16.5 typ.
Oscillation mode*	Funda-mental

*characteristics at 25°C ± 2°C

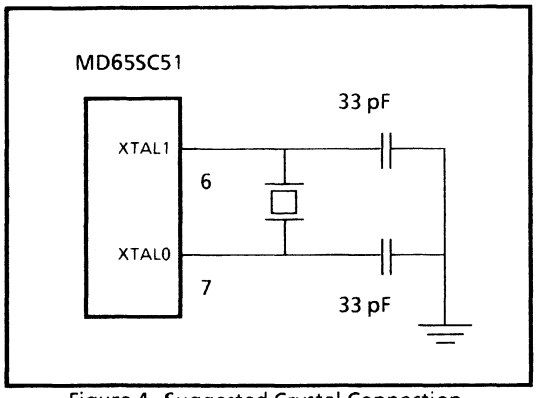


Figure 4. Suggested Crystal Connection

word will be transmitted, if the transmitter is still enabled internally (see figure 8).

Data Set Ready. The $\overline{DSR}$ signal from the DCE tells the ACIA that the DCE is ready to operate. A transition on this pin can cause an interrupt (if interrupts are enabled) and the state of the pin is reflected in the state of SR_b6. Transitions that follow will not affect the status bit until after the μP has serviced the first interrupt (read the SR). At that point the SR will again reflect the current level of the $\overline{DSR}$ input, and an interrupt will occur again if it has changed. Transmitter and receiver operation is not affected by the level of this pin.

Data Carrier Detect. The $\overline{DCD}$ signal from the DCE indicates to the ACIA that the received signal is within specified limits. When $\overline{DCD}$ is not true, the receiver of the ACIA will be disabled and the data being shifted in at that moment is lost. A transition on this pin, like the $\overline{DSR}$ input, causes an interrupt. Subsequent transitions will not affect the status bit until the first interrupt is serviced. If the pin has changed since the first occurred and before it was serviced, another interrupt will occur. An even number of level changes on $\overline{DSR}$ and $\overline{DCD}$, before the first interrupt has been serviced, will not cause another interrupt. This is because the status bits will be at the same logic level that caused the original interrupt.

REGISTER DESCRIPTION

The MD65SC51 contains 7 registers, 5 that are visible to the μP. These registers are: the Transmit Shift Register (TSR, not available to μP), the Receive Shift Register (RSR, not available to μP), the Transmit Data Register (TDR), the Receive Data Register (RDR), the Status Register (SR), the Command Register (COMR), and the Control Register (CR). One of the 5 latter registers is visible to the μP when the chip selects (CS0, CS1) are asserted and the E clock is true (high); the register chosen by the state of the register selects (RS0, RS1). The direction of μP bus transfer is determined by the state of the R/$\overline{W}$ signal (a high indicates a read of the contents of the register, a low a write to a register). When the SR is written to (the data written doesn't matter) a software reset will occur. For a comparison between the effect of a hardware reset and a software reset, see table 2.

Transmit Data Register

The Transmit Data Register (TDR), in conjunction with the Transmit Shift Register, is used to place data on the transmit channel (TxD). If no word is being transmitted, a data word written to the TDR is immediately transferred into the TSR to be shifted out. A start bit precedes the data on the TxD channel; parity is added to the end of the word as needed (after the valid MSB is shifted out); and 1, 1.5, or 2 stop bits follow to end the transmitted information. If the ACIA is programmed to send a data word that is less than 8 bits in length (5, 6 or 7 bits), the extra bits in the data word are ignored.

While the TSR is occupied shifting out active data onto TxD (including the bit periods for the transmission of parity bits and stop bits), information written to TDR will be latched and held. When the last stop bit of the previous word is finished, the ACIA will transfer the data word in the TDR into the TSR and transmit it. If the TDR is written to more than once while information is

being transmitted on TxD, the data word in TDR will be overwritten and retain the data associated with the last write.

If transmit interrupts are enabled, when the TDR is empty an interrupt will occur and SR_b4 will be set (SR_b4 will be set even if interrupts are disabled). This coincides with the beginning of the start bit for the data just transferred to the TSR. The interrupt must be serviced to be removed (by reading SR), but SR_b4 may only be cleared by a write to the TDR. If the interrupt is serviced but TDR is not written to, another interrupt will occur at the next word boundary (word boundaries are referenced to the start of the last transmitted word, and occur every full word period after the end of that word. This timing is reset by a new transmission because, if TxD is idle the new word is transmitted immediately - see figures 5 & 7).

Receive Data Register

Data on the receive channel (RxD) is stripped of the overhead bits (start, parity and stop) by the ACIA and shifted into the Receive Shift Register (RSR). When a full data word has been received (depending on the programmed length), the contents of the RSR are transferred into the Receive Data Register (RDR). If receive interrupts are enabled, this transfer will cause an interrupt to occur and SR_b3 to be set (SR_b3 is set even when interrupts are disabled). The interrupt actually occurs about 9/16 through the last stop bit. As with the TDR, the interrupt is removed by reading SR and SR_b3 is cleared by reading the RDR.

If $\overline{DCD}$ is not asserted, the RSR is immediately disabled and any word being received at the time is lost. If the receive circuitry is disabled through the Command Register, a data word in the process of being received will be finished before the the RSR is disabled.

When a continuous break character is received, the first character period will look like a data word of all zeroes and a framing error. If interrupts are enabled, an interrupt will occur. Thereafter the receiver will be disabled until a stop bit is received, so no more interrupts will occur. It is possible that the μP could interpret a data word made up of zeroes, without a stop bit in the correct position, as a received break condition (see figure 6 and 12).

Command Register

The Command Register (COMR) determines the type of parity used in the transmitted word, and the type of parity checked for in the received word. Parity is controlled by COM_b5 - COM_b7 (see table 3). The bit position normally occupied by a parity bit may be forced to a mark or a space if required.

$COMR_b4$ enables or disables echo mode (for echo to be enabled, COM_b2 and COM_b3 must both be 0). When in echo mode, the ACIA's receive circuitry is still operational, but data written to the TDR will not be transmitted until echo mode is disabled and the transmitter is reenabled. $\overline{RTS}$ is asserted in echo mode, even though it is not programmed to be active by $COMR_b3$ and $COMR_b2$.

When data is received on RxD (the receiver must be enabled internally and $\overline{DCD}$ true) it is transmitted 1/2 bit period after it has been received. Interrupts occur just as they would when initiated by any received data (If interrupts are enabled). If echo mode is disabled during reception of a character, transmission on TxD stops immediately and $\overline{RTS}$ is negated. The word continues to be shifted into the RSR if it is still enabled (see figures 10 and 11).

$COMR_b2$ and $COMR_b3$ control the transmit circuitry, disabling or enabling the transmitter and $\overline{RTS}$, and disabling or enabling transmit interrupts. If continuous break mode is selected during the transmission of a data word, the current word will be transmitted and the break condition will begin immediately after. Transmit interrupts are automatically disabled during the transmit break condition.

The break condition will last for at least one character period, so if the transmitter is enabled immediately after the break condition has been set (assuming the ACIA has begun to transmit the break) the transmitter will not return to normal operation until after one character period of break. When the break mode is removed, one stop bit will be placed on TxD before the transmission of the next word.

$COMR_b1$ enables or disables receiver interrupts and $COMR_b0$ enables or disables the receiver circuitry, all interrupts and the $\overline{DTR}$ signal. See figure 3.

Control Register

The Control Register (CR) determines the number of stop bits in transmitted and received information; the length of the word: the source of the receive and transmit timing and the divisor used by the baud rate generator.

Note that when the receiver clock source is chosen such that RxC is an input, the setting of the baud rate generator has no effect on the receiver speed. See table 4.

Status Register

The Status Register (SR) performs a "housekeeping" function for the ACIA. The SR contains several error bits, 2 bits to display the state

of the transmit and receive registers, 2 bits used for modem status and 1 bit for displaying interrupt status.

SR_b7 is the inverse of the $\overline{IRQ}$ signal. When an interrupt is active, SRb7 is set. It is cleared by reading the SR.

SR_b5 and SR_b6 reflect the state of the $\overline{DCD}$ pin and the $\overline{DSR}$ pin respectively. These bits cannot be reset or cleared by the μP.

SR_b3 is the Receive Data Register full bit and SR_b4 is the Transmit Data Register Empty bit. These bits have been described fully in the TDR and RDR sections.

The 3 LSB bits in the SR are error bits, set when a specific error condition occurs. These bits may only be cleared if the RDR is read and a word is received without an error (the error that occurred previously). SR_b0 is the parity error detect bit. When this bit is set, it indicates that parity is enabled and the level of the parity bit received by the ACIA was incorrect. SR_b1 is the Framing error detect bit. If a word is received that does not have a stop bit where expected, the framing error bit will be set.

SR_b2 is the Overrun error bit. This bit is set if a data word is received without the previous word having been read. The word in the RDR is maintained until it is read, so subsequent words in the RSR, that result in an overrun condition, are lost. Interrupts continue to occur with each data word received in the RSR as normal (see figure 9). When an overrun occurs in echo mode, the TxD channel goes to a mark until the first start bit after the RDR is read by the μP.

Suggested sequence for reading SR after interrupt

1/ *Read Status Register.*
This operation automatically clears SR_b7 and negates the $\overline{IRQ}$ signal. Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2/ *Check SR_b7*
If not set, source was not the ACIA.

3/ *Check SR_b6 and SR_b5*
These must be compared to their previous levels, which must be stored externally by the processor. If they are both a logical low (modem on-line) and they are unchanged then the remaining bits must be checked.

4/ *Check SR_b3*
Is RDR full?

5/ *Check SRb0, SRb1, SRb2*
Only if RDR is set.

6/ *Check SR_b4*
Is TDR empty? Check even if RDR is full when in full duplex operation.

7/ If none of the above occurred, $\overline{CTS}$ must have been negated.

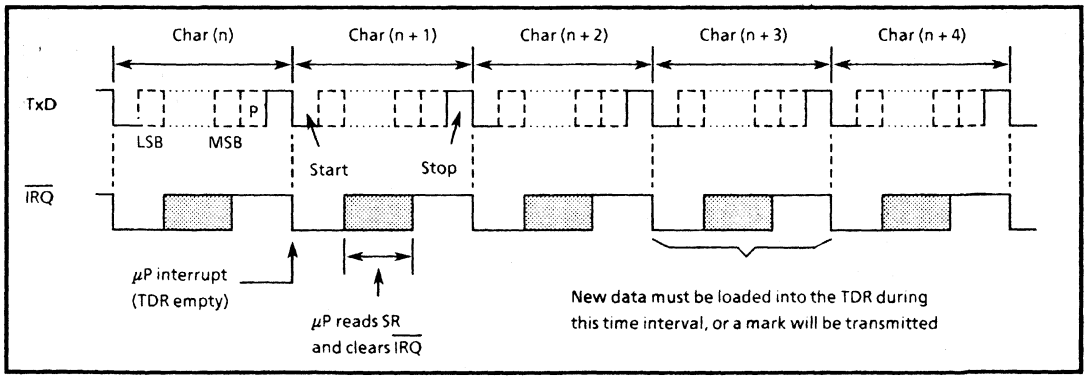


Figure 5. Continuous Data Transmit

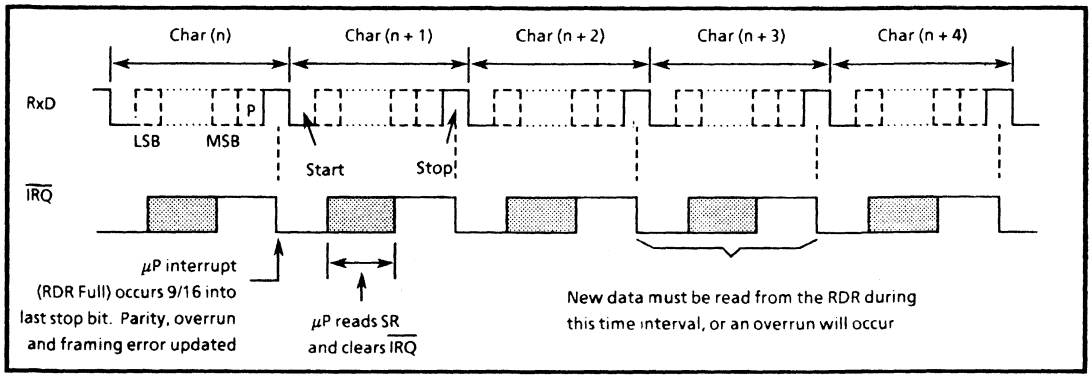


Figure 6. Continuous Data Receive

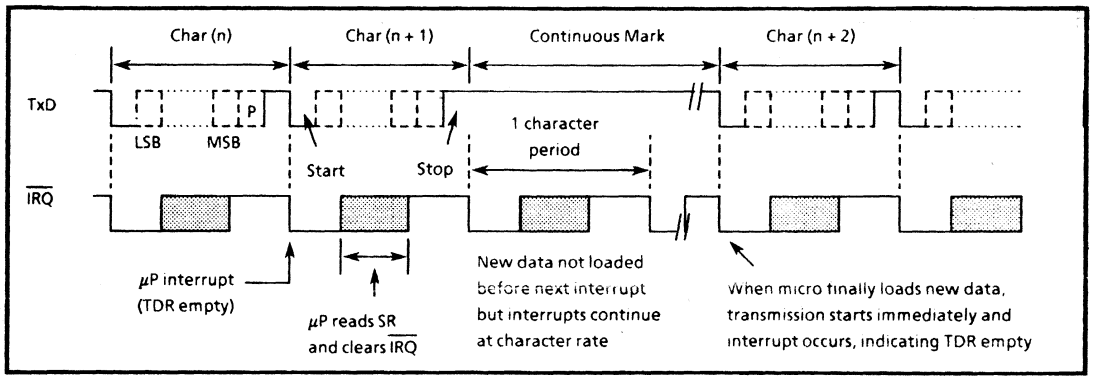


Figure 7. TDR not Loaded by Processor

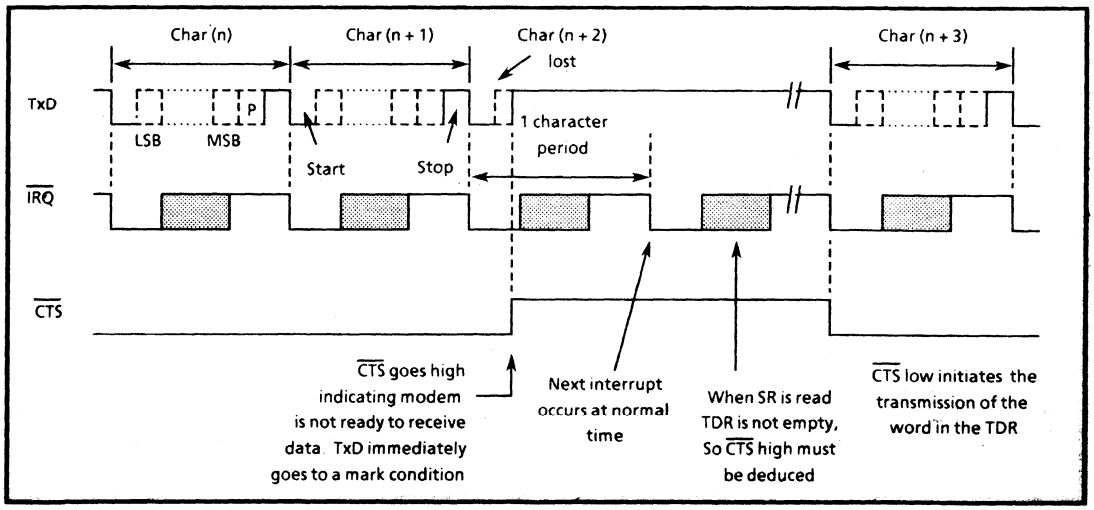


Figure 8. Effect of $\overline{CTS}$ on TxD

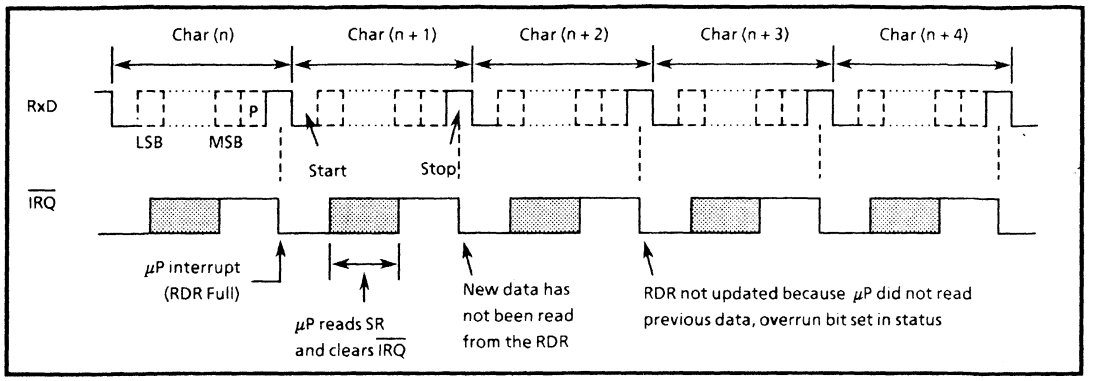


Figure 9. Effect of overrun on receiver

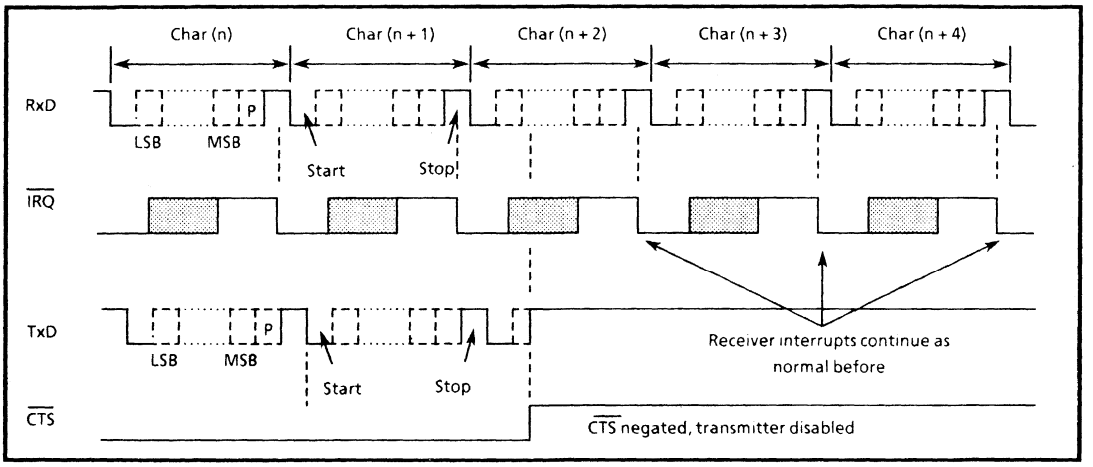


Figure10. Effect of $\overline{CTS}$ on Echo mode operation

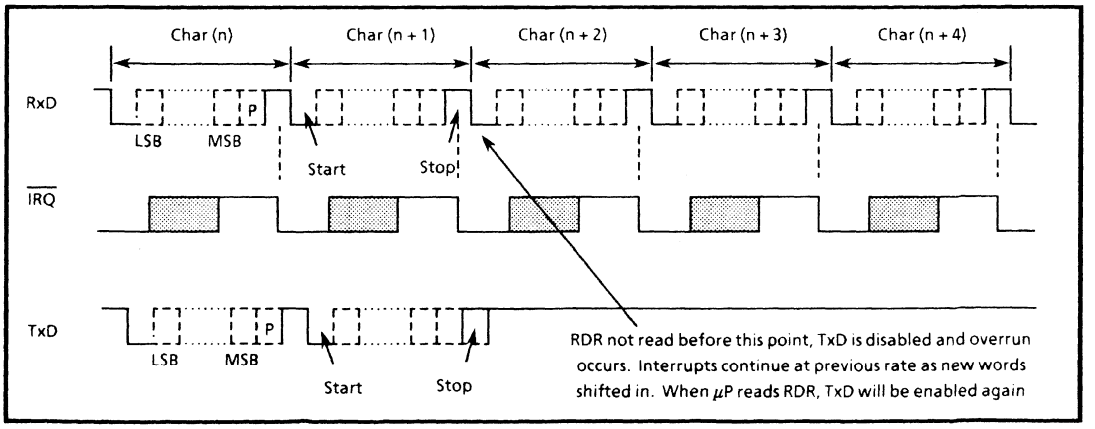


Figure11. Overrun in Echo mode

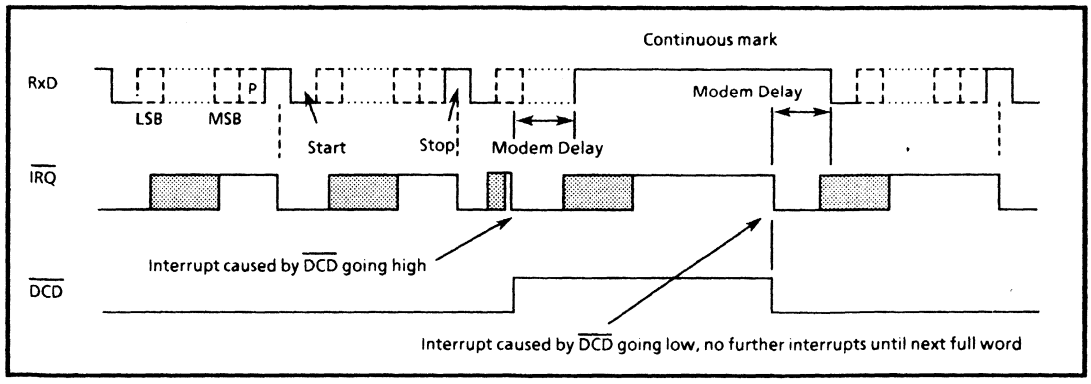


Figure12. Effect of $\overline{DCD}$ on receiver

Notes:

Notes:

ISO-CMOS MD68SC21
Peripheral Interface Adapter

Preliminary Information

9161-002-005 NA ISSUE 2 JANUARY 1985

Features

- Single 3-6 volt power supply.
- Low power ISO-CMOS technology.
- Fully TTL compatible.
- High voltage (10v) open drain drivers.
- Two 8-bit peripheral ports.
- Handshake control for peripheral control.
- Static Operation
- Replacement for NMOS part.

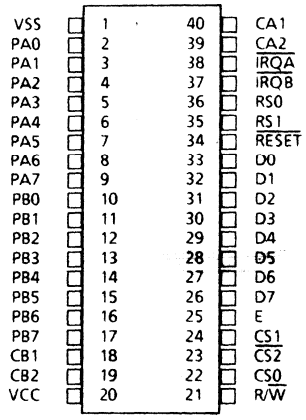
Applications

- Peripheral controller.
- Serial interface.
- Industrial process controller.

Description

The MD68SC21 is a Peripheral Interface Adapter (PIA) fabricated in Mitel's ISO-CMOS technology. Two 8-bit bidirectional ports are available for interfacing, with the direction of each bit being software controlled. The interrupt handshaking to (Write operation port B) and from (Read operation port A) the peripheral can be performed by the device for both ports.

Pin Connections



Ordering Information

MD68SC21AC 40 Pin Ceramic Package
MD68SC21AE 40 Pin Plastic Package

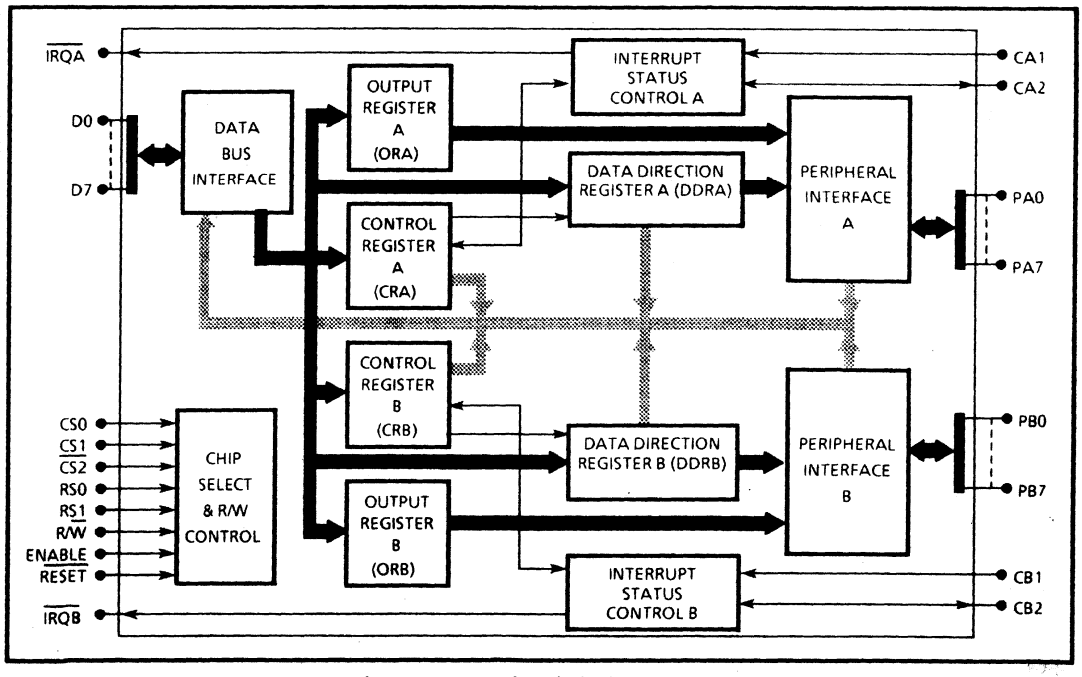


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{CC} - V_{SS}	- 0.3	7.0	V
2	Voltage on any I/O pin	V_I	V_{SS}-0.3	V_{CC} + 0.3	V
3	Current on any I/O pin	I_I		± 10	mA
4	Operating Temperature	T_A	-40	+ 85	°C
5	Storage Temperature	T_S	-65	+ 150	°C
6	Power Dissipation Plastic	P_D		1.0	W
	Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recomended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	I	Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
2	N	Input Voltage	V_I	0.0		V_{CC}	V	
3	P	Output Voltage	V_O	0.0		V_{CC}	V	
4	U	Operating Temperature	T_A	-40	+ 25	+ 85	°C	
5	T S	Operating Frequency	f			2.0	MHZ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

V_{CC} = 5.0V ± 5% V_{SS}/GND = 0V Voltages are refenced to V_{SS}/GND unless otherwise stated figures given for full temperature range

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent Supply Current	I_{CC1}		2		μA	Outputs Unloaded
2		Operating Supply Current	I_{CC}		2		mA/MHz	Outputs Unloaded
3	I	Input High Voltage	V_{IH}	2.0		V_{CC}	V	
4	N	Input Low Voltage	V_{IL}	0.0		0.8	V	
5	P	Input High Current (PA0-7,CA2)	I_{IH}	-200			μA	V_{IH} = 2.4V
6	U T S	Input Low Current (PA0-7,CA2)	I_{IL}			-1.6	mA	V_{IL} = 0.4V
7		Input Low Current (PB0-7,CB2,D0-7, $\overline{IRQA}$, $\overline{IRQB}$)	I_{IZ}			± 10.0	μA	V_{IN} = 0toV_{CC}
		Other Inputs	I_{IZ}			± 2.5	μA	V_{IN} = 0toV_{CC}

†DC Electrical Characteristics are over recommended temperature range & recommended Power Supply voltages

‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

V_{CC} = 5.0V ± 5% V_{SS}/GND = 0V Voltages are refenced to V_{SS}/GND, figures are for full temperature range, unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
8		Input Capacitance (D0-7)	C_{IZ}		10.0		pF	V_{IN} = 0V f = 1.0 MHz
		(Other Inputs)	C_{IN}		5.0		pF	V_{IN} = 0V f = 1.0 MHz
9	OUTPUTS	Output High Voltage (D0-7)	V_{OH}	2.4			V	I_{OH} = -50μA
		(PA0-7, CA2, PB0-7, CB2)	V_{OH}	2.4			V	I_{OH} = -100μA
		(PB0-7)	V_{OH}	4.0			V	I_{OH} = -10μA
10		Output Low Voltage ($\overline{IRQA}$, $\overline{IRQB}$)	V_{OL}			0.4	V	I_{OL} = 3.2 mA
		(D0-7)	V_{OL}			0.4	V	I_{OL} = 1.6 mA
		(PA0-7, CA2, PB0-7, CB2)	V_{OL}			0.4	V	I_{OL} = 3.2 mA
11		Output Drive Current (PA0-7, CA2, PB0-7, CB2)	I_{OH}	1.0	10.0		mA	V_{OH} = 1.5V
12		Output Capacitance ($\overline{IRQA}$, $\overline{IRQB}$)	C_O		5.0		pF	V_0 = 0V f = 1.0 MHz
13		Output Leakage ($\overline{IRQA}$, $\overline{IRQB}$)	I_{OZ}			10.0	μA	V_0 = V_{SS} to V_{CC}

† DC Electrical Characteristics are over recommended temperature range and recommended Power Supply Voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

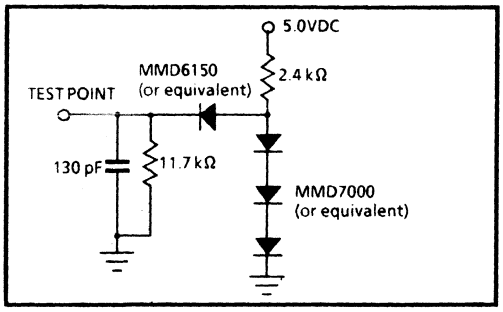


Figure 1. Test load for Data bus

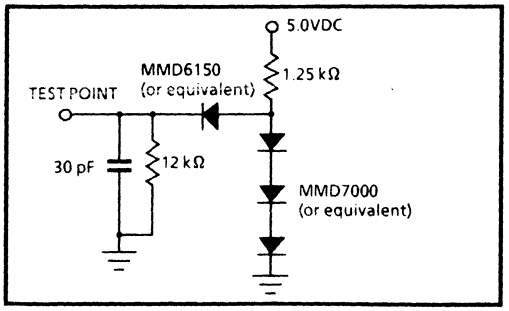


Figure 2. Test load for PA0-7,PB0-7,CA2 & CB2

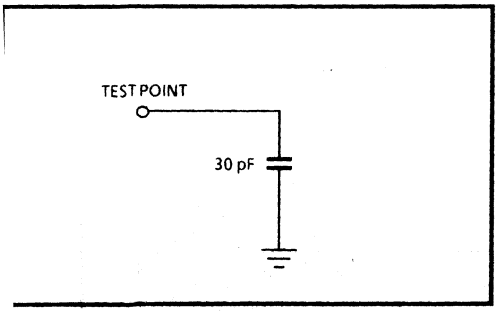


Figure 3. Test load for PA0-7 & CA2 (CMOS Load)

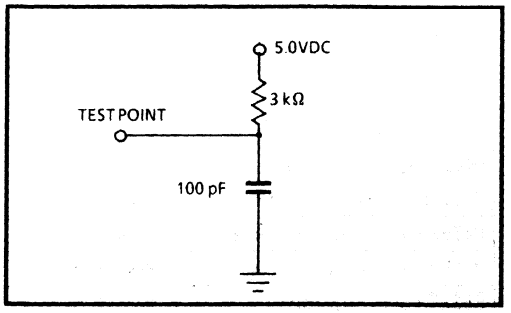


Figure 4. Test load for $\overline{IRQA}$ and $\overline{IRQB}$

AC Electrical Characteristics†

V_{CC} = 5.0V ± 5% V_{SS}/GND = 0V Voltages are referenced to V_{SS}/GND, figures are for full temperature range, unless otherwise stated

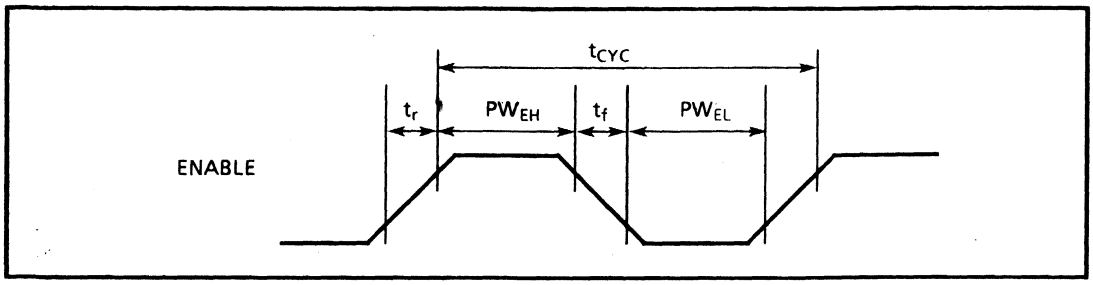
		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	MPU INTERFACE	Enable Cycle Time	t_{CYC}	500			ns	See Timing Diagram 1
2		Enable High Pulse Width	PW_{EH}	220			ns	See Timing Diagram 1
3		Enable Low Pulse Width	PW_{EL}	210			ns	See Timing Diagram 1
4		Enable Rise and Fall Time	t_r & t_f			20	ns	See Timing Diagram 1
5		Address $\overline{CS}$ & R/$\overline{W}$ Set-up Time (Access Set-up Time)	t_{AS}	40			ns	See Timing Diagram 2,3
6		Address $\overline{CS}$ & R/$\overline{W}$ Hold Time (Access Hold Time)	t_{AH}	10			ns	See Timing Diagram 2,3
7		Data Output Delay (Read)	t_{DDR}			150	ns	See Timing Diagram 2
8		Data Output Hold Time (Read)	t_{DHR}	20		100	ns	See Timing Diagram 2
9		Data Input Set-up Time (Write)	t_{DSW}	60			ns	See Timing Diagram 3
10		Data Input Hold Time (Write)	t_{DHW}	10			ns	See Timing Diagram 3
11	INPUTS	Data Set-up Time (Peripheral Read)	t_{PDS}	100			ns	See Timing Diagram 5
12		Data Hold Time (Peripheral Read)	t_{PDH}	0			ns	See Timing Diagram 5
13		Delay Enable to CA2 Active State	t_{CA2}			500	ns	See Timing Diagram 4,5
14		CA2 Reset (Reset by Enable: Mode 1)	t_{RS1}			500	ns	See Timing Diagram 4
15		CA1 & CA2 Rise and Fall Times	t_r & t_f			1.0	μs	See Timing Diagram 4,5
16		CA2 Reset (Reset by CA1: Mode 2)	t_{RS2}			1.0	μs	See Timing Diagram 5
17		Enable to Valid Data Delay (Peripheral Write) TTL	t_{PDW}			500	ns	See Timing Diagram 6
		CMOS(PA0-7, CA2 only)	t_{CMOS}			1.0	μs	See Timing Diagram 6
18		Delay Enable to CB2 Active State	t_{CB2}			500	ns	See Timing Diagram 6
19		CB2 Reset (Reset by Enable: Mode 1)	t_{RS1}			500	ns	See Timing Diagram 6
20		Valid Data to Delay CB2	t_{DC}	20			ns	See Timing Diagram 6
21		CA2/CB2 Control Pulse Width	PW_{CT}	250			ns	See Timing Diagram 4,6
22		CB1 & CB2 Rise and Fall Times	t_r & t_f			1.0	μs	See Timing Diagram 6,7
23		CB2 Reset (Reset by CB1: Mode 2)	t_{RS2}			1.0	μs	See Timing Diagram 7
24		Enable to INTERRUPT Delay	t_{IR}			850	ns	See Timing Diagram 8
25		INTERRUPT Response Time	t_{RS3}			1.0	μs	See Timing Diagram 8
26		INTERRUPT Input Pulse Width	PW_I	500			ns	See Timing Diagram 8
27		$\overline{RESET}$ Low Duration	t_{RL}	0.5			μs	See Timing Diagram 9
28		$\overline{RESET}$ High to Chip Select	t_{RS}	1.0			μs	See Timing Diagram 9

† Timing is over recommended temperature & Power Supply voltages

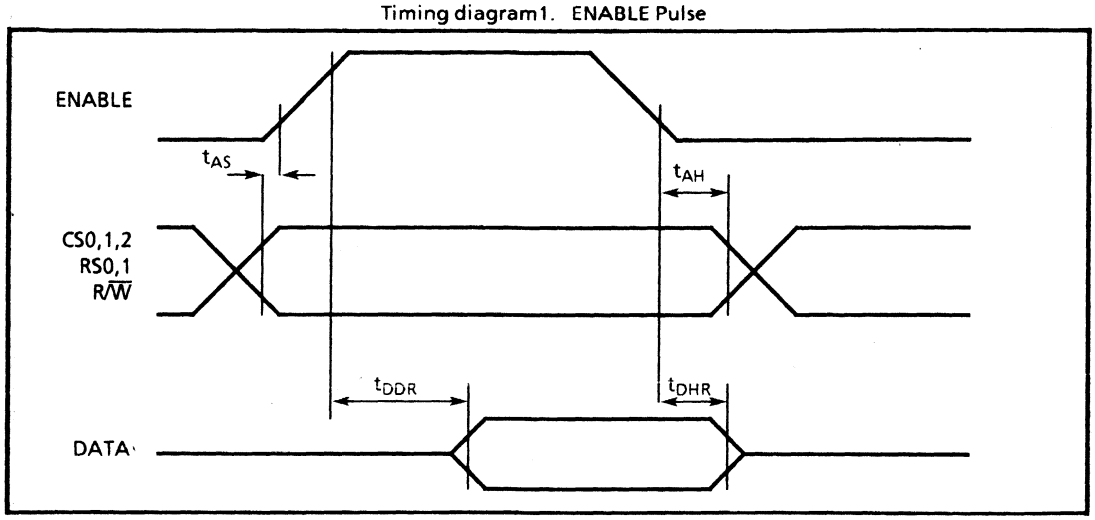
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Timing Diagrams

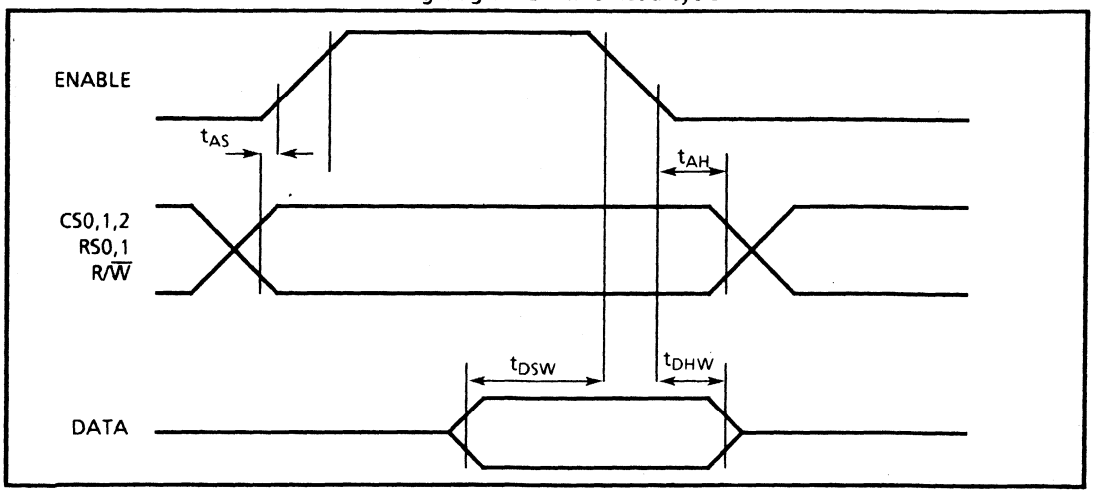
The points from which these timing values are measured are + 0.8V and 2.0V



Timing diagram1. ENABLE Pulse



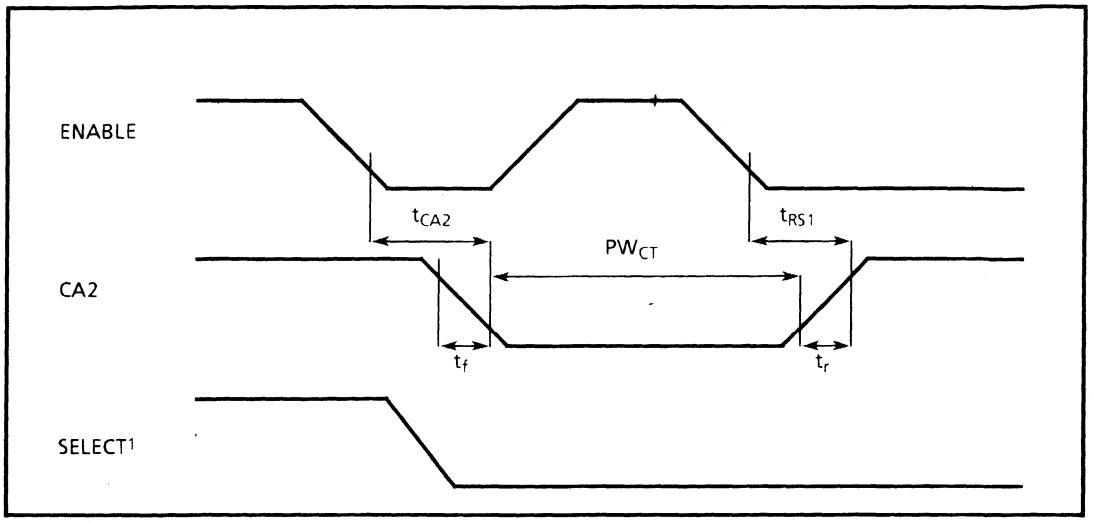
Timing diagram 2. MPU Read Cycle



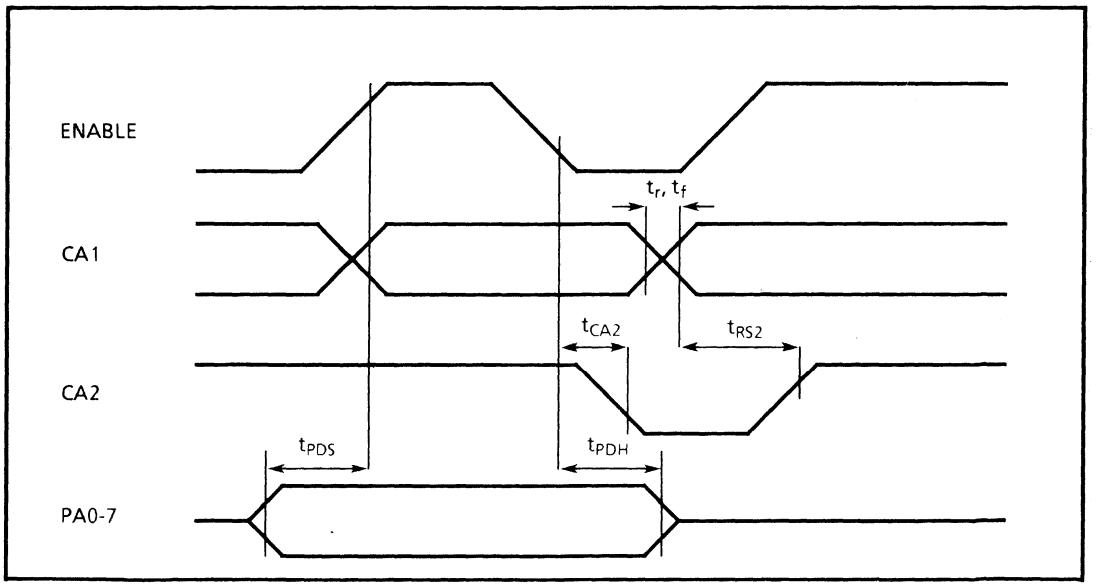
Timing diagram 3. MPU Write Cycle

Timing Diagrams

The points from which these timing values are measured are + 0.8V and 2.0V



Timing diagram 4. Read from Peripheral with ENABLE Reset
(MODE 1: CRA b_5 = CRA b_3 = 1 CRAb_4 = 0)



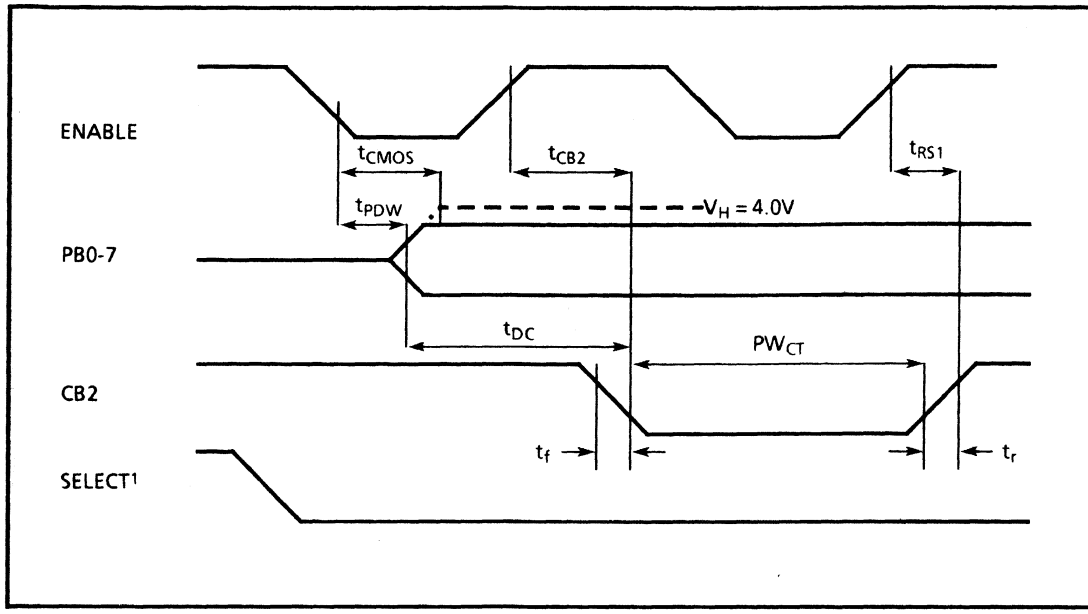
Timing diagram 5. Read from Peripheral with CA1 Reset
(MODE 2: CRA b_5 = 1 CRA b_3 = CRAb_4 = 0)

Notes.

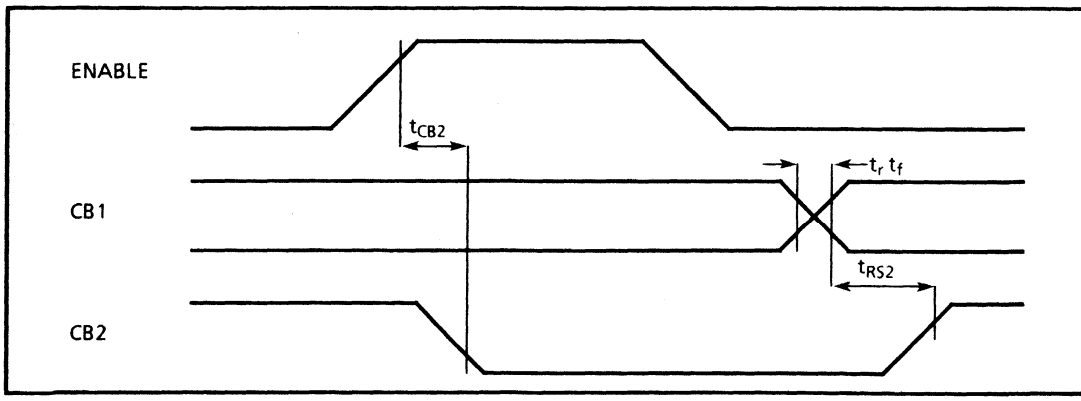
1 The MD68SC21 is DESELECTED during the previous ENABLE cycle
(SELECT = CS0 • CS1 • $\overline{CS2}$)

Timing Diagrams

The points from which these timing values are measured are +0.8V and 2.0V



Timing diagram 6. Write from Peripheral with ENABLE Reset
(MODE 1 : CRB b_5 = CRB b_3 = 1 CRB b_4 = 0)



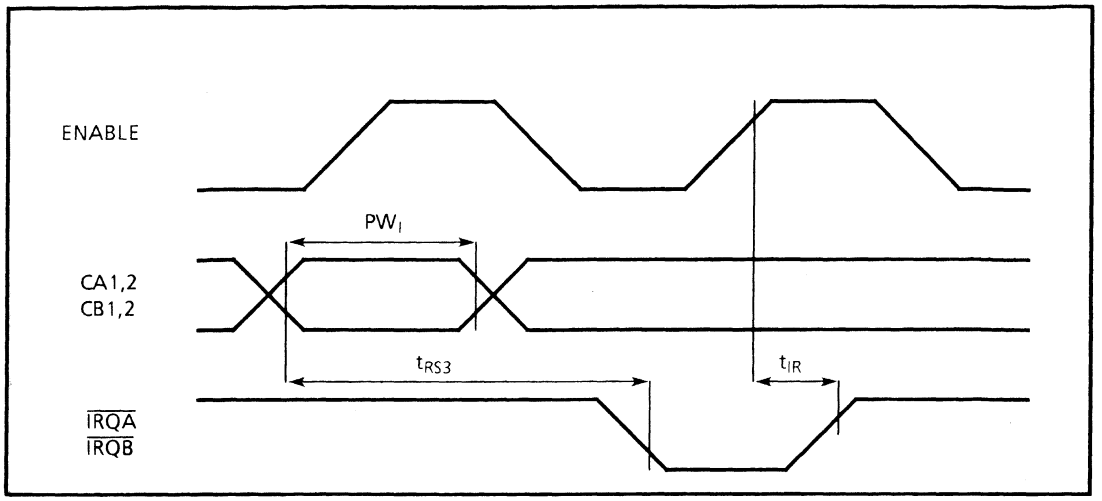
Timing diagram 7. Write from Peripheral with CB1 Reset
(MODE 1 : CRB b_5 = 1, CRB b_3 = CRB b_4 = 0)

Notes.

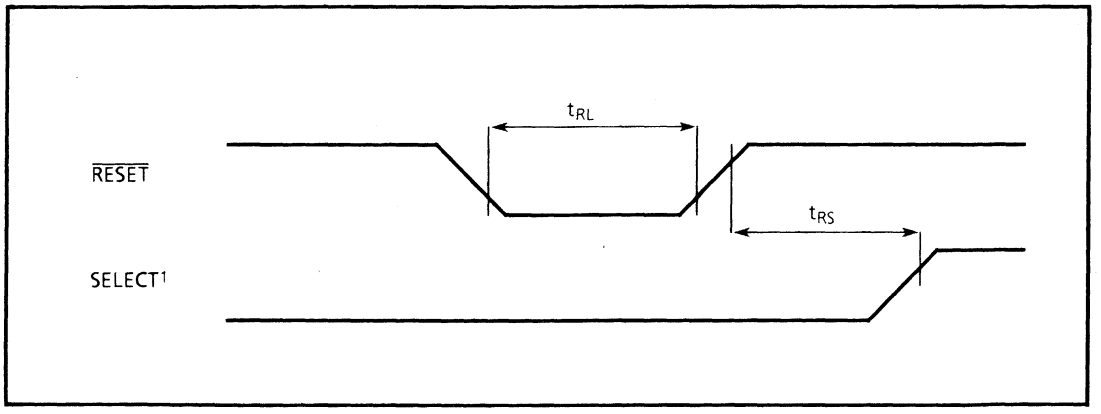
1 The MD68SC21 is DESELECTED during the previous ENABLE cycle
(SELECT = CS0 • CS1 • $\overline{CS2}$)

Timing Diagrams

The points from which these timing values are measured are + 0.8V and 2.0V



Timing diagram 8. INTERRUPT TIMING



Timing diagram 9. RESET TIMING

Notes

1 The MD68SC21 is DESELECTED during the previous ENABLE cycle (SELECT = CS0 • CS1 • $\overline{CS2}$)

TABLE 1.
Pin Description

Pin	Name	Description
1	V_{SS}/GND	**Negative power supply** and logic ground.
2-9	PA0-PA7	**Port A Bidirectional Data Interface.** TTL compatibility.
10-17	PB0-PB7	**Port B Bidirectional Data Interface.** TTL compatibility.
18	CB1	**Port B Control 1.** This input signal can be used in port B data transfer control.
19	CB2	**Port B Control 2.** This signal can be used in port B data transfer control.
20	V_{CC}	**Positive power supply.**
21	R/$\overline{W}$	**Read / Write control.** A logic '1' will allow the MPU to read data from the PIA and a logic '0' to write data to the PIA.
22-24	CS0, $\overline{CS2}$ & CS1	**Chip select input** . The device is selected for microprocessor data transfers when these inputs are active (CS1 = CS0 = '1' and $\overline{CS2}$ = '0').
25	ENABLE	**System clock input.** Timing of all MPU signals are referenced to this input signal.
26-33	D7-0	**Bidirectional 8-bit data bus.** Three-state interface between the MPU and PIA.
34	$\overline{RESET}$	**Hardware reset input.** A hardware reset is initiated when a logic '0' is applied. All internal registers are cleared to a logic '0'.
35 & 36	RS1&RS0	**Register select inputs.** The address for the corresponding registers is applied to these inputs when a MPU data transfer is performed.
37 & 38	$\overline{IRQB}$, $\overline{IRQA}$	**Interrupt request outputs.** These are active LOW,open drain outputs which may be wire OR-ed.
39	CA2	**Port A Control 1.** This signal can be used in port A data transfer control.
40	CA1	**Port A Control 2.** This input signal can be used in port A data transfer control.

TABLE 2.
Register Address Decoding

Register Select		Control Register bit		Internal Register Selected	
RS1	RS0	CRA b_2	CRB b_2	MPU Read Operation	MPU Write Operation
0	0	1	X	Port A peripheral Register	Output Register A (ORA)
0	0	0	X	Data Direction Register A (DDRA)	Data Direction Register A (DDRA)
0	1	X	X	Control Register A (CRA)	Control Register A (CRA)
1	0	X	1	Port B peripheral Register	Output Register B (ORB)
1	0	X	0	Data Direction Register B (DDRB)	Data Direction Register B (DDRB)
1	1	X	X	Control Register B (CRB)	Control Register B (CRB)

Functional Description

The MD68SC21 Peripheral Interface Adapter contains two 8-bit bidirectional ports to provide an interface between an 8-bit microprocessor bus and a peripheral, e.g. a keyboard or printer. The device contains two ports for parallel communication with each port consisting of 8 data lines and two control lines. The function of these two ports and the data which is transferred through them is controlled by six internal registers. These registers are addressed by two external inputs, RS0 and RS1, and one internal input, bit two of the respective port control register, as outlined in Table 2.

Each port can be configured as all inputs, all outputs or a mixture of both. The direction of data flow through each of the I/O lines is controlled by the Data Direction Register (DDR). Each of the bits in the DDR corresponds to an I/O line e.g. DDRA b_7 corresponds to PAb_7. If the DDR bit is a logic '1' the I/O line is an output. Conversely, if the DDR bit is a logic '0', the I/O line is an input. The data to be output from the MPU is first written into the Output Register and is then output from the port. When reading the port in the case where the port is configured as an output, the two ports behave differently. In the case of port B, the data contained in the output register is returned. However, for the situation in which port A is read when in an output configuration, the actual value seen at the pin is returned (Note: this may not be the same value as contained in the output register). See figure 5 for the logical representation of the port interface.

The MD68SC21 also provides interrupt and peripheral handshaking facilities. When a port B is used as an output, CB2 can be used as a "Data

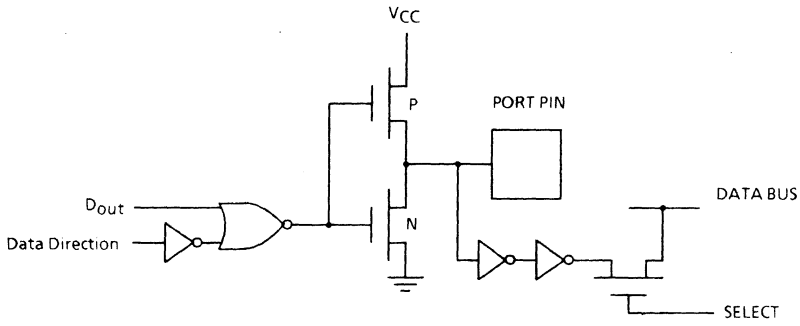


Figure 5a. Port A Equivalent Circuit.

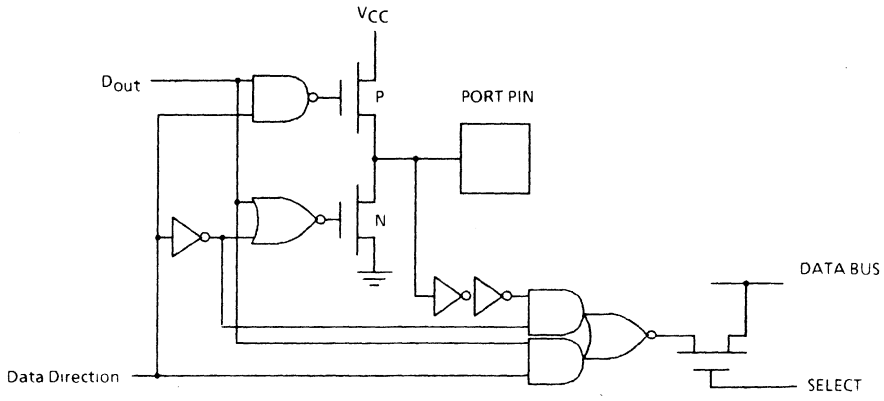


Figure 5b. Port B Equivalent circuit.

Figure 5. Port A and Port B Equivalent Circuits.

Valid" output and CB1 used as a "Data Accepted" input from the peripheral. Similarily, when an input configuration is used with port A, CA1 receives the "Data Valid" signal from the peripheral and returns a "Data Accepted" signal via CA2 . In both cases the CA1 (or CB1) signal can be used to generate an interrupt on the $\overline{IRQA}$ ($\overline{IRQB}$) line. The function of these lines CA1, CA2 (CB1, CB2) is controlled by the contents of the Control Register.

The Control Register

Below is a detailed explanation of the functions of each bit of the control registers. It should be that the functions of the two Control Registers, CRA & CRB, are not identical.

The hardware reset ($\overline{RESET}$) will clear all the internal register bits to logic 0. This results in the clearing and disabling of interrupts and causes all I/O lines to be inputs.

A power down mode may be achieved by disabling the clock input. All the internal register contents and conditions are conserved. Further power saving may be made by subsequently reducing VCC to + 3V. This is particularly useful for battery powered applications.

TABLE 3.
Control Register Functions

Control Register bit	Other Conditions	Resulting Function
b_7		**Interrupt Flag IRQA(B)1** Set to logic '1' on active transition of CA1(CB1) Cleared to logic '0' by MPU read of corresponding Output Register or Hardware reset.
b_6	$b_5 = 0$	**IRQA(B)2 Flag** is set by an active transition of CA2(CB2). Cleared by MPU read of corresponding Port or Hardware reset.
	$b_5 = 1$	**IRQA(B)2 Flag** not affected by CA2(CB2) transitions
$b_5 = 1$	$b_4 = 0, b_3 = 0$	**CA2** is cleared by MPU read of Port A and set by next active CA1 transition (see timing diagram5). **CB2** is cleared by MPU write to Port B and set by next CB1 active transition (see timing diagram 7).
	$b_4 = 0, b_3 = 1$	**CA2** is cleared by MPU read of Port A and set by next active ENABLE transition (see timing diagram4). **CB2** is cleared by MPU write to Port B and set by next ENABLE active transition (see timing diagram 6).
	$b_4 = 1$	CRA(B)b_3 is output to CA2(CB2) as soon as it is written to the control register by the MPU.
$b_5 = 0$	$b_4 = 0, b_3 = 1$	**IRQA(B)** set by high to low transition of CA2(CB2). **IRQA(B)2 Flag** set
	$b_4 = 1, b_3 = 1$	**IRQA(B)** set by low to high transition of CA2(CB2). **IRQA(B)2 Flag** set
	$b_3 = 0$	**IRQA(B)** Disabled
	$b_3 = 1$	**IRQA(B)** Enabled
b_2		LSB of register address. See register address table
$b_1 = 0$		**IRQA(B)1 (CRA(B) b_7)** is set by high to low transition of CA1(CB1)
$b_1 = 1$		**IRQA(B)1 (CRA(B) b_7)** is set by low to high transition of CA1(CB1)
$b_0 = 0$		Disables IRQA(IRQB) interrupt by CA1(CB1) transition
$b_0 = 1$		Enables IRQA(IRQB) interrupt by CA1(CB1) transition

Notes

ISO-CMOS MD68SC40
Programmable Timer Module
Preliminary Information

9161-002-017-NA ISSUE 3 JUNE 1986

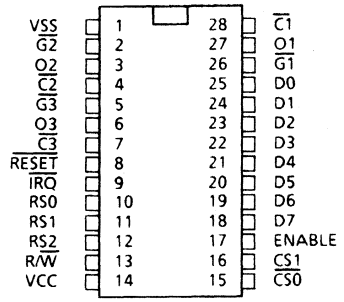
Features

- Single 3-6 volt power supply.
- Low power ISO-CMOS technology.
- Fully TTL compatible.
- Software counter control.
- Hardware reset (RESET).
- Asynchronous clock and gating inputs.

Applications

- Software controlled waveform generation.
- Frequency and pulse width comparison.
- Pulse width modulation.
- System timing waveform synthesis.
- Event counting.
- Time interval measurements.

Pin Connections



Ordering Information

MD68SC40AE Plastic Dual-in-Line Package
MD68SC40AC Ceramic Dual-in-Line Package

Description

The MD68SC40 is a programmable Timer Module consisting of three 16-bit counter/timer modules. The MD68SC40 is fabricated in MITEL ISO-CMOS technology to give low power dissipation. The device interfaces with an 8-bit microprocessor data-bus and uses three address lines for register selection and two chip select lines ($\overline{CS0}$, active low and CS1, active high). The timers can be individually configured, under software control, to provide a variety of timing and waveform generation functions.

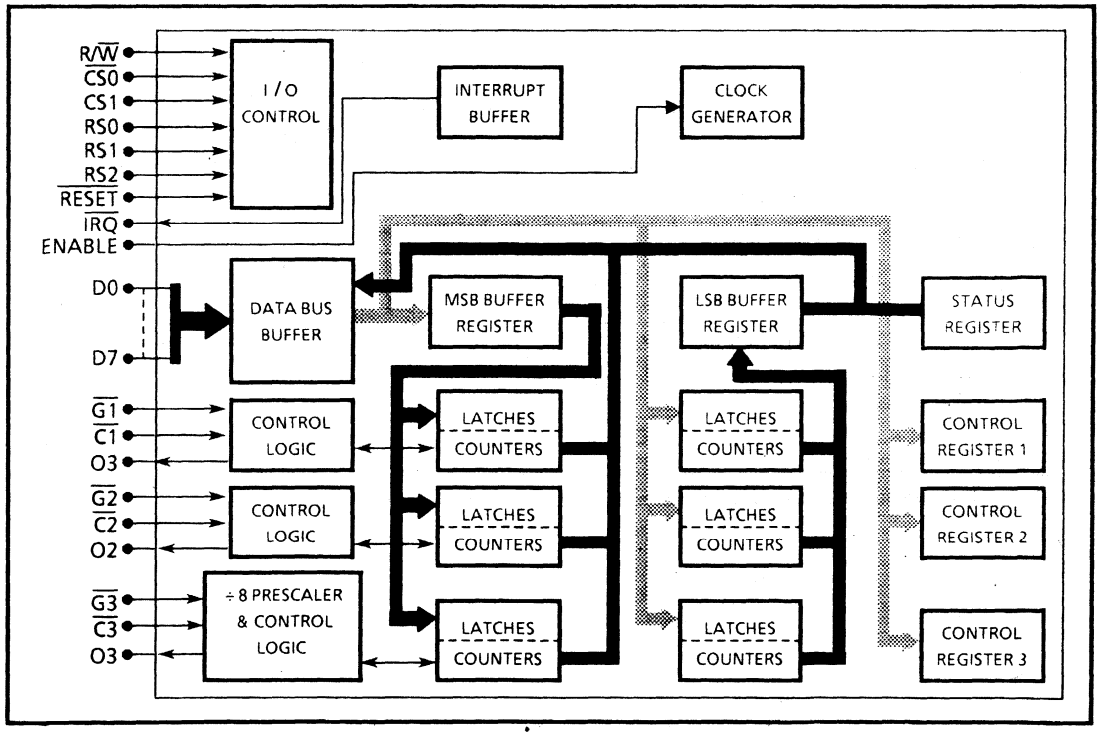


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{CC} - V_{SS}	- 0.3	7.0	V
2	Voltage on any I/O pin	V_I	V_{SS}-0.3	V_{CC} + 0.3	V
3	Current on any I/O pin	I_I		± 10	mA
4	Operating Temperature	T_A	-40	+ 85	°C
5	Storage Temperature	T_S	-65	+ 150	°C
6	Power Dissipation Plastic	P_D		1.0	W
	Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply Voltage	V_{CC}	3.0	5.0	6.0	V	
2		Input Voltage	V_I	0		V_{CC}	V	
3		Output Voltage	V_O	0		V_{CC}	V	
4		Operating Temperature	T_A	-40	+ 25	+ 85	°C	
5		Operating Frequency	f	0		2.0	MHz	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent Supply Current	I_{CC1}		2		µA	Outputs Open
2		Operating Supply Current	I_{CC}		4		mA/MHz	Outputs Open
3	INPUTS	Input High Voltage		2.0		V_{CC}	V	
4		Input Low Voltage		-0.3		0.8	V	
5		Input Leakage Current (D0-7)	I_{IZ}			10	µA	V_{IN} = 0 to V_{CC}
		Other Inputs	I_{IZ}			2.5	µA	V_{IN} = 0 to V_{CC}
6		Input Capacitance (D0-7)	C_{IN}		5.0		pF	T_A = 25°C f = 1.0 MHz
		Other Inputs	C_{IN}		10.0		pF	T_A = 25°C f = 1.0 MHz
7	OUTPUTS	Output High Voltage (D0-7)	V_{OH}	2.4			V	I_{OH} = 205 µA
		(Other Inputs)	V_{OH}	2.4			V	I_{OH} = 200 µA
8		Output Low Voltage (D0-7)	V_{OL}			0.4	V	I_{OH} = 1.6 mA
		(Other Inputs)	V_{OL}			0.4	V	I_{OH} = 3.2 mA
9		Output Leakage Current IRQ (OFF state)	I_{OZ}		10		µA	V_{OH} = 2.4 V
10		Output Capacitance	C_O		5.0		pF	T_A = 25°C F = 1.0 MHz

†DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

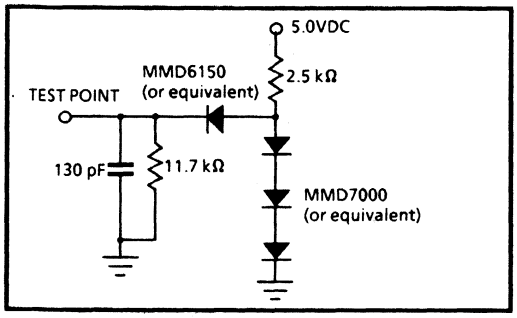


Figure 2. Test load for D_0 - D_7

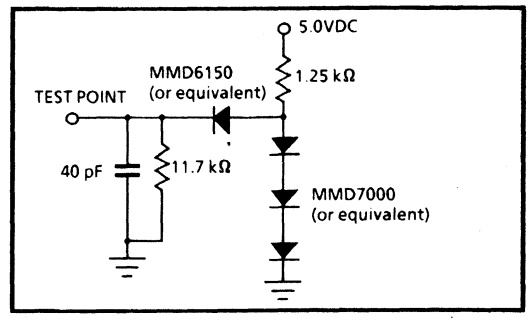


Figure 3. Test load for O1, O2, & O3 (TTL Load)

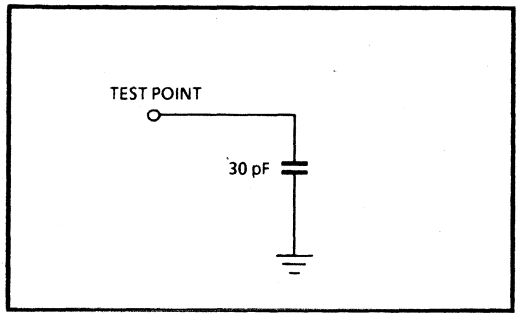


Figure 4. Test load for O1, O2, & O3 (CMOS Load)

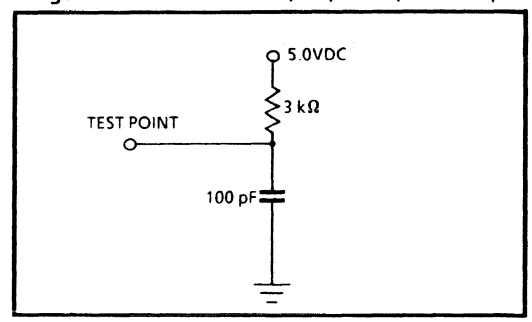


Figure 5. Test load for $\overline{IRQ}$

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	MPU INTERFACE	Enable Cycle Time	t_{CYC}	500	320		ns	See Timing Diagram 1
2		Enable Low Pulse Width	PW_{EL}	210	135		ns	See Timing Diagram 1
3		Enable High Pulse Width	PW_{EH}	220	145		ns	See Timing Diagram 1
4		Enable Rise and Fall Time	t_r, t_f		16	25	ns	See Timing Diagram 1
5		Address CE & R/$\overline{W}$ Set-up Time (Access Set-Up)	t_{AS}	40	25		ns	See Timing Diagrams
6		Address CE & R/$\overline{W}$ Hold Time (Access Hold)	t_{AH}	10	7		ns	See Timing Diagrams
7		Data Output Delay (Read)	t_{DDR}		95	150	ns	See Timing Diagram 2
8		Data Output Hold Time (Read)	t_{DHR}	20		100	ns	See Timing Diagram 2
9		Data Input Set-Up Time (Write)	t_{DSW}		40		ns	See Timing Diagram 3
10		Data Input Hold Time (Write)	t_{DHW}	10	7		ns	See Timing Diagram 3
11	PERIPHERAL INTERFACE	Control Input Signal Set-up	t_{SU}	70	45		ns	See Timing Diagram 4
12		Control Input Signal Hold	t_{HD}	70	45		ns	See Timing Diagram 4
13		Control Input Signal Rise & Fall	t_r, t_f		350	500	ns	See Timing Diagram 4
14		Control Input Signal Pulse						
		Pulse width High	PW_H	t_{PW}*				See Timing Diagram 4
		Pulse width Low	PW_L	t_{PW}*				See Timing Diagram 4
15		Counter Output Delay						
		TTL	t_{CO}		220	340	ns	See Timing Diagram 5
		MOS	t_{CM}		220	340	ns	
		CMOS	t_{CMOS}		0.6	1.0	µs	
16		Interrupt Reset Time	t_{IR}		450	700	ns	See Timing Diagram 6
17		Prescaler Input Sync. Time (C3)	t_{SYNC}	175			ns	See Timing Diagram 7
18		Prescaler Input Pulse Width	PW_H	60			ns	See Timing Diagram 7
			PW_L	60			ns	See Timing Diagram 7

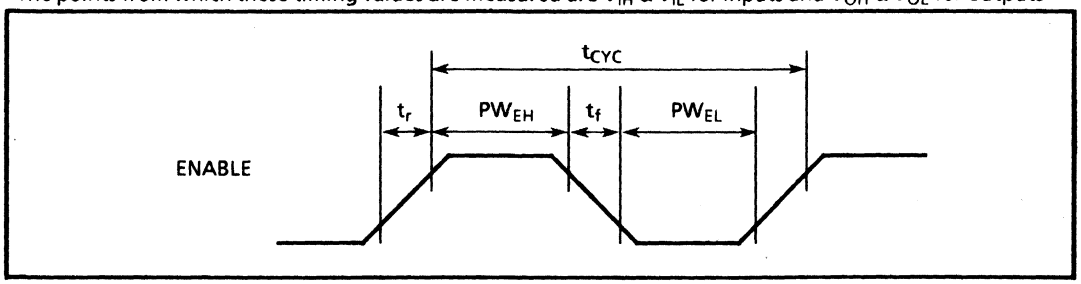
† Timing is over recommended temperature range & V_{CC} = 5V ±5%.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

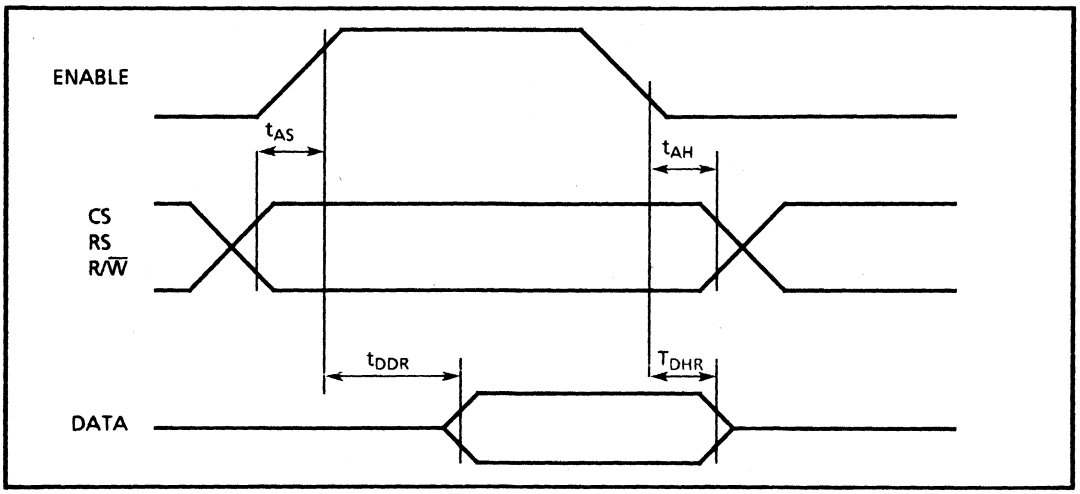
* $t_{PW} = t_{CYC} + t_{SU} + t_{HD}$

Timing Diagrams

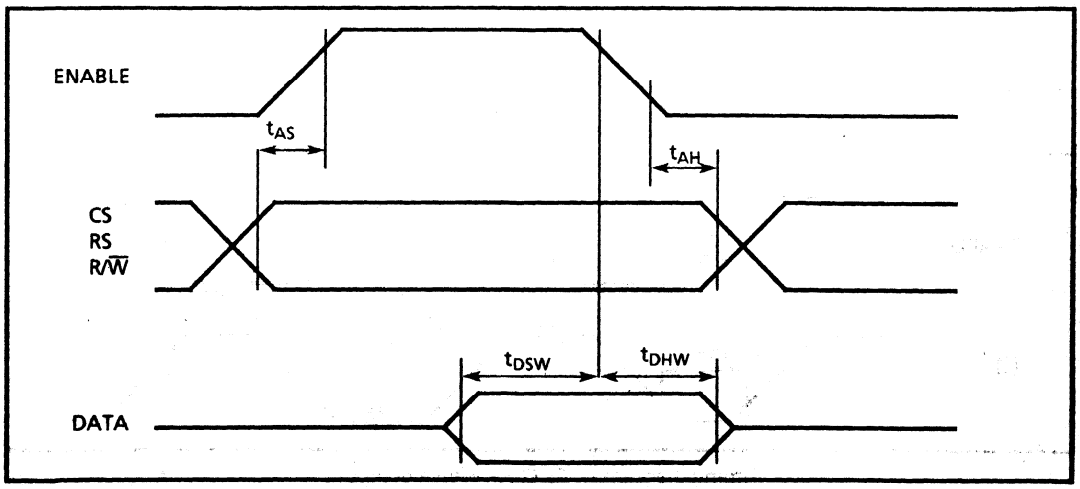
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs



Timing diagram 1. ENABLE Pulse



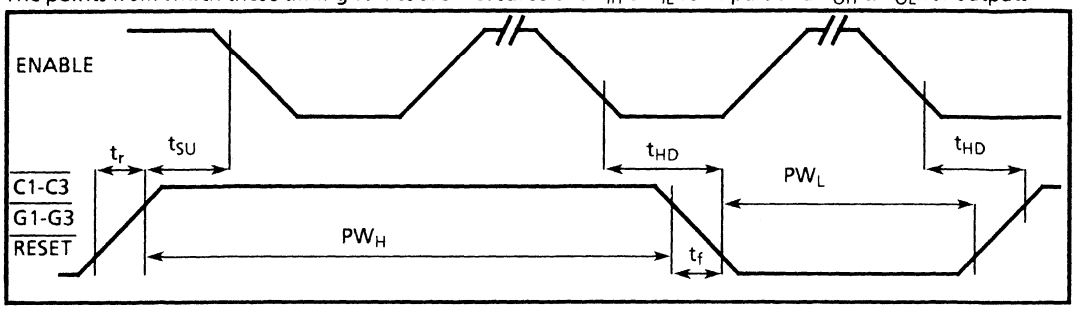
Timing diagram 2. MPU Read Cycle



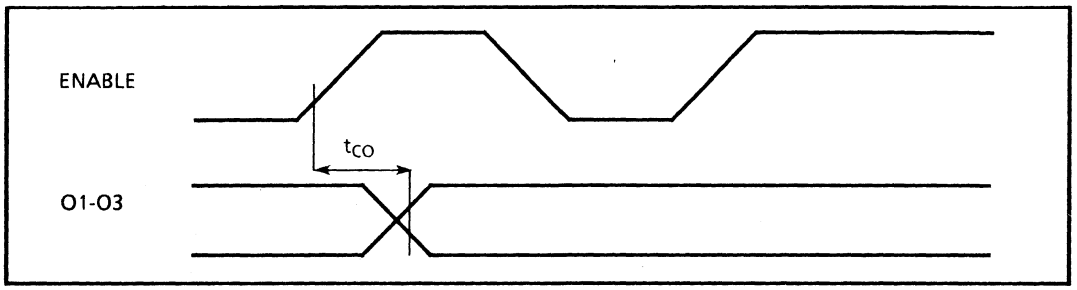
Timing diagram 3. MPU Write Cycle

Timing Diagrams

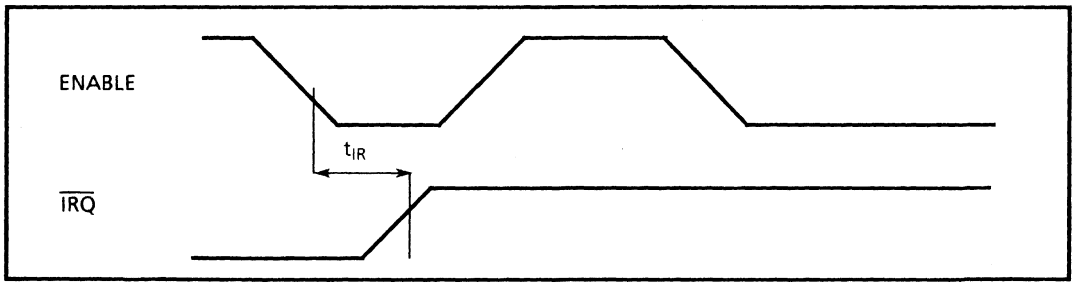
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs



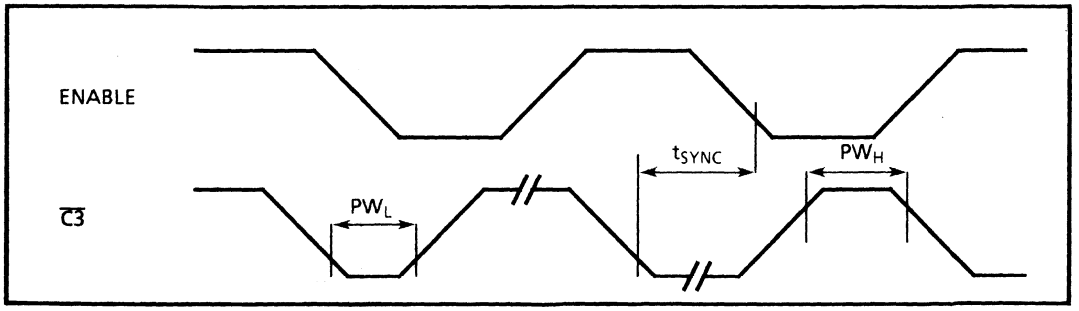
Timing diagram 4. Input Pulse timing



Timing diagram 5. Counter Output Delay



Timing diagram 6. Interrupt Reset timing.



Timing diagram 7. C3 Clock Prescaler Input.

Table 1.
Pin Description

Pin	Name	Description
1	V_{CC}	Positive Supply input
2	$\overline{G2}$	Counter #2 gate input. TTL level.
3	O2	Counter #2 output.
4	$\overline{C2}$	Counter #2 clock input. TTL level.
5	$\overline{G3}$	Counter #3 gate input. TTL level.
6	O3	Counter #3 output.
7	$\overline{C3}$	Counter #3 clock input. TTL level.
8	$\overline{RESET}$	External reset input. Active low.
9	$\overline{IRQ}$	Interrupt request. Open drain output to MPU.
10-12	RS0-RS2	Register select inputs. See Register Address Decoding (Table 2.).
13	R/$\overline{W}$	Read/$\overline{Write}$ input. Control of data direction between the 68SC40 and the MPU.
14	V_{SS}/GND	Negative Supply input.
15,16	$\overline{CS0}$,CS1	Chip select inputs. TTL level. $\overline{CS0}$ = 0 and CS1 = 1 to select chip for data transfer.
17	ENABLE	System clock input
18-25	D0-D7	Data bus interface to MPU.
26	$\overline{G1}$	Counter #1 gate input. TTL level.
27	O1	Counter #1 output.
28	$\overline{C1}$	Counter #1 clock input. TTL level.

Table 2.
Register Address Decoding

Register Select Inputs			Internal Register Selected	
RS2	RS1	RS0	MPU Write Operation	MPU Read Operation
0	0	0	**$CR2b_2 = 0$** Control Register Timer #3	No Operation
			$CR2b_2 = 1$ Control Register Timer #1	No Operation
0	0	1	Control Register Timer #2	Status Register
0	1	0	MSB of Timer Latch Buffer	Timer #1 Latch
0	1	1	Timer #1 Latch (LSB & MSB)[1]	LSB of Timer #1 Latch Buffer[2]
1	0	0	MSB of Timer Latch Buffer	Timer #2 Latch
1	0	1	Timer #2 Latch (LSB & MSB)[1]	LSB of Timer #2 Latch Buffer[2]
1	1	0	MSB of Timer Latch Buffer	Timer #3 Latch
1	1	1	Timer #3 Latch (LSB & MSB)[1]	LSB of Timer #3 Latch Buffer[2]

Footnote. 1. The Data for the LSB is written from the microprocessor into the LSB latch of the respective counter/timer. Simultaneously, the data in the MSB Buffer is written into the MSB latch of the respective counter/timer

2. The Data for the MSB is read by the microprocessor from the MSB latch of the respective counter/timer. Simultaneously, the data in the LSB latch of the respective counter/timer is written into the LSB Buffer to be read later by the microprocessor

Functional Description

The MD68SC40 contains three 16-bit programmable timers. Each timer can be controlled by an 8-bit word contained in the respective control register. The internal 8-bit registers can be selected for read/write operations using the RS0, RS1 and RS2 inputs (table 2.). The MSB and LSB buffer registers are used when writing to, or reading from, the counter latches so that an 8-bit bus can be used to access the 16-bit latches. When writing to a counter latch the contents of the databus are loaded into the selected LSB latch of the counter. The contents of the MSB buffer register are automatically loaded into the MSB latch of the same counter. When a counter latch read operation is performed the MSB latch data is presented to the databus and the LSB latch data stored in the LSB buffer register to be accessed later.

The Control Register holds the 8-bit control word. This is a write only register so the contents cannot be examined externally. The least significant bit of the control words ($CRXb_0$) has an individual function, whereas the remaining seven bits select common functions for each counter. $CR2b_0$ (Control Register 2 Bit 0) acts as a supplmentary address bit for selection of Control Register 1 and 3, $CR1b_0$ is a software reset and $CR3b_0$ enables or disables the ÷ 8 prescaler. The remaining control bits are used as follows: $CRXb_1$ clock source, $CRXb_2$ counting mode, $CRXb_{3-5}$ counter mode, $CRXb_6$ timer interrupt enable and $CRXb_7$ counter output enable.

If $CRXb_1$ is set to 0 then an external clock input is used by the timer: This input is synchronized to the enable (system clock) and requires three pulses to achieve synchronization. The gating input to the counters can be used to stop and start the counter.

The MD68SC40 has an internal read only status register. This contains the status of the individual counter interrupts and a composite interrupt which is set if any of the counter interrupts are set.

The external RESET input resets all the internal registers to FF_{16} (hex) and disables the counter outputs.

The Control Register

A detailed explanation of the functions of each bit of the control registers is given in Table 3.

Table 3.
Control Register bit Functions

Control Register bit CRX[1]	Function	Description	
		Control Register bit = 0	Control Register bit = 1
$CRXb_7$	Counter/Timer Output Control	Output masked	Output enabled
$CRXb_6$	Counter/Timer Interrupt Enable	Interrupt output to processor masked	Interrupt output to processor enabled
$CRXb_5$, $CRXb_4$, $CRXb_3$	Counter/Timer Mode Control	See Table 4	See Table 4
$CRXb_2$	Counting Mode Control	16 bit count (normal mode)	8 bit count (dual mode)
$CRXb_1$	Counter/Timer Clock Source	External clock source from CX input	Internal clock source from ENABLE clock
$CR1b_0$	Software Reset bit	Normal operation	Timers held in reset state
$CR2b_0$	Partial Register Address bit	CR3 Selected	CR1 Selected
$CRXb_3$	Counter/Timer 3 Prescaler Control	Clock is not pre-scaled	Clock frequency divided by 8

footnote 1. X = 1, 2, or 3

Counter Control

Table 4.
Waveform generation modes

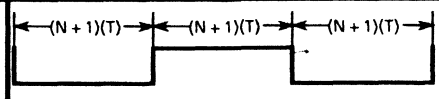
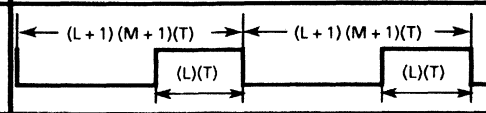
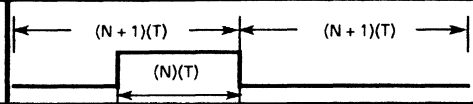
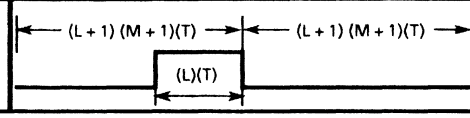
Control Register bit								Counter Intialisation	Counter Mode	Counter Output Waveform
7	6	5	4	3	2	1	0			
1	X	0	0	0	0	X	X	$\overline{G}\downarrow$ + Write + Reset	Continuous 16 bit	
1	X	0	1	0	0	X	X	$\overline{G}\downarrow$ + Reset		
1	X	0	0	0	1	X	X	$\overline{G}\downarrow$ + Write + Reset	Continuous 8 bit	
1	X	0	1	0	1	X	X	$\overline{G}\downarrow$ + Reset		
1	X	1	0	0	0	X	X	$\overline{G}\downarrow$ + Write + Reset	Single Shot 16 bit	
1	X	1	1	0	0	X	X	$\overline{G}\downarrow$ + Reset		
1	X	1	0	0	1	X	X	$\overline{G}\downarrow$ + Write + Reset	Single Shot 8 bit	
1	X	1	1	0	1	X	X	$\overline{G}\downarrow$ + Reset		

Table 5.
Pulse Width & Frequency Measurement Modes

Control Register bit								Counter Mode	Condition required to generate counter interrupt
7	6	5	4	3	2	1	0		
X	X	0	0	1	X	X	X	Frequency Comparison	Interrupt generated if period of the Gate input is less than the timer Time Out
X	X	1	0	1	X	X	X	Frequency Comparison	Interrupt generated if period of the Gate input is greater than the timer Time Out
X	X	0	1	1	X	X	X	Pulse Width Measurement	Interrupt generated if the pulse width of the low portion of the Gate input is less than the timer Time Out
X	X	1	1	1	X	X	X	Pulse Width Measurement	Interrupt generated if the pulse width of the low portion of the Gate input is greater than the timer Time Out

footnote

$\overline{G}\downarrow$	represents	Negative transition of external gate input (G1-G3).
N	represents	Number contained in 16-bit Couter/Timer latch.
M	represents	Number contained in Most Significant Byte of 16-bit Couter/Timer latch.
L	represents	Number contained in Least Significant Byte of 16-bit Couter/Timer latch.
T	represents	Input clock period.
Reset	represents	Hardware or software reset

ISO-CMOS MD68SC49B Bus Monitor

Preliminary Information

9161-002-033 NA ISSUE 2 JUNE 1986

Features

- Address range checking.
- Data pattern match/mismatch detection.
- Control bus condition checking.
- Single or multi-pass mode.
- Freeze or continuous output.
- Capture and storage of bus image.
- 8 or 16 bit operation.
- Low power ISO-CMOS technology.

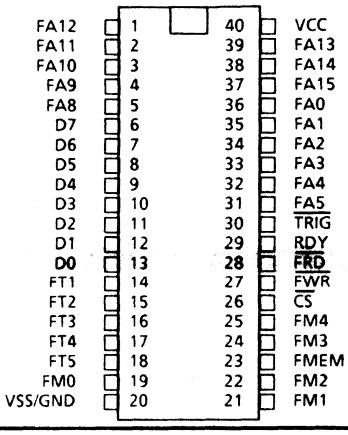
Applications

- Remote maintenance of processor systems.
- Microprocessor controlled test equipment.
- Microprocessor/multiprocessor development.
- Logic analyzer replacement for small systems.

Description

The MD68SC49 Bus Monitor, which is fabricated in MITEL ISO-CMOS technology, will perform several logic analyzer type functions under microprocessor control. This device will interface directly with the following processors: 6802, 6809, 6502, 68000, 8085, 8086, 8088, Z80 & Z8000. For AC timing for all interfaces contact the nearest Mitel Sales Office.

Pin Connections



Ordering Information

MD68SC49BC	Ceramic Dual-in-line Package
MD68SC49BD	Cerdip Dual-in-line Package
MD68SC49BE	Plastic Dual-in-line Package

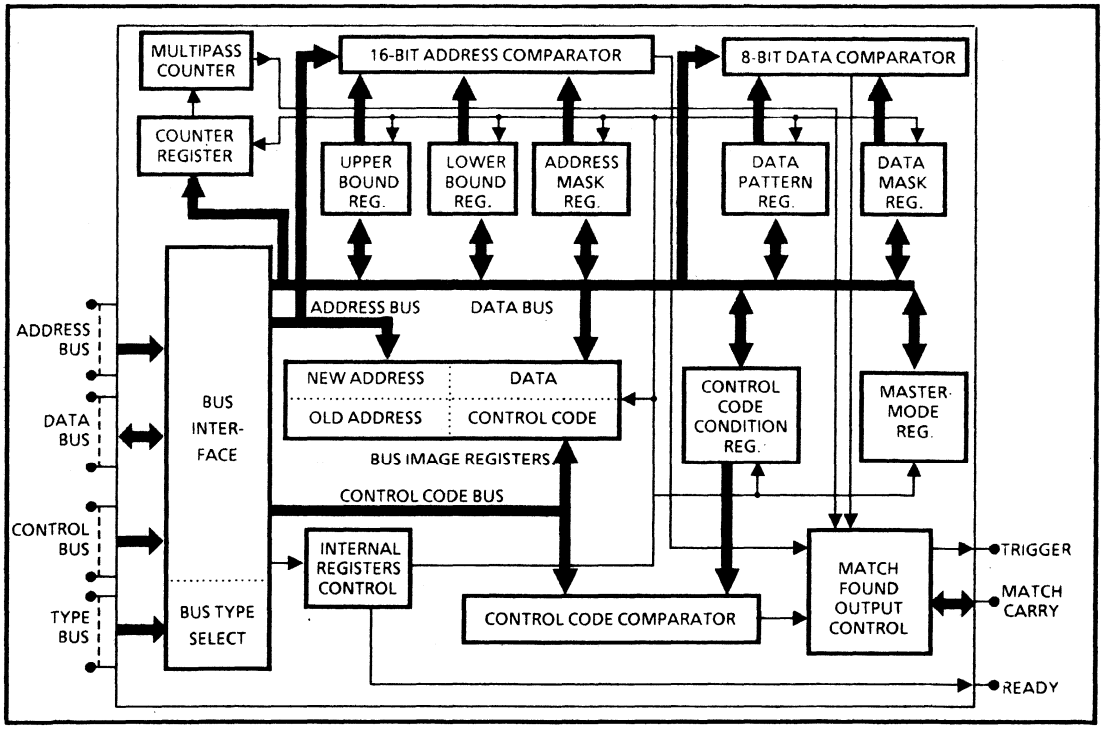


Figure 1 Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{CC}	-0.3	+7.0	V
2	Voltage on any pin	V_I	-0.3	V_{CC} + 0.3	V
3	Current through any I/O pin	I_I		10	mA
4	StorageTemperature	T_S	-65	+150	°C
5	Package Power Dissipation	P		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply Voltage	V_{CC}	4.75	5	5.25	V	
2		Input Voltage	V_I	0		V_{CC}	V	
3		Output Voltage	V_O	0		V_{CC}	V	
4		Operating Temperature	T_A	-40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

V_{CC} = 5V ± 5% V_{SS} = 0V Voltages are referenced to V_{SS}/GND, figures for full temperature range, unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent Supply Current	I_{CC1}			8	μA	Deselected; all outputs open. 6802 Interface
2		Operating Supply Current	I_{CC}		4	8	mA	f = 2MHz. 6802 Interface
3	INPUTS	Input HIGH Voltage	V_{IH}	2		V_{CC}	V	
4	INPUTS	Input LOW Voltage	V_{IL}	0		0.8	V	
5	INPUTS	Input Leakage Current	I_I			± 10	μA	$V_I = V_{SS}$ to V_{CC}
6	INPUTS	Input Capacitance	C_I		5		pF	$V_I = V_{SS}$ to V_{CC}
7	OUTPUTS	Output HIGH Voltage	V_{OH}	2.4			V	I_{OH} = -2.5mA
8	OUTPUTS	Output HIGH Current	I_{OH}	-2.4	-3.0		mA	V_{OH} = 2.4V
9	OUTPUTS	Output LOW Voltage	V_{OL}			0.4	V	I_{OL} = 6.5mA
10	OUTPUTS	Output LOW Current	I_{OL}	6.5	8.0		mA	V_{OL} = 0.4 V
11	OUTPUTS	Output Leakage Current	I_{LO}			± 10	μA	$V_O = V_{SS}$ to V_{CC}
12	OUTPUTS	Output Capacitance	C_O		10		pF	$V_O = V_{SS}$ to V_{CC}

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

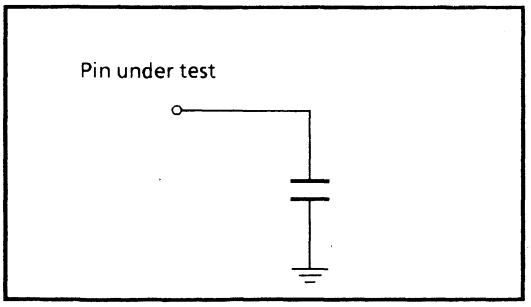


Figure 3. Test Load

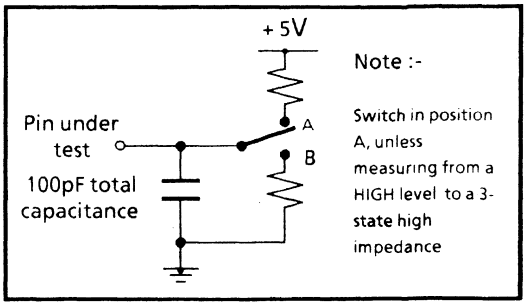


Figure 4. Test Load for Data Bus Release

Introduction

The MD68SC49 Bus Monitor encompasses the power of a logic analyser trigger generator in a single 40 pin, low power device. The device will independently monitor the activity on the microprocessor bus. A signal will be generated by the Bus Monitor when a user-defined pattern is detected on the bus. In addition to providing this signal, the device will also store the bus image present at that point in time. A unique feature of this peripheral is the ability of the device to be configured to directly interface with several different microprocessor families.

The function of a tool of this nature has in the past been difficult to incorporate into a design due to the microprocessor program overhead and the amount of circuitry involved. By including a small amount of initialization software (30-50 bytes), the Bus Monitor can be used to perform a variety of analysis functions simultaneously with the execution of the host processor's program. These functions could be expanded upon to give an even more powerful tool by the addition of more software. The enhancements of including the device in a system are not only seen in the design phase in the areas of reducing test and development equipment usage, but also similar effective improvements can be gained in the production and end-user phases of the life cycle of a design. Due to the interface reconfigurability of the device, it is particularly suited to multiprocessor designs.

In addition to the approach outlined previously, the Bus Monitor can be used as an active participant in the function of a system. By altering the contents of the user-defined pattern the device can reduce proccessing time or add a unique feature to a system. Such examples of this are, memory protection and data transmission monitoring. These applications are covered later.

Functional Description

The device contains a set of programmable comparators which are used to monitor the different microprocessor busses. The control of these comparators is achieved by the use of 13 internal registers. These registers store the user-defined condition used in the comparison, the input masks, and the information governing the mode of operation of the device. Once the user-defined condition has been detected on the bus, a signal is generated to inform the host processor of the event (i.e. a MATCH has been found).

The logical state of each of the monitored signals present on the bus are stored on an additional 5 internal registers ready for later scrutiny. Under the control of a programmable counter, the detection of a match can be delayed by a pre-programmed number of occurrences which is determined by the contents of two of the internal registers.

For certain of the microprocessors to which the Bus Monitor can be interfaced, it is necessary to use two devices. The processors for which two devices are required are the 16-bit varieties, i.e 68000, 8086, 8088 and Z8000. In this event a Match Carry bus is used to signal information from one Bus Monitor device to the other. This interconnection allows two devices to be effectively considered as one, acting in a master/slave configuration. More information concerning the use of the Bus Monitor in this case is given later.

The determination of the configuration of the device in the previous case, and the type of microprocessor family to which the Bus Monitor will interface, is determined by the signals presented to the Bus type inputs.

To help simplify the description, the microprocessor bus will be referred to as consisting of three separate busses :

Address Bus:	An address bus up to 24 bits wide can be handled by the Bus Monitor.
Data Bus:	An 8 or 16 bit wide data bus can be handled (two Bus Monitor Devices are required for 16 bit processors)
Control Bus:	As many as 10 control bus states, the control code, can be monitored (read/write, I/O memory control signals, etc.).

Register Description

The Bus Monitor is able to monitor any combination of the three microprocessor busses. Address, data and control bus images, the type of matching and the bits of each bus being monitored, are defined by the contents of eighteen internal 8-bit registers (as can be seen from the functional block diagram shown in Figure 1). These registers can be addressed by the microprocessor when the chip select line is low. The address, data and control busses are used by the processor to read from or write to the various registers. The decoding for the register addresses is given in Tables 1 and 2. The Internal Register address bits

TABLE 1
16-bit (Master Mode) Register Addressing

Internal Register Address②					Internal Register Selected	
RA5	RA4	RA3	RA2	RA1		
0	0	0	0	0	R0	Lower Address Boundary (bits 16 - 23)①
0	0	0	0	1	R1	Lower Address Boundary (bits 24 - 31)
0	0	0	1	0	R2	Upper Address Boundary (bits 16 - 23)①
0	0	0	1	1	R3	Upper Address Boundary (bits 24 - 31)
0	0	1	0	0	R4	Address Mask (bits 17 - 23)
0	0	1	0	1	R16	Control Code Image (bits 0 - 7)③
0	0	1	1	0	R6	Address Image (bits 8 - 15)①③
0	0	1	1	1	R17	Control Code Image (bits 8 - 9)
0	1	0	0	0	R8	Data Pattern (bits 8 - 15)
0	1	0	0	1	R9	Data Mask (bits 8 - 15)
0	1	0	1	0	R10	Data Image (bits 8 - 15)③
0	1	0	1	1	R11	Master Mode (bits 0 - 7)
0	1	1	0	0	R12	Control Code Condition (bits 0 - 7)
0	1	1	0	1	R13	Control Code Condition (bits 8 - 9)
0	1	1	1	0	R14	Multipass (bits 0 - 7)
0	1	1	1	1	R15	Multipass (bits 8 - 11)

Notes: ① Address bits 17-23 for 68000.
② These are the bottom five address bits when the chip is selected.
③ Read only registers.

TABLE 12
8-bit or 16-bit (Slave Mode) Register Description

Internal Register Address②					Internal Register Selected	
RA5	RA4	RA3	RA2	RA1		
0	0	0	0	0	R0	Lower Address Boundary (bits 0 - 7)③
0	0	0	0	1	R1	Lower Address Boundary (bits 8 - 15)③
0	0	0	1	0	R2	Upper Address Boundary (bits 0 - 7)③
0	0	0	1	1	R3	Upper Address Boundary (bits 8 - 15)③
0	0	1	0	0	R4	Address Mask (bits 0 - 7)
0	0	1	0	1	R5	Address Mask (bits 8 - 15)
0	0	1	1	0	R6	Address Image (bits 0 - 7)③④
0	0	1	1	1	R7	Address Image (bits 8 - 15)③④
0	1	0	0	0	R8	Data Pattern (bits 0 - 7)
0	1	0	0	1	R9	Data Mask (bits 0 - 7)
0	1	0	1	0	R10	Data Image (bits 0 - 7)④
0	1	0	1	1	R11	Master Mode (bits 0 - 7)
0	1	1	0	0	R12	Control Code Condition (bits 0 - 7)②
0	1	1	0	1	R13	Control Code Condition (bits 8 - 9)②
0	1	1	1	0	R14	Multipass (bits 0 - 7)②
0	1	1	1	1	R15	Multipass (bits 8 - 15)②
1	x	x	x	0	R16	Control Code Image (bits 0 - 7)②④
1	x	x	x	1	R17	Control Code Image (bits 8 - 9)②④

Notes: ① : RA - Register address from address bus when chip selected.
② : These registers are only used in 8-bit applications.
③ : Address bits (1-8) & (9-16) for 68000 microprocessors.
④ : Read only registers.

RA1-5 correspond to the least significant address bit of the address bus of the device in question. In the case of a 16-bit processor the two devices, master and slave, are selected by activating their respective chip select input. The two devices are then programmed independently. Care should be taken when accessing the registers as the Bus Monitor will continue to monitor the busses during the access period unless in a RESET condition (b_7 of Master Mode register set to logic '0'). The function of each of these registers and how they affect the operation of the Bus Monitor is also outlined in Table 1, 2 & 3 (Register bit 0 in each case contains the least significant bit). Additional information concerning the operation of the master mode (R11) register and the control code registers (R12, R13, R16 and R17) is given later.

TABLE 3
Internal Register Functions

Reg.#	Mnemonic	Description	Function
R0 R1	LBADD (L) LBADD (H)	Lower Bound Register	Contains a 16 bit address which is used as the lower boundary for address range checking.
R2 R3	UBADD (L) UBADD(H)	Upper Bound Register	Contains the higher 16 bit address boundary for address range checking.
R4 R5 ①,③	AMSK(L) AMSK(H)	Address Mask Register	Holds a 16-bit address mask.
R6 R7②	AIMA(L) AIMA(H)	Address Image Register	These registers are used to store the address bus image. Both the current (new) and previous (old) image are captured on each cycle, unless the Bus Monitor is in the FREEZE mode and a trigger has been generated. The processor can read either one or the other of the stored addresses depending on the setting of b_6 in the master mode register.
R8	DPAT	Data Pattern Register	Holds the data pattern to be used to search for a data match condition.
R9①	DMSK	Data Mask Register	This register contains the data mask.
R10	DIMA	Data Image Register	Holds the data bus image which is stored after each cycle, unless the Bus Monitor is in the FREEZE mode and a trigger has been generated.
R11②	MODE	Master Mode Register	The contents of this register controls the operating modes of the Bus Monitor.
R12 R13①,②	CCCR(L) CCCR(H)	Control Code Condition Register	The contents of these registers determine the Control bus condition to be monitored (i.e. active Control bus signals are monitored).
R14 R15②	MCNT(L) MCNT(H)	Multipass Counter Register	The Bus Monitor will generate a trigger after a number of matches, determined by the contents of these two registers, if in the multipass mode.
R16 R17②	CIMA(L) CIMA(H)	Control Code Image Register	Holds the control code image stored each cycle, unless the Bus Monitor is in the FREEZE mode and a Trigger has been generated (the condition of the Control bus signals are stored in this register. Logic "1" = ACTIVE).

Notes: ① With the mask registers a logic 1 will cause the Bus Monitor to disregard the state of the corresponding bit of the respective bus and always give a match for that particular bit.
② See 'Additional information for 16 bit microprocessors'.

Bus Interface

This provides the interface logic between the microprocessor bus and the internal registers of the device. When selected ($\overline{CS}$ is LOW), the address, data and control busses are used for data transfers between the internal registers and the controlling processor. When the device is deselected ($\overline{CS}$ is HIGH), these busses are monitored by the device. The bus interface can be reconfigured to satisfy the various microprocessor busses both with respect to pin connections and timing. This is done under the control of the type-bus inputs. Once these inputs have been set up, the Bus Monitor will be directly compatible with the microprocessor bussing structure that is selected.

The Type Bus is used to control the selection of the required microprocessor interface. These input pins should be connected to select the required microprocessor interface (see Table 4).

TABLE 4
Type Bus Decoding

Bus Type		T1	T2	T3	T4	T5
6502		1	1	1	0	0
6809		1	1	1	0	0
6802		1	1	1	0	0
8085		1	1	1	0	1
Z80		1	1	1	1	0
68000	MASTER	1	0	1	X	X
	SLAVE	1	0	0	X	X
8086	MASTER	1	1	0	0	0
	SLAVE	1	1	0	0	1
8088	MASTER	1	1	0	1	0
	SLAVE	1	1	0	1	1
Z8000	MASTER	0	0	X	X	X
	SLAVE	0	1	X	X	X
UNDEFINED		1	1	1	1	1

Depending on the Type Bus inputs, the internal interface logic will reconfigure the microprocessor bus timing requirements of the Bus Monitor to suit a specified processor. This removes the need for any extra circuitry to match the Bus Monitor to a specified bus structure. The Type Bus also redefines the pin connections of the Bus Monitor. A cross reference of the different pinouts has been included in the microprocessor interface sections. By hardwiring the respective address on the Type Bus, the Bus Monitor can be programmed to operate as the master or slave in 16 bit applications.

The Master Mode Register

This register permits the selection of the different operating modes of the Bus Monitor. Each of the eight bits will independently control a particular function of the device as outlined in Table 5 below. The least significant four bits of the Master Mode Register can be used to select whether the data or address comparators are used in the generation of a match and the type of comparisons which they perform.

Bit 4 controls the operation of the Multipass Counter, with bit 5 and 6 controlling the storage and reading of the bus images.

Bit 7 is a software reset. It is advisable to set this bit to logic '0' as early as possible in the execution of a program. This will inhibit the generation of a trigger in the subsequent microprocessor cycles. The bit can be set to a logic '1' later to "arm" the device.

Address Bound and Mask Registers

These registers are used to specify the pattern on the address bus for which the device will monitor. The Mask Register, AMSK(L) and AMSK(H), contain the control information which determines which of the address inputs are used in the pattern matching of the Address Comparator. Each of the bits correspond to an address input, i.e. bit 0 of AMSK(L) controls address input A_0 with bit 0 of AMSK(H) corrisponding to A_8. The Upper Bound and Lower Bound Registers, UBADD(H), UBADD(L), LBADD(H), and LBADD(L), contain the two 16 bit words which define the limits of the address for which the Bus Monitor will examine for a match.

Address Comparator

By examining the Upper Bound, Lower Bound and Address Mask Registers, the Address Comparator generates a signal to the Match Found control. An image of the address bus being monitored is compared to the Upper and Lower Bound Registers and a signal is generated if the image is in/out, depending on the mode selected by the Master Mode register, of the address range specified by these boundaries. The Address Mask registers are used to mask out individual bits of the address bus image on the comparison.

When a match is found, the address image at that moment is stored in the New Address Image register. The previous address image is also retained, but moved to the "Old Address " image store. These registers are updated on every cycle, except after a match has been detected when the

device is in a Freeze Mode. The Address Comparator can also be set to an "always matched" state by the Master Mode Register when address bus monitoring is not required.

Data Pattern and Mask Registers

This register is used to specify the pattern on the data bus for which the device will monitor. The mask register, DMSK, contains the control information which determines which of the data inputs are used in the pattern matching of the data comparator. Each of the bits correspond to a data input, i.e. bit 0 of DMSK controls data input D_0. The data pattern register, DPAT, contains the pattern which the data comparator will use to reference the data bus against in the generation of a match.

MASTER MODE Register (R11) Bit Positions

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
$\overline{RST}$	O/$\overline{N}$	FRZ	SP	DC	DM	AC	IR

TABLE 5
MASTER MODE Register (R11) Bit Function

Bit #	Name	Function	Description
b_7	RST	RESET	Controls the internal reset. A logic '0' in this bit position will cause the internal bus image registers to be cleared, the multipass counter to be loaded from its associated registers and disable the trigger. A logic '1' will cause the Bus Monitor to commence bus pattern matching at the start of the next microprocessor instruction.
b_6	O/N	OLD / NEW Address Image	Selects whether the "old" or "new" address bus image is read. A logic '1' in this bit position will select the address image captured from the address bus on the cycle prior to the matched cycle ("old" address bus image).
b_5	FRZ	Freeze / Continuous Mode	Will control the freeze mode. If selected (FRZ = Logic '1'), the Bus Monitor will only give a trigger output on the first match and can subsequently only be reset by the processor. If de-selected a trigger signal of one cycle duration will be output on the cycle following a MATCH. The Bus Monitor will reset on the next cycle and continue to monitor for further matches.
b_4	SP	Single / Multipass Mode	Selects single or multipass mode. If multipass mode is selected (SP = Logic '0') a 12 bit counter will decrement from the value stored in R14, R15 on every occurrence of a match. On reaching zero a trigger output signal is generated.
b_3	DC	Enable DATA Comparison	A Logic '0' in this bit position will effectively make the data bus always appear matched.
b_2	DM	DATA Match / Mismatch	This controls data match/mismatch. A trigger output will be generated on a match (DM = Logic '1') or a mismatch (DM = Logic '0') of the databus to the Data Pattern Register.
b_1	AC	Enable ADDRESS Comparison	A Logic '1' will enable the address bus comparison to the boundary. A Logic '0' in this bit position will effectively make the address bus appear matched.
b0	IR	ADDRESS In / Out of Range	Selects the in-range or out-of-range address comparison. In both cases the boundary addresses are included in the range to be considered. A Logic '1' in this bit position will cause addresses to be monitored inside the boundaries.

Data Comparator

The function of the Data Comparator is to compare the contents of the Data Pattern Register to an image of the Data Bus being monitored. The Data Comparator, under the control of the Master Mode Register, sends a signal to the Match Found control when the data bus image matches, or mismatches (as required) the contents of the Data Pattern Register. The Data Mask Register masks out individual bits of the data bus image used in the comparison. When a match is found the data bus image is stored in the Data Bus Image Register. As in the previous case, the Data Comparator can be set to "always matched" by the Master Mode Register when data bus monitoring is not required.

Control Code Condition Register

This register contains the pattern of ACTIVE states which will be used to reference the control signal inputs. If a logic '1' is contained in the relevant bit position then the device will require an active level on the control signal input, this may not necessarily be a logic '1'. If a logic '0' is contained then the state of the signal is ignored, i.e. it is masked out.

Further information is contained in Figure 2 and, since each set of microprocessor control signals is different, in each of the microprocessor interface sections.

Control Code Comparator

This comparator is used to monitor the state of the microprocessor control signals. When a match is found, an image of the control bus signals being monitored is stored in the Control Code Image register.

The Control Code Condition register is used to select which of these microprocessor control inputs are used by the comparator. As mentioned earlier, each microprocessor has different control signals. Correspondingly, there is internal logic in the comparator which will not only discern active levels for each of these signals but will also decode any of the signals which are multiplexed. In the case of a microprocessor with a multiplexed control signal structure, a table of the decoding is given in the relevant interface section. For a match condition to be detected it is necessary to have ALL of the monitored signals to be in an active state simultaneously. Care must be taken that a mutually exclusive state is not required for the generation of the match, i.e. an active level on read and a write signal is require to generate a match.

When reading the Control Code Condition register, the image returned is the state of the control signals on the busses at the time when the match was found and not the logical level of the inputs. A logical "0" represents an active control condition (R17 is always 00_{16} for 8-bit μProcessors).

An example of the operation of these registers would be in the detection of a memory write operation (it is assumed that the relevant control signals are available e.g. a Z80 interface). Toprogram this register for such an operation 00_{16} is written into R13 (CCCR(H)) and 11_{16} into R12 (CCCR(L)). If a write operation to the Data memory occurs as specified, then a trigger would be output. The image which would be read back in register R17 (CIMA(H)) would be 00_{16} and in R16 (CIMA(L)) 66_{16}, reflecting that an 8-bit write operation in the data memory area was performed (R17 follows the exception for 8-bit μPs here).

Image Registers

The Image Registers hold the stored image of the bus. There is an image register corresponding to each of the processor busses. Depending on the information contained in the Master Mode register, this image can be stored for one bus cycle (Continuous mode) or until reset by software (Freeze mode). As previously outlined, there are two address image registers which contain the present and previous image, a data image register and control code image register. These can be accessed by the processor. However, in the continuous mode their contents will have little meaning as they will only reflect the status of the bus during the read operation. Also these are Read only registers and can only be cleared by altering b_7 of the Master Mode register.

Multipass Counter and Register

The Multipass Counter Register contains the number of matches that are required before the device will output a trigger signal. When the microprocessor reads this register, it is the value previously loaded by the microprocessor which is read, not the value of the count contained in the counter.

If enabled by the Master Mode Register, the Multipass Counter will be decremented when a match has been found on all of the busses, thus delaying the generation of a trigger output. When the count has reached zero a trigger is output (TRIG = LOW).

Every time the Bus Monitor is reset (either by writing a logic '0' to b_7 of the MASTER MODE Register or after a trigger in the Continuous operating mode), the Multipass Counter is loaded with the number stored in the Multipass Counter Register.

Match Found Control

The Match Found Control combines the outputs from the bus comparators to generate the trigger signal. The three comparators shown in the functional block diagram (Fig. 1) are used to detect a match condition. The 16 bit address comparator is used to compare the address bus image with the upper bound register and the lower bound register. Similarily the 8 bit data comparator is used to compare the data bus image, the contents of the data pattern register and the control code comparator is used to detect a match condition on the control bus. All three of these comparasons are performed simultaneously at the end of every machine cycle. The results of these comparisons are combined under the control of the contents of the Master Mode Register, to generate a trigger. It is necessary for a match condition to exist on all three comparators or, in the case of the data and address comparators, they are set to "always matched" by the bits b_3 and b_1, respectively, of the Master Mode Register, before a trigger will be generated.

When two Bus Monitors are used in a Master/Slave configuration, a match on the slave busses must also have been found in addition to a match on the Masters busses. The Match' Carry bus is used to inform the Master of the status of the Slaves' comparisons. The functions of the Match Carry signals are shown in Table 6. The master will halt its bus comparisons until the slave has checked for a pattern match. The slave in this case would monitor the lower address boundary and 8 least significant data bits. If a match has been found by the slave, it is taken into consideration when the master performs its comparisons. The trigger output signal is used to inform the microprocessor that a match condition has been found and normally takes the form of an interrupt request.

If the multipass counter is used, the Bus Monitor will not output a trigger immediately. Instead, the contents of the multipass counter are decremented. The start value of this count is derived from the contents of the multipass counter register (a 12 bit word). When the count value becomes zero, a trigger is generated and the start value reloaded into the counter.

Additional Information for 16 Bit Processor Applications.

There are a number of differences between the use of the Bus Monitor in an 8-bit microprocessor

Register 13② (17)								Register 12② (16)							
b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
X	X	X	X	X	X	USR	SUP	DAT	CDE	IO	M	LB	HB	RD	WR

USR - Processor is in user or normal mode (16 bit processors only).①
SUP - Processor is in system or supervisor mode (16 bit processors only).①
DAT - Processor is accessing data memory. (Read or Write operation)
CDE - Processor is accessing opcode memory. (Fetch cycle)
IO - Processor is in Input / Output cycle. (Read or Write operation)
M - Processor is addressing memory. (of any type)
LB - Indicates a data transfer on bits 0-7 of the data bus.
HB - Indicates a data transfer on bits 8-15 on the data bus (16 bit processors only)
RD - Indicates a read cycle.
WR - Indicates a write cycle.

Notes:
① - Refer to the relevant 16 bit processor manual.
② - Care should be taken that a mutually exclusive condition is not programmed into this register, e.g. setting both RD & WR to logic "1".
③ - X = NOT USED A logic '0' should be written to these bit positions in the Control Code Condition Register. A logic '0' will be stored in the Control Code Image Register.
④ - Refer to the microprocessor interface sections for additional information.

TABLE 6
MATCH CARRY Bus Description

MASTER		SLAVE		Function
Pin #	IDENT.	Pin #	IDENT.	
19	SR in	19	SR out	Indicates to the Master that the Slave inputs can be combined with Master compare results. This allows the Slave to delay the Master comparason.
21	$\overline{A>U}$ in	21	$\overline{A>U}$ out	Indicates to the Master that the Slave's portion of the current address is greater than the upper bound address.
22	A<L in	22	A<L out	Indicates to the Master that the Slave's portion of the current address is less than the lower bound address.
24	DM in	24	DM out	Indicates to the Master that the Slave's portion of the current data is matched to the data pattern register.
25	SD out	25	SD in	The Master will output this signal to disable the Slave.

environment and a 16-bit one, that should be brought to the attention of the user.

When two Bus Monitors are used in a Master/Slave 16-bit application, a total of 32 internal registers are used by the two devices. The internal registers of both the Bus Monitors are re-structured to optimize the required address space. Consequently, as with the 8-bit application, only 5 address bits are required to access all the registers in both devices (once they have been selected). Tables 1 & 2 show the register functions and their respective addresses for both the 8 & 16-bit applications. Also the data and address registers are concatenated to span the full lengths of the busses. The Slave is used to monitor the least significant bits and the Master the most significant ones. Care should be taken in the masking of the most significant address bits as not all of the microprocessors utilize all of the address bits available. It is only necessary to mask out the ones that are not used.

In a 16-bit application, R4 should be set to FF_{16} to inhibit the most significant address byte from the pattern matching. In the master mode, R16 & R17 are re-located into the space previously occupied by R5 and R7 respectively. In the slave Bus Monitor registers R16 & R17 are no longer used.

In this configuration the master is in sole control of the trigger generation. The slave Bus Monitor is only used for address and data matches. Therefore slave registers R12 to R15 serve no purpose and should be set to all logic '0'

Analog Telecom Components

ISO-CMOS **MT4320**
Keypad Pulse Dialer

JAN 1985

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Applications

- Pushbutton telephones
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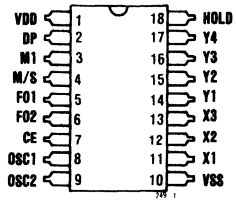
- Repertory dialers

Pin Connections

DUAL IN-LINE PACKAGE



Ordering Information

MT4320AC 18 Pin Ceramic DIP

MT4320AE 18 Pin Plastic DIP

Description

The MITEL MT4320 is fabricated using MITEL ISO-CMOS™ high density technology. The device is a pin for pin replacement for the DF320 Loop Disconnect Dialer and offers lower power dissipation. The MT4320 accepts up to 20 digits from a standard 2 of 7 keypad and offers a REDIAL option activated by key #. The device provides dial pulsing and muting outputs and has a HOLD pin for interrupting a dialing sequence. Outpulsing mark/space ratio and dialing speed are pin selectable.

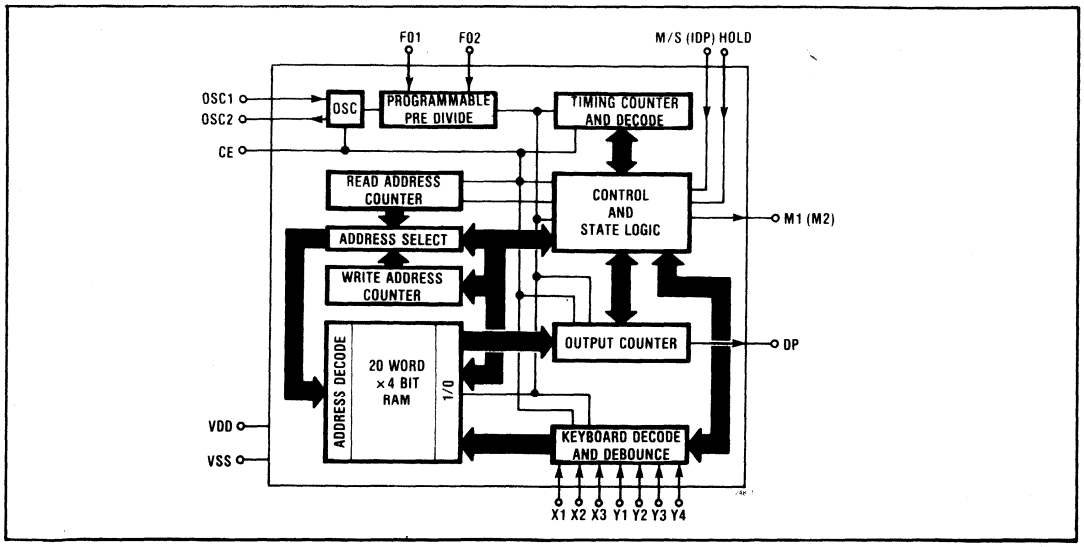


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings

	MIN	MAX
$V_{DD}-V_{SS}$	-0.3V	10V
Voltage on any pin	V_{SS}-0.3V	V_{DD} + 0.3V
Current at any pin		10mA
Operating Temperature	-40 °C	+ 85 °C
Storage Temperature (C Package)	-65 °C	+ 150 °C
Power Dissipation (C Package) #		1000mW
#Derate 16mW/ °C above 75 °C. All leads soldered to PC board.		

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics

All voltages referenced to V_{SS} unless otherwise noted.

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS UNLESS NOTED V_{DD} = 3.0V, T_A = 25 °C f_{CLK} = 3.579545 MHz	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.5		5.5	V		
2		Standby Supply Current		I_{DDS}		1.0	10.0	µA	CE = V_{SS}	
3		Operating Supply Current		I_{DD}		125	250	µA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-8.0	µA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S, IDP, F01,
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	10.0	µA	$V_{IN} = V_{DD}$	F02, FD, HOLD
8		Logic '0' Level		V_{IL}			0.9	V	All inputs	
9		Logic '1' Level		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M1
13			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	

AC Electrical Characteristics

All voltages referenced to V_{SS} unless otherwise noted.

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS UNLESS NOTED V_{DD} = 3.0V, T_A = 25 °C f_{CLK} = 3.579545 MHz
1	DYNAMIC	Output Rise Time	t_R		1.0		µs	DP, M_1.
2		Output Fall Time	t_F		1.0		µs	C_L = 50pF
3		Maximum Clock Frequency	t_{CLK}	3.58			MHz	3.579545 MHz Crystal
4		Mark to Space Ratio (DP Output)	M/S		2:1			Note 1
5					3:2			
6		Impulsing Rate = $\frac{1}{T}$			10		Hz	Note 1
7					16			
8					20			
9					932			
10		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE '1'
11		Input Capacitance	C_{in}		5.0		pF	Any Input

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

Note 1. See Pin Function, Table 1.

TABLE 1

PIN FUNC.	DESCRIPTION					
V_{DD}	Positive voltage supply					
DP	Dial Pulsing Output Buffer					
M1	Mute Output (Off Normal) Buffer					
M/S	Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}.				O/C	2:1
	Note: O/C = Open Circuit				V_{DD}	3:2
F01, F02	Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}	F01	F02	Nominal Impulsing Rate	Actual* Impulsing Rate	System Clock Frequency
		O/C	O/C	10 Hz	10.13 Hz	303.9 Hz
		O/C	V_{DD}	20 Hz	19.42 Hz	582.6 Hz
	*Assumes f_{CLK} = 3.579545 MHz.	V_{DD}	O/C	932 Hz	932.17 Hz	27,965.1 Hz
		V_{DD}	V_{DD}	16 Hz	15.54 Hz	466.1 Hz
CE	Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.					
OSC1	Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.					
OSC2	Crystal Output Buffer to drive crystal.					
V_{SS}	System ground					
X_1, X_2, X_3	Column keyboard inputs. On-chip pull-up transistors to V_{DD}. Active LOW.					
Y_1, Y_2, Y_3, Y_4	Row keyboard inputs. On-chip pull-up transistors to V_{DD}. Active LOW.					
HOLD		O/C	Normal Operation			
		V_{DD}	No impulsing. If activated during impulsing, hold occurs when the current digit is complete.			
	Prevents further impulsing. On-chip pull-down transistor to V_{SS}.					

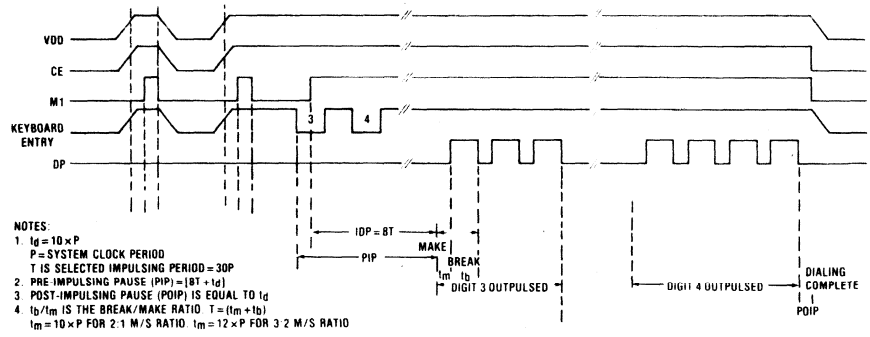


Fig. 2 Keypad Pulse Dialer Timing Diagram CE-External Control

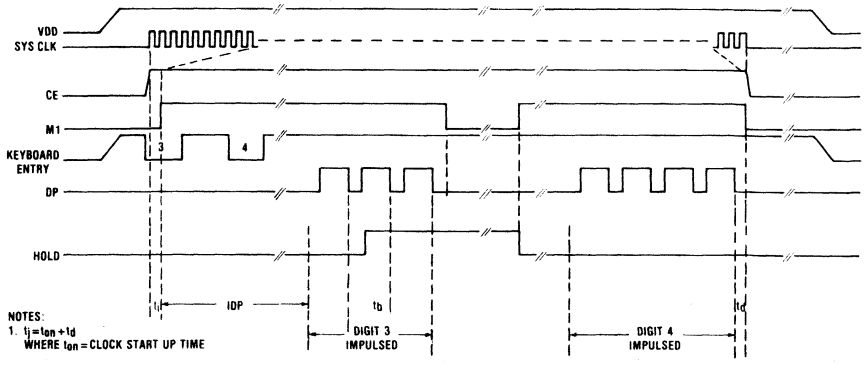


Fig. 3 Keypad Pulse Dialer Timing Diagram CE-Internal Control

Functional Description

The Mitel MT4320 keypad pulse dialer is optimized for use in key operated pulse dialing telephone sets. The MT4320 accepts keypad information directly from a dual contact keypad having two single pole switches per key; one switch common to the column and one switch common to the row. The common row contacts are connected Y1 to Y4 and the column common contacts connected X1 to X3. The other side of each switch is connected to a common V_{SS} line. The keypad code is shown in Table 2.

The MT4320 will accept up to 20 digits. Prior to a keypad input being accepted, contact bounce is eliminated by a circuit which ensures that any input which is valid for less than 10 ms is rejected and any input valid for greater than 17 ms is accepted as a valid key input. This circuit operates similarly on the trailing edge of a valid key input preventing multiple digit recognition in the presence of noise. Debounce operation is shown in Figure 4.

The first key entered in any dialing sequence initiates the oscillator on the MT4320 by internally taking CE high. The oscillator signal is divided down to the System Clock (SYS CLK) frequency by a programmable pre-divide circuit. The internal SYS CLK signal is used for all input and output timing. Digits may be entered asynchronously from the keypad. Dialing and mute functions are output as shown in Figure 2 and Figure 3. Figure 2 shows use of the MT4320 with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialer circuit. In this mode, the pulse occurring on M1 when CE is taken high with no keypad input can be used to initiate the bistable latching relay.

Figure 3 shows the timing diagram of the MT4320 in the CE-internal control mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously and dialing commences after recognition of the leading edge of the first valid key input. Upon completion of dialing of all entered digits, CE goes low internally, signifying the end of the dialing sequence. Any subsequent digits entered will be interpreted as a new dialing sequence for redial purposes. If the key # is activated after CE goes low, redialing of the previous dialing sequence will occur.

The Hold input may be used to interrupt dialing at any time. If the Hold input is taken high while a digit is being outpulsed, outpulsing of the current digit will be completed prior to interruption of the dialing sequence. At this time M1 goes low. Dialing recommences when the Hold input is taken low.

TABLE 2 KEYPAD INPUT CODE

No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
# RE-DIAL		1	1	1	0	1	1	0

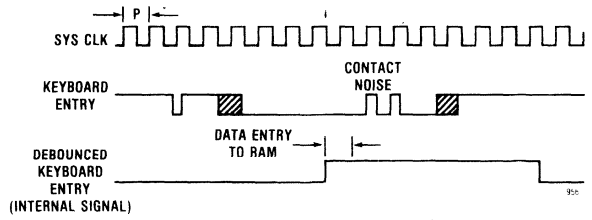


Fig. 4 Keypad Input Debounce Timing Diagram

Applications

Keypad Pulse Dialing Telephone

The MT4320 provides all of the signals required to implement a keypad pulse dialing telephone. The circuit in Figure 5 shows how the MT4320 is interfaced to the telephone line and 500 type network to provide the following capabilities:

(1) Operation independent of TIP to RING D.C. polarity.
(2) High voltage transient protection.
(3) Present a minimum A.C. impedence of 270K ohm during dialing break periods.
(4) Operation on line impedences up to 1275 ohm driving into 150 ohm D.C. load from 900 ohm source impedence.
(5) Power-on-reset.
(6) Muting during dialing sequence.

Protection against TIP to RING polarity reversal and voltage transients is provided by diode bridge BR1 and varistor VR1 respectively, and added by diode D1 and capacitor C1.

When DP is low, transistor Q1 is turned on, providing base current to Q2. In this condition, loop current flows from BR1 +, through the speech network and Q2 to BR1 −. During outpulsing, a high level at the DP output turns Q1 off, removing base drive from Q2 which in turn blocks the loop current. Muting is provided by transistor Q4 which presents a high impedence in series with the receiver whenever M1 (or M2) is high.

In the loop condition (Q2 on), the supply current for the MT4320 flows from BR1 +, through the device and returns to BR1 − via D2, R2 and Q2. During a loop break (Q2 off), the supply current returns to BR1 − via R1 only. The value of this resistor ensures a high A.C. impedence during loop breaks. Capacitor C1 provides auxiliary supply current during these periods. Diode D2 prevents the speech network and R2 from shorting the MT4320 supply. Under the various conditions of loop state and line length, the V_{DD} to V_{SS} voltage is limited by zener diode D1 and smoothed by capacitor C1.

Capacitor C2 provides a power on reset function for the MT4320 to prevent unwanted dialing when the handset is taken off-hook. Resistor R8 ensures that the MT4320 is reset should the hook switch be flashed during dialing. This resistor forms the bottom leg of a voltage divider is series with the CE output transistor.

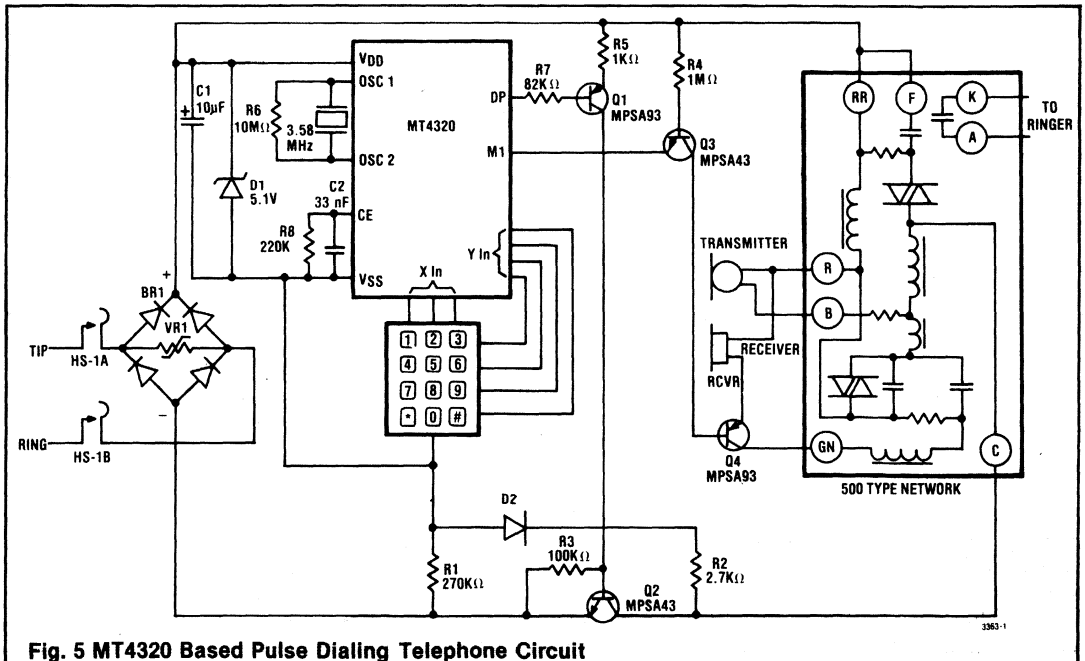


Fig. 5 MT4320 Based Pulse Dialing Telephone Circuit

Keypad Pulse Dialing Telephone with Redial Capability

If redialing of the last number dialed is a required feature of a pulse dialing telephone, then the CE input of the MT4320 must be held high during the entire dialing period to allow for pauses. The circuit shown in Figure 6 provides this function. Upon recognition of the first valid keypad entry, CE goes high and sets the NOR R-S latch, formed with gates G1 and G2. The output of G2, now high, holds the CE input high for the remainder of the dialing sequence.

To redial the previous number entered, the hookswitch is depressed and released, and the key# activated. "Flashing" the hook switch as described causes capacitor C3 to charge via the base emitter junction of Q5. This base current spike causes Q5 to turn on momentarily, pulling the inputs of G1 low and resetting the latch. Pressing the key# results in the redialing of the last number dialed.

Diode D4 prevents the output of G2 from clamping CE low during detection of the first valid keypad entry of a dialing sequence. Resistor R8 is a current limiting resistor. Of special significance in this circuit are the placement of the hookswitches after the diode bridge and the inclusion of resistor R10. These changes insure that standby supply current is provided for memory retention when the phone is on-hook.

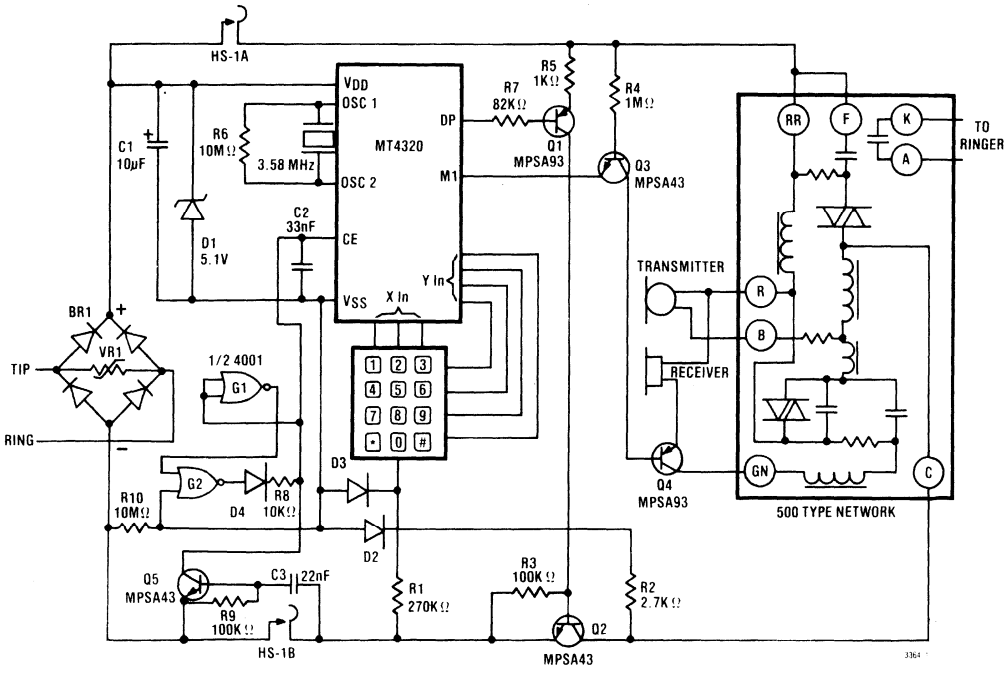


Fig. 6 MT4320 Based Pulse Dialing Telephone Circuit with Redial Capability

Bistable Relay Telephone Connection

In applications where no semiconductor components are allowed in the telephone loop during normal speech, a bistable relay may be used as shown in Figure 7 to isolate the MT4320 and associated devices. A keyboard common changeover switch is required to short circuit the MT4320 during normal speech and short circuit the telephone network during keying of the first digit. The positive transition of M1 pulses the bistable relay to ensure that the network is short circuited for the remainder of the dialing period. When dialing is complete, the bistable relay is pulsed again, connecting the telephone network back into the loop and short circuiting the MT4320 via the keyboard common switch.

If the bistable relay is set such the MT4320 is connected into the loop when the handset is lifted, a pulse on M1 resets the relay such that the network is reconnected. This pulse is a result of CE being pulled high by R8 in the absence of a keyboard input.

Impulsing is controlled by DP via transistors Q1 and Q2. Resistor R4 provides D.C. termination of the line during dialing to generate voltage for the MT4320 power supply.

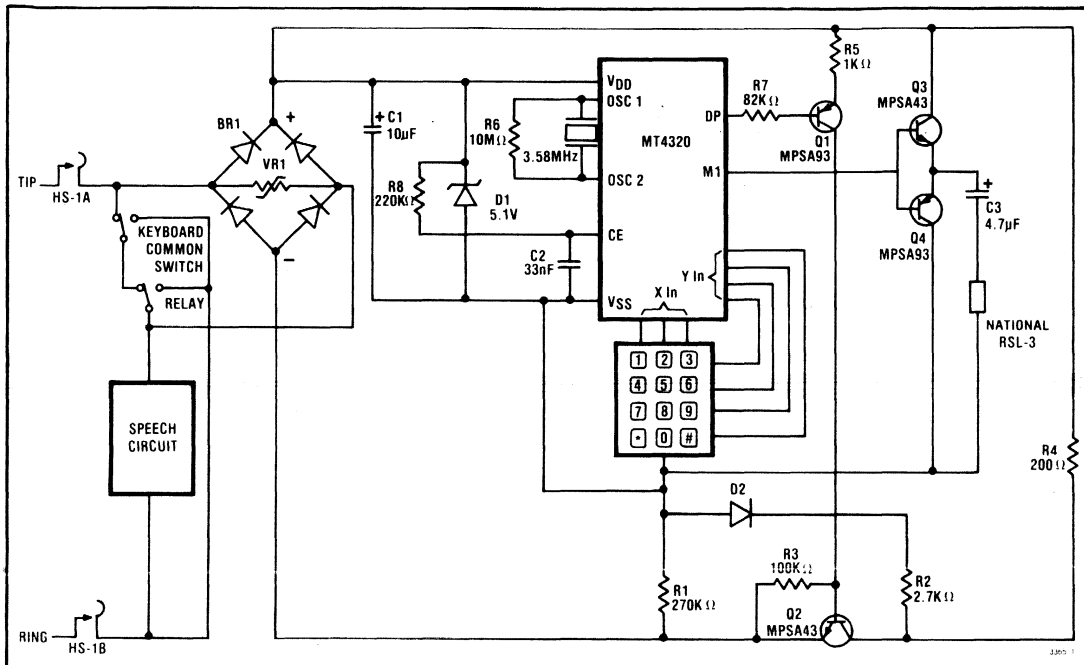


Fig. 7 Bistable Relay Telephone Connection

Single Contact Keyboard Interface

A single contact, matrix-type keyboard may be used with the MT4320 by the addition of the simple interface circuit shown in Figure 8. Depressing any key connects the on-chip pull-up transistor to the base of an external bipolar transistor. The corresponding row input (Y) is clamped to approximately 0.7V by the base-emmiter junction of the transistor. The pull-up transistor on this row input supplies base drive to the bipolar transistor whose collector, in turn, clamps the column input (X) to approximately 0.2V. With these levels on the row and column inputs, a valid keypad entry is obtained.

Tone to Pulse Converter

The MT4320 is ideally suited for use in various tone to pulse converter designs. A typical system is shown in the block diagram, Figure 9. The 20 digit on-chip, first in-first out memory serves as a buffer to allow asynchronous dialing into the converter and a tone dialing rate considerably faster than the normal outpulsing rate (10 pulses per second with 800 ms. interdigit pause). All signals required to control the loop during outpulsing are provided by the MT4320.

The tone receiver portion of the converter is efficiently constructed with the MT8865 and MT8862, Mitel's 2-chip DTMF receiver. The output code of the MT8862 decoder is compatible with the input code of the MT4320 allowing direct interconnection of the two parts. (Q1 to Q4 of the MT8862 to Y1 to Y4 of the MT4320, and Q5 to Q7 of the MT8862 to X1 to X3 of the MT4320). A differential input stage interfaces the tone receiver to the telephone line. The steering output, STD, from the tone receiver is fed into the control circuitry to control line splitting.

Off-hook detection, ringing voltage detection, and battery feed circuitry complete the converter, respectively providing signals for the timing circuitry and holding current during the line split condition.

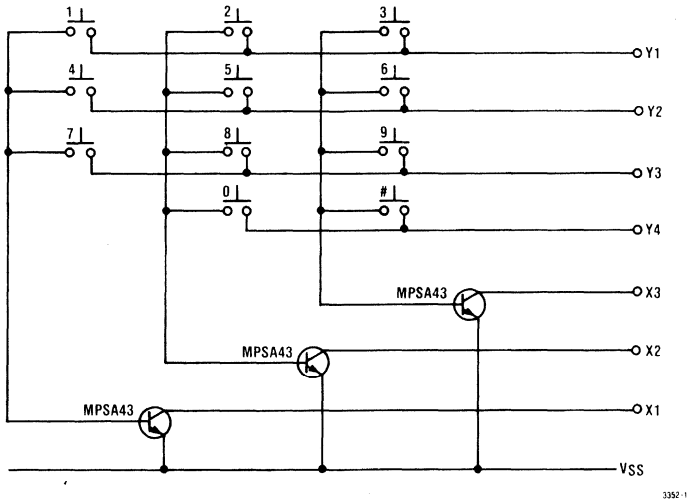


Fig. 8 Single Contact Keyboard Interface

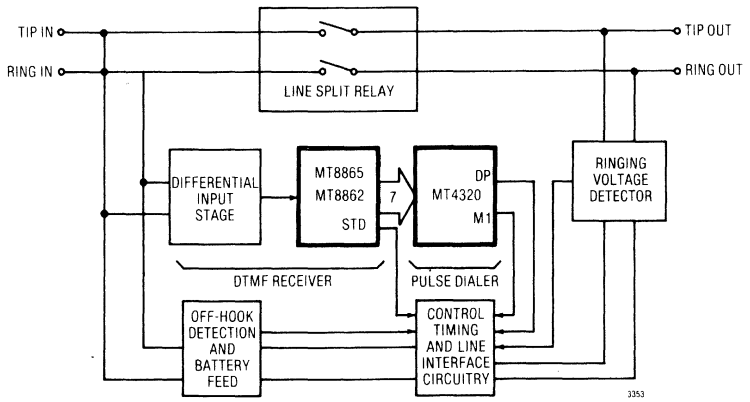


Fig. 9 Tone to Pulse Converter

Repertory Dialer

Figure 10 illustrates the use of the MT4320 in a keypad pulse dialing repertory dialer. The 20 digit on-chip memory of the MT4320 is useful as buffer storage to allow ansynchronous loading of digits from

the main telephone number memory. The main storage is provided by the MD21SC14, Mitel's 1024 word by 4 bit RAM. The 2-of-7 keyboard information is encoded to reduce the amount of RAM required. This information is then decoded by the MD74SC139 back to 2-of-7 format for the pulse dialer.

Three modes of operation (NORMAL, PROGRAM, and DIAL), are provided as selected by the MODE SWITCH. In the NORMAL mode, keypad data is fed directly to the MT4320 via the encode-decode loop. Dialing commences upon entry of the first digit. To facilitate redialing of the previous number, the CE input must be held high during the entire dialing sequence.

When the PROGRAM mode is selected, the first two digits keyed in are interpreted as the telephone number address. These numbers are stored in BCD format to alleviate the need for a complex encoding scheme. As such the capacity of the repertory dialer is limited to 48, 16 digit numbers. Each subsequent digit entered, is stored in the main memory and causes the DIGIT ADDRESS COUNTER to be incremented. This is repeated until the entire number has been entered.

The DIAL mode is selected to dial a number from the main memory. Again the first two digits entered are interpreted as the telephone number address. In this mode, the second digit entered triggers the control circuitry to clock the DIGIT ADDRESS COUNTER, read the digits from the main memory, and load them into the buffer memory of the MT4320. These digits are immediately dialed out by the pulse dialer. Redialing of this number can be accomplished by returning to the NORMAL mode and activating the key "#".

The line interface and speech network control can be derived from the circuits shown in Figure 5 and Figure 6. With selection of low power CMOS control circuitry, telephone line powering of the entire circuit becomes a possibility.

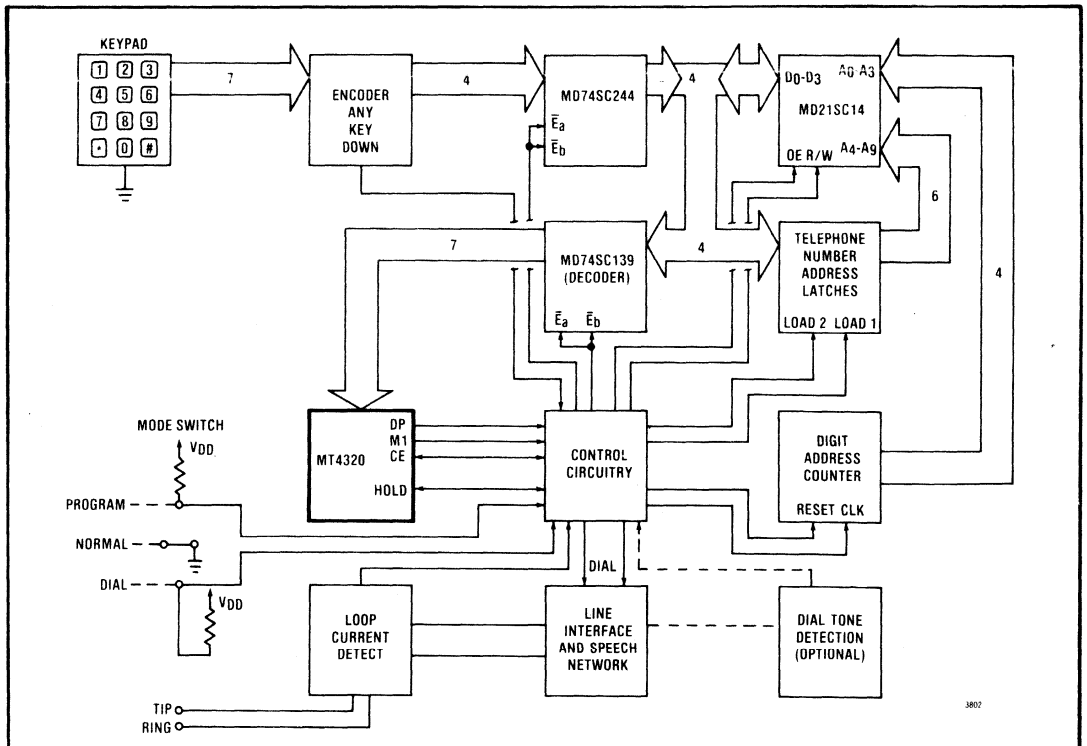


Fig. 10 Keypad Pulse Dialing Repertory Dialer

ISO-CMOS **MT4325**
Programmable Keypad Pulse Dialer

FEB. 1985

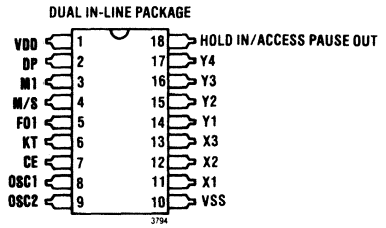
Features

- Last number redial
- Multiple access pause programming
- Any valid keypad input or HOLD IN causes exit from access pause
- Oscillator start up controlled from keypad input
- Oscillator power down whilst not dialing
- 300Hz Key Tone indicates valid key
- 2.0V to 7.0V supply voltage operating range
- Stores up to 20 digits and access pauses
- Digit memory retained down to 1.5V at 1µA
- Selectable mark/space ratio 66⅔:33⅓ or 60:40
- 10Hz dialing speed (932Hz fast test)

Applications

- Pushbutton telephones with last number redial
- Repertory dialers
- Tone to pulse converters

Pin Connections



Ordering Information

MT4325AC	18-Pin Cerdip DIP
MT4325AE	18-Pin Plastic DIP

Description

The Mitel MT4325 Keypad Pulse Dialer contains all the logic necessary to interface a 2 of 7 keypad and convert this key information to control and mute pulses simulating a telephone rotary dial. The MT4325 has programmable access pause capability to provide automatic interruption of dialing needed when accessing the toll network, WATS line or public network via a PABX. The device is fabricated using Mitel ISO-CMOS™ technology which enables functionality down to 2.0V making the device ideal for long loop operation.

The MT4325 will accept up to 20 digits and access pauses and will redial stored information at a later time by activation of # key. Device current in standby is less than 1µA at 1.5V.

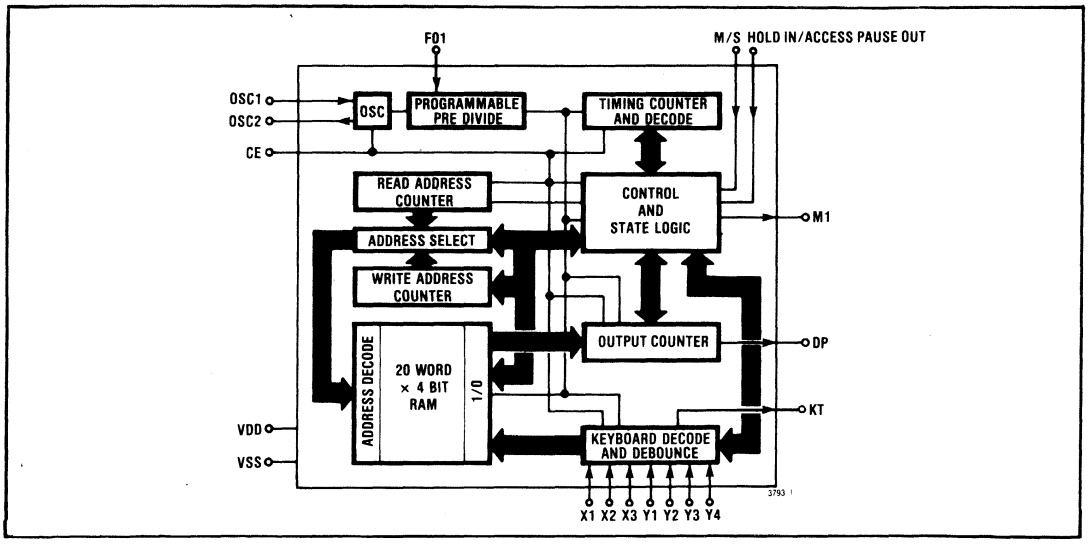


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings#

	MIN	MAX
$V_{DD}-V_{SS}$	−0.3V	10V
Voltage on any pin	V_{SS} − 0.3V	V_{DD} + 0.3V
Current at any pin		10mA
Operating Temperature	−40 °C	+85 °C
Storage Temperature (C Package)	−65 °C	+150 °C
Power Dissipation (C Package) #		1000mW

#Derate 16mW/ °C above 75 °C. All leads soldered to PC board.

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics

All voltages referenced to V_{SS} unless otherwise noted.

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS UNLESS NOTED V_{DD} = 3.0V, T_A = 25 °C f_{CLK} = 3.579545 MHz	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.0		7.0	V		
2	SUPPLY	Standby Supply Current		I_{DDS}		1.0	3.0	µA	CE = M/S = F01 = HOLD IN = V_{SS}, V_{DD} = 1.5V	
3	SUPPLY	Operating Supply Current		I_{DD}		125	250	µA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	−0.5	−3.0	−8.0	µA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5	INPUT	Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6	INPUT	Input Leakage Current		I_{IL}		−0.1		nA	$V_{IN} = V_{SS}$	M/S, F01
7	INPUT	Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	100	µA	$V_{IN} = V_{DD}$	
8	INPUT	Input Low Level Voltage		V_{IL}			0.9	V	All inputs	
9	INPUT	Input High Level Voltage		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11	OUTPUT	Voltage Levels	High-level	V_{OH}	2.99	3		V		
12	OUTPUT	Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M_1, KT
13	OUTPUT	Drive Current	N-Channel Sink	I_{OL}	0.2	0.5		mA	V_{OUT} = 0.5V	DP, M_1, KT
14	OUTPUT	Drive Current	P-Channel Source	I_{OH}	−0.8	−2.0		mA	V_{OUT} = 0.7V	DP, M_1, KT
15	OUTPUT	Drive Current	P-Channel Source	I_{OH}	−0.2	−0.5		mA	V_{OUT} = 2.5V	DP, M_1, KT
16	IN/OUTPUT	Input Low Level Voltage		V_{IL}			0.9	V		
17	IN/OUTPUT	Input High Level Voltage		V_{IH}	2.1			V		
18	IN/OUTPUT	Output Low Level Current		I_{OL}	8	15		µA	V_{OUT} = 0.5V	CE,
19	IN/OUTPUT	Output High Level Current		I_{OH}	5	−12		µA	V_{OUT} = 2.5V	HOLD IN/ACCESS
20	IN/OUTPUT	Input Force High Current (from V_{OL})		I_{FH}		55	100	µA	V_{IN} = 2.5V	PAUSE OUT
21	IN/OUTPUT	Input Force Low Current (from V_{OH})		I_{FL}		−70	−100	µA	V_{IN} = 0.5V	

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

AC Electrical Characteristics

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS UNLESS NOTED V_{DD} = 3.0V, T_A = 25°C f_{CLK} = 3.579545 MHz
1	DYNAMIC	Output Rise Time	t_R		1.0		µs	DP, M_1
2		Output Fall Time	t_F		1.0		µs	C_L = 50pF
3		Maximum Clock Frequency	f_{CLK}	3.58			MHz	3.579545 MHz Crystal
4		Mark to Space Ratio (DP Output)	M/S		2:1			M/S = O/C (V_{SS})
5					3:2			M/S = V_{DD}
6		System Clock Frequency (Internal)			300		Hz	F01 = V_{SS}
7		Impulsing Rate = I/T			10		Hz	F01 = V_{SS}
8		Fast Test Impulsing Rate			932		Hz	F01 = V_{DD}
9		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE ↑ '1'
10		Input Capacitance	C_{in}		5.0		pF	Any Input

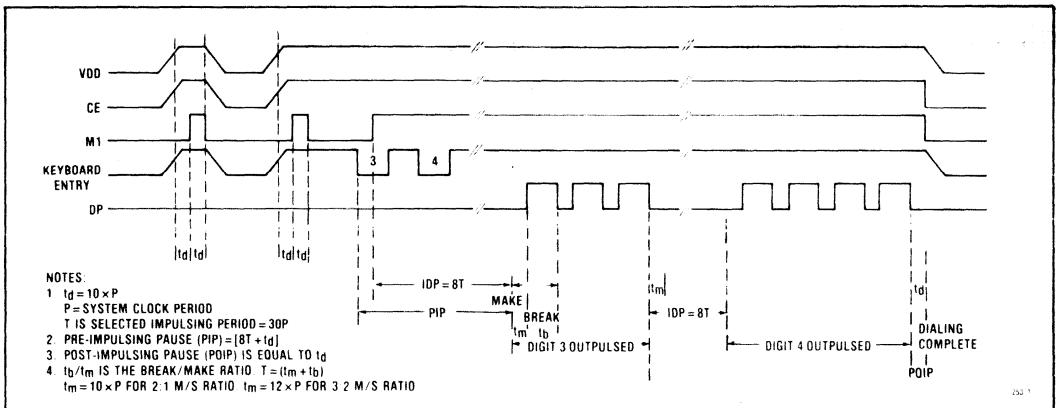


Fig. 2 MT4325 Programmable Keypad Pulse Dialer Timing Diagram
CE External Control

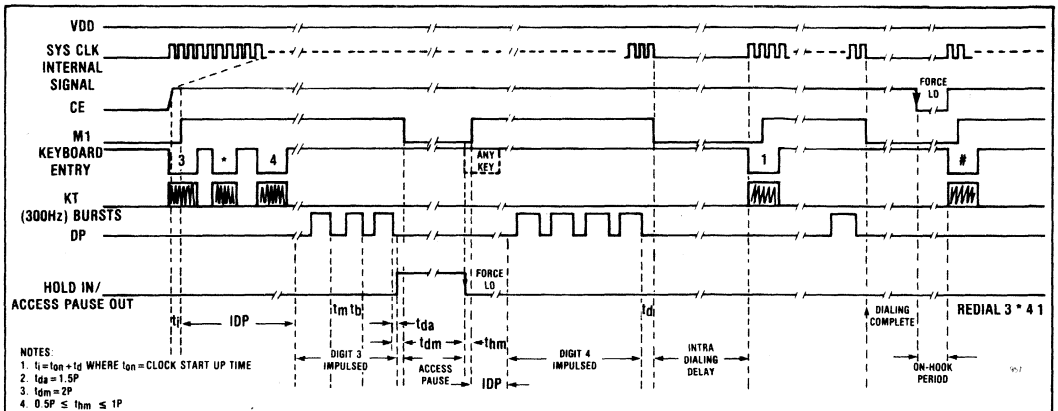


Fig. 3 MT4325 Programmable Keypad Pulse Dialer Timing Diagram
CE Internal Control

TABLE 1

PIN FUNCTION	DESCRIPTION				
V_{DD}	Positive voltage supply				
DP	Dial Pulsing Output Buffer				
M1	Mute Output Buffer				
M/S	Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}. Note: O/C = Open Circuit			O/C	2:1
				V_{DD}	3:2
F01	Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}. * Assumes f_{CLK} = 3.579545MHz.	F01	Nominal Impulsing Rate	Actual* Inpulsing Rate	System Clock frequency
		O/C	10Hz	10.13Hz	303.9Hz
		V_{DD}	932Hz	932.17Hz	27,965.1Hz
CE	Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.				
XTAL IN	Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.				
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.				
V_{SS}	System ground				
X_1,X_2,X_3	Column keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
Y_1,Y_2,Y_3,Y_4	Row keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
HOLD IN/	INPUT/OUTPUT	O/C	Normal Operation		
ACCESS	INPUT	V_{DD}	No impulsing. If activated during impulsing, hold occurs when the current digit is complete.		
PAUSE OUT	OUTPUT	V_{DD}	Logic "1" level output indicates access pause condition.		
KT	300Hz	Square wave bursts indicate valid keypad input.			

TABLE 2 KEYPAD INPUT CODE

No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
# RE-DIAL		1	1	1	0	1	1	0
* ACCESS PAUSE		1	1	1	0	0	1	1

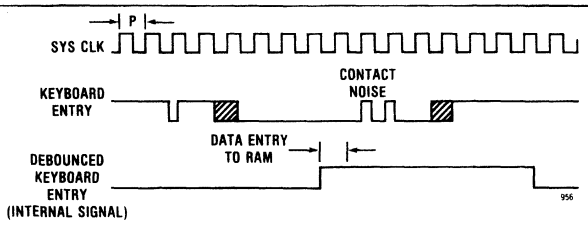


Fig. 4 Keypad Input Debounce Timing Diagram

Functional Description

The Mitel MT4325 programmable keypad pulse dialer is optimized for use in key-operated pulse dialing telephone sets and contains features which make it particularly suitable for applications where redial of last number dialed and repertory dial facilities are required.

The MT4325 accepts keypad information directly from a dual contact keypad having two single pole switches per key; one switch common to the column and one switch common to the row. The common row contacts are connected Y1 to Y4 and the common column contacts connected X1 to X3. The other side of each switch is connected to a common VSS line. The keypad code is shown in Table 2.

The MT4325 will accept up to 20 digits and access pauses; e.g., 18 digits plus 2 access pauses or alternately 19 digits plus 1 access pause. Prior to a keypad input being accepted contact bounce is eliminated by a circuit which ensures that any input which is valid for less than 10 ms is rejected and any input valid for greater than 17 ms is accepted as a valid key input. This circuit operates similarly on the trailing edge of a valid key input preventing multiple digit recognition in the presence of noise. Debounce operation is shown in Fig. 4.

The first key entered in any dialing sequence initiates the oscillator on the MT4325 by internally taking CE high. The oscillator signal is divided down to the System Clock (SYS CLK) frequency by a programmable pre-divide circuit. This internal SYS CLK signal is used for all input and output timing. Digits may be entered asynchronously from the keypad. Dialing and mute functions are output as shown in Fig. 2 and Fig. 3. Fig. 2 shows use of the MT4325 with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialer circuit. In this mode the pulse occurring on M1 when CE is taken high with no keypad input can be used to initiate the bistable latching relay.

Fig. 3 shows the timing diagram of the MT4325 including access pause and redial mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously and dialing commences after recognition of the leading edge of the first valid key input. When an access pause is reached M1 goes low and Hold In/Access Pause Out goes high, indicating the device is in an access pause. This output signal can be used to enable an external dial tone recognition circuit. Exit from the access pause is achieved by one of two methods. One method is by the next valid key operation. If a valid digit is entered, the digit will be entered in the next consecutive storage location in the digit memory. If the key # is activated, redialing of the number in memory will occur only if the device is in the redial mode. The alternative method to exit from an access pause is to pulse Hold In/Access Pause Out low resetting the output latch associated with this input/output pin.

Fig. 3 shows a pause in dialing between the completion of dialing digit "4" and keying digit "1". In this condition, the oscillator powers down to minimize power consumption and interfering signals, whilst CE remains high. On recognition of the next digit, the digit is entered in the next consecutive memory location and dialing resumes.

The end of a key entry sequence is indicated to the MT4325 by externally pulsing or clamping CE low. This causes the on chip latch holding CE high to reset.

If the first key entered after a CE low period is #, redial of the last number dialed will occur. Access pause operation is as previously described. In the standby condition, the MT4325 dissipates typically less than 1.5 μW.

Applications

Keypad Pulse Dialing Telephone With Redial Capability

The MT4325 provides all of the signals required to implement a keypad pulse dialing telephone. The circuit in Figure 5 shows how the MT4325 is interfaced to the telephone line and 500 type network to provide the following capabilities:

(1) Operation independant of TIP to RING D.C. polarity.
(2) High voltage transient protection.
(3) Present a minimum A.C. impedence of 270K ohm during dialing break periods.
(4) Operation on line impedences up to 1275 ohm driving into 150 ohm D.C. load from 900 ohm source impedence.
(5) Power-on-reset.
(6) On-hook memory retention of last number dialed (for redial).
(7) Draw less than 5µA on-hook.
(8) Insensitivity to keypad depressions on-hook.
(9) Insensitivity to hook switch bounce or sequencing.

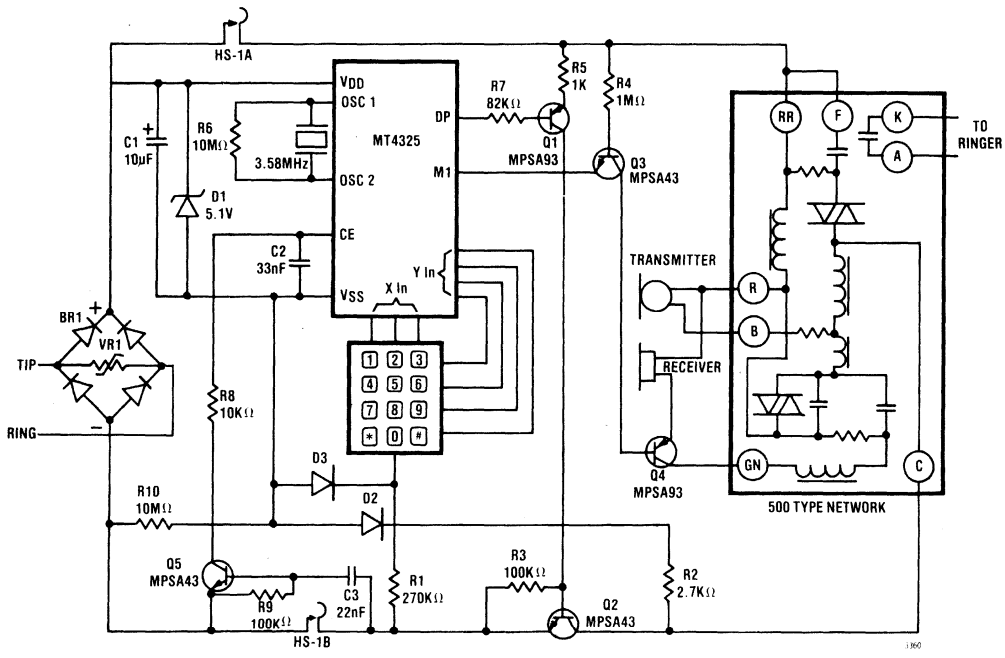


Fig. 5 MT4325 Based Pulse Dialing Telephone Circuit

Protection against TIP to RING polarity reversal and voltage transients is provided by diode bridge BR1 and varistor VR1 respectively, and aided by diode D1 and capacitor C1.

When DP is low, transistor Q1 is turned on, providing base current to Q2. In this condition, loop current flows from BR1 + , through the speech network and Q2 to BR1 − . During outpulsing, a high level at the DP output turns Q1 off, removing base drive from Q2 which in turn blocks the loop current. Muting is provided by transistor Q4 which presents a high impedance in series with the receiver whenever M1 (or M2) is high.

In the loop condition (Q2 on), the supply current for the MT4325 flows from BR1 + , through the device and returns to BR1 − via D2, R2 and Q2. During a loop break (Q2 off), the supply current returns to BR1 − via R1 only. The value of this resistor ensures a high A.C. impedance during loop breaks. Capacitor C1 provides auxiliary supply curent during these periods. Diode D2 prevents the speech network and R2 from shorting the MT4325 supply. Under the various conditions of loop state and line length, the V_{DD} to V_{SS} voltage is limited by zener diode D1 and smoothed by capacitor C1.

The redial function of the MT4325 is enabled by resetting the CE latch and activated by pressing the key #. The latch is reset by momentarily pulling the CE pin low. The circuit shown connected around HS-1B performs this function and is activated by opening the hook-switch. As HS-1B opens, capacitor C3 charges via the base-emitter junction of Q5. This base current pulse causes Q5 to turn on momentarily, pulling CE low. R8 is a current limiting resistor.

An alternative method of resetting the CE latch is simply to connect an auxiliary, normally open hook-switch in parallel with C2 in Figure 5. Under normal dialing conditions, the switch is open and CE is allowed to function normally. When the phone is placed on-hook, this switch connects CE to V_{SS}, resetting the latch.

In the on-hook condition, memory retention of the last number dialed is assured by supplying power to the MT4325 via the 10 Mohm resistor R10. In this condition, the keypad is disabled by D3 which is reverse biased.

Bistable Relay Telephone Connection

In applications where no semiconductor components are allowed in the telephone loop during normal speech, a bistable relay may be used as shown in Figure 6 to isolate the MT4325 and associated devices. A keyboard common changeover switch is required to short circuit the telephone network during keying of the first digit. The positive transition of M1 pulses the bistable relay to ensure that the network is short cirulted for the remainder of the dialing period. When dialing is complete, the bistable relay is pulsed again, connecting the telephone network back into the loop and short circuiting the MT4325 via the keyboard common switch.

If the bistable relay is set such that the MT4325 is connected into the loop when the handset is lifted, a pulse on M1 resets the relay such that the network is reconnected. This pulse is a result of CE being pulled high by R10 in the absence of a keyboard input.

Impulsing is controlled by DP via transistors Q1 and Q2. Resistor R4 provides D.C. termination of the line during dialing to generate voltage for the MT4325 power supply.

The CE reset circuit connected around HS-1B is used to reset the on-chip latch should the hook-switch be flashed during dialing.

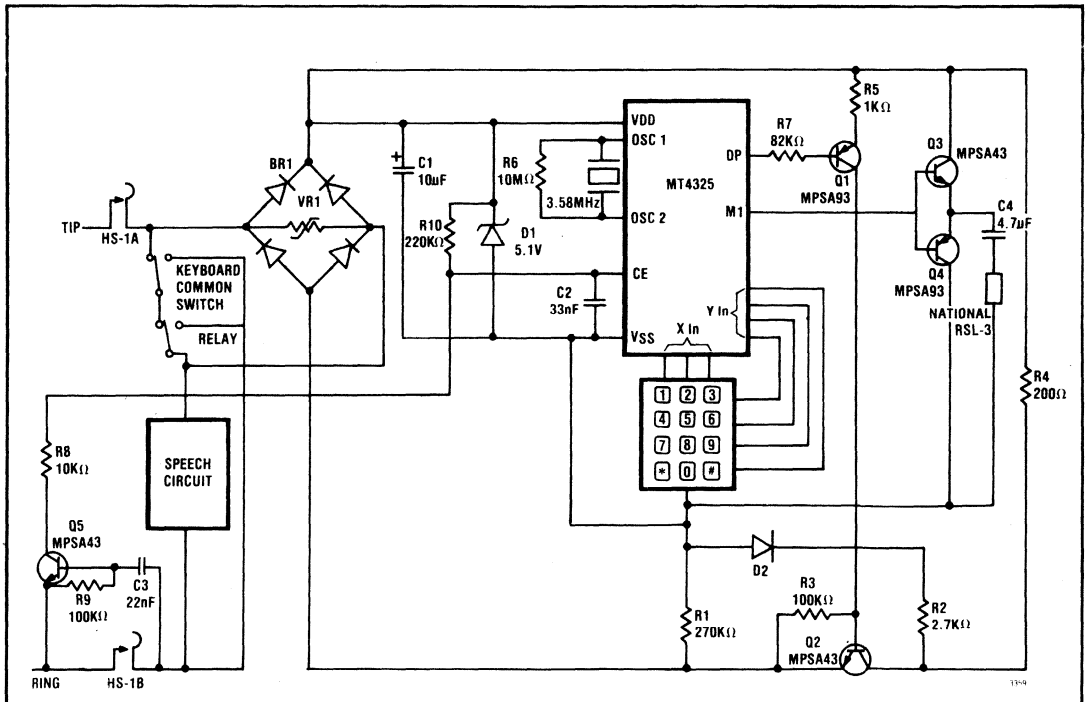


Fig. 6 Bistable Relay Telephone Connection

Single Contact Keyboard Interface

A single contact, matrix-type keyboard may be used with the MT4325 by the addition of the simple interface circuit shown in Figure 7. Depressing any key connects the on-chip pull-up transistor to the base of an external bipolar transistor. The corresponding row input (Y) is clamped to approximately 0.7V by the base-emitter junction of the external transistor. The pull-up transistor on this row input supplies base drive to the bipolar transistor whose collector, in turn, clamps the column input (X) to approximately 0.2V. With these levels on the row and column inputs, a valid keypad entry is obtained.

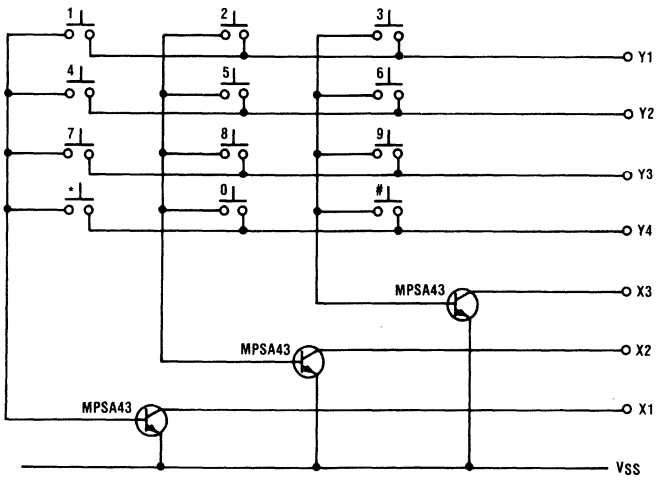


Fig. 7 Single Contact Keyboard Interface

Reset Delay Circuit

If a requirement exists such that the pulse dialer chip should not be reset for loop breaks less than 300ms in duration, then the circuit shown in Figure 8 should be used in place of the standard CE reset circuit. Resistor R2 is connected in series with the loop, with one end referenced to V_{DD} the positive supply of the MT4325. When loop current is flowing, sufficient foltage develops across R2 to turn Q1 on. Capacitor C1 charges to a voltage V_{DD}-V_{CESAT}. This voltage will be greater than the positive threshold of ST1, causing its output to go low and the output of ST2 to go high.

If a loop break occurs, Q1 turns off and C1 discharges via R1. The values of R1 and C1 are chosen such that the discharge time to the negative threshold of ST1 equals 300ms. As this threshold is crossed the output of ST2 goes low. This negative voltage transition is coupled by capacitor C2 and resets the CE latch. Diode D1 blocks positive voltage transitions that occur when loop current is initiated.

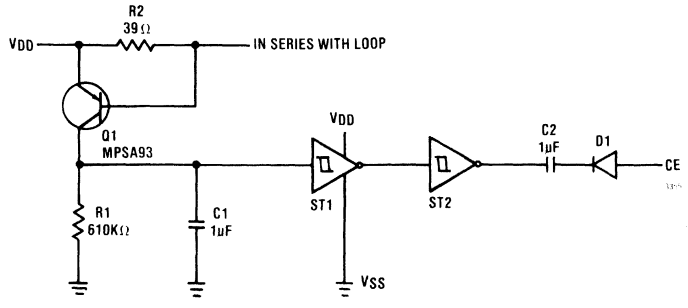


Fig. 8 CE Reset Delay Circuit

Automatic Access Pause Entry

The circuit shown in Figure 9 provides a method for loading access pauses automatically into the MT4325 memory. Upon recognition of the first valid key entry, M1 goes high and charges C1 via R1. When the voltage across C1 becomes greater than the positive threshold of schmitt trigger ST1, its output goes low and the output of ST2 goes high. If a pause in the dialing sequence occurs, (such as waiting for dial tone after the digit 9), then M1 goes low and C1 discharges via R1. When the negative threshold of ST1 is crossed, its output goes high, forcing the output of ST2 low. This negative voltage transistion is coupled via C2 to the keypad input X1 and Y4 causing an access pause to be loaded. The length of the dialing pause required to load an access pause is determined by the time constant R1C1.

When a number is redialed and an access pause state is entered, the Access Pause output goes high and M1 goes low. Transistor Q1 is used to buffer the Access Pause output and prevent loading of unwanted access pauses under these conditions. Diodes D1 and D2 provide isolation between the keypad inputs X1 and Y4.

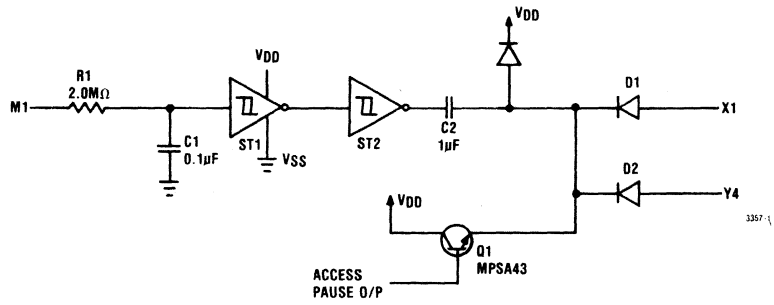


Fig. 9 Automatic Access Pause Entry

Automatic Access Pause Reset

Exiting from an access pause can be done by activating any valid key or alternatively by pulsing the Hold In/Access Pause Out pin low. The circuits of Figures 10 and 11 show two implementations of the latter technique.

In Figure 10, Hold In/Access Pause Out is used to enable a dial tone recognition circuit. This would normally consist of one or more bandpass filters, a level detector, and a pulse generating circuit. Once dial tone has been detected the output pulse is used to momentarily pull Hold-In/Access Pause Out low, resetting the on-chip latch and allowing dialing to continue.

The circuit of Figure 11 relies on the fact that M1 goes low when an access pause is entered. At the beginning of a dialing sequence, M1 goes high, charging C1 via D1. When the access pause is entered, M1 goes low and discharges C1 via R1. As the voltages across C1 drops below the negative threshold of ST1, its output goes high, forcing the output of ST2 low. This negative voltage transition pulls Hold-In/Access Pause Out low, allowing dialing to continue. Diode D2 prevents the output of ST2 from interrupting dialing by holding Hold In/Access Pause Out high whenever M1 is high.

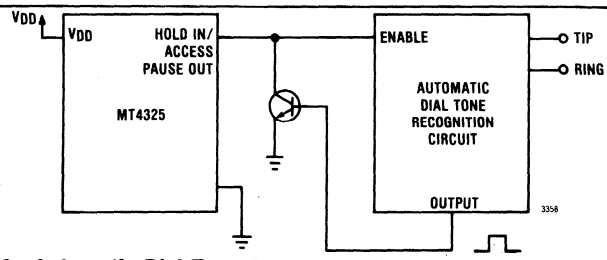


Fig. 10 Automatic Dial Tone Recognition for Access Pause Reset

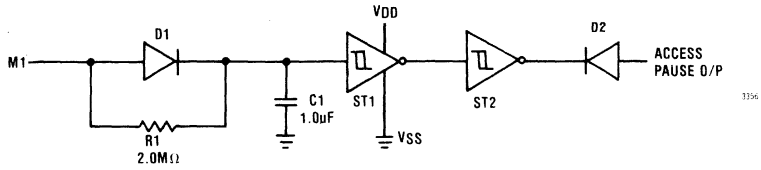


Fig. 11 Automatic Access Pause Reset

Tone to Pulse Converter

The MT4325 is ideally suited for use in various tone to pulse converter designs. A typical system is shown in the block diagram, Figure 12. The 20 digit on-chip, first in-first out memory serves as a buffer to allow asynchronous dialing into the converter and a tone dialing rate considerably faster than the nominal outpulsing rate (10 pulses per second with 800ms interdigit pause). All signals required to control the loop during outpulsing are provided by the MT4325.

The tone receiver portion of the converter is efficiently constructed with the MT8865 and MT8862, Mitel's 2-chip DTMF receiver. The output code of the MT8862 decoder is compatible with the input code of the MT4325 allowing direct interconnection of the two parts. (Q1 to Q4 of the MT8862 to Y1 to Y4 of the MT4325, and Q5 to Q7 of the MT8862 to X1 to X3 of the MT4325). A differential input stage interfaces the tone receiver to the telephone line. The steering output, STD from the tone receiver is fed into the control circuitry to control line splitting.

Off-hook detection, ringing voltage detection, and battery feed circuitry complete the converter, respectively providing signals for the timing circuitry and holding current during the line split condition.

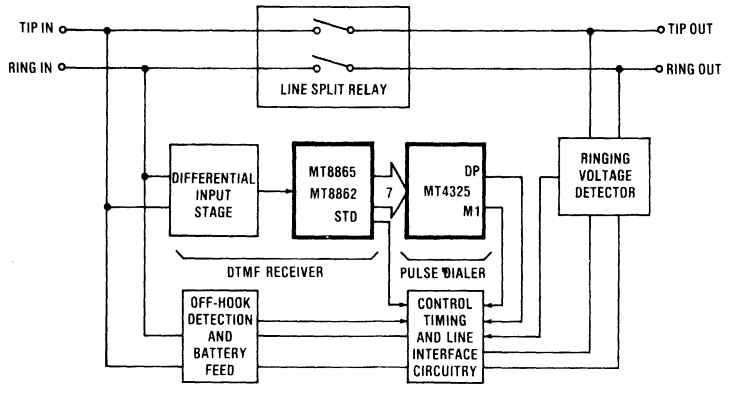


Fig. 12 Tone to Pulse Converter

Repertory Dialer

Figure 13 illustrates the use of the MT4325 in a keypad pulse dialing repertory dialer. The 20-digit on-chip memory of the MT4325 is useful as buffer storage to allow asynchronous loading of digits from the main telephone number memory. The main storage is provided by a 21C14, 24-word by 4-bit RAM. The 2-of-7 keyboard information is encoded to reduce the amount of RAM required. This information is then decoded by the MD74SC139 back to 2-of-7 format for the pulse dialer.

Three modes of operation (NORMAL, PROGRAM, and DIAL), are provided as selected by the MODE SWITCH. In the NORMAL mode, keypad data is fed directly to the MT4325 via the encode-decode loop. Dialing commences upon entry of the first digit.

When the PROGRAM mode is selected, the first two digits keyed in are interpreted as the telephone number address. These numbers are stored in BCD format to alleviate the need for a complex encoding scheme. As such, the capacity of the repertory dialer is limited to 48 16-digit numbers. Each subsequent digit entered, is stored in the main memory and causes the DIGIT ADDRESS COUNTER to be incremented. This is repeated until the entire number has been entered.

The DIAL mode is selected to dial a number from the main memory. Again the first two digits entered are interpreted as the telephone number address. In this mode, the second digit entered triggers the control circuitry to clock the DIGIT ADDRESS COUNTER, read the digits from the main memory, and load them into the buffer memory of the MT4325. These digits are immediately dialed out by the pulse dialer. Redialing of this number can be accomplished by returning to the NORMAL mode and activating the key "#". Access pauses, for use in PABX environments, are stored as any other digit. When an access pause is entered by the MT4325, the HOLD IN/ACCESS PAUSES OUT pin goes high. This signal is used by the control circuitry to interrupt loading of the digit stream until the access pause condition is reset. This prevents unwanted cancellation of the access pause by loading of subsequent digits.

The line interface and speech network control can be derived from the circuits shown in Figure 5. With selection of low power CMOS control circuitry, telephone line powering of the entire circuit becomes a possibility.

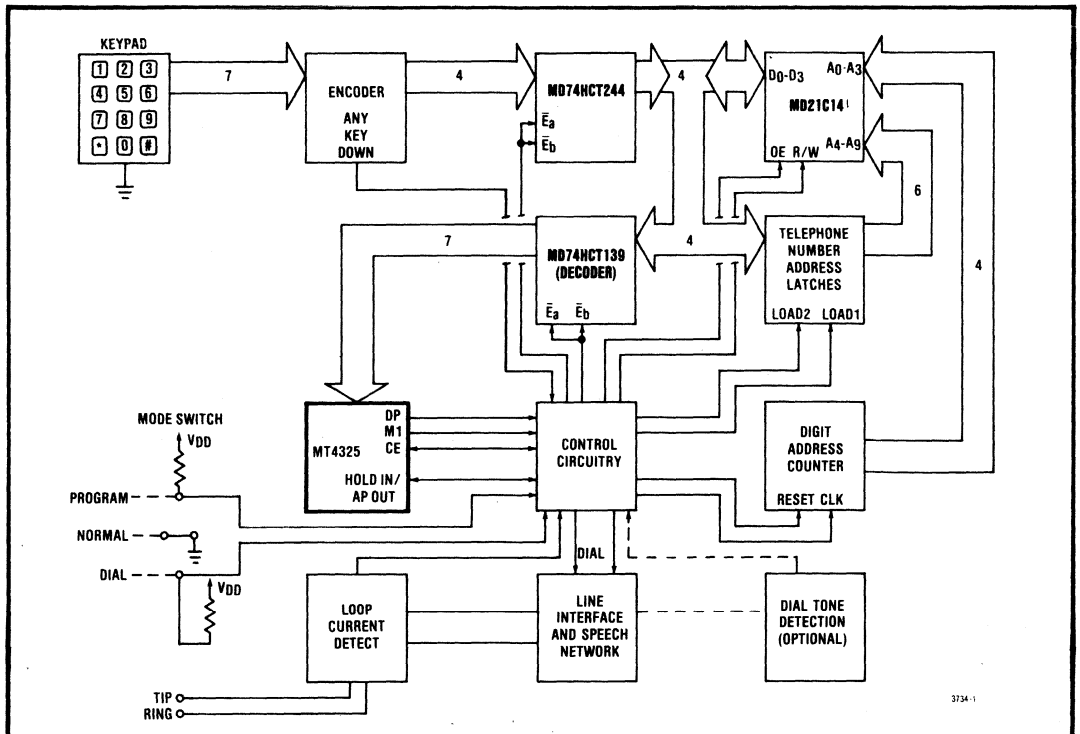


Fig. 13 Keypad Pulse Dialing Repertory Dialer

MITEL®

CMOS **MD4330B/MD4332B** 30/32 Segment LCD Driver

FEB. 1985

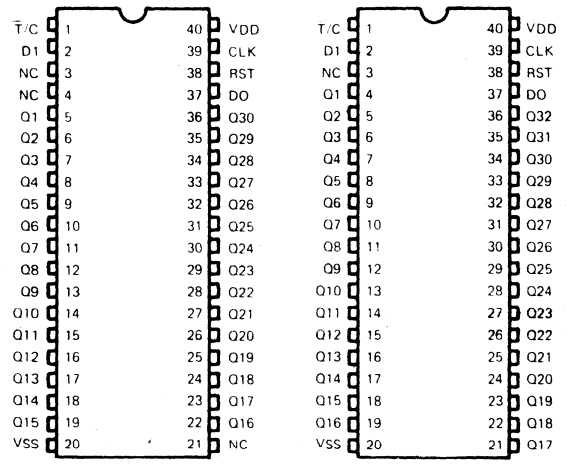
Features

- CMOS Low power
- 3 to 18 volt operation
- On-chip wave-shaping
- High-speed (typ. 3 MHz) shift register
- Std. 40-pin Dual-In-Line packages

Pin Names

- DI – Serial Data Input
- DO – Serial Data Output
- CLK – Clock (positive transition) Input
- RST – Master Reset (active HIGH) Input
- $\overline{T}/C$ – True/Complement (active LOW) Input
- Q1 thru Q32 – True/Complement Outputs

Pin Connections



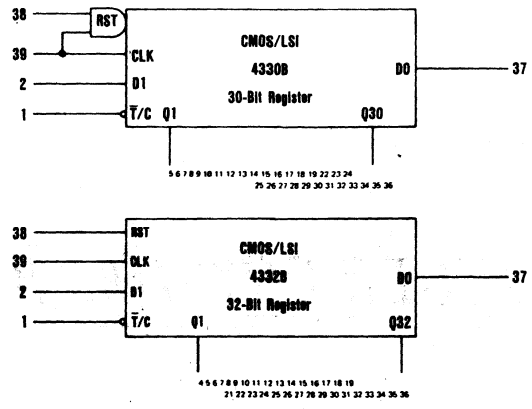
Ordering Information

MD4330BC	40-Pin Ceramic DIP
MD4330BE	40-Pin Epoxy DIP
MD4332BC	40-Pin Ceramic DIP
MD4332BE	40-Pin Epoxy DIP

Description

The MD4330B and 4332B are CMOS 30- and 32-bit static shift registers incorporating selectable true/complement outputs for each bit. These devices are well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. One of these devices can drive four 7-segment displays or two 14-segment alphanumeric displays plus decimal points or two 16-segment alphanumeric displays directly.

Logic Diagrams



V_{DD} – pin 40
V_{SS} – pin 20

Absolute Maximum Rating (Referenced to VSS)

Item	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	Vdc
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Ranges	TA	−40 to 85	°C
Storage Temperature Range	T_{STG}	−65 to 125	°C

Functional Description

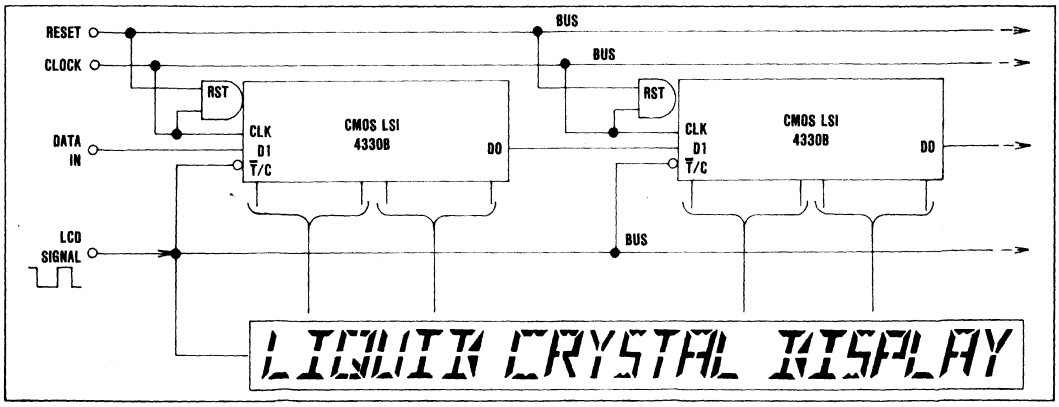
The 4330B and 4332B are CMOS/LSI static shift registers designed to drive all types of LCD readouts directly or as serial-to-parallel converters where both the true and complementary parallel outputs are available.

The circuits accept a serial input DI which is shifted into the register on the positive transition of the clock (CLK) input. A feature of these circuits is that the clock input and the true/complement control (T/C) input have wave-shaping circuits to ensure fast edges on-chip regardless of the shape of the incoming signals.

The 4330B type also has the reset (RST) input gated with the clock input for synchronous reset on the positive transition of the clock. The 4332B has asynchronous reset (RST) inputs which are active logic-level HIGH.

The parallel outputs of the shift registers are available in either true or complementary form dependent on the state of the true/complement control input. When input is logic-level LOW, the true form is available at all parallel outputs and when the input goes HIGH, the parallel outputs immediately revert to the complementary form of the data stored in each register. This action is independent of the clock input condition. A serial data (D_O) output is provided for applications using longer shift registers, etc. This output is the true form of the last stage of the register.

Application



D.C. Electrical Characteristics at $T_A = 25°C$

Characteristic		Symbol	Test Conditions	V_O Volts	V_{DD} Volts	Limits Min.	Limits Typ.	Limits Max.	Units
Quiescent Device Current		I_L			5	–	0.5	50	μA
					10	–	1	100	
Output Voltage	Low-Level	V_{OL}			5	–	0	0.01	V
					10	–	0	0.01	
	High-Level	V_{OH}			5	4.99	5	–	
					10	9.99	10	–	
Noise Immunity (Any Input)		V_{NL}		0.8	5	1.5	2.25	–	V
				1.0	10	3	4.5	–	
		V_{NH}		4.2	5	1.5	2.25	–	
				9.0	10	3	4.5	–	
Output Drive Current	D OUT	I_DN	N-Channel	0.5	5	0.8	1.7	–	mA
				0.5	10	1.0	3.0	–	
		I_DP	P-Channel	4.5	5	0.35	−0.9	–	
				9.5	10	−0.8	−1.9	–	
	Q OUT	I_DN	N-Channel	0.5	10	50	250	–	μA
		I_DN	P-Channel	9.5	10	−50	−250	–	
Input Current		I_I				–	10	–	pA

A.C. Electrical Characteristics at $T_A = 25°C$, $C_L = 50$ pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. All input rise and fall times = 20 ns.

Characteristic	Symbol	Test Conditions	V_{DD} Volts	Limits Min.	Limits Typ.	Limits Max.	Units
Propagation Delay Time	t_{PHL} t_{PLH}		10	–	300	–	ns
Transition Time	t_{THL}	D OUT (CL = 50 pF)	10	–	70	130	ns
	t_{TLH}	Q OUT (CL = 15 pF)	10	–	300	–	ns
Maximum Clock Frequency	f_{CL}		10	1.0	3.0	–	MHz
Minimum Clock Pulse Width	t_{WL} t_{WH}		10	–	200	–	ns
Minimum Reset Pulse Width	$t_{WH(R)}$		10	–	200	–	ns
Input Capacitance	C_I	Any Input		–	5	–	pF

CMOS **MT8804A**
8 × 4 Analog Switch Array

JAN. 1985

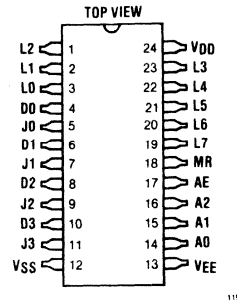
Features

- Microprocessor compatible control inputs
- On chip control memory and address decoding
- Row addressing
- Master reset
- 32 Crosspoint switches in 8 × 4 array
- 5.0 V to 15.0 V operation
- Low crosstalk between switches
- Low on resistance: 90Ω (typ.) at 13 V
- Matched switch characteristics
- Switches frequencies up to 40 MHz

Applications

- PABX and key systems
- Data acquisition systems
- Test equipment/instrumentation
- Analog/digital multiplexers

Pin Connections



Ordering Information

MT8804AE	24 Pin Plastic DIP	−40 °C to 85 °C
MT8804AC	24 Pin Cerdip DIP	−40 °C to 85 °C

Description

The 8804A is a CMOS/LSI 8 × 4 Analog Switch Array incorporating control memory (32-bits), decoder and digital logic-level convertors. This circuit has digitally controlled analog switches having very low "ON" resistance and very low "OFF" leakage current. Switches will operate with analog signals at frequencies to 40 MHz and up to 15.0 V p-p. A "HIGH" on the Master Reset input switches all channels "OFF" and clears the memory. This device is ideal for crosspoint switching applications.

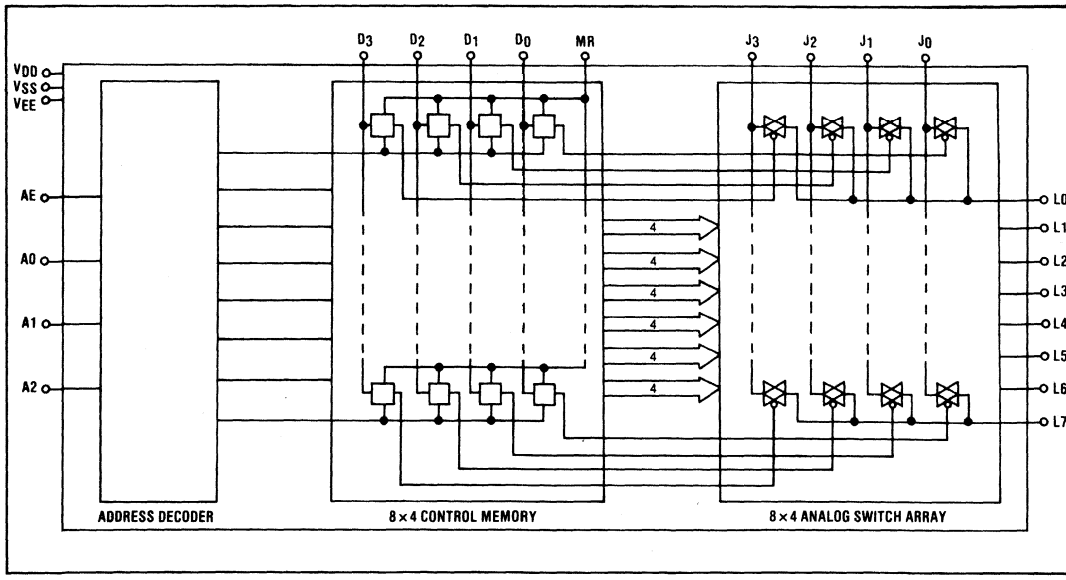


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings#

	MIN	MAX		MIN	MAX
V_{DD}-V_{SS}	−0.3 V	16 V	Storage Temperature	−65 °C	+125 °C
V_{DD}-V_{EE}	−0.3 V	16 V	(E Package)		
V_{SS}-V_{EE}	−0.3 V	16 V	Power Dissipation		1200 mW
Voltage on any logic pin	V_{SS}−0.3 V	V_{DD}+0.3 V	(C Package)*		
Voltage on any line or junctor	V_{EE}−0.3 V	V_{DD}+0.3 V	Power Dissipation (E Package)**		600 mW
Current at any logic pin		10 mA			
Operating Temperature (C/E Package)	−40 °C	+85 °C			
Storage Temperature (C Package)	−65 °C	+150 °C			

* Derate 16 mW/°C above 75 °C. All leads soldered to PC board.

** Derate 6.3 mW/°C above 25 °C. All leads soldered to PC board.

#Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics

	CHARACTERISTICS	SYMBOL	MIN	TYP[1]	MAX	UNITS	TEST CONDITIONS T_A = 25 °C, V_{SS} = V_{EE} = 0 V	
							V_{DD}	
1	Operating Voltage Range Digital Analog Logic Level Convertor	 V_{DD}-V_{SS} V_{DD}-V_{EE} V_{SS}-V_{EE}	 5 5 0	 5 10 5	 15 15 10	 V V V		
2	On State Resistance	R_{ON}	60	90 105 290	108 160 650	Ω Ω Ω	13 V 10 V 5 V	$V_{JUNCTOR}$-V_{LINE} = 0.6 V
3	Difference in On State Resistance Between Any Switches	R_{ON}		20 30		Ω Ω	13 V 10 V	
4	Off State Leakage Current (Any Line to Any Junctor)	I_{OFF}		±0.1	±500	nA	13 V	Selected Cross-point in Off State
5	Input Logic "0" Level	V_{IL}			3.0 1.5	V V	10 V 5 V	V_{is} = V_{DD} through 1 k
6	Input Logic "1" Level	V_{IH}	7.0 3.5			V V	10 V 5 V	V_{is} = V_{DD} through 1 k
7	Quiescent Device Current (Per Package)	I_Q		1.0	100	uA	15 V	
8	Maximum Current Through Crosspoint Switch	I_{MAX}			±8.0	mA	13 V	
9	Switch Input Capacitance	C_{is}		5		pF	10 V	V_{in} = 0 V
10	Switch Output Capacitance	C_{os}		20		pF	10 V	V_{in} = 0 V
11	Feedthrough Capacitance	C_{ios}		0.2		pF	10 V	V_{in} = 0 V
12	Digital Input Capacitance	C_{in}		5		pF	10 V	V_{in} = 0 V

Note 1: Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing.

AC Electrical Characteristics

CHARACTERISTICS		SYMBOL	MIN	TYP[1]	MAX	UNITS	TEST CONDITIONS $V_{SS}=V_{EE}=0$ V, $T_A=25°C$		
							V_{DD}	V_{is}	
1	Sine Wave Response (Distortion)			0.1 0.2 1.0		% % %	15 V 10 V 5 V	5 V (p-p)	$R_L=10\ k\Omega$ $f_{in}=1$ kHz
2	Frequency Response Channel "ON" (Sine Wave Input)			40		MHz	10 V	5 V (p-p)	$V_C=V_{DD}$ $R_L=1\ k\Omega$ $\left(\frac{V_o}{V_i}\right)_{dB}=-3$ dB
3	Feedthrough Channel "OFF"			−50		dB	10 V	5 V (p-p)	$V_C=V_{EE}$ $f_{in}=1$ MHz $R_L=1\ k\Omega$
4	Crosstalk Between Any Two Channels			−40 −90		dB dB	10 V 10 V		$f_{in}=1.0$ MHz $f_{in}=3.4$ kHz Switch A "ON" Switch B "OFF"
5	Propagation Delay Time Signal Input to Signal Output	t_{PS}		10		ns	10 V		Switch "ON" $C_L=50$ pF $t_r=t_f=5$ ns (input signal)
6	Turn "ON" Propagation Delay Data Input to Signal Output	t_{PLH} t_{PHL}		250 650	400 1000	ns ns	10 V 5 V		$C_L=50$ pF $R_L=10\ k\Omega$ $t_r=t_f=5$ ns (input signal)
7	Address Enable to Signal Output	t_{PAE}		200 650	300 900	ns ns	10 V 5 V		$C_L=50$ pF $R_L=10\ k\Omega$ $t_r=t_f=5$ ns
8	Address Enable Pulse Width	t_{AE}	100 250			ns ns	10 V 5 V		$t_r=t_f=5$ ns
9	Set Up Time — Address to AE	t_s	0 50			ns ns	10 V 5 V		$t_r=t_f=5$ ns
	Set Up Time — Data in to AE	t_s	150 200			ns ns	10 V 5 V		$t_r=t_f=5$ ns
10	Hold Time Address or Data In to Address Enable	t_h	120 300			ns ns	10 V 5 V		$t_r=t_f=5$ ns
11	Memory Reset Time	t_{MR}		250 500	400 600	ns ns	10 V 5 V		$C_L=50$ pF $R_L=1\ k\Omega$
12	Memory Reset Recovery Time	t_{MRR}		200 500	350 750	ns ns	10 V 5 V		$C_L=50$ pF $R_L=1\ k\Omega$

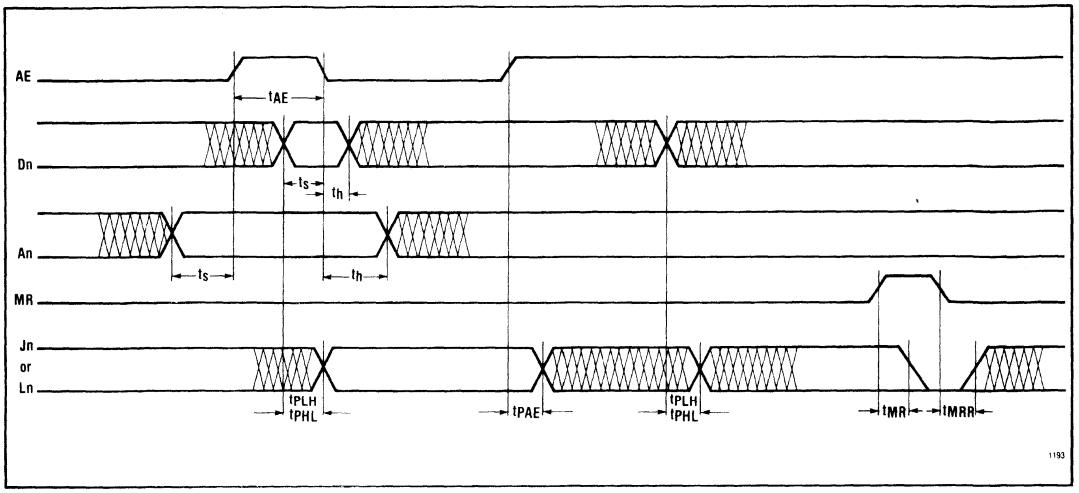


Fig. 2 Timing Waveforms

Pin Description

PIN	NAME	DESCRIPTION
1	L_2	Analog Switch Array Input/Output Line
2	L_1	Analog Switch Array Input/Output Line
3	L_0	Analog Switch Array Input/Output Line
4	D_0	Control Memory Data Line Input
5	J_0	Analog Switch Array Input/Output Junctor
6	D_1	Control Memory Data Line Input
7	J_1	Analog Switch Array Input/Output Junctor
8	D_2	Control Memory Data Line Input
9	J_2	Analog Switch Array Input/Output Junctor
10	D_3	Control Memory Data Line Input
11	J_3	Analog Switch Array Input/Output Junctor
12	V_{SS}	Negative Digital Power Supply
13	V_{EE}	Negative Analog Power Supply
14	A_0	Control Memory Address Input
15	A_1	Control Memory Address Input
16	A_2	Control Memory Address Input
17	AE	Control Memory Address Enable Input (Strobe)
18	MR	Master Reset
19	L_7	Analog Switch Array Input/Output Line
20	L_6	Analog Switch Array Input/Output Line
21	L_5	Analog Switch Array Input/Output Line
22	L_4	Analog Switch Array Input/Output Line
23	L_3	Analog Switch Array Input/Output Line
24	V_{DD}	Positive Analog/Digital Power Supply

Logic Table

MEMORY RESET	ADDRESS ENABLE	ADDRESS			ADDRESSED LINE	INPUT DATA TO CONTROL MEMORY				JUNCTORS CONNECTED TO ADDRESSED LINE			
	AE	A_2	A_1	A_0		D_3	D_2	D_1	D_0	J_3	J_2	J_1	J_0
H	X	X	X	X	All	X	X	X	X	All Switches "Off"			
L	L	X	X	X	None	X	X	X	X	No Change Of State			
L	H	L	L	L	L0	L	L	L	L	•	•	•	•
L	H	L	L	L	L0	L	L	L	H	•	•	•	+
L	H	L	L	L	L0	L	L	H	L	•	•	+	•
L	H	L	L	L	L0	L	L	H	H	•	•	+	+
L	H	L	L	L	L0	L	H	L	L	•	+	•	•
L	H	L	L	L	L0	L	H	L	H	•	+	•	+
L	H	L	L	L	L0	L	H	H	L	•	+	+	•
L	H	L	L	L	L0	L	H	H	H	•	+	+	+
L	H	L	L	L	L0	H	L	L	L	+	•	•	•
L	H	L	L	L	L0	H	L	L	H	+	•	•	+
L	H	L	L	L	L0	H	L	H	L	+	•	+	•
L	H	L	L	L	L0	H	L	H	H	+	•	+	+
L	H	L	L	L	L0	H	H	L	L	+	+	•	•
L	H	L	L	L	L0	H	H	L	H	+	+	•	+
L	H	L	L	L	L0	H	H	H	L	+	+	+	•
L	H	L	L	L	L0	H	H	H	H	+	+	+	+
L	H	L	L	H	L1	Each addressed line may have 16 different combinations of junctors connected to it by inputing data to the control memory as shown for LO.							
L	H	L	H	L	L2								
L	H	L	H	H	L3								
L	H	H	L	L	L4								
L	H	H	L	H	L5								
L	H	H	H	L	L6								
L	H	H	H	H	L7								

Notes: L - Low Logic Level
H - High Logic Level
X - Don't Care Condition
+ - Indicates Connection Between Junctor and Addressed Line
• - Indicates No Connection Between Junctor and Addressed Line

Functional Description

The MT8804A is a CMOS/LSI 8×4 ANALOG SWITCH ARRAY incorporating an 8×4 analog switch array, address decoder, control memory, and digital logic level convertor.

The analog switch array is arranged in 8 rows and 4 columns. The row input/outputs are referred to as LINES (L0-L7) and the column input/outputs as JUNCTORS (J0-J3). The crosspoint analog switches interconnect the lines and junctors when turned "ON" and provide a high degree of isolation when turned "OFF". Interchannel crosstalk is minimal despite the high density of the analog switch array. The control memory of the MT8804A can be treated as an 8 word by 4 bit random access memory. The 8 words are selected by the ADDRESS (A0-A2) inputs through the on chip address decoder. Data is presented to the memory via the 4 DATA inputs (D0-D3). This data is asynchronously written into the control memory whenever the ADDRESS ENABLE (AE) input is HIGH. A HIGH level written into a memory cell turns the corresponding crosspoint switch "ON" while a LOW level causes the crosspoint to turn "OFF".

Only the crosspoint switches corresponding to the addressed memory word are affected when data is written into the memory. The remaining switches retain their previous states. By establishing appropriate patterns in the control memory, any combination of lines and junctors may be interconnected. A HIGH level on the MASTER RESET (MR) input returns all memory locations to a LOW level and turns all crosspoint switches "OFF" effectively isolating the lines from the junctors. The digital logic level convertors allow the digital input levels to differ from limits of the analog levels switched through the array. For example, with $V_{DD} = 5$ V, $V_{SS} = 0$ V and $V_{EE} = -6$ V, the control inputs can be driven by a 5 V system while the analog voltages through the crosspoint switches can swing from +5 V to −6 V.

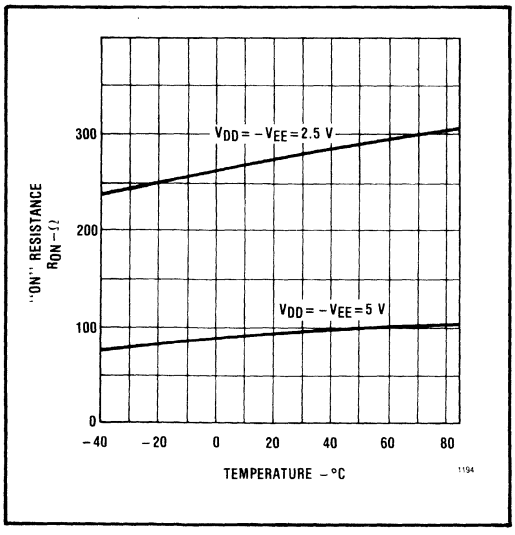


Fig. 3 On Resistance vs Temperature (Input Signal Voltage = Supply Voltage/2)

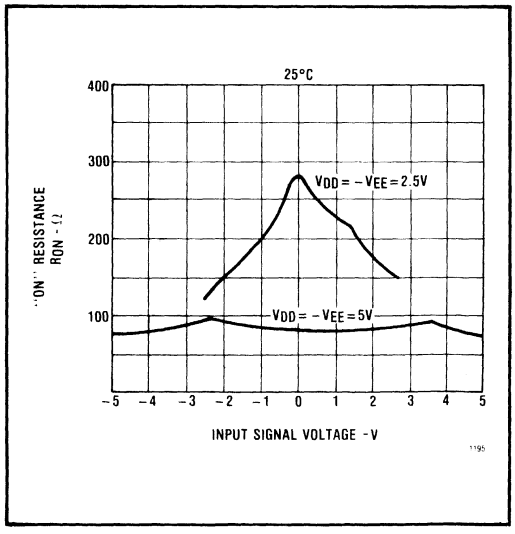


Fig. 4 On Resistance vs Input Signal Voltage

8 × 8 Analog/Digital Switch

Two MT8804A's configured as shown, implement an 8 × 8 analog/digital switch. The switch capacity can be expanded to an M × N array of inputs/outputs. Expansion in the M dimension is as shown with the MT8804A lines (L0 - L7) commoned. Expansion in the N dimension is accomplished by replicating the circuit shown and connecting the MT8804A junctors (J0 - J3) in common. The address and data control inputs of the MT8804A's can be connected in common for any size and switch provided that the address enable (AE) inputs are driven individually. A particular signal path is connected by setting up the appropriate signals or the address and data lines and taking the corresponding address enable input high. The master reset (MR), when taken high, disconnects all signal paths.

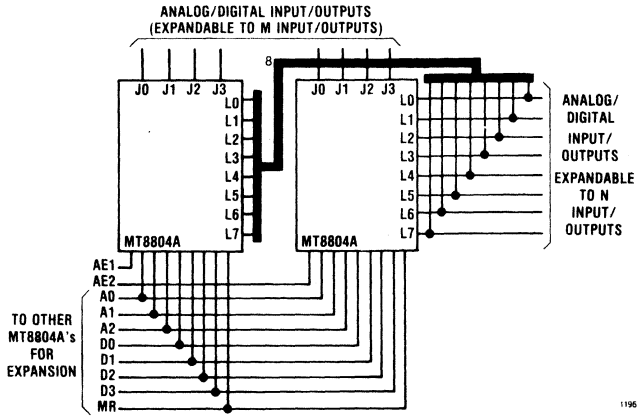


Fig. 5 8×8 Analog/Digital Switch

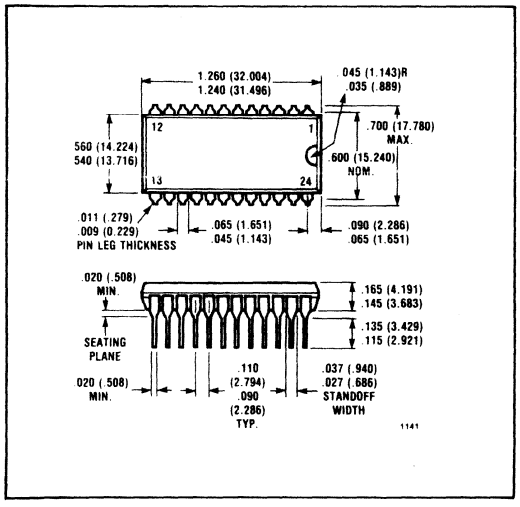


Fig. 6 24 Lead Dual/In-Line Package (Cerdip)

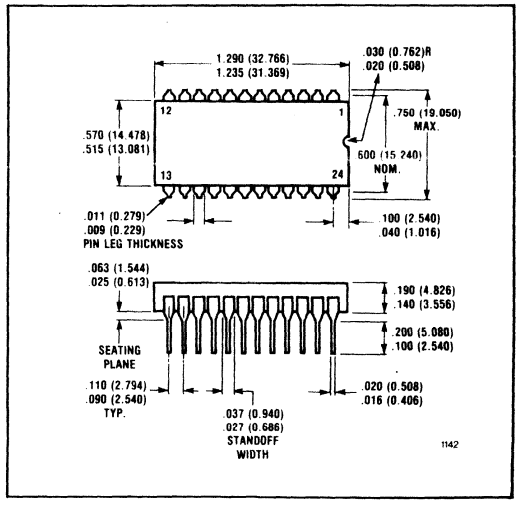


Fig. 7 24 Lead Dual/In-Line Package (Plastic)

ISO-CMOS **MT8812**
8X12 Analog Switch Array
Preliminary Information

9161-002-059-NA ISSUE 2 July 1986

Features

- Low ON resistance
- Internal control latches
- Large amplitude analog signal capacity
- Low distortion
- Typical -90 dB crosstalk at 1 KHz 2 Vpp
- Low power consumption ISO-CMOS technology

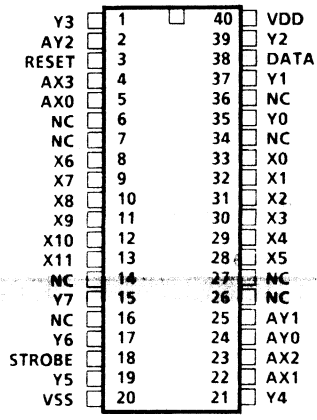
Applications

- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers

Description

The Mitel MT8812 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8X12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.

Pin Connections



Ordering Information

MT8812AC 40 Pin CERDIP
MT8812AE 40 Pin PLASTIC DIP
0° to 70° C

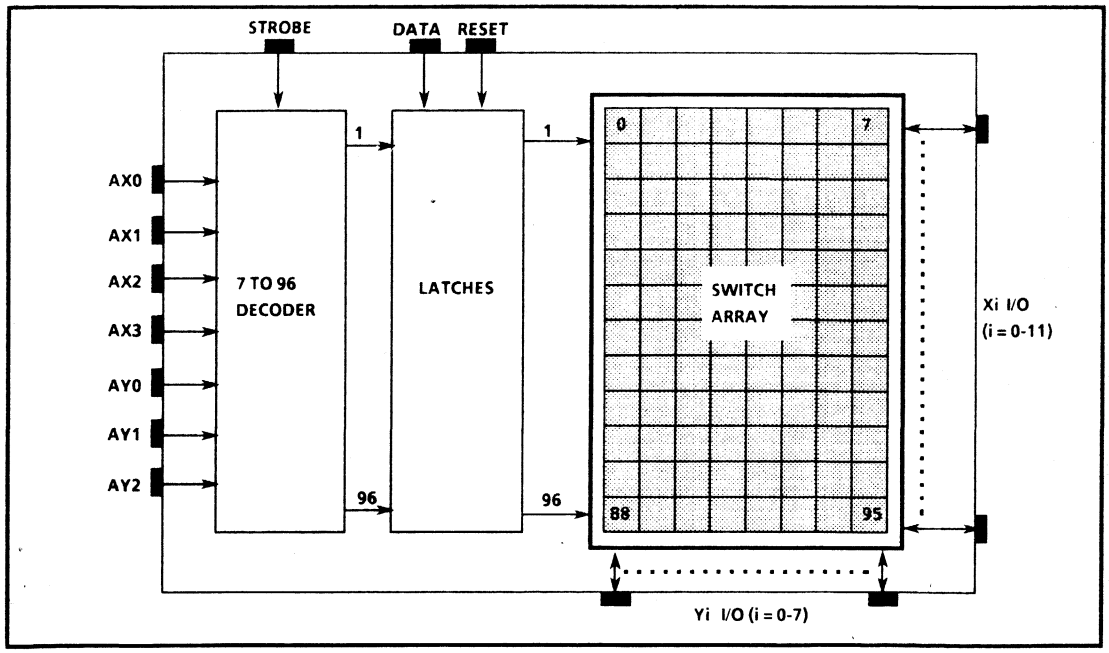


Figure 1- Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	16.0	V
2	Voltage on any I/O pin	V_I	V_{SS}-0.3	V_{DD} + 0.3	V
3	Current on any I/O pin	I_I		± 12	mA
4	Storage Temperature	T_S	-65	+ 150	°C
5	Power Dissipation PLASTIC DIP	P_D		0.6	W
	CERDIP	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating Temperature	T_O	0		70	°C	
2	Supply Voltage	V_{DD}	4.5		14.5	V	
3	Input Voltage	V_I	V_{SS}		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) and V_{DD} = 14V unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	µA	All Digital Inputs at V_{SS} = 0V or V_{DD} = 14V
				7	15	mA	All Digital Inputs at V_{IN} = 2.4V
2	On-state Resistance V_{DD} = 14V	R_{ON}		45	75	Ω	V_{DC} = V_{DD}/2, $\lvert V_X - V_Y \rvert$ = 0.4V
	V_{DD} = 10V			70	120	Ω	
	V_{DD} = 5V			130	200	Ω	
3	Difference in on-state resistance between 2 switches	ΔR_{ON}		10	14	Ω	V_{DD} = 14V, V_{DC} = V_{DD}/2 $\lvert V_X - V_Y \rvert$ = 0.4V
4	Off-state Leakage Current	I_{OFF}		1	± 500	nA	$\lvert V_X - V_Y \rvert$ = 14V
5	Max. Current through a Switch	I_{MAX}			± 10	mA	
6	Input Logic "0" level	V_{IL}			0.8	V	
7	Input Logic "1" level	V_{IH}	2.4			V	
8	Input Leakage Digital	I_{LEAK}		0.1	10	µA	All Digital Inputs at V_{SS} = 0V or V_{DD} = 14V

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) and V_{DD} = 14V unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch Input Capacitance	C_{IS}		5		pF	
2	Switch Output Capacitance	C_{OS}		20		pF	
3	Digital Input Capacitance	C_{DI}		5		pF	
4	Feedthrough Capacitance	C_F		0.2		pF	
5	Hold Time Data to Strobe	t_{DH}	20			ns	R_L = 1kΩ, C_L = 50pF
6	Set-up Time Data to Strobe	t_{DS}	20			ns	R_L = 1kΩ, C_L = 50pF
7	Set-up Time Address to Strobe	t_{AS}	20			ns	R_L = 1kΩ, C_L = 50pF
8	Hold Time Address to Strobe	t_{AH}	20			ns	R_L = 1kΩ, C_L = 50pF
9	Min. Strobe Pulse Width	t_{SPW}	40			ns	
10	Crosstalk between any 2 channels			-90		dB	f_{IN} = 1 kHz, V_{IN} = 2Vpp
11	Delay through switch	t_{PS}		10	40	ns	R_L = 1kΩ, C_L = 50 pF

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) and V_{DD} = 14V unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
12	Feedthrough Channel Off			-95		dB	All switches OFF, f_{IN} = 1 kHz, V_{IN} = 2Vpp
13	Frequency Response at -3dB			45		MHz	Channel is ON, Sinewave input, R_L = 1kΩ, V_{IN} = 2Vpp
14	Harmonic Distortion			0.05		%	R_L = 10kΩ, f_{IN} = 1kHz, V_{IN} = 2Vpp
15	Minimum Reset Pulse Width	t_{RPW}	200			ns	R_L = 1kΩ, C_L = 50pF
16	Strobe to Switch Status Delay	t_S		150	200	ns	R_L = 1kΩ, C_L = 50 pF
17	Data to Switch Status Delay	t_D		150	200	ns	R_L = 1kΩ, C_L = 50 pF
18	Reset to Switches Status Delay	t_R		150	200	ns	R_L = 1kΩ, C_L = 50 pF

† Timing is over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

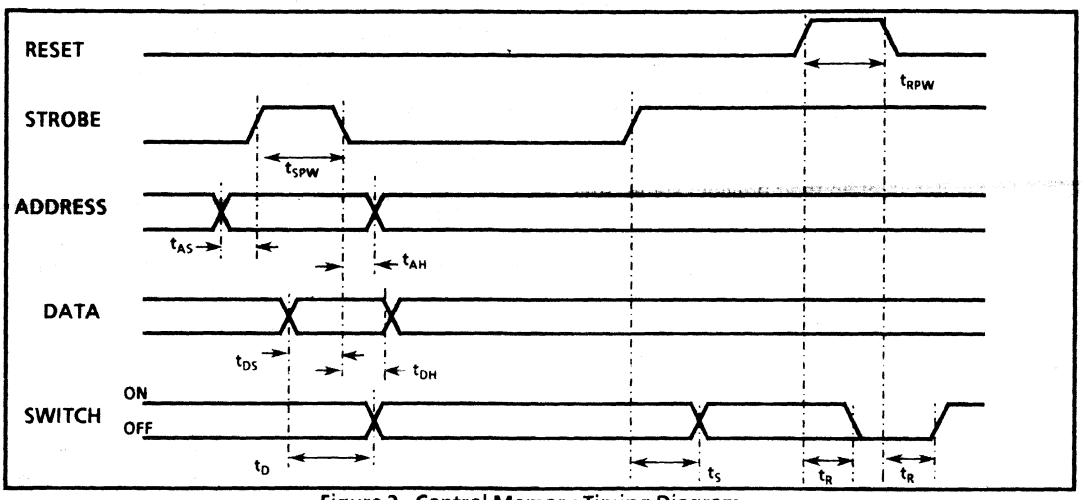


Figure 2 - Control Memory Timing Diagram

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection
1	1	1	0	0	0	0	No Connection
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection
1	1	1	1	0	0	0	No Connection
0	0	0	0	0	1	0	X0-Y2
1	0	1	1	1	1	1	X11-Y7

Figure 3 - Address Decode Truth Table

Functional Description

The MT8812 is an analog switch matrix with an array size of 8X12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y input/output lines and the rows are the X input/output lines. The crosspoint analog switch array will interconnect any X line with any Y line when turned ON and provide a high degree of isolation when turned OFF. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address input lines (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input line. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch ON and a logical "0" turns the crosspoint OFF. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y lines can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input line will asynchronously return all memory locations to logical "0" turning OFF all crosspoint switches.

Address Decode

The seven address lines along with the STROBE input are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data lines are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn ON and OFF in accordance with the data. Data must be stable on the falling edge of STROBE in order for correct data to be written to the latch. The STROBE input incorporates a small amount of delay allowing the STROBE input to rise at the same time as the address lines.

Applications

The MT8812 is shown in Figure 4 as a switching matrix for a typical key system. The system shown below allows connection of outside Central Office telephone lines to inside extension telephones.

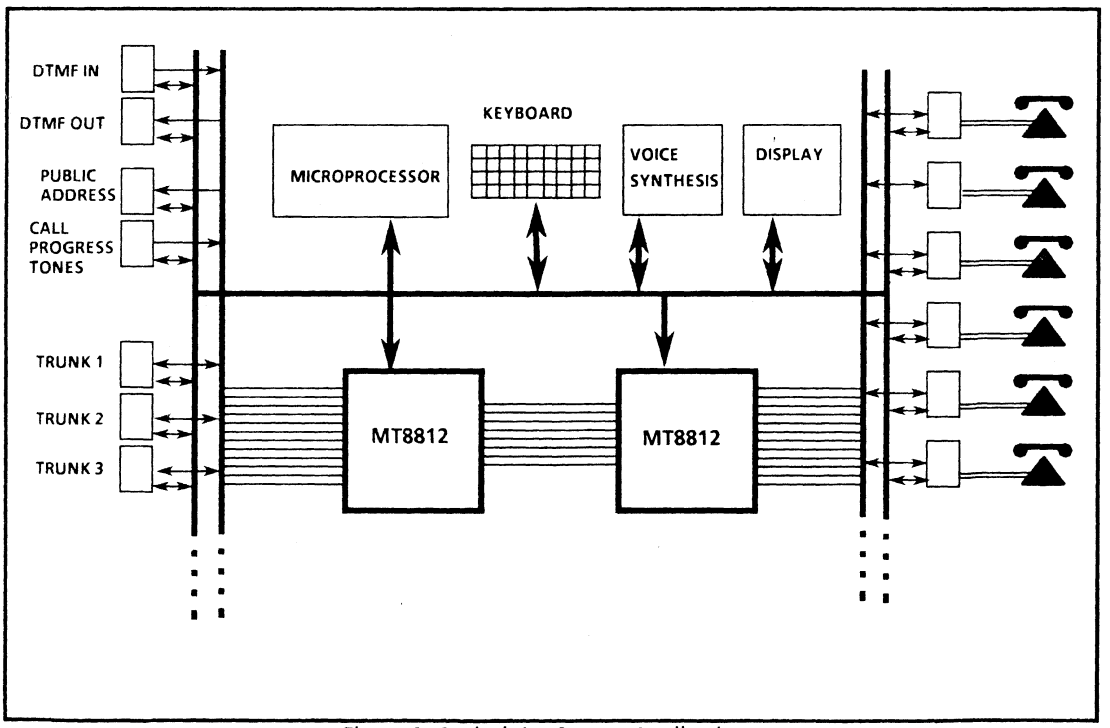


Figure 4 - Typical Key System Application

MH88305
Hybrid DTMF Receiver System

FEB 1985

Features

- Up to 55 dB Dynamic Range
- AGC for precise twist adjustment
- No external components needed
- Direct connection to telephone line
- Exceptional talk off
- 14 dB acceptable signal to noise ratio
- Acquisition time adjustable down to 10 ms
- Major parameters externally adjustable
- 5 V and 8 V to 12 V operation
- Replacement for MH88205

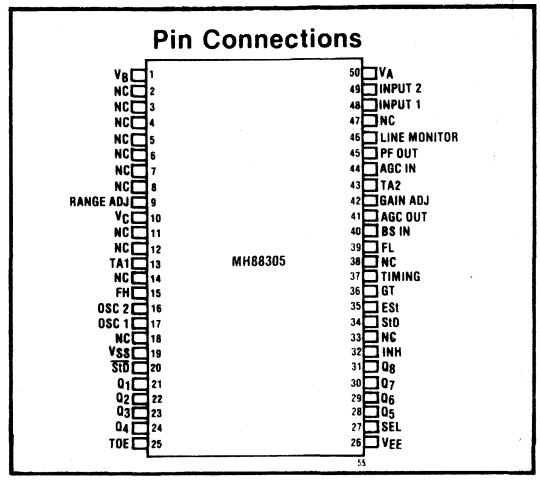
Applications

- End to end signalling
- Control systems
- Mobile radio
- Central office
- PABX
- Key systems

Description

The Mitel MH88305 Hybrid TOUCH-TONE® Receiver is a high performance, high quality unit, packaged in a dual-in-line hybrid measuring only 2.5″ × 1.5″ × 0.25″, and requires no external components for normal operation. The unit features exceptional dynamic range and precise twist performance, both adjustable to meet the exacting demands of end to end signaling applications as well as providing a unit of excellent central office quality.

Pin Connections



The MH88305 utilizes a digital detection algorithm incorporated in the MITEL CMOS/LSI MT8863 Digital Tone Decoder, which provides the unit with excellent talk-off immunity and signal to noise performance. Band split filtering is achieved using the Mitel ISO²-CMOS™ MT8865 DTMF filter.

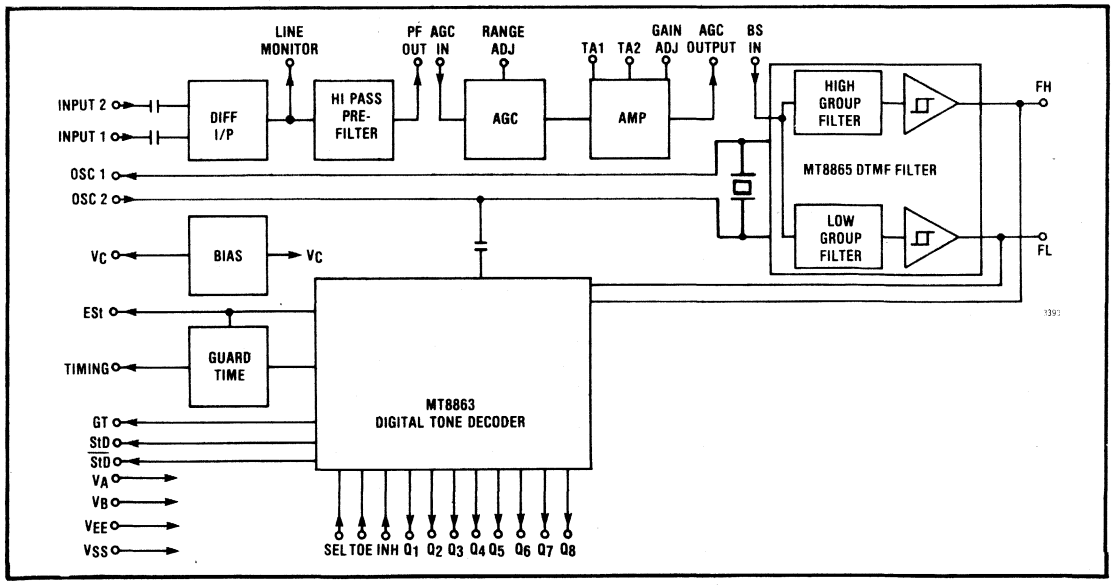


Fig. 1 Functional Block Diagram

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Absolute Maximum Ratings

PARAMETER			SYMBOL	MIN	MAX	UNIT
Supply voltage			V_A-V_{EE} V_A-V_B		15 15	V V
	$V_{SS} = V_{EE}$	5 V Operation	V_A-V_{SS}		5.5	V
Input Current on any logic pin			I_{IN}		10	mA
Voltage on any logic pin			V_{IN}	$V_{EE} - 0.3$	$V_A + 0.3$	V
Operating Temperature Range			T_A	−40	+85	°C
Storage Temperature Range			T_{STG}	−55	+100	°C

DC Electrical Characteristics (TA = 25 °C)

		CHARACTERISTIC		SYMBOL	$V_A = 5$ V MIN	TYP	MAX	$V_A = 12$ V MIN	TYP	MAX	UNITS	TEST CONDITIONS unless noted. See note 1 below.
1.	SUPPLY	Analog Operating Voltage		V_A-V_B	4.75					13	V	Ref to V_B
2.		Digital Operating Voltage		V_A-V_{EE}	4.75					13	V	
3.		Internal Logic Ground Voltage		V_A-V_{SS}	4.75		5.25	6.0	6.5	7.5	V	Ref. to V_{SS}
4.		Operating Supply Current		I_A		10			15		mA	
5.	LOGIC INPUTS	High Level Input Voltage		V_{IH}	3.5			8.5			V	
6.		Low Level Input Voltage		V_{IL}			1.5			3.5	V	
7.		Pull Down Sink Current (INH/SEL)		I_{SI}	10	25	75	10	200	400	μA	$V_{IH} = V_A$
8.		Pull Up Source Current (TOE)		I_{SO}	2	7	45	2	7	45	μA	$V_{IL} = V_{EE}$
9.		Input High Leakage Current		I_{IH}		.1	1.5		.1	1.5	μA	$V_{IH} = V_A$
10.		Input Low Leakage Current		I_{IL}		.1	1.5		.1	1.5	μA	$V_{IL} = V_{EE}$
11.	LOGIC OUTPUTS	Output Drive Current (Except StD)	Sink	I_{OL}	0.8	1.2		1	1.6		mA	Note 2
12.			Source	I_{OH}	0.4	0.6		0.5	0.8		mA	Note 3
13.		Tristate Output Leakage Current		I_{OZ}		0.1	1.5		0.3	1.5	μA	Note 4
14.		StD Output Sink Current		I_{OLS}	35.0			45			μA	$V_{OL} = .5$ V
15.		StD Output Source Current		I_{OHS}	35.0			45			μA	$V_{OH} = V_A - .5$ V
16.		High Level Output Voltage		V_{OH}	4.9			11.9			V	Outputs
17.		Low Level Output Voltage		V_{OL}			.1			.1	V	Open Circuit

Test Condition Notes:
1. $V_{EE} = V_B = 0$ V. All voltages referenced to V_{EE}
2. $V_{OL} = .4$ V ($V_A = 5$ V), $V_{OL} = .5$ V ($V_A = 12$ V)
3. $V_{OH} = 4.6$ V ($V_A = 5$ V), $V_{OH} = 11.5$ V ($V_A = 12$ V)
4. $V_{OH} = V_A$, $V_{OL} = V_{EE}$

A.C. Electrical and Timing Characteristics

CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS[1]
Maximum Valid Input Signal	V_A = 5 V	+3			dBm	V_A = 5 V
(Each tone of composite signal)	V_A = 12 V	+3			dBm	V_A = 12 V
Minimum Valid Input Signal	NORMAL	−26		−20	dBm	
(Each tone of composite signal)	EXTENDED	−46		−40	dBm	R_{RD} = 2kΩ. Note 5
Acceptable Signal to Noise Ratio		14			dB	Note 2
Maximum Twist Acceptance		+6	+9		dB	
Frequency Detect Bandwidth	Δf_A	+1.8		+3.5	%Nom	
Differential Input Impedance		360	400		kΩ	f = 1 kHz
DC Common Mode Tolerance		+200			V	
AC Common Mode Tolerance		70			Vrms	15-60 Hz
Dial Tone Tolerance		30			dB	Note 3
Tone Present Detection Time	t_{DP}	6		10	ms	
Tone Absent Detection Time	t_{DA}	0.6		6	ms	
Tone Present Guard Time	t_{GTP}		25		ms	Note 4
Tone Absent Guard Time	t_{GTA}		35		ms	Note 4
Minimum Tone Duration	t_{REC}			40	ms	Note 4
Maximum Invalid Tone Duration	$t_{\overline{REC}}$	20			ms	Note 4
Minimum Interdigit Pause	t_{ID}			40	ms	Note 4
Maximum Intradigit Dropout	t_{DO}	20			ms	Note 4
Data Valid to StD Delay	t_{PStD}	6		10	μs	

NOTES:
1. Unless otherwise noted: T_A = 25 °C; V_A = 5 V or 12 V; normal mode; no external adjustment.
2. Band-limited white noise, 300 Hz-3400 Hz. 50 ms on/50 ms off. Error rate < 1 in 10,000.
3. Relative to minimum valid input signal level (A).
4. No external guard-time components; V_A = 12 V.
5. No external twist adjustment. Typically up to a further 6 dB of sensitivity is available by insertion of R_{TI} (Fig. 10), see text.

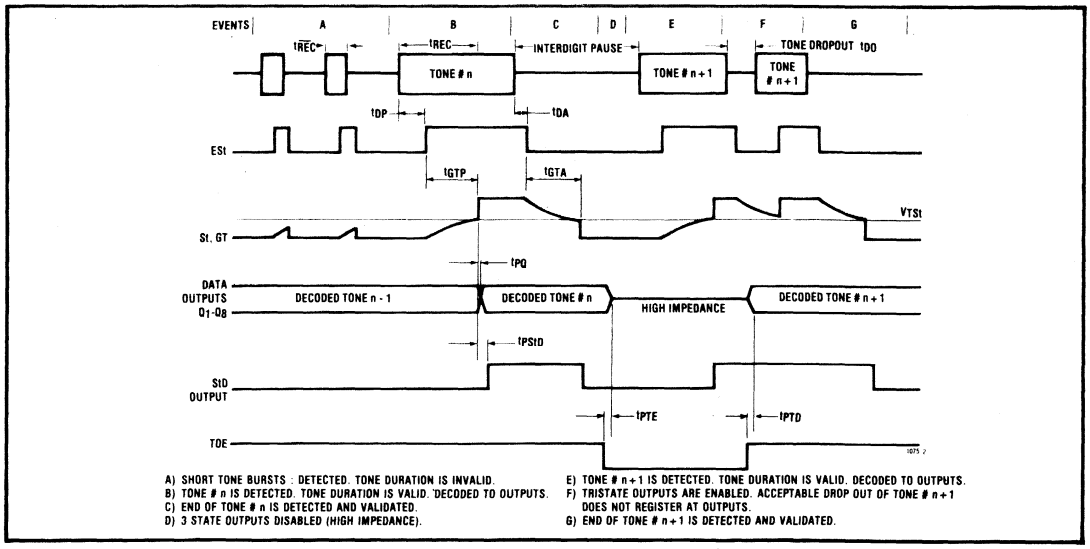


Fig. 2 Timing Diagram

Pin Description

PIN	NAME	DESCRIPTION
1	V_B	Negative Analog Power Supply.
9	RANGE ADJ	Resistor connected between Pin 9 and V_C (Pin 10) increases input sensitivity.
10	V_C	Internally derived reference voltage output.
13	TA1	Twist Adjust 1. Resistor connected between Pin 13 and TA2 (Pin 42) increases twist acceptance. See Figs. 9 and 10.
15	FH	Test Output of High Group Schmitt trigger.
16	OSC 2	Test Output of internal oscillator amplifier. 3.579545 MHz.
17	OSC 1	Test Input of internal oscillator amplifier.
19	V_{SS}	Internal Logic Ground for MT8863. Shorted to V_{EE} (Pin 26) for 5 V Logic Operation.
20	$\overline{StD}$	Buffered Inverted StD.
21 22 23 24	Q_1 Q_2 Q_3 Q_4	Data outputs 3-state buffered. Provides 4 bit binary word (SEL. LOW) or half of 2 of 8 binary word (SEL. HIGH), corresponding to the tone pair decoded, when enabled by TOE. See Table 1 for state table.
25	TOE	3-State Output Enable logic input. Active HIGH enables Q_1-Q_8 data output. When TOE = LOW; Q_1-Q_8 are high impedance.
26	V_{EE}	Negative Logic Power Supply. Logic ground for output signals.
27	SEL	Output Code Select logic input. HIGH on this input selects 2 of 8 code active HIGH on Q_1-Q_8. LOW selects two 4-bit codes on Q_1-Q_4 and Q_5-Q_8.
28 29 30 31	Q_5 Q_6 Q_7 Q_8	Date outputs 3-state buffered. Provides 4 bit binary word (SEL. LOW) or half of 2 of 8 binary word (SEL. HIGH), corresponding to the tone pair decoded, when enabled by TOE. See Table 1 for state table.
32	INH	Inhibit logic input. Active HIGH disables detection of A, B, C, D, *, #.
34	StD	Valid Tone Detect indication, logic output. Active HIGH.
35	ESt	Early Steering Digital Output. Active HIGH indicates digital detection of valid tone pair.
36	GT	Guard Time Output. Normally connected to (PIN 37), TIMING.
37	TIMING	Guard Time Adjust. A capacitor connected between Pin 37 and V_A (Pin 50) increases guard time. A resistor connected between Pin 37 and EST (Pin 35) decreases guard time.
39	FL	Test Output of Low Group Schmitt trigger.
40	BS IN	Analog input to the bandsplitting filters. Normally connected to AGC OUT (Pin 41).
41	AGC OUT	Analog output of the AGC circuit. Normally connected to BS IN (Pin 40).
42	GAIN ADJ	Adjusts signal level into MT8865. Shorted to TA2 (Pin 43) for 5 V analog operation.
43	TA2	Twist adjust 2. Resistor connected between Pin 43 and AGC output (Pin 41) decreases twist acceptance. See Figs. 9 and 10.
44	AGC IN	Analog input to the AGC circuit. Normally connected to PF OUT (Pin 45).
45	PF OUT	Analog output from Dial Tone Reject High pass filter. Normally connected to AGC IN (Pin 44).
46	LINE MONITOR	Single ended test output of the differential line input. Attenuated 6 dB referred to line input signal.
48 49	INPUT 1 INPUT 2	Differential line inputs AC coupled. Direct connection to telephone line.
50	V_A	Positive Power Supply.

N.B. All pins not referred to are not internally connected.

Functional Description

The MITEL hybrid DTMF tone receiver offers small size (2.5″ × 1.5″), exceptional signal detection performance, and high quality through the use of state of the art thick film and CMOS/LSI technology. No external components are needed and the unit can be directly connected to telephone lines. Digital outputs are CMOS and Low Power Schottky TTL compatible (2 loads). The unit is particularly suited to applications where high sensitivity, high twist, and detection in the presence of noise is required, such as end to end signaling, mobile radio, Central Office, PABX and other applications. For maximum flexibility all major functional blocks of the receiver are externally accessible, and the use of an external resistor provides adjustment of input sensitivity, twist accept/reject limits and guard-time decrement while the use of an external capacitor allows an increase of guard-time.

The MH88305 is designed to accept the standard DTMF frequencies as recommended by CCITT normally generated from a push-button TOUCH-TONE® telephone set. See Fig. 4.

The input signal is received on INPUT 1 and INPUT 2 which provide an AC-coupled balanced differential input impedance of approximately 400 kΩ. The signal is fed into a high-pass prefilter providing 60 db dial-tone rejection over the frequency range 0-480 Hz.The use of an AGC circuit provides the unit with up to 55 dB dynamic range, and the AGC output amp has provision for precise adjustment of twist.

The high- and low-frequency signals are separated by the MT8865 DTMF filter/limiter, the outputs of which are rectangular waves having the same frequency as the incoming high and low tones and appear at FH and FL respectively.

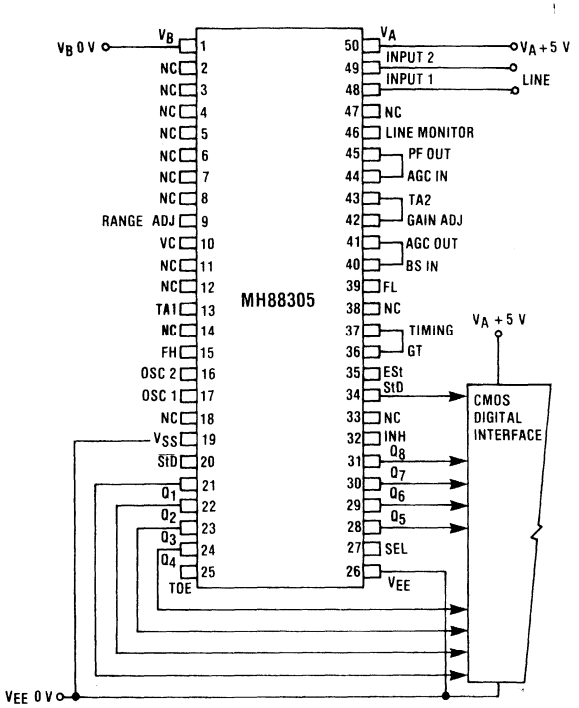
The MITEL MT8863 Digital Tone Decoder chip accepts FH and FL and performs a complex proprietary averaging algorithm empirically developed in a practical telecommunications environment. On valid detection of both the high and low tone the early steering output (ESt) goes HIGH. (Refer to Fig. 2.) This activates a simple analog guard-time circuit which operates on tone acquisition and release, preventing multiple digit recognition in the presence of impulse noise, or tone interruption less than the allowable tone drop-out time, t_{DO}. In the event of a tone drop-out or frequency error prior to elapse of the guard time (t_{GTP}), ESt goes low resetting the analog guard-time circuit and the digital detection algorithm is repeated.

The positive transition of StD indicates that the output latches Q_1-Q_8 have been updated. Three output formats are selectable via SEL, Pin 27. These formats are 2 of 8 active high and two 4-bit codes. The truth table is listed in Table 1. The data in the output latches will remain stable until the valid recognition of the subsequent tone pair. The delayed strobe signal (StD) is available on Pin 34 and this signal remains HIGH for the duration of the detected tone pair and goes low after the release guard time (t_{GTA}) has elapsed. Additionally, a 3-state output enable, TOE, (Pin 25) is provided to enable bussing of the data outputs.

The INH pin taken HIGH allows the user to inhibit the decode of tone pairs corresponding to the keypad designations, A, B, C, D, *, #, for security uses or for further reducing susceptibility to "talk-off".

TABLE 1 OUTPUT TRUTH TABLE

	SEL = H (2-of-8 Code)								SEL = L (Two 4-Bit Binary Codes)							
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
1	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L
2	H	L	L	L	L	H	L	L	L	H	L	L	L	H	L	L
3	H	L	L	L	L	L	H	L	H	H	L	L	L	L	H	L
4	L	H	L	L	H	L	L	L	L	L	H	L	L	L	L	H
5	L	H	L	L	L	H	L	L	H	L	H	L	L	H	L	H
6	L	H	L	L	L	L	H	L	L	H	H	L	L	L	H	H
7	L	L	H	L	H	L	L	L	H	H	H	L	H	L	L	L
8	L	L	H	L	L	H	L	L	L	L	L	H	H	H	L	L
9	L	L	H	L	L	L	H	L	H	L	L	H	H	L	H	L
0	L	L	L	H	L	H	L	L	L	H	L	H	L	H	H	L
*	L	L	L	H	H	L	L	L	H	H	L	H	H	L	H	H
#	L	L	L	H	L	L	H	L	L	L	H	H	H	L	L	H
A	H	L	L	L	L	L	L	H	H	L	H	H	H	H	H	L
B	L	H	L	L	L	L	L	H	L	H	H	H	H	H	L	H
C	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H
D	L	L	L	H	L	L	L	H	L	L	L	L	H	H	H	H



TYPICAL PERFORMANCE

DYNAMIC RANGE	27 dB
TWIST	± 9 dB
ACC. S/N RATIO	14 dB
T_{REC}	30 ms
MAX INVALID TONE DURATION	20 ms
MIN INTERDIGIT PAUSE	30 ms
MAX ACCEPTABLE DROPOUT	20 ms

Fig. 3 Typical Connection Diagram for 5V Operation

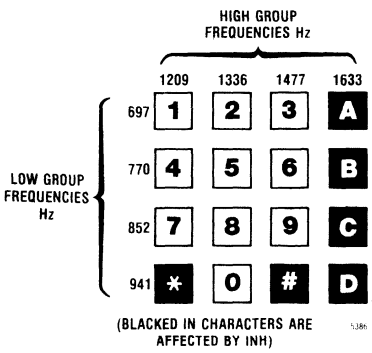


Fig. 4 DTMF Matrix Indicating Character Tone Pair Correspondence

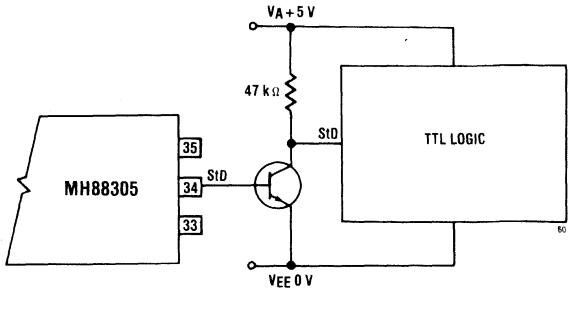


Fig. 5 Interfacing StD to TTL

Applications

The typical connection diagram, Fig. 3, illustrates the ease with which the MH88305 may be applied in a system, requiring no extra external components to perform the tone receiving and decoding function, and providing direct connection to 5 V CMOS Logic.

The outputs Q_1-Q_8, and $\overline{StD}$ are directly interfaceable to Low Power Schottky TTL if V_A and V_{EE} are connected to the TTL positive and common rails respectively. However, it is necessary to buffer StD as shown in Fig. 5. The StD output is current-limited to provide functional compatibility with MH88205.

A feature of the MH88305 is the flexibility to adjust tone recognition parameters by the use of single external components. The following parameters are adjustable:

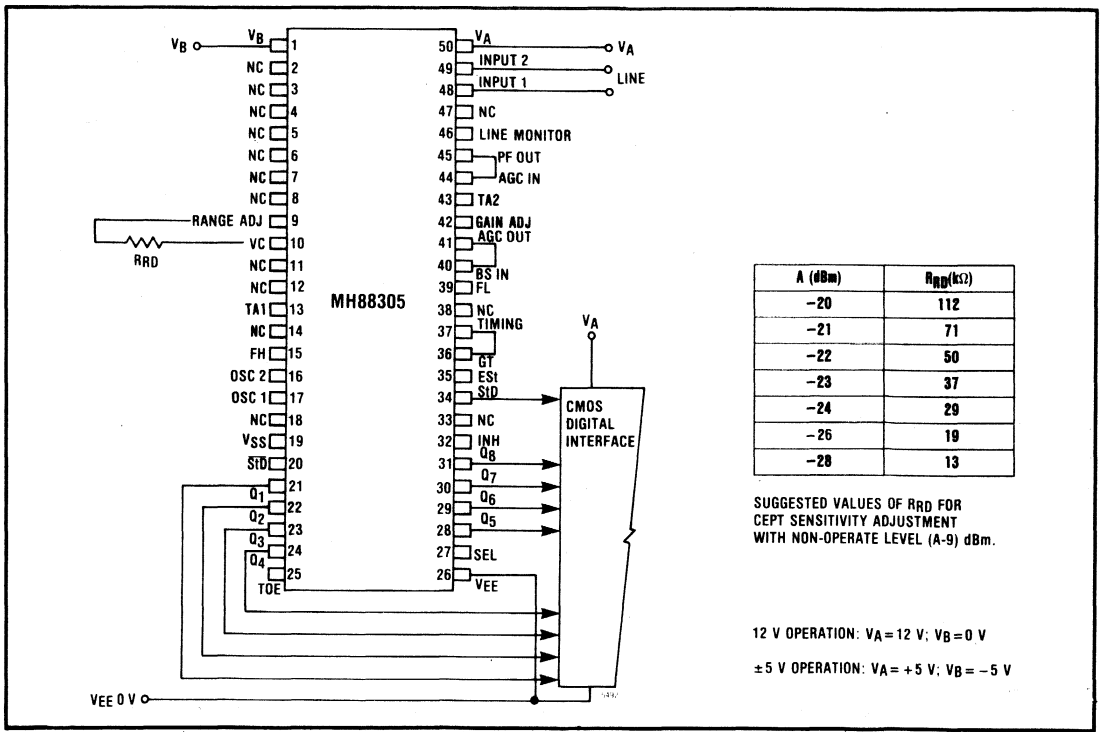
- input sensitivity
- guard time
- twist accept/reject limit.

The methods of increasing or decreasing each one of these parameters are shown in Figs. 7, 8, 9 and 10 respectively. Note that the minimum Valid Input Signal Levels as specified in the AC electrical characteristics and Fig. 7 apply when the input signal has no twist.

Adjustment to the twist acceptance level and minimum Valid Input Signal, may be performed as follows: Using Fig. 9 or 10, determine the twist adjust resistor value (R_T) giving the desired twist acceptance level. Subtract 9 dB from this twist acceptance level (in dB) and add this result to the desired minimum Valid Input Signal. With this adjusted Signal Level use Fig. 7 to determine the range adjust resistor value (R_R) and connection configuration.

Example: V_A = +5 V V_{EE} = V_B = 0
Required Twist Acceptance Level = 18 dB
Required Valid Input Signal Level = −35 dBm
Fig. 9, Twist Increment, gives R_{TI} = 70 kΩ
Adjusted Signal Level = (18-9) dB +(−35) dBm = −26 dBm
Fig. 7 Valid Input Signal Level Decrement gives R_{RD} = 25 kΩ .

To change the minimum Valid Input Signal Level, with a twist level unchanged from the typical value of 9 dB, use Fig. 7 to determine the required range adjust resistor value (R_R) and connection configuration.



A (dBm)	R_{RD}(kΩ)
−20	112
−21	71
−22	50
−23	37
−24	29
−26	19
−28	13

SUGGESTED VALUES OF R_{RD} FOR CEPT SENSITIVITY ADJUSTMENT WITH NON-OPERATE LEVEL (A-9) dBm.

12 V OPERATION: V_A = 12 V; V_B = 0 V

±5 V OPERATION: V_A = +5 V; V_B = −5 V

Fig. 6 Typical Connection Diagram for 12 V or ±5 V Operation

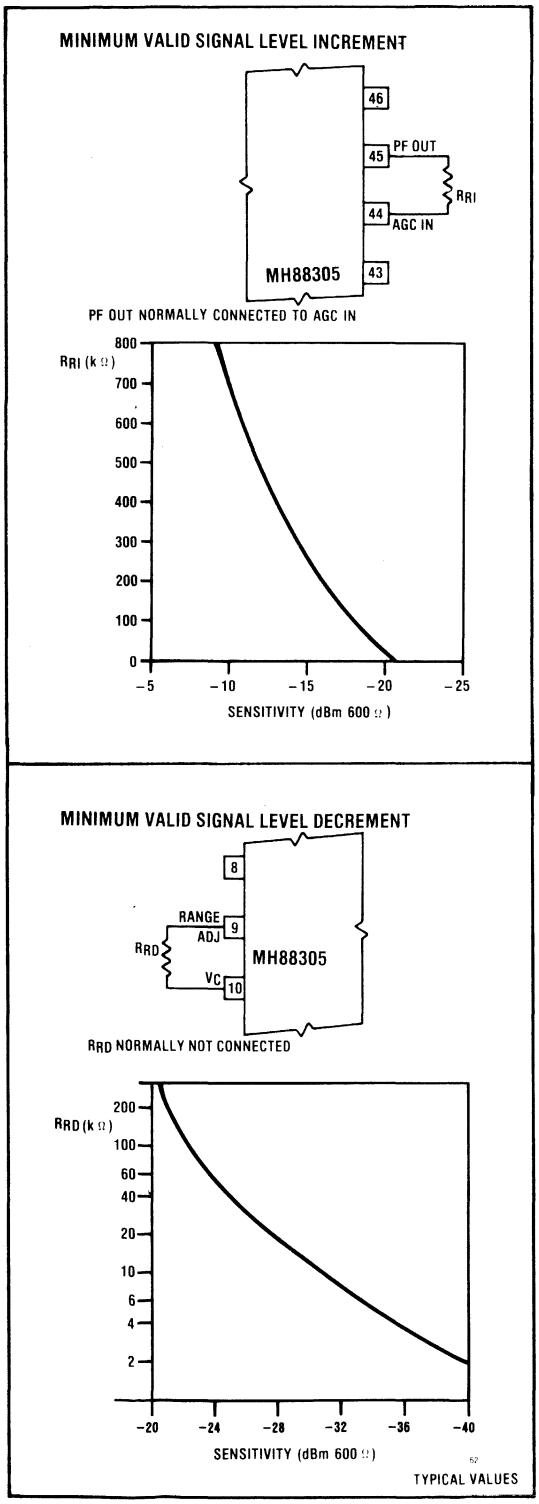


Fig. 7 Input Sensitivity Adjustment

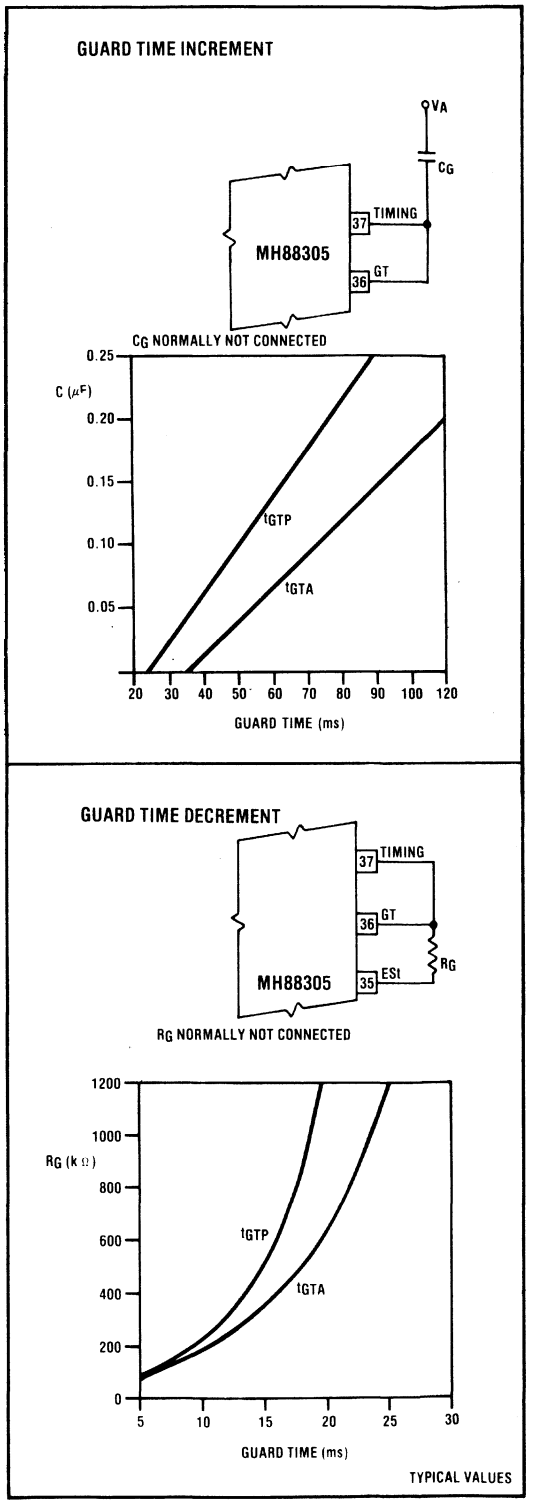


Fig. 8 Guard Time Adjustment

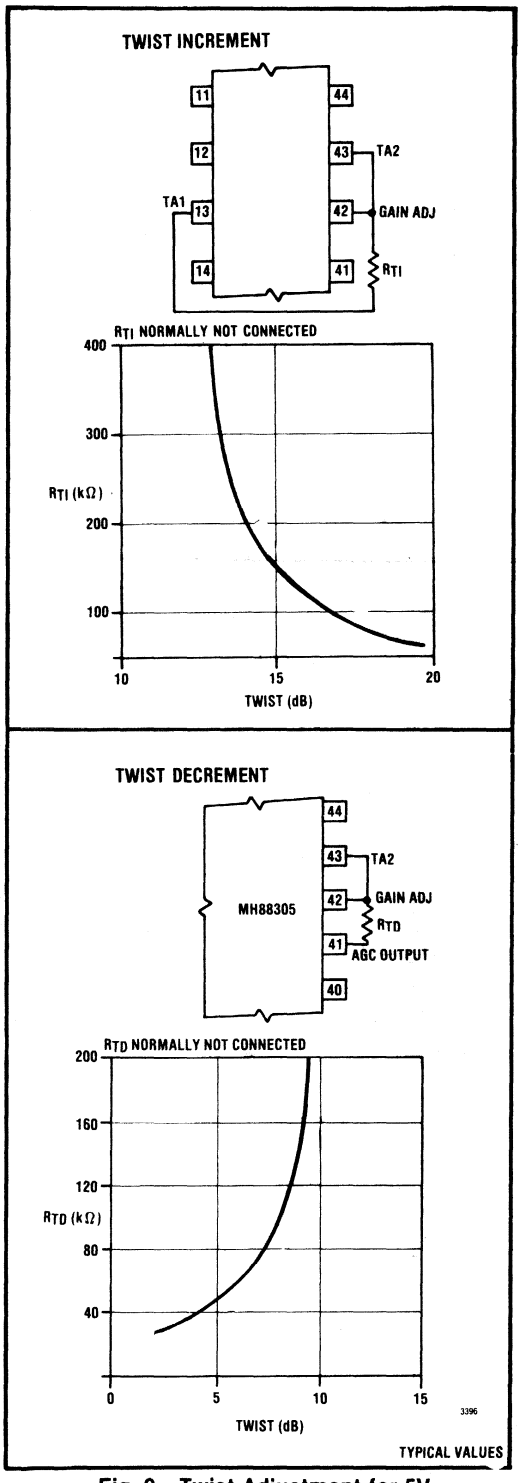


Fig. 9 Twist Adjustment for 5V Analog Operation

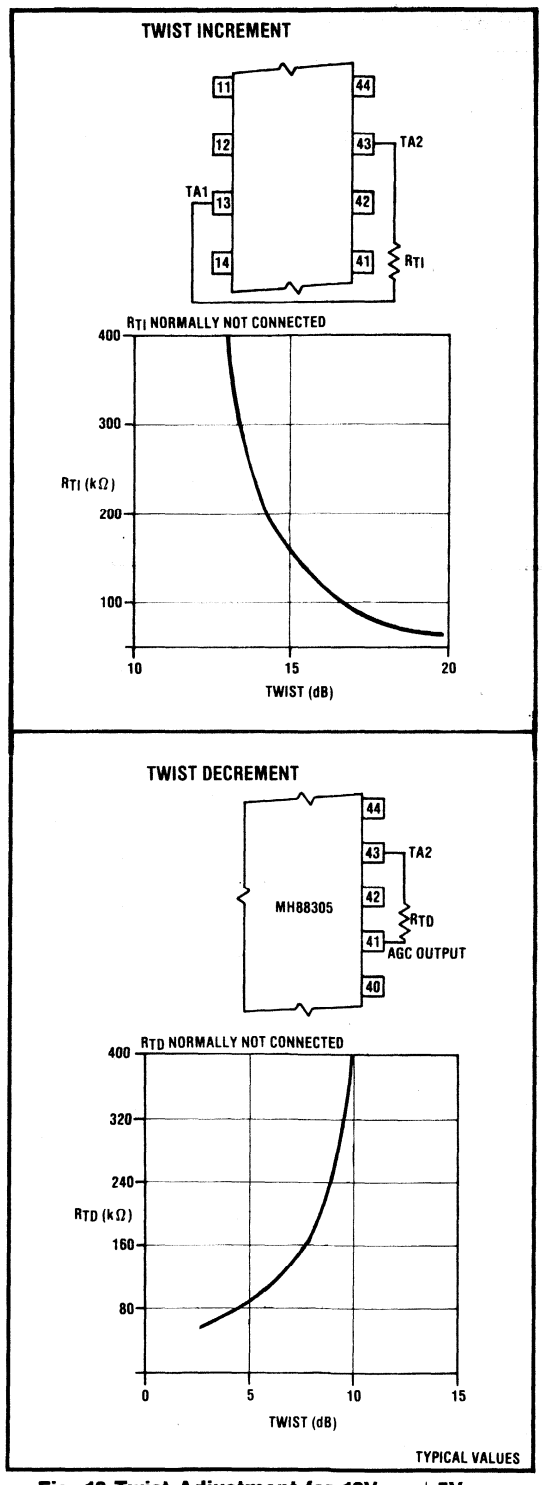


Fig. 10 Twist Adjustment for 12V or ±5V Analog Operation

Interchanging the 88205 & 88305 when using a ±5 V Supply

The following schematic (Fig. 11) shows the connections required to allow the user to interchange the 88305 and 88205 when using a ±5 volt split power supply.

With the components shown in the diagram below, the receiver will have the following Twist and Sensitivity characteristics:

MAXIMUM TWIST ACCEPT ≈ ±6 dB
MINIMUM VALID SIGNAL ≈ −32 dBm

The output coding is 2 of 8 format when the SEL pin is connected as shown.

Care must be taken when using the $\overline{StD}$ output on the 88305 (pin 20) since this pin corresponds to the CO2 output on the 88205. This CO2 output toggles continuously when the device is powered up.

Pin names in brackets are those for the 88205. Pin names without brackets are common to both devices.

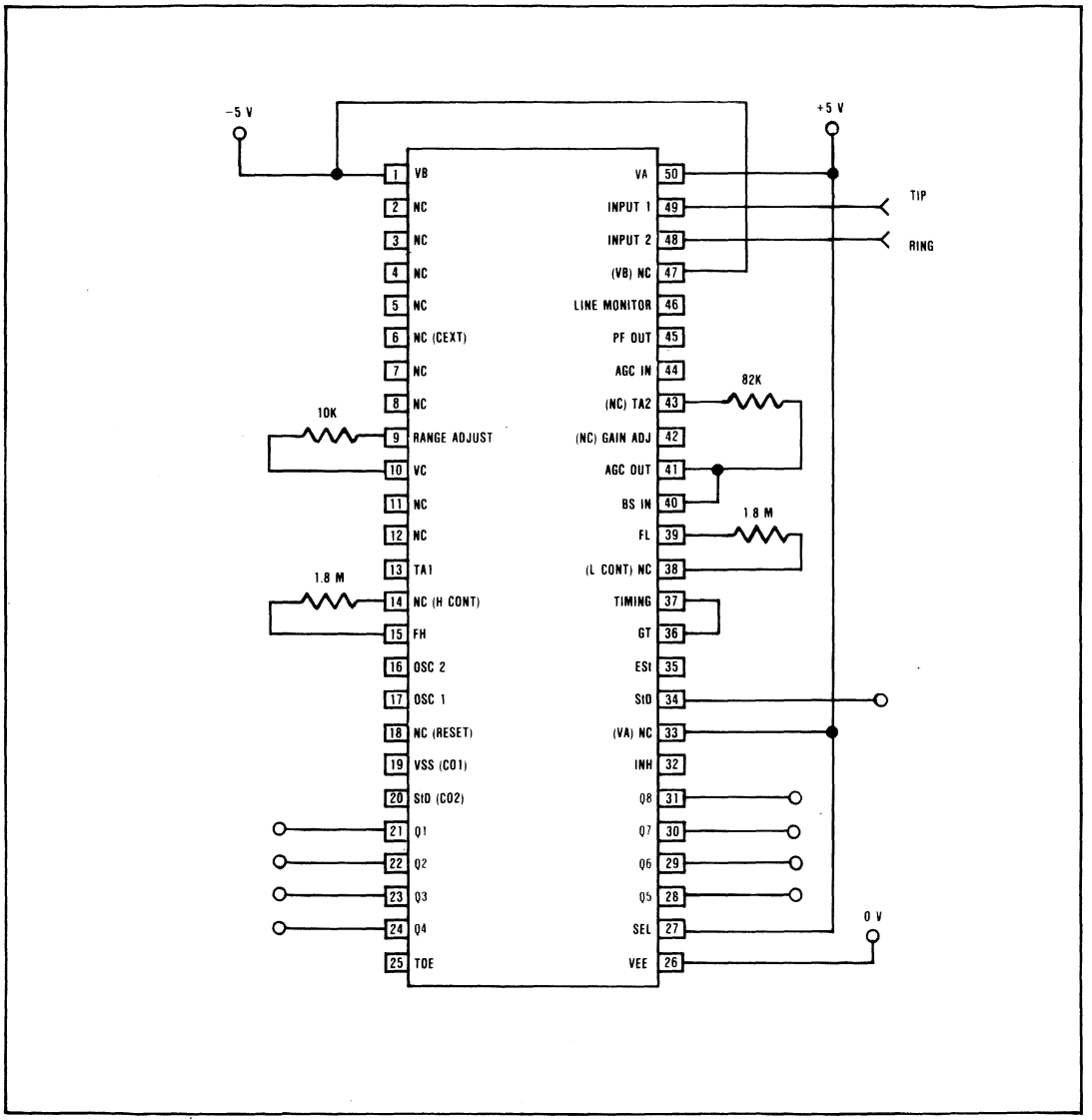


Fig. 11

Adjustment of Twist Acceptance with a ± V Supply

When using the MH88305 with a split supply (VA = 5 V, VB = −5 V) the schematic shown in Fig. 6 should be referred to for proper connections.

To choose a twist adjust resistor, use the graphs shown in Fig. 10 to obtain the required resistance. These graphs are in fact also used for 12 volt operation (VA = 12, VB = 0).

The selection of a range adjust resistor, however, is independent of supply voltage. Refer to Fig. 7 for selection of this resistor.

It should be noted that with split supply operation (VA = 5, VB = −5), the digital outputs will toggle from 0 volts to +5 volts.

Adjustment to the twist acceptance level and minimum valid input signal level may be performed as follows. Using Fig. 10, determine the twist adjust resistor value giving the desired twist acceptance level. Subtract 12 dB from this twist acceptance level (in dB) and add the result to the desired minimum valid input signal level. With this adjusted signal level, use Fig. 7 to determine the range adjust resistor value and connection configuration.

EXAMPLE:

VA = +5 VB = −5 VEE = 0

Required Twist Acceptance Level = 6 dB

Required Valid Input Signal Level = −30 dBm

The corresponding twist adjustment resistor is 82K (from Fig. 10).

The adjusted signal level
= (6−12) dB + (−30) dBm = −36 dBm

The corresponding input sensitivity adjust resistor is 5K (from Fig. 7).

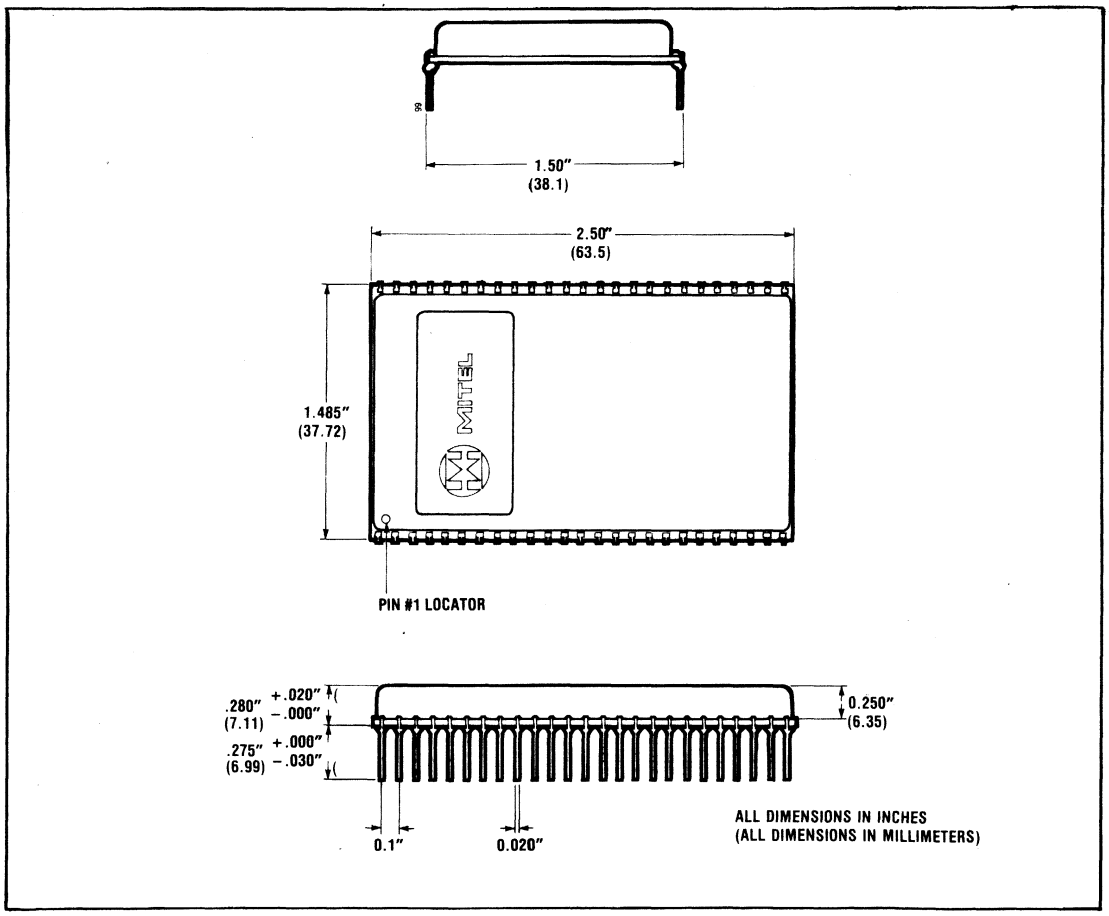


Fig. 12 Mechanical Data

ISO²-CMOS™ MT8840
Data Over Voice Modem
Preliminary Information

9161-002-011 NA ISSUE 2 JANUARY 1985

Features

- Performs ASK (amplitude shift keyed) modulation and demodulation
- 32KHz carrier frequency
- Up to 2KBps full duplex data transfer rate
- On-chip oscillator
- On-chip tone caller for alerting functions
- Adjustable tone caller frequencies
- Selectable self-loop test mode
- 5V/2.5mA power supply
- ISO²-CMOS and switched capacitor technologies
- 18 Pin DIP

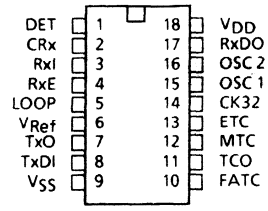
Applications

- Simultaneous data & voice communication in PABXs
- 2 KBps data modem
- "Smart" telephone sets

Description

The MT8840 is a carrier over voice modem which allows simultaneous transfer of voice and data over a single pair of wires. Data is transferred on an amplitude shift keyed (ASK) 32kHz carrier. On-chip filters remove voice frequency signals from the received composite voice and data signal prior to demodulation. The modulating signal is a bit stream with a typical data rate of 2KBps . In addition, the device contains a two tone warbler which functions as a telephone ringer. The device is fabricated in Mitel's double-poly ISO²-CMOS™ technology utilizing switched-capacitor techniques.

Pin Connections



Ordering Information

MT8840AC 18 Pin Ceramic Package
MT8840AE 18 Pin Plastic Package

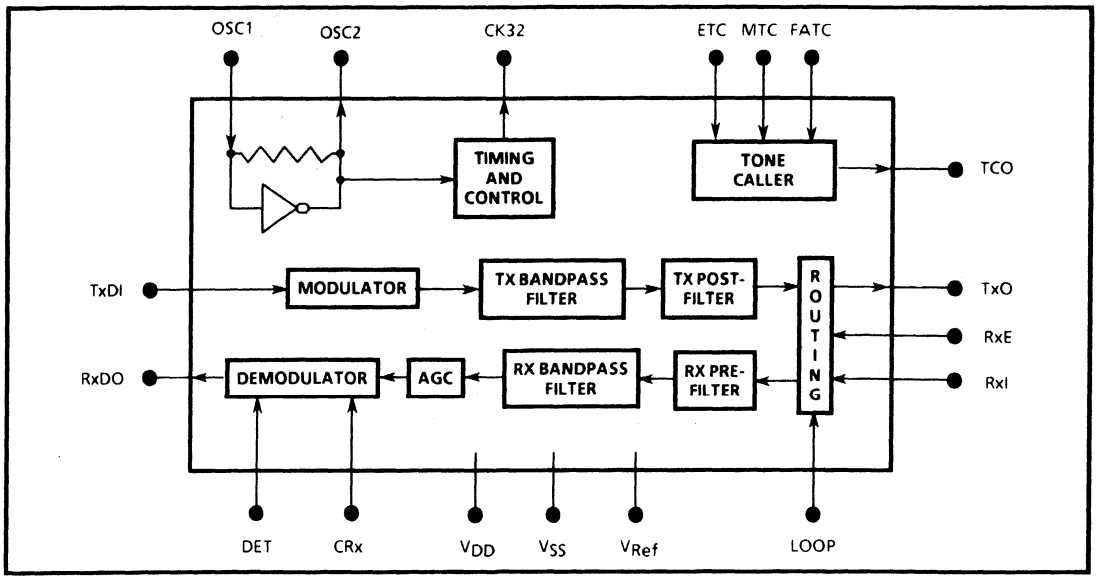


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

#	Parameter	Symbol	Min	Max	Unit
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	+7.0	V
2	Voltage On Any Pin	V_{Max}	V_{SS}-0.3	V_{DD} + 0.3	V
3	Current On Any Pin	I_{Max}		20	mA
4	Storage Temperature	T_S	-65	+150	°C
5	Package Power Dissipation	P_{Diss}		850	mW

*Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Recomended Operating Conditions

#	Parameter	Symbol	Min	Typ	Max	Unit
1	Operating Supply Voltages	V_{DD}	4.75	5	5.25	V
2		V_{Ref}		0.4V_{DD}		V
3	Operating Supply Currents	I_{DD}		2.5	5.0	mA
4		I_{Ref}			200	µA
5	Operating Temperature	T_O	0		+85	°C
6	Load Capacitance (TxO)	C_L			50	pF
7	Load Resistance (TxO)	R_L	10			KΩ

D.C. Characteristics

V_{DD} = 5.0 V ± 5% V_{SS} = 0V T = 0 - 85°C (All voltages are referenced to V_{SS}/GND)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
1	DIGITAL I/O	Input Current	I_{IN}			± 10	µA	V_{IN} = 0 to V_{DD}
2		Input Low Voltage	V_{IL}	0		1.5	V	
3		Input High Voltage	V_{IH}	3.5		5.0	V	
4		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 0.4mA
5		Output High Voltage	V_{OH}	4.6			V	I_{OH} = 0.4mA
6		Output Drive Current						
7		N Channel Sink (Except OSC2)	I_{OL}	0.4			mA	V_{OL} = 0.4V
8		OSC2		0.1			mA	
9		P Channel Source (Except OSC2)	I_{OH}	0.4			mA	V_{OH} = 4.6V
10		OSC2		0.1			mA	
11	ANALOG I/O	Input Current (RxI, FATC)	I_{IN}			± 10	µA	V_{IN} = 0 to 5.0V
12		Input Resistance (FATC)	R_{IN}	500			KΩ	
13		(DET to V_{DD})			170		KΩ	
14		(DET to V_{Ref})			23		KΩ	
15		Input Capacitance (RxI)	C_{IN}		50		pF	
16		(FATC)			10		pF	
17		Any Digital Input			5.0	7.5	pF	
18		Output Resistance (TxO)	R_O		100		Ω	
19		(TCO)			3		KΩ	MTC = 0
20		(TCO)			30		KΩ	MTC = 1
21		Output Offset Voltage (TxO)	V_O		± 25	± 200	mV	
22		Output Voltage (DET)	V_O	2.20	2.36	2.55	V	See Note 1

Notes: 1. Voltage specified is generated internally and measured with no external components connected to DET

A.C. Characteristics

V_{DD} = 5.0V ± 5% V_{SS} = 0V T = 0 - 85°C (All voltages are referenced to V_{SS}/GND)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
1	DIGITAL I/O	Crystal/Clock Frequency	f_C	3.5759	3.5795	3.5831	MHz	OSC 1, OSC 2
2		Clock Input (OSC 1)						
3		Rise Time	t_{LHCI}			100	ns	10% - 90% of (V_{DD} - V_{SS})
4		Fall Time	t_{HLCI}			100	ns	
5		Duty Cycle	DC_{CI}	40	50	60	%	
6		Clock Output (OSC 2)						
7		Rise Time	t_{LHCO}		100		nS	C_L = 30pF, 3.58MHz ext.
8		Fall Time	t_{HLCO}		100		nS	clock to OSC1
9		Duty Cycle	DC_{CO}		50		%	
10		Capacitive Load	C_{LCO}			30	pF	
11		Clock Output (CK32)	F_{C32}	32508	32541	32574	Hz	fc = 3.5795MHz
12		Rise Time	t_{LH32}		100		nS	10% - 90% of (V_{DD} - V_{SS})
13		Fall Time	t_{HL32}		100		nS	C_L = 100pF
14		Duty Cycle	DC_{32}		50		%	
15		Capacitive Load	C_{L32}			100	pF	
16	TONE CALLER	Warbler Frequency (TCO)	f_W	7.935	7.945	7.955	Hz	fc = 3.5795MHz ± 0.1%
17		Low Tone Frequency	f_{LT}	352	390	428	Hz	FATC = 0, f_c = 3.5795MHz
18				1036	1148	1260	Hz	FATC = V_{DD}, f_c = 3.5795MHz
19		High Tone Frequency	f_{HT}	440	487	535	Hz	FATC = 0, f_c = 3.5795MHz
20				1295	1434	1574	Hz	FATC = V_{DD}, f_c = 3.5795MHz
21		Harmonic Relationship	f_{HT}/f_{LT}		1.25			
22		Warbler Output (TCO)						
23		Rise Time	t_{LHWO}		500		nS	100KΩ load to V_{REF}
24		Fall Time	t_{HLWO}		500		nS	C_L = 30pF, MTC = 0
25		Duty Cycle	DC_{WO}		50		%	
26		Output Level (TCO)	V_{TCC}		V_{DD}		V_{pp}	MTC = 0
27					0.5	0.625	V_{pp}	MTC = 1 (100KΩ load to V_{Ref})
28	MODULATOR	Modulated Frequency	f_{MOD}		32541		Hz	
29		Output Level (TxO)	V_{TxO}	225	250	270	mV_{pp}	V_{DD} = 5V
30		Output Level (TxO)						
31		variation vs. V_{DD}	V_{TxO}		100		%	
32		Transmit Data Input (TxDI)						
33		Rise Time	t_{LHTxDI}			100	nS	
34		Fall Time	t_{HLTxDI}			100	nS	
35		Data Rate (TxDI)	f_{Data}		2		KBps	See Note 1
36	DEMODULATOR	Input Impedance (RxI)	Z_{IN}		50		KΩ	32KHz Input Frequency
37		Valid Input Level - Data (RxI)	V_{RxI}	40		400	mV_{pp}	See Note 2
38		Valid Input Level - Data + Voice	V_{RxI}			3.0	V_{pp}	
39		Receive Data Output (RxDO)	f_{Data}		2		KBps	
40		Rise Time			100		nS	10% - 90% of (V_{DD} - V_{SS})
41		Fall Time			100		nS	C_L = 100pF
42		Capacitive Load				100	pF	
43		Duty Cycle		40	50	60	%	

Notes: 1. All A.C. parameters are based on a typical data rate of 2KBps.
2. Measured with no external resistor to DET input. Detection level internally set to 2.36V typical.

A.C. Characteristics (Continued)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
44	D	Inband Noise Rejection (S/N)		12			dB	Input Sig. (RxI) = 400mV$_{pp}$
45	E	Attenuation to Voice Signals		40			dB	f_{in} = 0 - 5KHz
46	M	Detect Filter Q	Q		3.8			
47	O D	Detector Center Frequency			32		KHz	

Pin Description

Pin #	Name	Description
1	DET	Demodulator detection level adjust input (Analog). Internal resistor divider applies 2.36V in open circuit condition. Connection of external resistor will vary detect level.
2	CRx	External AGC time constant adjust input (Analog). Connect external capacitor to V_{SS}.
3	RxI	Modulated receive signal input (Analog). Biased at V_{Ref}
4	RxE	Receive enable input (Digital) with internal pull up. Active high.
5	LOOP	Self-test mode select input (Digital) with internal pull down. Active high.
6	V_{Ref}	Internal reference supply voltage input (Analog).
7	TxO	Modulated transmit carrier output (Analog).
8	TxDI	Transmit data input (Digital).
9	V_{SS}	Negative power supply.
10	FATC	Tone caller center frequency adjust input (Analog).
11	TCO	Tone caller output (Digital).
12	MTC	Mute tone caller input (Digital) with internal pull down. Active high.
13	ETC	Enable tone caller input (Digital) with internal pull down. Active high.
14	CK32	32 kHz data strobe output (Digital).
15	OSC1	Clock Input — 3.579545 MHz crystal connected between
16	OSC2	Clock Output to drive external devices. — these pins completes internal oscillator.
17	RxD0	Receive data output (Digital). Synchronized to CK32.
18	V_{DD}	Positive power supply.

Functional Description

The MT8840 contains the modulator and demodulator circuitry for 32 KHz ASK signalling as well as a two-tone warbler (tone caller) to replace the function of the mechanical telephone ringer.

A 32KHz carrier is 100% amplitude modulated by the digital bit stream applied to input TxDI. This results in an amplitude shift keyed (ASK) 32KHz carrier. A logical high at TxDI disables the carrier and a logical low enables it. The digitally modulated waveform is shaped by the Tx BANDPASS FILTER and smoothed by the Tx POST FILTER. The signal then enters the routing block where it is transferred to the TxO output.

The modulated 32 KHz receive signal is applied to RxI. With a logical low applied to LOOP and a logical high applied to RxE, receive signals are routed to the Rx PREFILTER. High frequencies are removed by the Rx PREFILTER to prevent aliasing in the switched capacitor Rx BANDPASS FILTER. Voice signals are removed by the bandpass filter which is followed by an AGC circuit. This provides a dynamic range of 20dB for the receiver. An external 1uF capacitor connected from CRx to V_{SS} is required to control the AGC attack and decay time constants. Data is recovered from the received signal in the demodulator. The minimum voltage level to which the demodulator responds may be adjusted by connecting a resistor from DET to V_{DD} or V_{Ref}. Since DET is the input to a comparator, noise should be kept to a minimum at this pin. The recovered receive data is synchronized to the leading edge of the 32 KHz clock (available at CK32) before appearing at RxD0.

When in loop around mode, the Rx PREFILTER input is internally disconnected from the RxI input pin and connected to TxO. The transmitter output is still available at TxO.

A two tone warbling audio signal is available at TCO when the tone caller enable input (ETC) is high. TCO is internally clamped to V_{Ref} when the tone caller is disabled. The tone output can be attenuated by 20dB if a logical high is applied to the tone caller mute input (MTC).

Applications

Figures 2 through 4 show how the MT8840 may be utilized to transfer data and voice simultaneously over a single pair of wires in digital or analog PABXs and "smart" telephone sets. In all 3 figures a microprocessor sends/receives data to/from the MT8840 via a UART which converts the data format from parallel to serial or serial to parallel for the transmit and receive directions respectively. In the receive direction the MT8840 has on-board filters to reject voice-band signals leaving only the 32KHz carrier. This carrier is then demodulated to recover the received data. In the transmit direction the data to be sent is modulated and passed on to a summing circuit which sums the modulated 32KHz carrier and voice-band signals for transmission over the telephone line. In the PABX the Filter/CODEC has filters which reject the 32KHz carrier from the received composite voice and data signal allowing only voice-band signals to pass through which are then PCM encoded for digital switching. However, in both the analog PABX and smart telephone set low-pass filters could be included to bandlimit the received signal leaving only voice signals to be passed on to the switch array or handset earpiece.

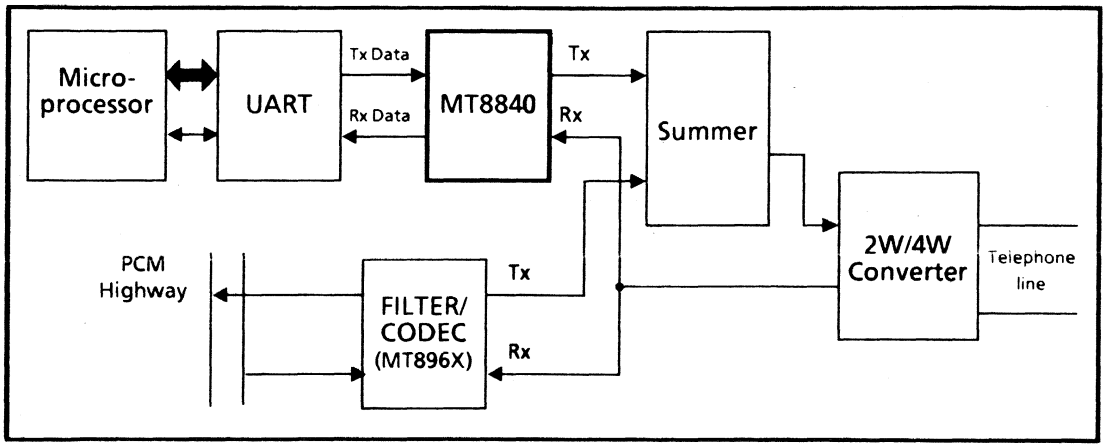


Figure 2 Digital PABX Block Diagram

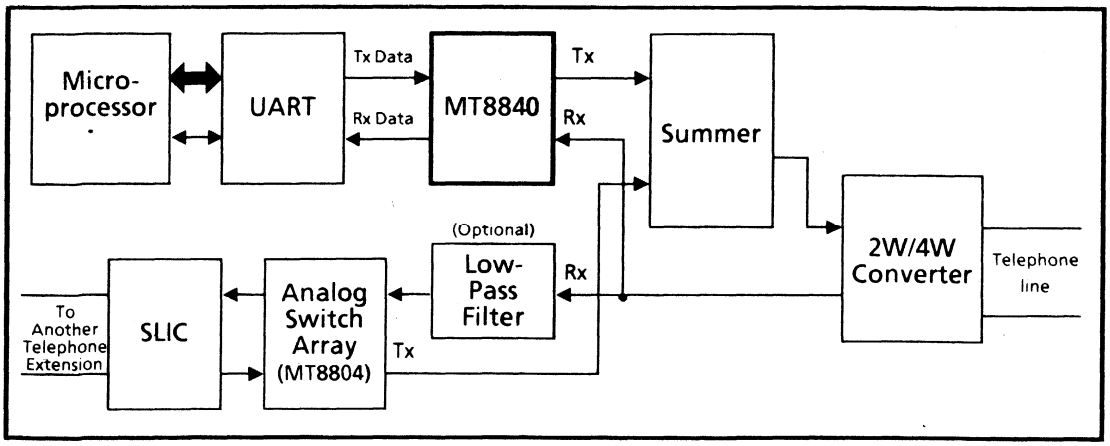


Figure 3 Analog PABX Block Diagram

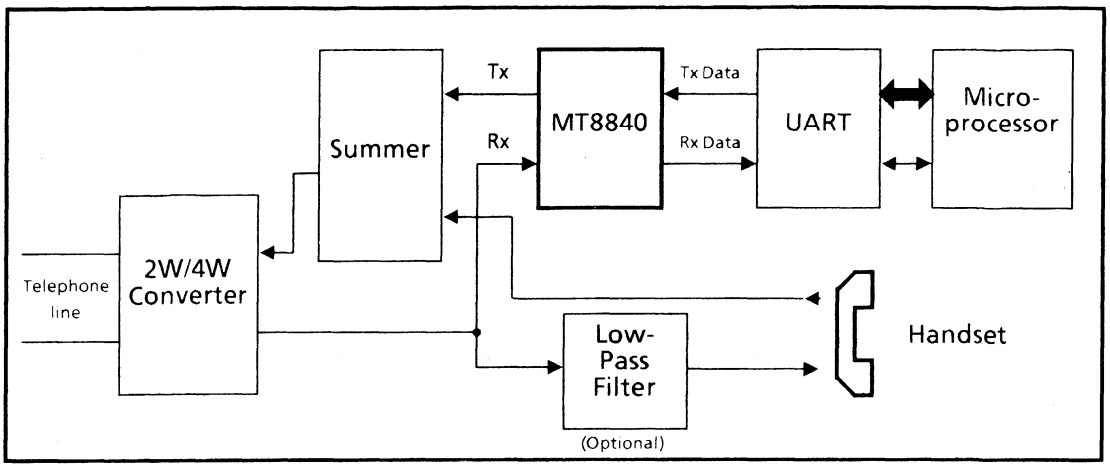
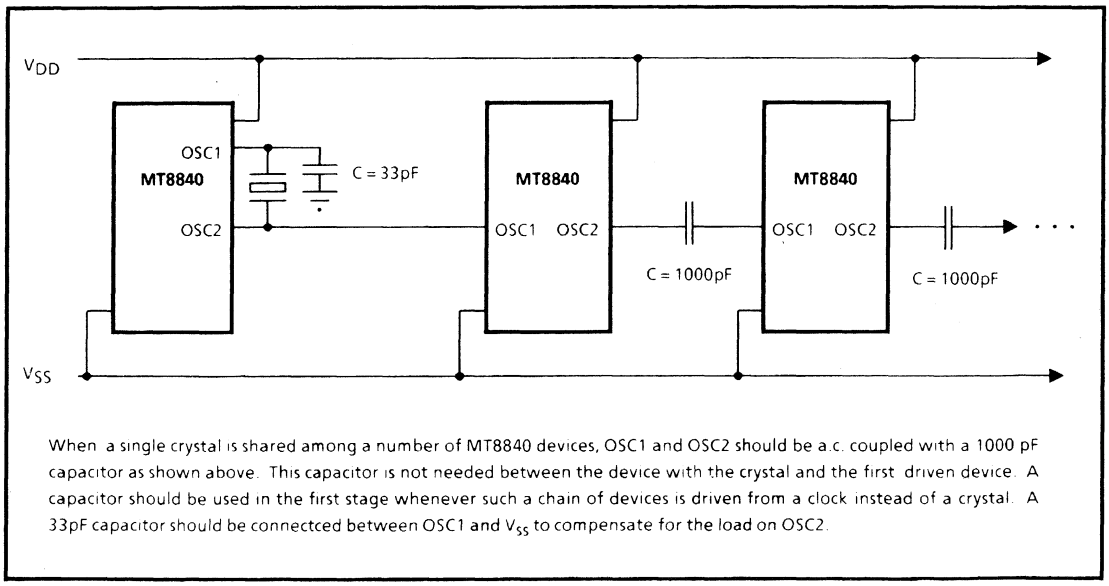


Figure 4 Smart Telephone Set Block Diagram



When a single crystal is shared among a number of MT8840 devices, OSC1 and OSC2 should be a.c. coupled with a 1000 pF capacitor as shown above. This capacitor is not needed between the device with the crystal and the first driven device. A capacitor should be used in the first stage whenever such a chain of devices is driven from a clock instead of a crystal. A 33pF capacitor should be connected between OSC1 and V_{SS} to compensate for the load on OSC2.

Figure 5 Crystal Oscillator Connections for Driving Multiple MT8840's

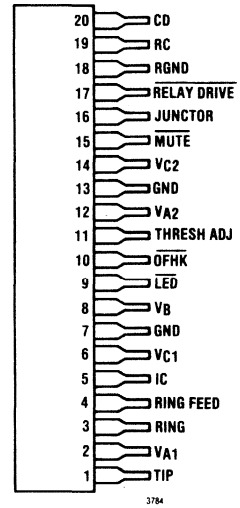
MH88500
Hybrid Subscriber Line Interface Circuit (SLIC)

SEPT. 1981

Features

- Differential to single ended conversion
- No transformers required
- Minimum installation space
- Off-hook detection and LED indicator drive
- Relay drive output
- Battery and ringing feed to line
- Logic interface: MUTE, OFHK, RC
- Mute of incoming audio
- Dial pulse detection
- Voltage surge protection

Pin Connections



Applications

Line interface for
- PABX
- Intercoms
- Key systems

Description

The Mitel MH88500 subscriber line interface circuit provides a complete interface between the telephone line and a speech switch requiring only a single bidirectional switch per crosspoint. The functions provided by the MH88500 include bidirectional differential to single ended conversion in the speech path, line battery feed, ringing feed and loop and dial pulse detection. The device is fabricated using thick film hybrid technology in a 20-pin 'single-in-line' package allowing optimum circuit board packing density.

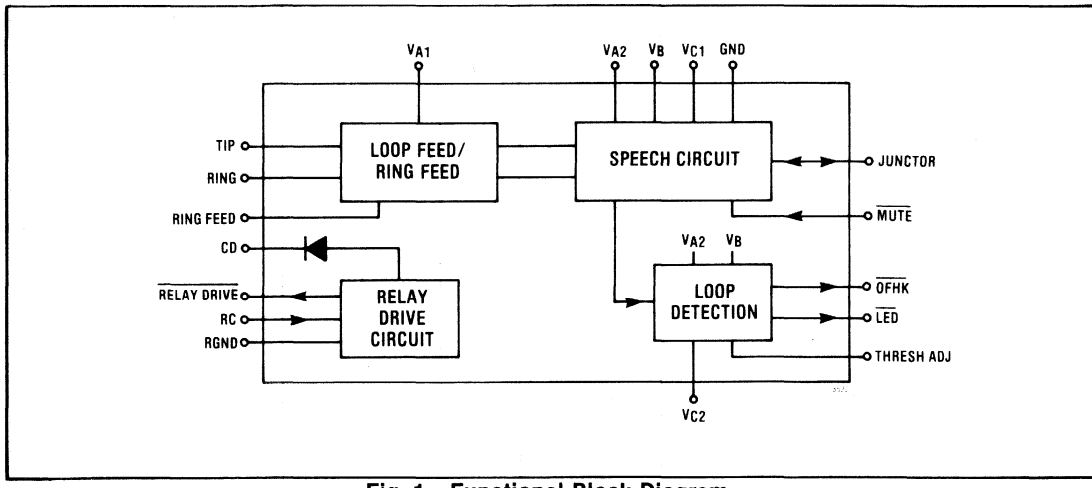


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltage Supplies	V_{A1}, V_{A2} V_B V_{C1}, V_{C2}	 – 18 – 35	+ 18	V Ref to GND V Ref to GND V Ref to GND
Clamp Diode Breakdown Voltage	V_{CD}		+ 15	V Ref to RGND
Operating Temperature	T_{AMB}	0	+ 70	°C
Storage Temperature	T_{STG}	– 40	+ 100	°C
Power Dissipation	P_D		1.2	Watt

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics

All Voltages Referenced to Ground (TA = 25°C)

	CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION UNLESS NOTED $V_{A1} = V_{A2} = +7V$, $V_B = -8V$, $V_{C1} = V_{C2} = -24V$
SUPPLY	Operating Supply Voltages	V_{A1}, V_{A2}			13	V	
		V_B	– 13			V	
		V_{C1}, V_{C2}	– 25			V	
	Operating Supply Currents	I_{A1}		7		mA	
		I_{A2}		8		mA	
		I_B		6		mA	
		I_{C1}		.2		mA	
		I_{C2}		.1		mA	

DC Electrical Characteristics (Cont'd)

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS Unless Noted $V_{A1}=V_{A2}=+7$ V, $V_B=-8$ V, $V_{C1}=V_{C2}=-24$ V
INPUTS	High Level Input Voltage	$\overline{\text{MUTE}}$	V_{IH}	4.2			V	
		RC	V_{IH}	3			V	
	Low Level Input Voltage	$\overline{\text{MUTE}}$	V_{IL}	.8			V	
		RC	V_{IL}	1			V	
	High Level Input Current	$\overline{\text{MUTE}}$	I_{IH}	−28			μA	
		RC	I_{IH}	700			μA	
	Low Level Input Current	$\overline{\text{MUTE}}$	I_{IL}	100			μA	
		RC	I_{IL}	1			μA	
OUTPUTS	Sink Current	$\overline{\text{LED}}$	$I_{\overline{\text{LED}}}$	2	6		mA	$V_{\overline{\text{OFHK}}} < -6$V
		$\overline{\text{RELAY}}$ $\overline{\text{DRIVE}}$	$I_{\overline{\text{RELAY}}}$	65	100		mA	CD = RC = 5V, RGND = 0V; $V_{\overline{\text{RELAY DRIVE}}} < 1.5$V
	Diode Clamp Current	CD	I_{CD}	65	100		mA	RC = RGND = 0V, CD = 5V; $V_{\overline{\text{RELAY DRIVE}}} >$
	High Level Output Voltage	$\overline{\text{OFHK}}$	V_{OH}	6			V	$\overline{\text{LED}}$ Unconnected
	Low Level Output Voltage		V_{OL}	−6.5			V	$\overline{\text{LED}}$ Unconnected
	High Level Output Current		I_{OH}	10			μA	
	Low Level Output Current		I_{OL}	10			μA	

AC Electrical Characteristics

(TA = 25 °C)

	CHARACTERISTIC		SYMBOL	MIN	TYP*	MAX	UNIT	TEST CONDITIONS UNLESS NOTED $V_{A1} = V_{A2} = +7V$, $V_B = -8V$ $V_{C1} = V_{C2} = -24V(\pm 5\%)$
	Junctor to differential output (tip, ring) Gain		A_{JL}	2.18	2.25	2.32	V/V	1KHZ, 400mV RMS Source on Pin 16 Note 2
	Differential Input (tip, ring) to junctor Gain		A_{LJ}	0.303	0.312	0.321	V/V	1KHZ, 1V RMS Source applied on pins 1&3 Notes 1, 2
	On/Off Hook Detection Threshold	Loop Resist.	R_{Thresh}	4.0	5.4	6.0	K Ω	Note 1
		Loop Current	I_{Thresh}	3.6	4.0	5.3	mA	Note 1
	Trans Hybrid Loss				55		dB	Notes 1, 2 See test circuit in Figure 2
	Passband Linearity				±1		dB	Notes 1, 2
	Power Supply Rejection Ratio (V_C to Junctor)		PSRR		40		dB	Notes 1, 2
	Common Mode Rejection Ratio (tip and ring to junctor)		CMRR		40		dB	Notes 1, 2
	Low Frequency Cutoff (3dB)	Junctor to Line	F_{LLJ}		53		Hz	Notes 1, 2
		Line to Junctor	F_{LJL}		20		Hz	Notes 1, 2
	High Frequency Cutoff (3dB)	Line to Junctor	F_{HLJ}		800		KHz	Notes 1, 2
		Junctor to Line	F_{HJL}		500		KHz	Notes 1, 2
	Longitudinal Balance				65		dB	Note 1
	Tip (or ring) to ground AC input impedance		Z_I		300		Ω	
	Junctor output impedance		Z_{OJ}		604		Ω	

Note 1: 754 ohms connected between JUNCTOR)pin 16) and 0 volts.
Note 2: 604 ohms connected between TIP (pin 1) and RING (pin 3).
* All "Typical" parametric information is for design aid only and not subject to production testing.

Pin Description

PIN	NAME	DESCRIPTION
1	TIP	Connection to telephone "TIP" wire.
2	V_{A1}	Positive line feed supply voltage. Normally connected to V_{A2}.
3	RING	Connection to telephone "RING" wire.
4	RING FEED	Negative line feed voltage and ringing input. Normally connected to ring relay.
5	IC	Internal connection. Leave open circuit. Use for testing only.
6	V_{C1}	Sense input. Normally connected to negative line feed voltage supply.
7	GND	Analog ground. (OV) Internally connected to pin 13.
8	V_B	Negative analog supply voltage.
9	$\overline{\text{LED}}$	LED drive output (Off-Hook condition, logic low).
10	$\overline{\text{OFHK}}$	Logic low output indicates closed loop condition (Off-Hook and dial pulsing)
11	THRESH. ADJ.	Allows adjustment of $\overline{\text{OFHK}}$ detection threshold.
12	V_{A2}	Positive analog supply voltage. Normally connected to V_{A1}.
13	GND	Analog ground (OV). Internally connected to pin 7.
14	V_{C2}	Loop detector voltage supply. Connect to negative line feed voltage supply.
15	$\overline{\text{MUTE}}$	Input mutes the incoming audio. Active low.
16	JUNCTOR	Receive/transmit audio speech path (referenced to OV GND).
17	$\overline{\text{RELAY}}$ $\overline{\text{DRIVE}}$	Relay driver output. Open collector sinks current when RC high. Diode clamp protected.
18	RGND	Ground for relay drive circuit.
19	RC	Relay control input. Active high.
20	CD	Clamping diode. Normally connected to relay positive supply voltage.

Functional Description
Speech Circuit

The speech circuit converts the bidirectional TIP and RING line pair to a bidirectional single ended junctor line. Figure 2 illustrates a typical connection between two SLIC's through two crosspoint switches. This configuration gives optimum transhybrid loss as seen from Figure 3 given that the output impedance of the junctor line is 604 Ω .

The $\overline{\text{MUTE}}$ input mutes signals coming from TIP and RING to the junctor line while allowing the signal from the junctor to the tip-ring pair to be transmitted.

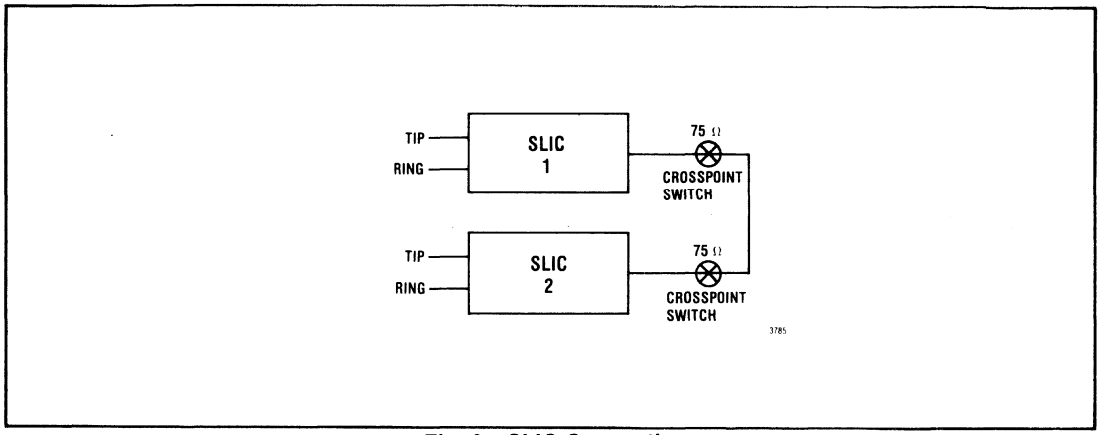


Fig. 2 SLIC Connection

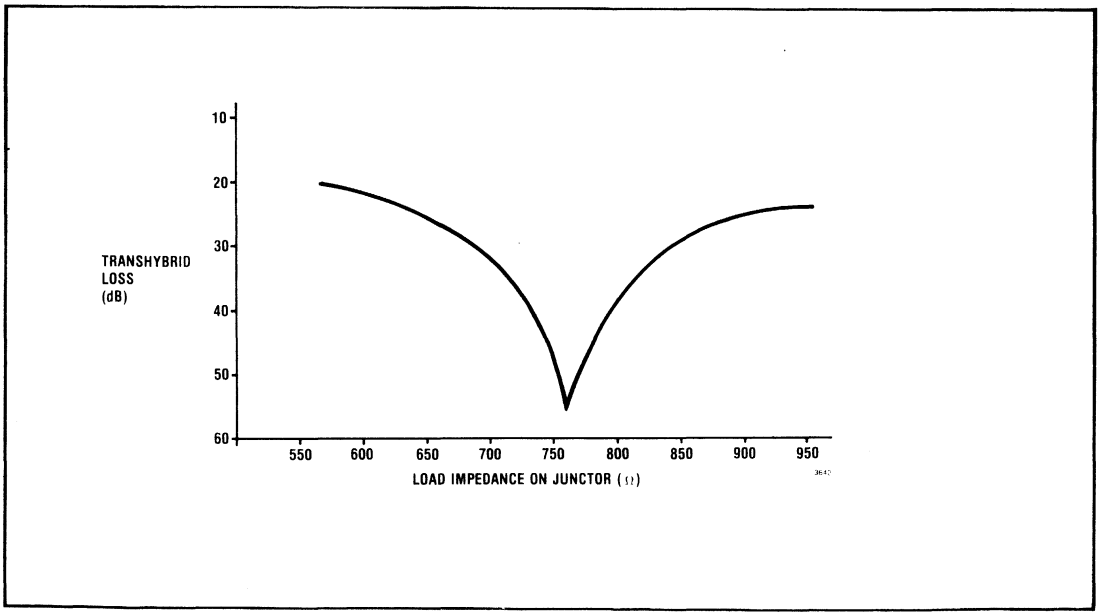


Fig. 3 Transhybrid Loss vs Junctor Load Impedance

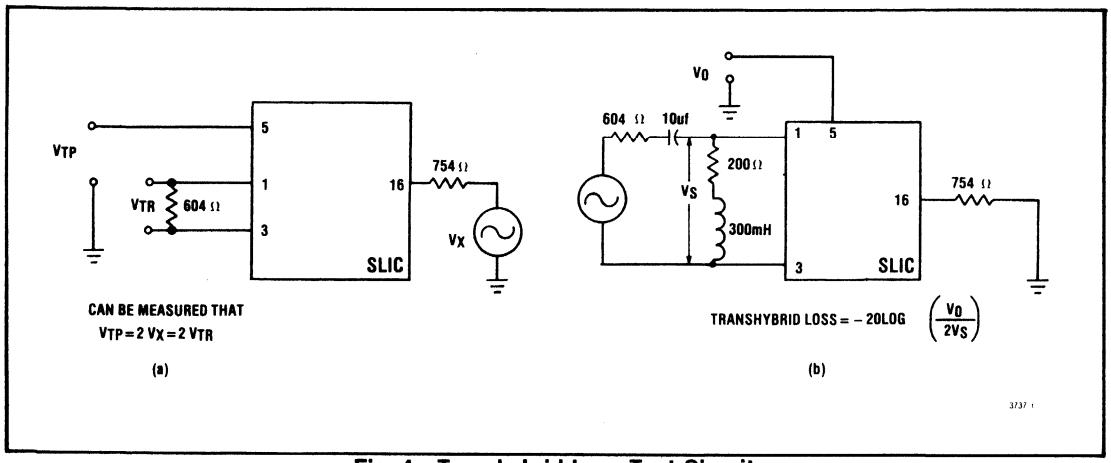


Fig. 4 Transhybrid Loss Test Circuit

Loop Detection

The loop detection circuit determines whether a low enough impedance is across TIP and RING to be recognized as an off-hook condition. (Threshold impedance = 5.4K Ω with no adjustment). This threshold level can be adjusted by the use of external resistors as shown in Figure 5. $\overline{OFHK}$ has low output drive capability so it may drive CMOS operating with different power supplies.

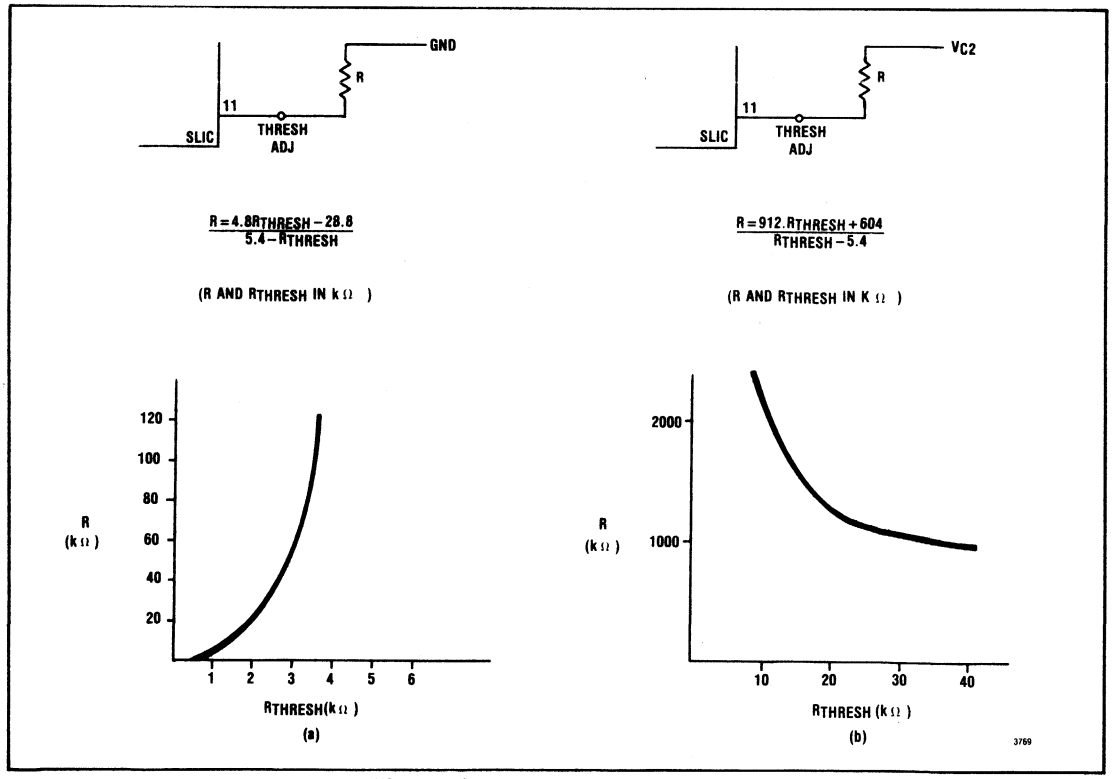


Fig. 5 Off-Hook Threshold Adjust

Line Feed/Ring Feed Circuit

The line feed circuit provides loop current and the ability to apply ringing onto TIP and RING. The impedance from RING FEED to GND is 600Ω which gives the loop current as:

$$\frac{\text{Voltage at RING FEED pin}}{\text{Telephone Impedance} + 600} \quad \text{Amp}$$

The positive supply for the line feed circuit is V_{A1} though the loop current is determined from RING FEED and GND.

Relay Drive Circuit

The relay drive circuit switches ringing onto RING FEED (FIG. 6). The diode is present to suppress voltage transients during relay switching caused by the inductive coils of the relay. Ringing Voltage includes AC ringing (90V typically) and DC line feed voltage (−24V typically).

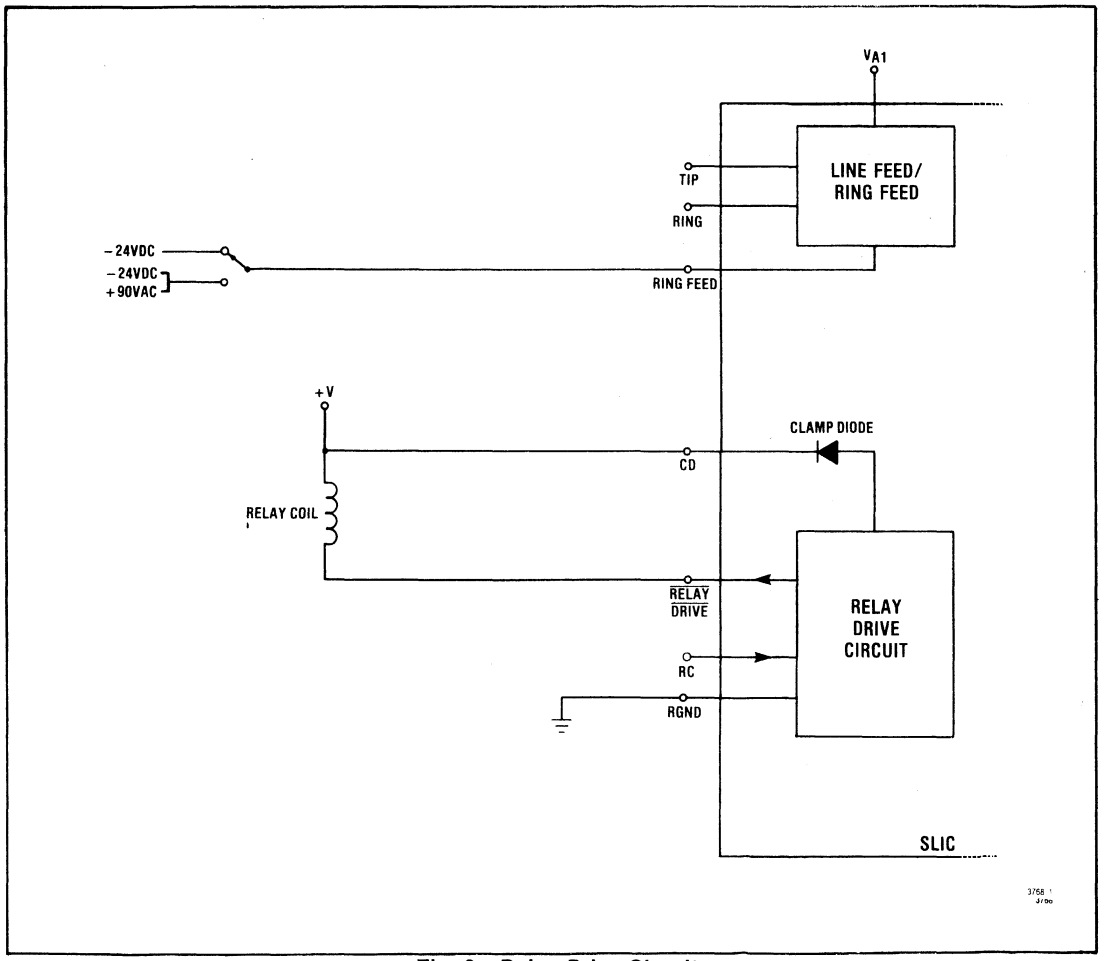


Fig. 6 Relay Drive Circuit

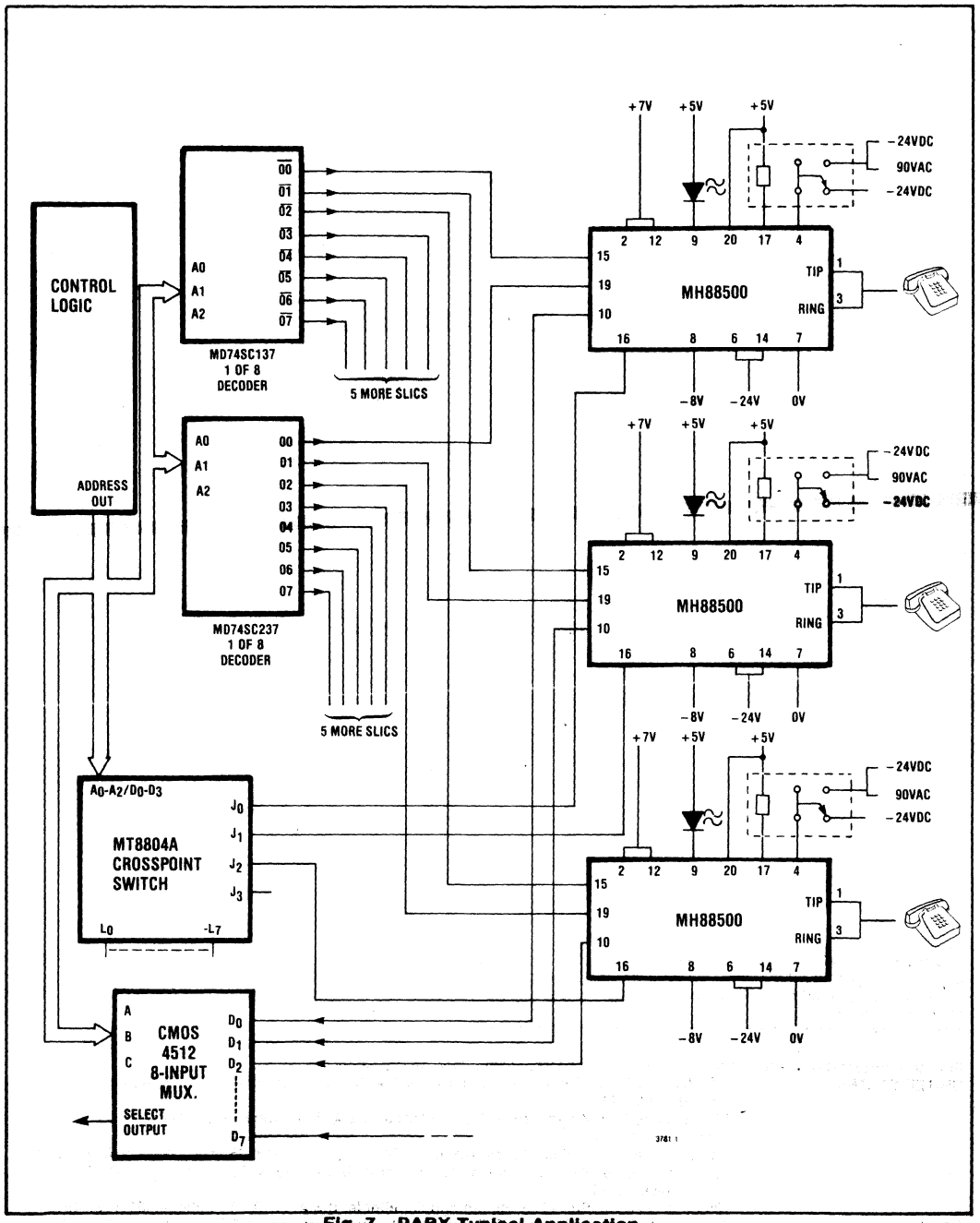


Fig. 7 PABX Typical Application

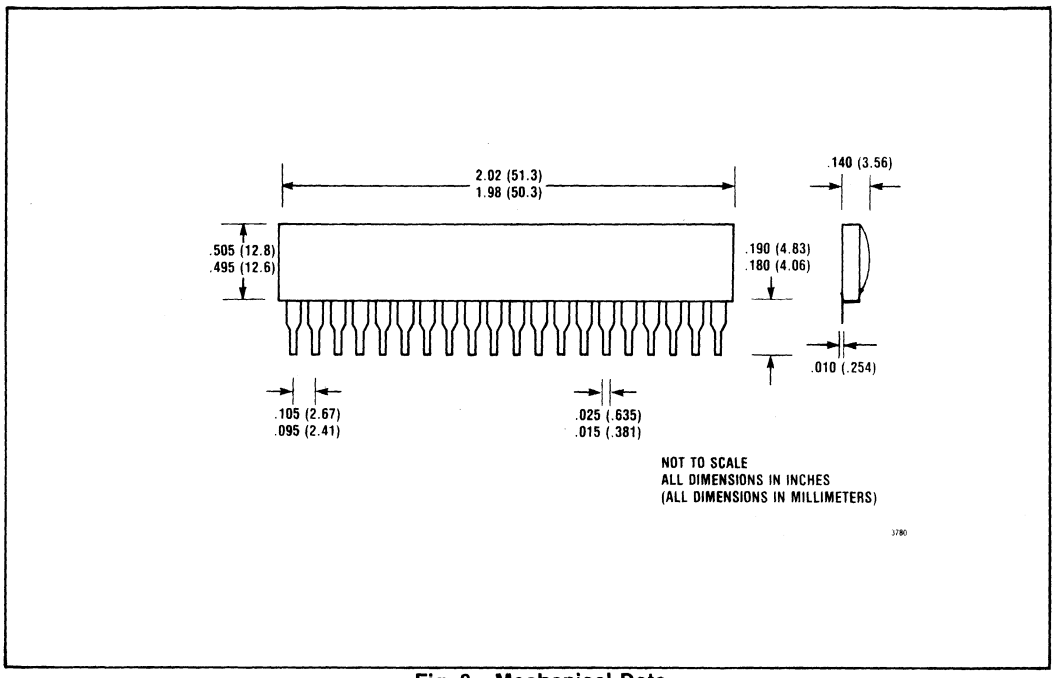


Fig. 8 Mechanical Data

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MITEL

CMOS MT8860 DTMF Decoder

FEB. 1985

Features

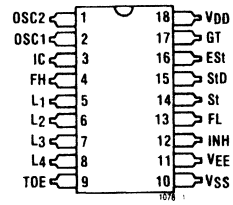
- 18 pin DIP package
- Central Office quality detection
- Excellent voice talk-off
- Detect times down to 20ms
- Single supply 5V or 8 to 13V operation
- Latched 3 state buffered outputs
- Detects all 16 DTMF combinations
- Uses inexpensive 3.58MHz crystal
- Low power CMOS circuitry
- Adjustable acquisition & release times

Applications

In DTMF Receivers For

- End to end signaling
- Control systems
- PABX
- Central Office
- Mobile Radio
- Key systems
- Tone to pulse converters

Pin Connections



Ordering Information

MT8860XC	18-Pin Ceramic DIP
MT8860XE	18-Pin Plastic DIP

(All types −40°C to +85°C)

Description

The MITEL MT8860 detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF FILTER (Mitel MT8865) and provides a 3 state buffered 4 Bit binary output. The clock signals are derived from an on chip oscillator requiring only a single resistor and low cost TV crystal as external components. The MT8860 is implemented in CMOS technology and incorporates an on chip regulator, providing low power operation and power supply flexibility. The MT8860X is an improved version of the MT8860A and is recommended for new designs.

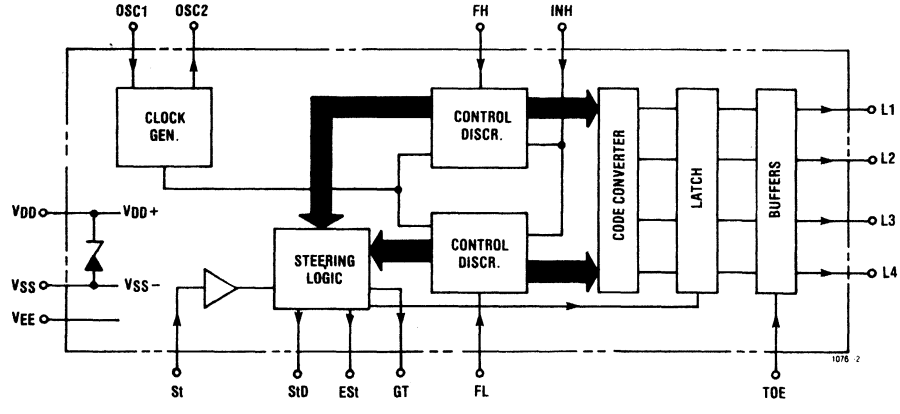


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings

Parameter		Min	Max	
V_{DD} - V_{EE}			15	V
V_{DD} - V_{SS} (Low Impedance Supply)			5.5	V
Voltage on any pin except OSC1 OSC2		V_{EE} −0.3	V_{DD} +0.3	V
Voltage OSC1 OSC2		V_{SS} −0.3	V_{DD} +0.3	V
Max current at any pin (except V_{DD} & V_{EE})			10	mA
Operating Temperature	C/E Package	−40	+85	°C
Storage Temperature	C Package	−65	+150	°C
	E Package	−65	+125	°C

		Max
Power Dissipation	C Package[1]	1000mW
	E Package[2]	450mW

[1] Derate 16mW/°C above 75°C
[2] Derate 6.3mW/°C above 25°C
All leads soldered to PC board.

Exceeding these ratings may cause permanent damage. Functional operation under these conditions in not implied.

DC Electrical Characteristics

All voltages referenced to V_{EE} unless otherwise noted.

		Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})	V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2				8		13	V	Connections Fig. 5b
3		Internal Logic Ground Voltage (V_{DD} - V_{SS})	V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4				6.0	6.5	7.5	V	I_{dd} = 7mA
5		Operating Supply Current	I_{DD}		1.3	4	mA	5V
6					2.5	5	mA	12V V_{DD} - V_{SS} = 5.5V
7		Internal Logic Ground Pin Current	I_{SS}		5.5	6.7	mA	12V R_{SSEE} = 900Ω
8		Operating Power Consumption	P_O		6.5		mW	5V
9					66		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)	V_{IH}	3.5			V	5V
11				8.5			V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)	V_{IL}			1.5	V	5V
13						3.5	V	12V
14		High Level Input Voltage OSC1	V_{IHO}	3.5			V	5V
15				10.5			V	12V
16		Low Level Input Voltage OSC1	V_{ILO}			1.5	V	5V Ref V_{SS}
17						1.5	V	12V Ref V_{SS}
18		Steering Input Threshold Voltage	V_{TSt}	2.04	2.27	2.5	V	5V
19				5.4	6.0	6.6	V	12V
20		Pull Down Sink Current (INH)	I_{SI}	10	25	75	µA	5V
21				10	190	400	µA	12V
22		Pull Up Source Current (TOE)	I_{SO}	2	7	45	µA	5V + 12V
23								
24		Input High Leakage Current	I_{IH}		0.1	1.5	µA	5V or 12V
25		Input Low Leakage Current	I_{IL}		0.1	1.5	µA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)	V_{OH}	4.9			V	5V
27				11.9			V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)	V_{OL}			0.1	V	5V
29						0.1	V	12V
30		High Level Output Voltage OSC2	V_{OHO}	4.9			V	5V
31				11.9			V	12V

DC Electrical Characteristics (Cont'd)

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions
32	OUTPUTS	Low Level Output Voltage OSC2		V_{OL}			0.1	V	5V Ref V_{SS}
33							0.1	V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V V_{OH} = 4.6V
35					0.5	0.8		mA	12V V_{OH} = 11.5V
36			N Channel Sink	I_{OL}	0.8	1.2		mA	5V V_{OL} = 0.4V
37					1.0	1.6		mA	12V V_{OL} = 0.5V
38		Output Drive Current OSC2	P Channel Source	I_{OH}	90	120		µA	5V V_{OH} = 4.6V
39					90	120		µA	12V V_{OH} = 11.5V
40			N Channel Sink	I_{OL}	100	160		µA	5V V_{OL} = 0.4V
41					100	160		µA	12V V_{OL} = 0.5V
42		Tristate Output Current (High Impedance State)	L_1 - L_4 = H	I_{OZ}		0.035	1.5	µA	5V Appl V_{OL} = 0V
43			L_1 - L_4 = L			0.1	1.5	µA	5V Appl V_{OH} = 5V
44			L_1 - L_4 = H			0.1	1.5	µA	12V Appl V_{OL} = 0V
45			L_1 - L_4 = L			0.3	1.5	µA	12V Appl V_{OH} = 12V

Test Conditions, T_A = 25°C f_c = 3.579545MHz Outputs are not loaded unless stated.
5V : V_{DD} - V_{EE} = 5V V_{SS} = V_{EE} Connection as Fig. 5a
12V : V_{DD} - V_{EE} = 12V R_{SSEE} = 900Ω Connection as Fig. 5b
For input current parameters only V_{IH} = V_{IHO} = V_{DD}, V_{IL} = V_{EE}, V_{ILO} = V_{SS}

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC Electrical Characteristics

		Characteristic		Symbol	Min	Typ*	Max	Unit	Test Conditions Unless Noted V_{DD} = 5 V, T_A = 25°C f_c = 3.579545 MHz
1	DETECTOR	Tone Frequency Deviation Accept		Δf_A			± 2.5	%Nom.	
2		Tone Frequency Deviation Reject		Δf_R	± 3.5			%Nom.	
3A									
4A									
3X		Tone Present Detection Time (MT8860X)		t_{DP}	6		10	ms	
4X		Tone Absent Detection Time (MT8860X)		t_{DA}	0.6		6	ms	
5		Guard Time		$t_{GT(P\ or\ A)}$	Adjustable Functions of t_{GT}. See Figs 3,6,7.				
6		Time to Receive = (t_{DP} + t_{GTP})		t_{REC}					
7		Invalid Tone Duration (f_n of t_{REC})		t_{REC}					
8		Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}					
9		Acceptable Drop Out (f_n of t_{ID})		t_{DO}					
10	I/P	FL FH Input Transition Time		t_T			1.0	µs	10%-90% V_{DD}
11		Capacitance Any Input		C		5	7.5	pF	
12	OUTPUTS	Propagation Delay St to L_1-L_4		t_{PL}		8	11	µs	V_{DD} 5 V or 12 V
13									
14		Propagation Delay St to StD		t_{PStD}		12	14	µs	V_{DD} 5 V or 12 V
15		Sync. Delay L_1-L_4 to StD		t_{LStD}		3.43		µs	
16		Propagation Delay TOE to L_1-L_4	Enable	t_{PTE}		300		ns	V_{DD} 5 V
17						200		ns	V_{DD} 12 V
18			Disable	t_{PTD}		300		ns	V_{DD} 5 V
19						200		ns	V_{DD} 12 V
20	CLOCK	Crystal/Clock Frequency		f_c	3.5759	3.5795	3.581	MHz	OSC 1 / OSC 2
21		Clock Input (OSC 1)	Rise Time	t_{LHCl}			110	ns	10%-90% V_{DD}-V_{SS} / Externally Applied Clock
22			Fall Time	t_{HLCl}			110	ns	
23			Duty Cycle	DC_{Cl}	40	50	60	%	
24		Clock Output (OSC 2)	Capacitive Load	C_{LO}			30	pF	
25									

Fig. 2 Coding Tables

a) Output Coding

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
DR	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
	*	H	H	L	H	H
	#	H	H	H	L	L
D	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

b) Inhibit Function

Detected Character	INH	ESt
None	Φ	L
X	L	H
DR	H	H
D	H	L

c) Steering

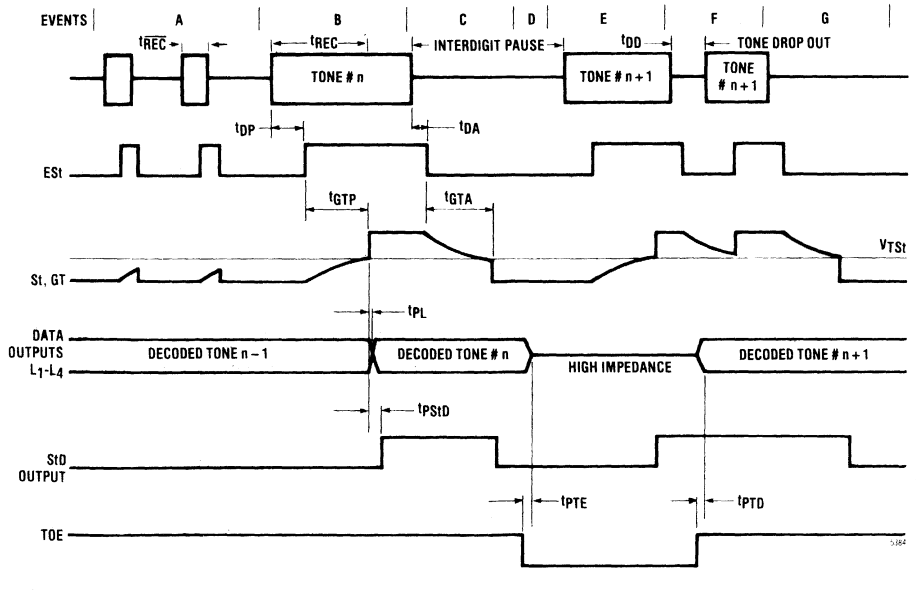
ESt	St	GT	StD*
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

* DELAYED WRT St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH L = LOGIC LOW
0 = "DON'T CARE" LOGIC HIGH OR LOW
Z = HIGH IMPEDANCE X = ANY CHARACTER



A) SHORT TONE BURSTS : DETECTED. TONE DURATION IS INVALID.
B) TONE #n IS DETECTED. TONE DURATION IS VALID. DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STATE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n+1 IS DETECTED. TONE DURATION IS VALID. DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE #n-1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n+1 IS DETECTED AND VALIDATED.

Fig. 3 Timing Diagram

Pin Description

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.579545MHz crystal with parallel 5MΩresistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only. Must be left open circuit.	
4	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter	
5	L1	Data Outputs. 3 state buffered Provides 4 Bit binary word corresponding to the tone pair decoded, when enabled by TOE See Fig. 2 for state table	
6	L2		
7	L3		
8	L4		
9	TOE	3 state output enable input. Logic high on this input enables outputs L1-L4. Internal pull up	
10	V_{SS}	Internal logic ground. For V_{DD} - V_{EE} = 5V V_{SS} connected to V_{EE}. For V_{DD} - V_{EE} > 8V, V_{SS} connected via resistor to V_{EE} see Fig. 5	
11	V_{EE}	Negative power supply. External logic ground	
12	INH	Inhibit input. Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull down	
13	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter	
14	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage< V_{TSt} on this pin frees the device to accept a new tone pair. See Fig. 2 c and Functional Description	
15	StD	Delayed Steering Output. Flags when a valid tone pair has been received. Presents logic high when output latch updated. When St voltage exceeds V_{TSt}. Returns to logic low when St voltage falls below V_{TSt}	
16	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low	
17	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Fig. 2 c)	
18	V_{DD}	Positive power supply	

Functional Description

The Mitel MT8860 is a CMOS Digital DTMF Detector and Decoder. Used in conjunction with a suitable DTMF filter (MITEL MT8865) it can detect and decode all 16 Standard DTMF tone pairs, accurately descriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MT8860 must be preceeded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sine wave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The High Group and Low Group rectangular waves are applied to the MT8860's FH and FL inputs respectively. Mitels MT8865 DTMF Filter provides these functions.

Within the MT8860 the FL and FL signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators Fig. 1) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both High Group and Low Group signals have been simultaneously detected a flag ESt (Logic High) is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig. 3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of "tone absent" before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig. 7a) is charged via resistor R from ESt when a DTMF tone pair is detected. After a period t_{GTP} V_C exceeds the St input threshold voltage V_{TSt} setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Fig. 2c) and timing diagram (Fig. 3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L_1 to L_4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig. 7a) falling below V_{TSt}.

Increasing the "time to receive" t_{REC} tends to further improve "talk-off" performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal-to-noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite affect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig. 7.

When L_1 - L_4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indication a character has been received.

The MT8860 may be operated from either a 5 volt or 8 to 15 volt supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig. 5.
When using the MT8860 with the MT8865 DTMF Filter it is only necessary to use the MT8865 crystal oscillator (see Fig. 6). When using the higher supply voltage range the 8865 OSC2 output should be capacitively coupled to the 8860 OSC1 input as shown in Fig. 6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves "talk-off" due to the reduced number of detectable tones.

The MT8860X differs from the MT8860A in that it has an improved decode algorithm giving enhanced talk-off performance. It also features a faster and more closely-controlled response time (see t_{DP} and t_{DA}). The MT8860X is recommended in preference to the MT8860A for all new designs and may normally be used as a direct replacement in existing designs, provided that consideration is given to the effect of shorter response time on system performance.

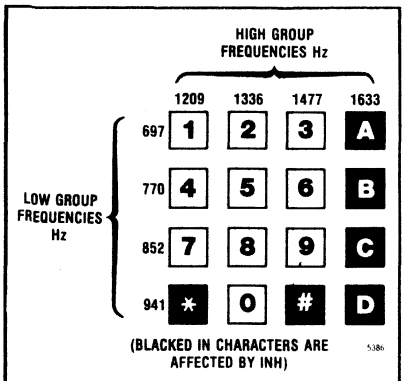


Fig. 4 DTMF Matrix Indicating Character - Tone Pair Correspondence.

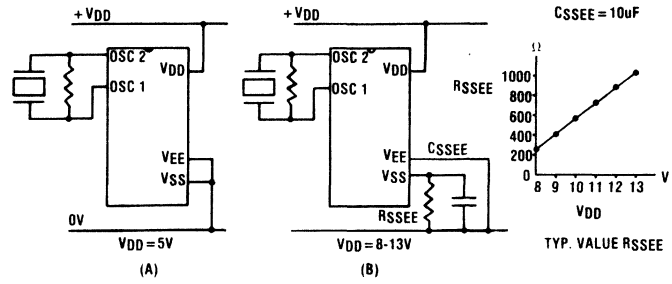


Fig. 5 Power Supply Connection Options

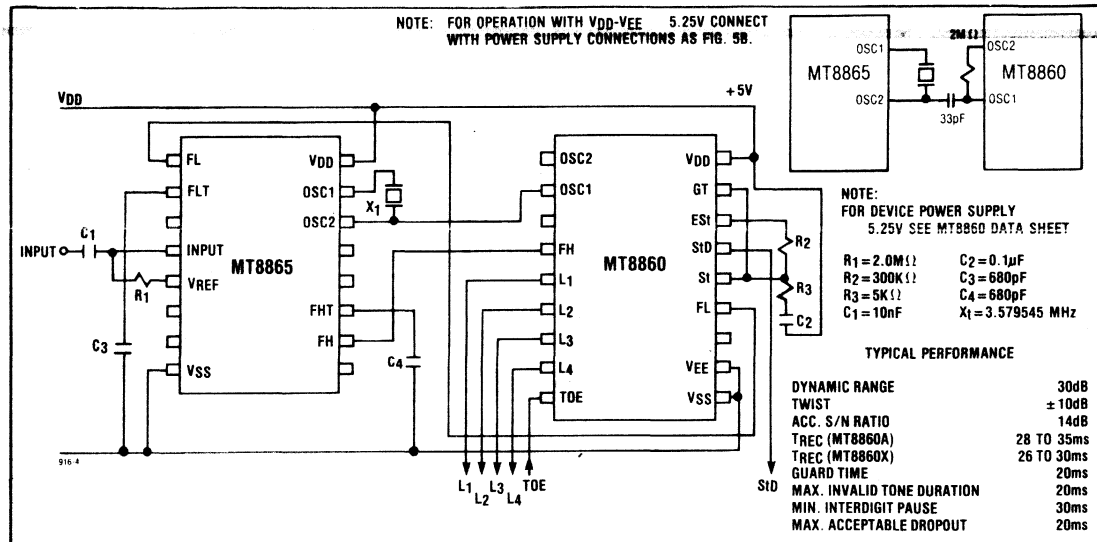


Fig. 6 Connection Diagram for Single Ended Input Receiver Using the MT8865 (5V Operation)

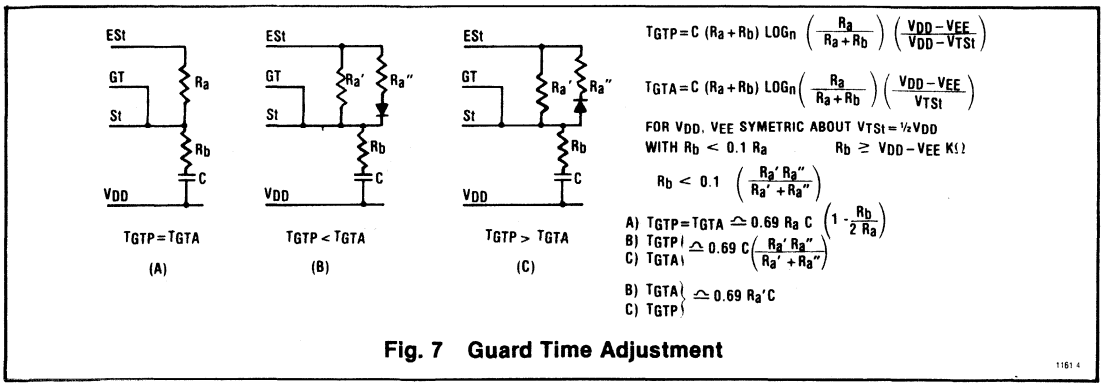
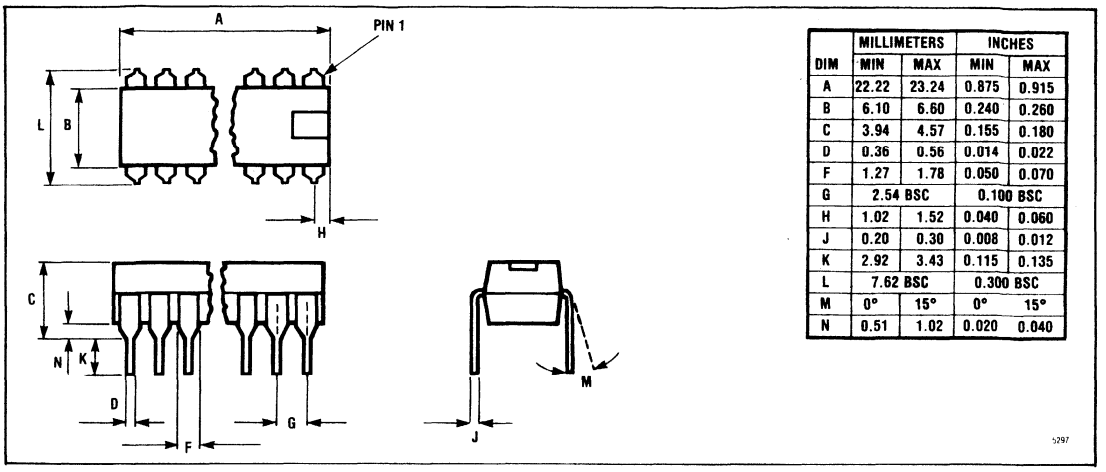
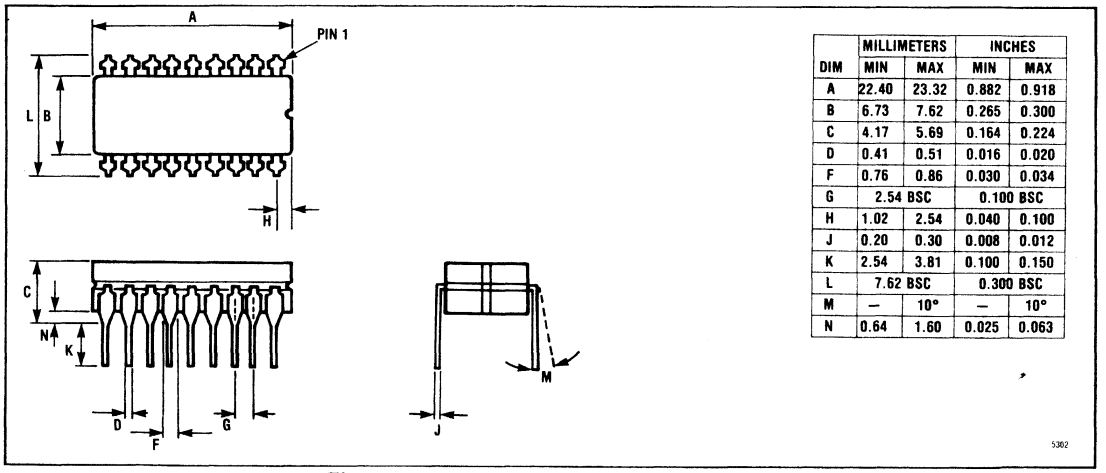


Fig. 7 Guard Time Adjustment



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Fig. 8 18 Lead Dual In-Line Package Plastic (E)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.40	23.32	0.882	0.918
B	6.73	7.62	0.265	0.300
C	4.17	5.69	0.164	0.224
D	0.41	0.51	0.016	0.020
F	0.76	0.86	0.030	0.034
G	2.54 BSC		0.100 BSC	
H	1.02	2.54	0.040	0.100
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.64	1.60	0.025	0.063

Fig. 9 18 Lead "CERDIP" Package

For more information write or phone the leaders in CMOS technology, MITEL Semiconductor:

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MITEL

CMOS MT8862/3 DTMF Decoder

FEB. 1985

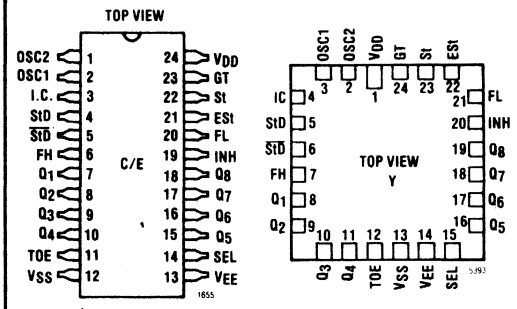
Features

- Hex or 2 of 8 output codes
- Central Office quality detection
- Excellent voice talk-off
- Detect times down to 20ms
- Single supply 5V or 8 to 13V operation
- Latched 3 state buffered outputs
- Detects all 16 DTMF combinations
- Uses inexpensive 3.58MHz crystal
- Low power CMOS circuitry
- Adjustable acquisition & release times

Applications

In DTMF Receivers For
- End to end signaling
- Control systems
- PABX
- Central Office
- Mobile Radio
- Key systems
- Tone to pulse converters

Pin Connections



Ordering Information

Type	Suffix	
MT8862X, MT8863X	C	24-Pin Ceramic DIP
	E	24-Pin Plastic DIP
	Y	24-Pad Chip Carrier

(All types −40°C to +85°C)

Description

The MITEL MT8862 and MT8863 each detect and decode all 16 DTMF tone pairs. The devices accept the high group and low group square wave signals from a DTMF FILTER (Mitel MT8865) and provide a 3 state buffered 8 Bit binary output with a choice of 3 coding formats. The two devices differ only in the specific output code formats they provide. The clock signals are derived from an on chip oscillator requiring only a single resistor and low cost TV crystal as external components. The MT8862/3 is implemented in CMOS technology and incorporates an on chip regulator, providing low power operation and power supply flexibility.

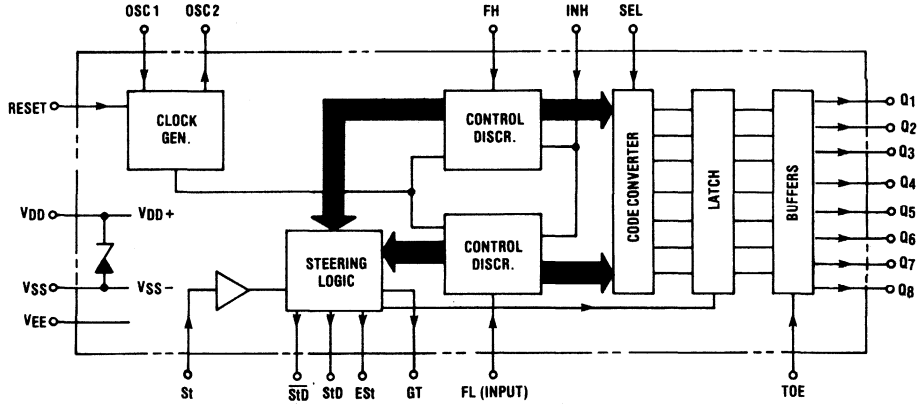


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings

Parameter	Min	Max	
V_{DD} - V_{EE}		15	V
V_{DD} - V_{SS} (Low Impedance Supply)		5.5	V
Voltage on any pin except OSC1, OSC2, V_{SS}	V_{EE} −0.3	V_{DD} +0.3	V
Voltage OSC1 OSC2	V_{SS} −0.3	V_{DD} +0.3	V
Max current at any pin (except V_{DD} & V_{EE})		10	mA
Operating Temperature All Packages	−40	+85	°C
Storage Temperature C/Y Package	−65	+150	°C
Storage Temperature E Package	−65	+125	°C

	Max
Power Dissipation C/Y Packages[1]	1200mW
Power Dissipation E Package[2]	600mW

[1] Derate 16mW/°C above 75°C
[2] Derate 6.3mW/°C above 25°C

All leads soldered to PC board.

Exceeding these ratings may cause permanent damage. Functional operation under these conditions in not implied.

DC Electrical Characteristics

All voltages referenced to V_{EE} unless otherwise noted.

		Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})	V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2				8		13	V	Connections Fig. 5b
3		Internal Logic Ground Voltage (V_{DD} - V_{SS})	V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4				6.0	6.5	7.5	V	Idd = 7mA
5		Operating Supply Current	I_{DD}		1.3	4	mA	5V
6					2.5	5	mA	12V V_{DD} - V_{SS} = 5.5V
7		Internal Logic Ground Pin Current	I_{SS}		5.5?	6.7	mA	12V R_{SSEE} = 900Ω
8		Operating Power Consumption	P_o		6.5		mW	5V
9					66		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)	V_{IH}	3.5			V	5V
11				8.5			V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)	V_{IL}			1.5	V	5V
13						3.5	V	12V
14		High Level Input Voltage OSC1	V_{IHO}	3.5			V	5V
15				10.5			V	12V
16		Low Level Input Voltage OSC1	V_{ILO}			1.5	V	5V Ref V_{SS}
17						1.5	V	12V Ref V_{SS}
18		Steering Input Threshold Voltage	V_{TSt}	2.04	2.27	2.5	V	5V
19				5.4	6.00	6.6	V	12V
20		Pull Down Sink Current (INH, Sel)	I_{SI}	10	25	75	µA	5V
21				10	190	400	µA	12V
22		Pull Up Source Current (TOE)	I_{SO}	2	7	45	µA	5V
23				2	7	45	µA	12V
24		Input High Leakage Current	I_{IH}		0.1	1.5	µA	5V or 12V
25		Input Low Leakage Current	I_{IL}		0.1	1.5	µA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)	V_{OH}	4.9			V	5V
27				11.9			V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)	V_{OL}			0.1	V	5V
29						0.1	V	12V
30		High Level Output Voltage OSC2	V_{OH}	4.9			V	5V
31				11.9			V	12V

DC Electrical Characteristics (Cont'd)

		Characteristics		Symbol	Min	Typ	Max	Unit	Test Conditions
32	OUTPUTS	Low Level Output Voltage OSC2		V_{OL}			0.1	V	5V Ref V_{SS}
33							0.1	V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V V_{OH} = 4.6V
35					0.5	0.8		mA	12V V_{OH} = 11.5V
36			N Channel Sink	I_{OL}	0.8	1.2		mA	5V V_{OL} = 0.4V
37					1.0	1.6		mA	12V V_{OL} = 0.5V
38		Output Drive Current OSC2	P Channel Source	I_{OH}	90	120		µA	5V V_{OH} = 4.6V
39					90	120		µA	12V V_{OH} = 11.5V
40			N Channel Sink	I_{OL}	100	160		µA	5V V_{OL} = 0.4V
41					100	160		µA	12V V_{SS} = 0.5V
42		Tristate Output Current (High Impedance State)	Q_1 - Q_8 = H	I_{OZ}		0.035	1.5	µA	5V Appl V_{OL} = 0V
43			Q_1 - Q_8 = L			0.10	1.5	µA	5V Appl V_{OH} = 5V
44			Q_1 - Q_8 = H			0.10	1.5	µA	12V Appl V_{OL} = 0V
45			Q_1 - Q_8 = L			0.30	1.5	µA	12V Appl V_{OH} = 12V

Test Conditions, T_A = 25° f_c = 3.579545MHz
5V : V_{DD} - V_{EE} = 5V V_{SS} = V_{EE} Connection as Fig. 5a
12V : V_{DD} - V_{EE} = 12V R_{SSEE} = 900Ω Connection as Fig. 5b
Outputs are not loaded unless stated.
For input current parameters only V_{IH} = V_{IHO} = V_{DD}, V_{II} = V_{EE}, V_{ILO} = V_{SS}

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC Electrical Characteristics

		Characteristic		Symbol	Min	Typ*	Max	Unit	Test Conditions Unless Noted V_{DD} = 5V T_A = 25°C f_c = 3.579545MHz
1	DETECTOR	Tone Frequency Deviation Accept		Δf_A			±2.5	% Nom.	
2		Tone Frequency Deviation Reject		Δf_R	±3.5			% Nom.	
3A									
4A									
3X		Tone Present Detection Time	X-Version	t_{DP}	6		10	ms	
4X		Tone Absent Detection Time		t_{DA}	0.6		6	ms	
5		Guard Time		$t_{GT(P\ or\ A)}$	Adjustable. Functions of t_{GT}. See Figs 3, 6, 7.				
6		Time to Receive = (t_{DP} + t_{GTP})		t_{REC}					
7		Invalid Tone Duration (f_n of t_{REC})		$\overline{t_{REC}}$					
8		Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}					
9		Acceptable Drop Out (f_n of t_{ID})		t_{DO}					
10	I/P	FL FH Input Transition Time		t_T			1.0	µs	10% - 90% V_{DD}
11		Capacitance Any Input		C		5	7.5	pF	
12	OUTPUTS	Delay St to Q_1 - Q_8		t_{PL}		8	11	µs	V_{DD} 5V or 12V
13									
14		Delay St to StD		t_{PStD}		12	14	µs	V_{DD} 5V or 12V
15		Sync. Delay Q_1 - Q_8 to StD		t_{QStD}		3.43		µs	
16		Propagation Delay TOE to Q_1 - Q_8	Enable	t_{PTE}		300		ns	V_{DD} 5V
17						200		ns	V_{DD} 12V
18			Disable	t_{PTD}		300		ns	V_{DD} 5V
19						200		ns	V_{DD} 12V
20	CLOCK	Crystal/Clock Frequency		f_c	3.5759	3.5795	3.5831	MHz	OSC 1 / OSC 2
21		Clock Input (OSC 1)	Rise Time	t_{LHCI}			110	ns	10% - 90% V_{DD} − V_{SS} / Externally Applied Clock
22			Fall Time	t_{HLCI}			110	ns	
23			Duty Cycle	DC_{CI}	40	50	60	%	
24		Clock Output (OSC 2)	Capacitive Load	C_{LO}			30		
25									

Fig. 2 Coding Tables **a) Output Coding**

Original Tone Character		TOE	SEL	MT8862 Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	MT8863 Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
	X	L	Ø	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
DR	1	H	L	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L	H
	2	H	L	L	L	H	L	L	L	H	L	L	L	H	L	L	L	H	L
	3	H	L	L	L	H	H	L	L	H	H	L	H	L	L	L	L	H	H
	4	H	L	L	H	L	L	L	H	L	L	H	L	L	L	L	H	L	L
	5	H	L	L	H	L	H	L	H	L	H	H	L	H	L	L	H	L	H
	6	H	L	L	H	H	L	L	H	H	L	H	H	L	L	L	H	H	L
	7	H	L	L	H	H	H	L	H	H	H	L	L	L	H	L	H	H	H
	8	H	L	H	L	L	L	H	L	L	L	L	L	H	H	H	L	L	L
	9	H	L	H	L	L	H	H	L	L	H	L	H	L	H	H	L	L	H
	0	H	L	L	L	L	L	H	L	H	L	L	H	H	L	H	L	H	L
D	*	H	L	H	L	H	L	H	L	H	H	H	H	L	H	H	L	H	H
	#	H	L	H	L	H	H	H	H	L	L	H	L	L	H	H	H	L	L
	A	H	L	H	H	L	L	H	H	L	H	L	H	H	H	H	H	L	H
	B	H	L	H	H	L	H	H	H	H	L	H	L	H	H	H	H	H	L
	C	H	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H
	D	H	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L
DR	1	H	H	H	H	H	L	H	H	H	L	L	L	L	H	L	L	L	H
	2	H	H	H	H	L	H	H	H	H	L	L	L	H	L	L	L	L	H
	3	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	L	H
	4	H	H	H	H	H	L	H	H	L	H	L	L	L	H	L	L	H	L
	5	H	H	H	H	L	H	H	H	L	H	L	L	H	L	L	L	H	L
	6	H	H	H	L	H	H	H	H	L	H	L	H	L	L	L	L	H	L
	7	H	H	H	H	H	L	H	L	H	H	L	L	L	H	L	H	L	L
	8	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	H	L	L
	9	H	H	H	L	H	H	H	L	H	H	L	H	L	L	L	H	L	L
	0	H	H	H	H	L	H	L	H	H	H	L	L	H	L	H	L	L	L
D	*	H	H	H	H	H	L	L	H	H	H	L	L	L	H	H	L	L	L
	#	H	H	H	L	H	H	L	H	H	H	L	H	L	L	H	L	L	L
	A	H	H	L	H	H	H	H	H	H	L	H	L	L	L	L	L	L	H
	B	H	H	L	H	H	H	H	H	L	H	H	L	L	L	L	L	H	L
	C	H	H	L	H	H	H	H	L	H	H	H	L	L	L	L	H	L	L
	D	H	H	L	H	H	H	L	H	H	H	H	L	L	L	H	L	L	L

b) Inhibit Function

Detected Character	INH	ESt
None	Ø	L
X	L	H
DR	H	H
D	H	L

c) Steering

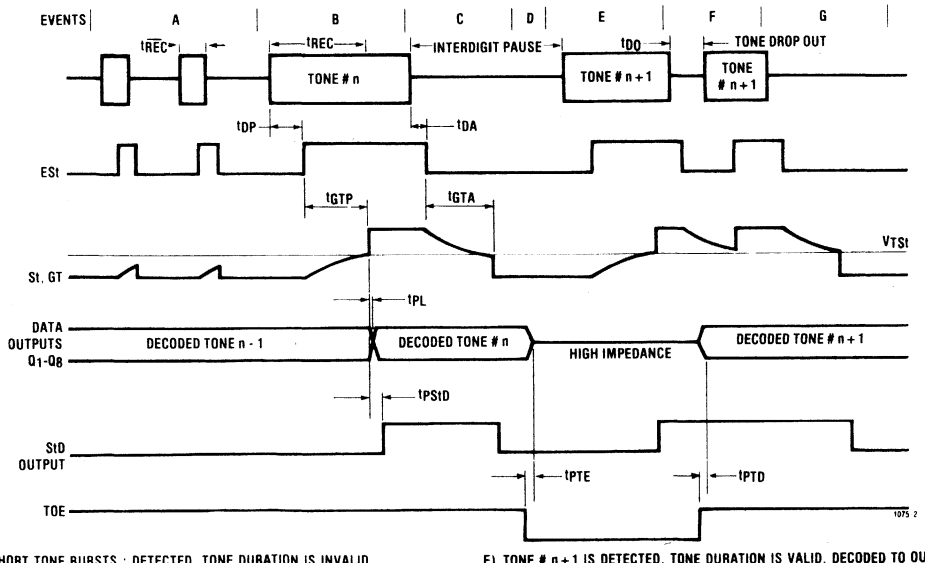
ESt	St	GT	StD*	$\overline{StD}$*
L	L	L	L	H
H	L	Z	L	H
L	H	Z	H	L
H	H	H	H	L

* DELAYED FROM St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH
X = ANY CHARACTER
L = LOGIC LOW
Z = HIGH IMPEDANCE
Ø = "DON'T CARE" LOGIC HIGH OR LOW



A) SHORT TONE BURSTS : DETECTED. TONE DURATION IS INVALID.
B) TONE # n IS DETECTED. TONE DURATION IS VALID. DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STATE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n+1 IS DETECTED. TONE DURATION IS VALID. DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE # n+1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n+1 IS DETECTED AND VALIDATED.

Fig. 3 Timing Diagram

Pin Description

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.579545MHz crystal with parallel 5M Ω resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only (reset) Note 1	
4	StD	Delayed Steering Output. Flags when a valid tone pair has been received. When the St voltage exceeds V_{TSt}, the output latch is updated, then StD presents a logic high. Returns to logic low when St voltage falls below V_{TSt}. (See Fig. 2 c)	
5	$\overline{StD}$	Inverted StD.	
6	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter.	
7	Q1	Data outputs 3 state buffered.	
8	Q2	Provides 4 bit binary word (SEL low) or half of 2 of 8 binary word (SEL high),	
9	Q3	corresponding to the tone pair decoded, when enabled by TOE.	
10	Q4	See Fig. 2 for state table.	
11	TOE	3 state output enable input. Logic high on this input enables outputs Q1-Q8. Internal pull up	
12	V_{SS}	Internal logic ground. For V_{DD} - V_{EE} = 5V, V_{SS} connected to V_{EE}. For V_{DD} - V_{EE} > 8V, V_{SS} connected via resistor to V_{EE} see Fig. 5	
13	V_{EE}	Negative power supply. External logic ground.	
14	SEL	Output Code Select. Logic low on this pin selects Q1-Q4, Q5-Q8 to provide 2 different 4 bit binary output codes. A logic high selects Q1-Q8 to provide a 2 of 8 output code (See Fig. 2).	
15	Q5	Data outputs 3 state buffered.	
16	Q6	Provides 4 bit binary word (SEL low) or half of 2 of 8 binary word (SEL high),	
17	Q7	corresponding to the tone pair decoded, when enabled by TOE.	
18	Q8	See Fig. 2 for state table.	
19	INH	Inhibit input. Logic high inhibits detection of tones (D tones in Fig. 2a) representing characters #, *, A, B, C, D. Internal pull down.	
20	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter.	
21	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low.	
22	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage less than V_{TSt} on this pin frees the device to accept a new tone pair. See Fig. 2 c and Functional Description.	
23	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Fig. 2 c)	
24	V_{DD}	Positive power supply	

Note 1: Must be left open circuit.

Functional Description

The Mitel MT8862 is a CMOS Digital DTMF Detector and Decoder. The MT8863 is an identical device except that it provides a different set of output codes. The codes of the MT8863 are the same as those provided by Mitel's MT8820. Used in conjunction with a suitable DTMF filter (MITEL MT8865) the MT8862 or MT8863 can detect and decode all 16 Standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MT8862(3) must be preceeded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sine wave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The High Group and Low Group rectangular waves are applied to the MT8862(3)'s FH and FL inputs respectively. Mitels MT8865 DTMF Filter provides these functions.

Within the MT8862(3) the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators Fig. 1) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both High Group and Low Group signals have been simultaneously detected a flag ESt (Logic High) is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig. 3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of "tone absent" before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig. 7a) is charged via resistor R from ESt when a DTMF tone pair is detected. After a period t_{GTP} V_C exceeds the St input threshold voltage V_{TSt} setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Fig. 2c) and timing diagram (Fig. 3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents an 8 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs Q_1 to Q_8. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig. 7a) falling below V_{TSt}.

Increasing the "time to receive" t_{REC} tends to further improve "talk-off" performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause time t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite affect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig. 7.

When Q_1 - Q_8 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MT8862(3) may be operated from either a 5 volt or 8 to 13 volt supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig. 5.
When using the MT8862(3) with the MT8865 DTMF Filter it is only necessary to use the MT8865 crystal oscillator (see Fig. 6). When using the higher supply voltage range the 8865 OSC2 output should be capacitively coupled to the 8862(3) OSC1 input as shown in Fig. 6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk-off due to the reduced number of detectable tones.

The MT8862X differs from the MT8862A in that it has an improved decode algorithm giving enhanced talk-off performance. It also features a faster and more closely-controlled response time (see t_{DP} and t_{DA}). The MT8862X is recommended in preference to the MT8862A for all new designs, and may normally be used as a direct replacement in existing designs, provided that consideration is given to the effect of shorter response-time on system performance. Similarly, the MT8863X is the preferred replacement for the MT8863A.

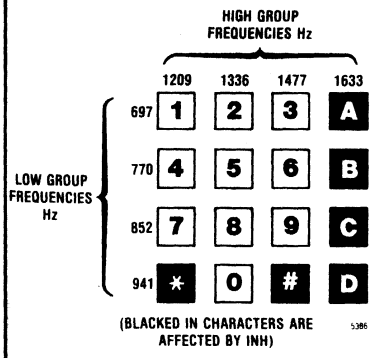


Fig. 4 DTMF Matrix Indicating Character - Tone Pair Correspondence

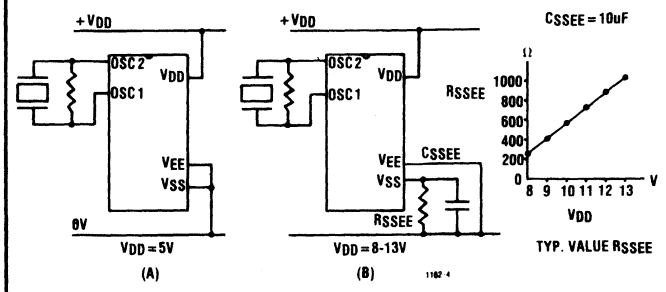


Fig. 5 Power Supply Connection Options

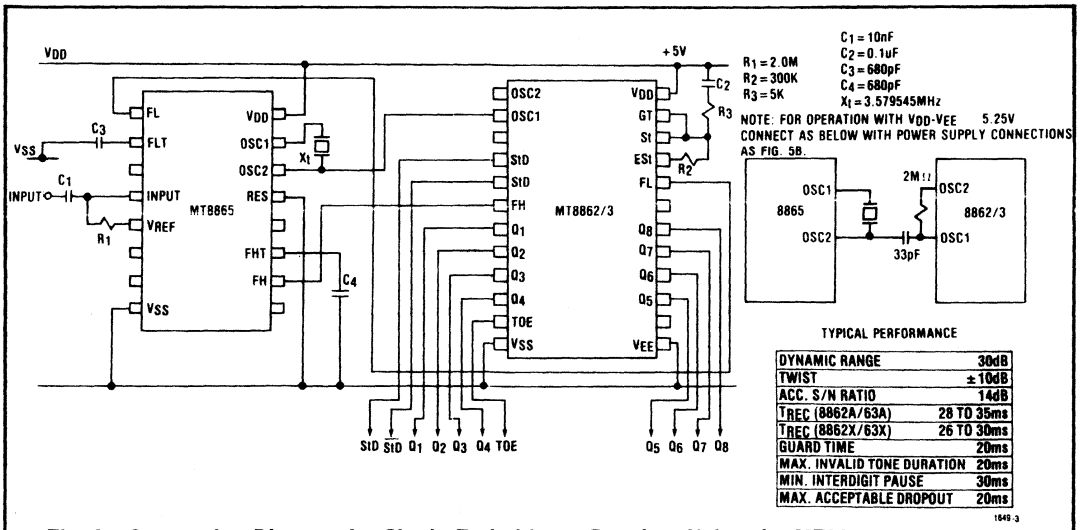


Fig. 6 Connection Diagram for Single Ended Input Receiver Using the MT8865 (5V Operation)

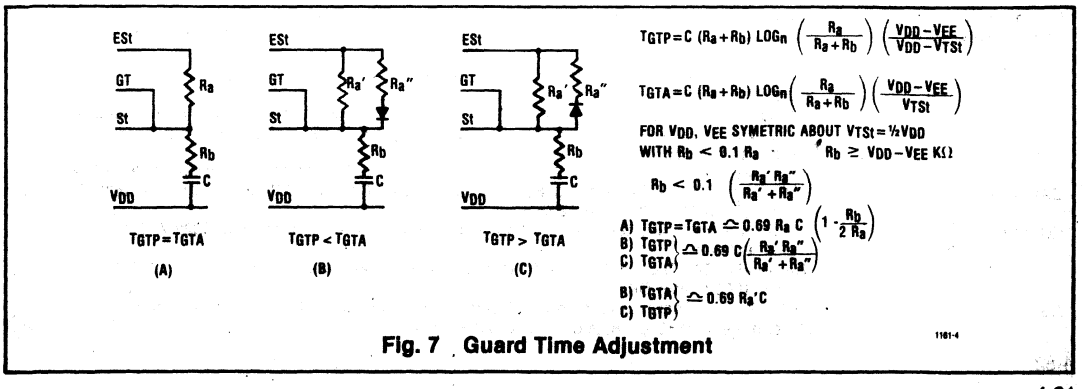


Fig. 7 Guard Time Adjustment

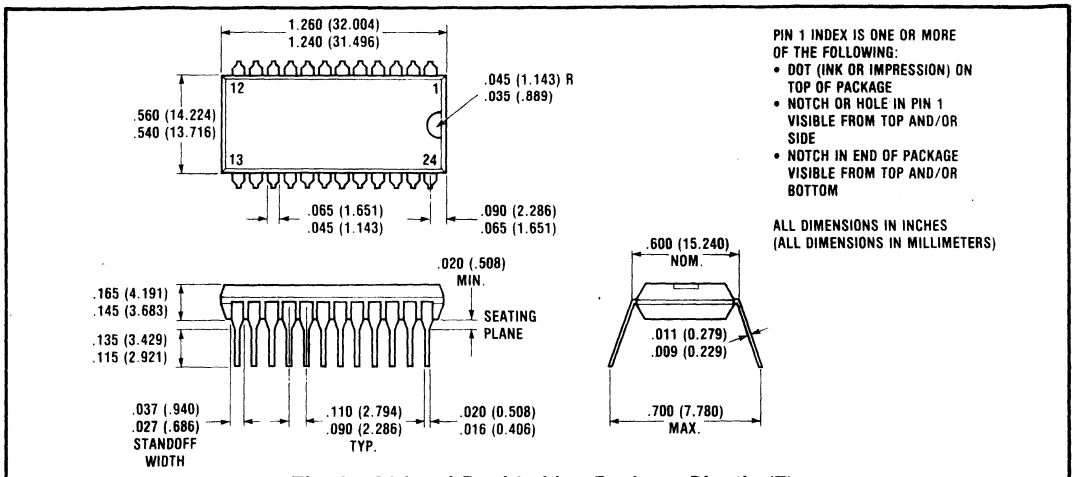


Fig. 8 24 Lead Dual In-Line Package Plastic (E)

1651

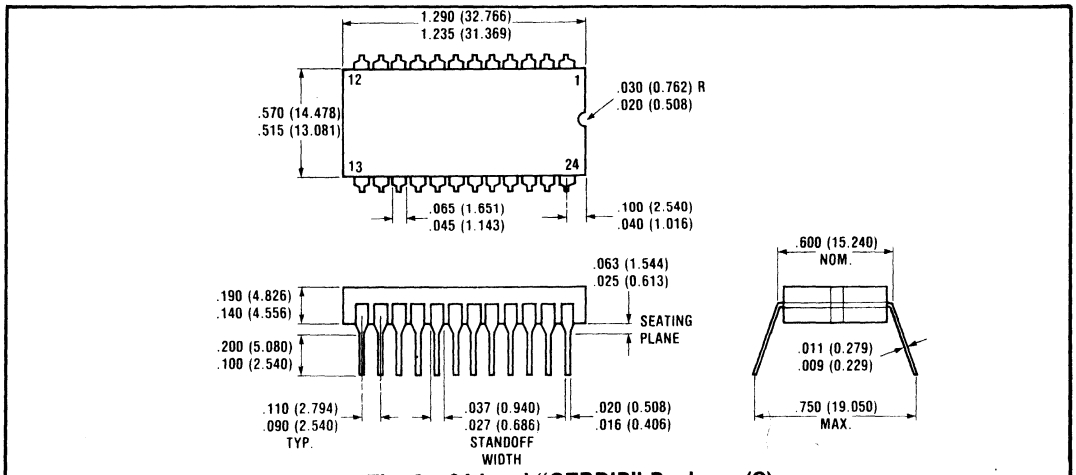


Fig. 9 24 Lead "CERDIP" Package (C)

1652

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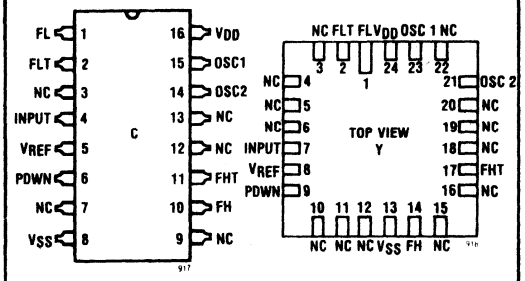
ISO²-CMOS™ MT8865
DTMF Filter

FEB. 1985

Features

- Provides DTMF high and low group filtering
- Hard limiting on filter outputs
- 6 pole band pass high and low group filters
- 40 dB (typ) Intergroup attenuation
- Dial tone suppression
- +5 to +12V single supply operation
- Logical power down
- Uses inexpensive 3.58MHz crystal
- Wide dynamic range 30dB

Pin Connections



Ordering Information

MT8865XC	16-Pin Cerdip CIP
MT8865XE	16-Pin Plastic DIP
MT8865XY	24-Pad Chip Carrier

Applications

In DTMF Receivers For:

- End to end signaling
- Control systems
- PABX
- Central Office
- Mobile Radio
- Key systems
- Tone to pulse converters

Description

The MITEL MT8865 contains both the high group and low group filtering and comparator functions required to implement a Dual Tone Multi Frequency tone receiver using a MITEL DTMF Digital Detector (i.e. MITEL MT8860/62/63). Switched capacitor techniques are used to implement the filters and the device is fabricated using MITEL's DOUBLE POLY ISO² - CMOS™ high density technology. The filter clocks are derived from an on-chip oscillator requiring only a low cost TV crystal as external components. The MT8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

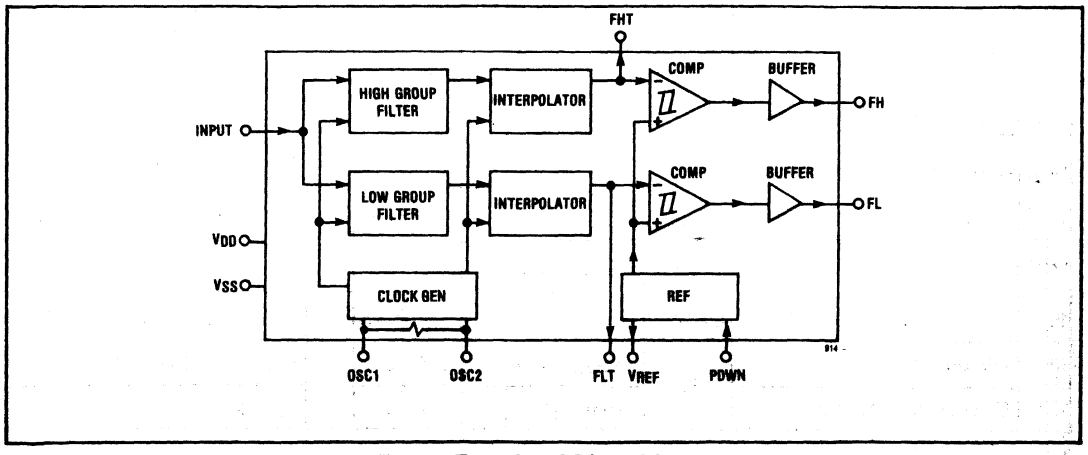


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings†

Parameter		Min	Max		Parameter		Max
$V_{DD} - V_{SS}$			15	V	Power Dissipation	C/Y Packages[1]	850mW
Voltage on any pin		$V_{SS} - 0.3$	$V_{DD} + 0.3$	V		E Package[2]	400mW
Max. current at any pin			10	mA	[1] Derate 16mW/°C above 75°C. [2] Derate 6.3mW/°C above 25°C. All leads soldered to PC board.		
Operating Temperature	All Packages	−40°C	+85	°C			
Storage Temperature	C/Y Packages	−65°C	+150	°C			
	E Package	−65°C	+125	°C			

† Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics

All voltages referenced to V_{SS} unless otherwise noted.

		Characteristics		Symbol	V_{DD} = 5V			V_{DD} = 12V			Unit	Test Conditions Unless Noted T_A = 25°C f_{CLK} = 3.579545MHz
					Min	Typ	Max	Min	Typ	Max		
1	SUPPLY	Operating Supply Voltage		V_{DD}	4.75					13	V	
2		Operating Supply Current		I_{DD}		1.2	3		5	10	mA	PDWN = V_{SS}
3		Standby Supply Current		I_{DDS}		70	100		300	500	µA	PDWN = V_{DD}
4		Operating Power Consumption		P_O		6			60		mW	PDWN = V_{SS} Fig. 5(c)
5		Standby Power Consumption		P_S		0.5			1.5		mW	PDWN = V_{DD} C = 15pF
6	INPUTS	Low Level Input Voltage	PDWN & OSC1	V_{IL}			1.5			3.5	V	
7		High Level Input Voltage		V_{IH}	3.5			8.5			V	
8		Pull Down Sink Current	PDWN	I_{IH}		3	6		12	24	µA	
9		Input Current	OSC1	I_I		±2.5			±6		µA	
10	OUTPUTS	Low Level Output Voltage	FL, FH	V_{OL}			0.1			0.1	V	No load
11		High Level Output Voltage	OSC2	V_{OH}	4.9			11.9			V	
12		Output Drive Current — N Channel Sink	FL, FH	I_{OL}	0.2			0.5			mA	V_{OL} = 0.4V (5V)
13			OSC2		0.1			0.25			mA	V_{OL} = 1.2V (12V)
14		P Channel Source	FL, FH	I_{OH}	0.2			0.5			mA	V_{OH} = 4.6V (5V)
15			OSC2		0.1			0.25			mA	V_{OH} = 10.8V (12V)
16		Output Voltage	V_{REF}	V_{REF}	2.3		2.6	5.4		6.2	V	No Load
17		Output Resistance		R_{OR}			16			8	kΩ	

AC Electrical Characteristics

		Characteristics		Symbol	Min	Typ	Max	Unit	Test Conditions Unless Noted T_A = 25°C f_c = 3.579545MHz V_{DD} = 4.75 – 13V	
1		Dynamic Range			30		36	dB		
2		Valid Input Signal Levels					$V_{DD}/2$	V_{pp}		
3		(Each tone of composite signal)			27.9		883	mVrms	V_{DD} = 5V	
4					67.0		2120	mVrms	V_{DD} = 12V	
5		Input Impedance		Z_I	10			MΩ		
6		Passband Ripple		A_V		±0.3	±1.0	dB	See Note 1	
7		Low Group	Lower Limit	f_{LL}		670	684	Hz		
8		1dB Bandwidth	Upper Limit	f_{LU}	958	990		Hz		
9	F	High Group	Lower Limit	f_{HL}		1162	1188	Hz		
10	I	1dB Bandwidth	Upper Limit	f_{HU}	1660	1740		Hz		
11	L	Intergroup	Low Group with	IR_{L1209}	34	45		dB	1209Hz	w.r.t.
12	T		High Tone	IR_{L1477}	36	40		dB	1477Hz	770Hz
13	E	Rejection	High Group with	IR_{H941}	38	50		dB	941Hz	w.r.t.
14	R		Low Tone	IR_{H770}	36	40		dB	770Hz	1336Hz
15		Dial Tone	Low Group	DR_{L440}	40	60		dB	440Hz	w.r.t
16				DR_{L350}	28	30		dB	350Hz	770Hz
17		Rejection	High Group	DR_{H440}	52	60		dB	440Hz	w.r.t.
18				DR_{H350}	50	55		dB	350Hz	1336Hz
19		FHT FLT Maximum Permissible Load		R_{LFT}	250			KΩ		
20				C_{LFT}			1000	pF		
21	L	Output Rise Time	FL, FH	t_{TLHO}		90	150	ns	10% to	
22	I M	Output Fall Time		t_{THLO}		60	100	ns	90% V_{DD}	
23		Crystal/Clock Freq.	OSC 1, OSC 2	f_c	3.5759	3.5795	3.5831	MHz		
24		Clock	Rise Time	t_{LHCI}			110	ns	10% to	Externally
25	C	Input	Fall Time	t_{HLCI}			110	ns	90% V_{DD}	Applied
26	L	(OSC 1)	Duty Cycle	DC_{CI}	40	50	60	%		Clock
27	O C K	Clock Output OSC 2	Capacitive Load	C_{LOC}			30	pF	Unbalanced load see page 6	
28		Capacitance Any Input		C_I		5	7.5	pF		

Note 1. Passband ripple measured with respect to a passband gain of 0 dB ± 1 dB.

Pin Description

DIP Pin	Name	Description
1	FL	Low group limiter output.
2	FLT	Test output. Monitors low group filter output. Decouple to V_{SS} with 680pF capacitor.
3	NC	Not connected.
4	INPUT	Tone signal input (single ended).
5	V_{REF}	Internal reference, can be used to bias input via 2MΩ resistor.
6	PDWN	Power down active high. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.
7	NC	Not connected.
8	V_{SS}	Negative (0V) power supply.
9	NC	Not connected.
10	FH	High group limiter output.
11	FHT	Test output. Monitors high group filter output. Decouple to V_{SS} with 680pF capacitor.
12	NC	Not connected.
13	NC	Not connected.
14	OSC2	Clock Output. — 3.579545 MHz crystal connected between these pins completes internal oscillator.
15	OSC1	Clock Input.
16	V_{DD}	Positive power supply.

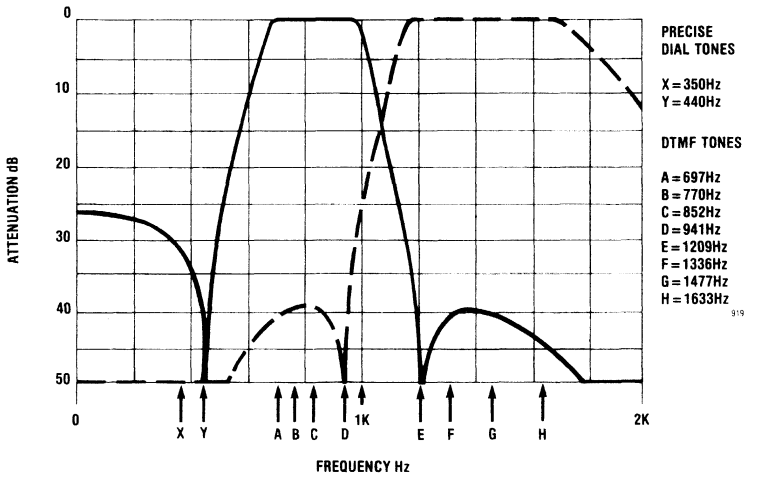


Fig. 2 Typical Filter Characteristics

Functional Description

The MT8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves, to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of one of MITEL's range of DTMF Digital Decoders (MT8860/62/63). See Fig. 3.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig. 2) also incorporates a notch at 440Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting. The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MT8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig. 3) or via a differential buffer to a telephone line (Fig. 4). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input capacitively coupled, this is achieved by connecting the signal input to V_{REF} (Pin 5) via a 2MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680pF capacitors.

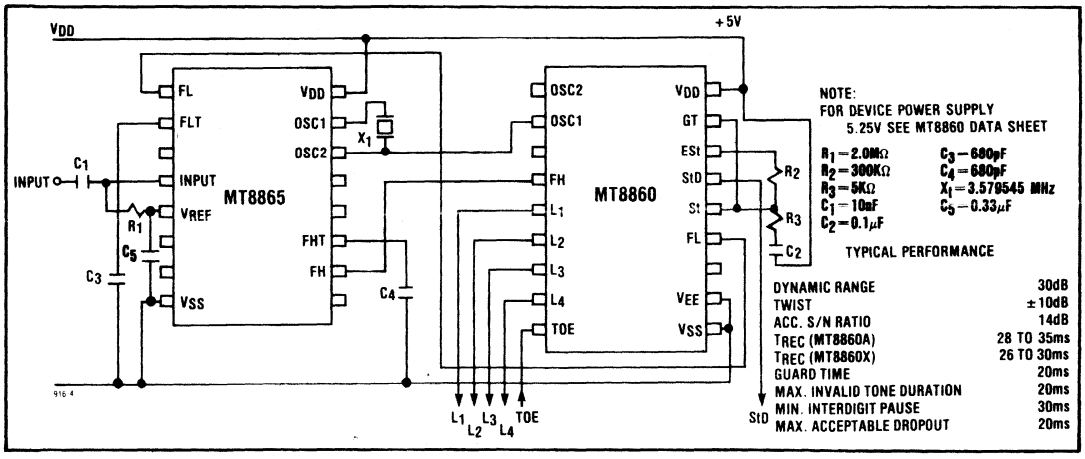


Fig. 3 Connection Diagram for Single Ended Input Receiver Using the MT8860 (5V Operation)

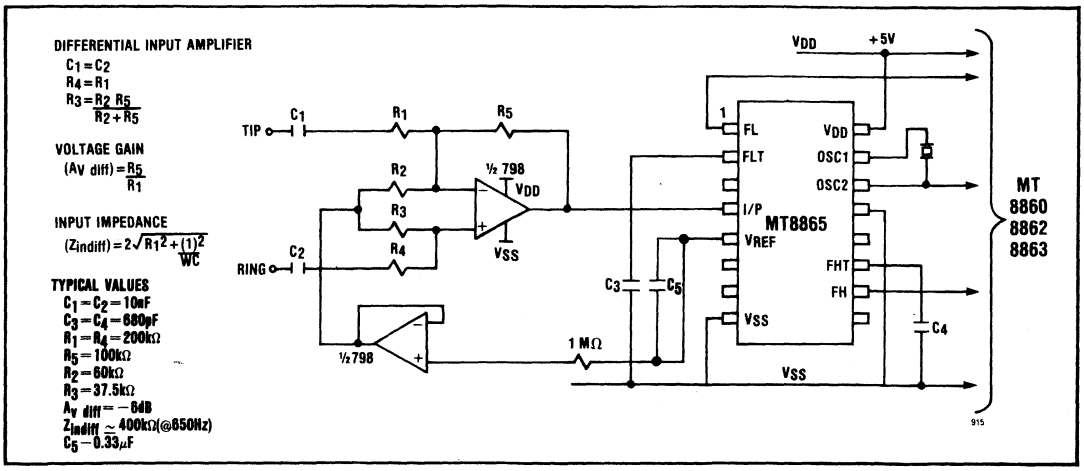


Fig. 4 Circuit for Connection to a Telephone Line

The MT8865 and its companion, the MT8860 DTMF decoder, can share a crystal by cascading the oscillator output (OSC2) to the adjacent device oscillator input (OSC1). The recommended circuit is shown in Figure 5.

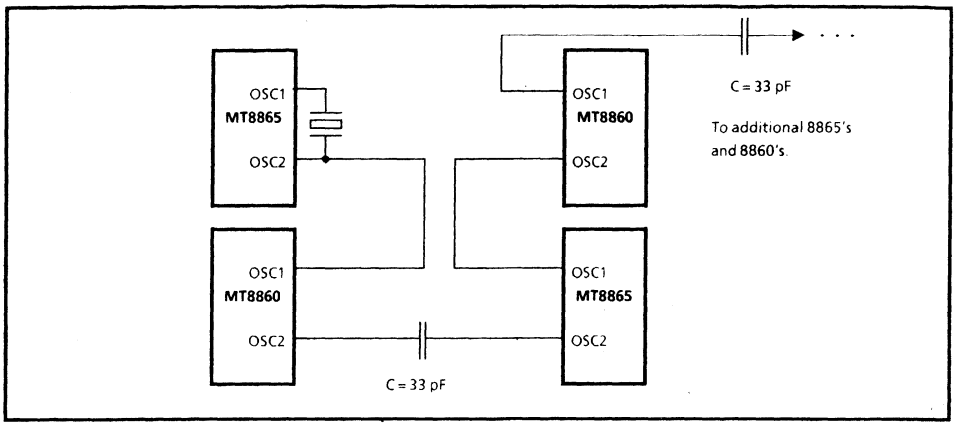


Fig. 5 Cascaded Oscillator Configuration

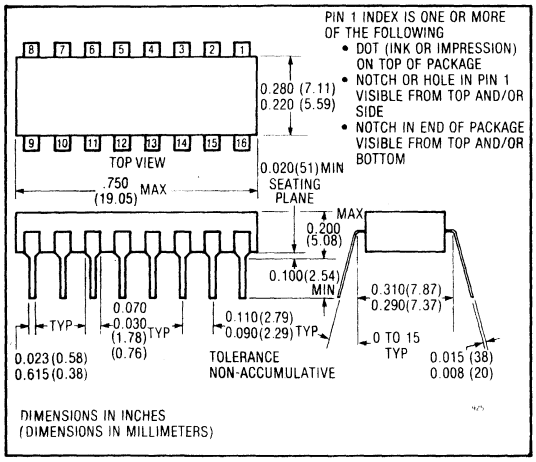


Fig. 6 16 Lead Dual In-Line Package Plastic (E)

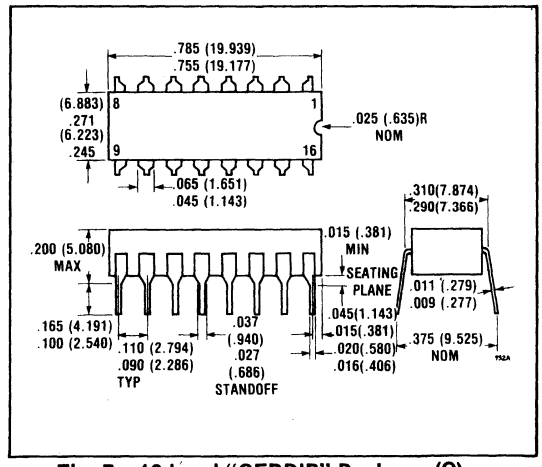


Fig. 7 16 Lead "CERDIP" Package (C)

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ISO²-CMOS MT8870
Integrated DTMF Receiver

9161-002-031-NA ISSUE 2 January 1985

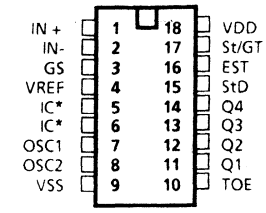
Features

- Complete DTMF receiver
- Low power consumption
- Internal gain setting amplifer
- Adjustable guard time
- Central Office Quality

Applications

- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote Control
- Personal Computers

Pin Connections



*connect to VSS

Ordering Information

MT8870BE 18 PIN PLASTIC
MT8870BC 18 PIN CERDIP

Description

The MT8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

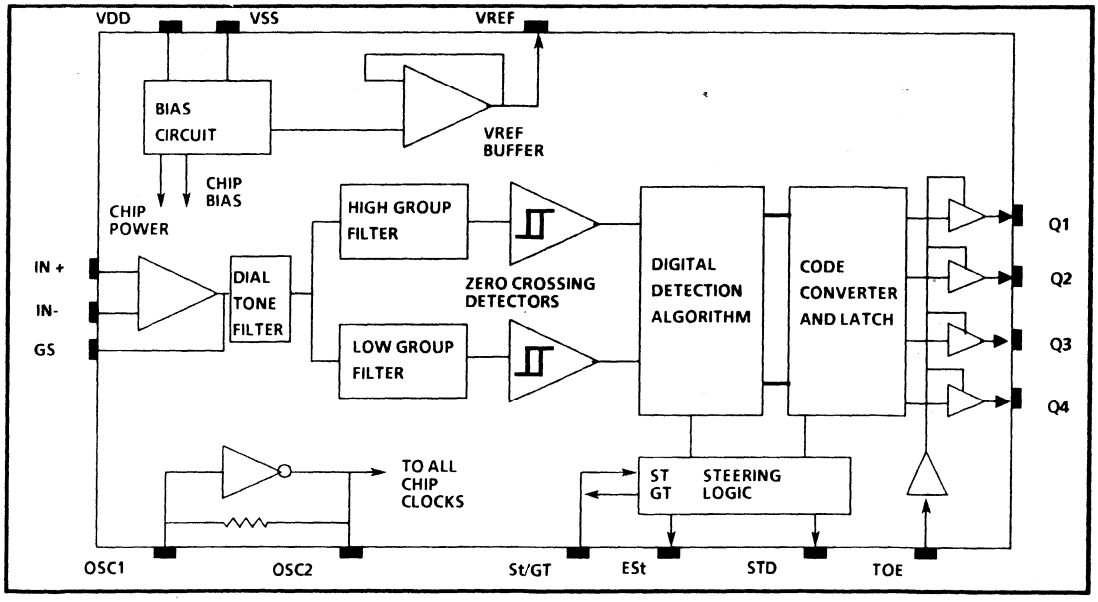


Figure 1. Functional Block Diagram

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}			6	V
2	Voltage on any pin		V_{SS}-0.3	V_{DD} + 0.3	V
3	Current at any pin			10	mA
4	Operating temperature		-40	+ 85	°C
5	Storage temperature		-65	+ 150	°C
6	Package power dissipation			1000	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C All leads soldered to board.

DC Electrical Characteristics

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions†
1	SUPPLY	Operating supply voltage		4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15	45	mW	f = 3.58MHz; V_{DD} = 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5		Low level input voltage	V_{IL}			1.5	V	
6		Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	15	μA	TOE (pin 10) = 0V
8		Input impedance (IN + , IN-)	R_{IN}		10		MΩ	@ 1 kHz
9		Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			0.03	V	No load
11		High level output voltage	V_{OH}	4.97			V	No load
12		Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4V
13		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
14		V_{Ref} output voltage	V_{Ref}	2.4		2.8	V	No load
15		V_{Ref} output resistance	R_{OR}		10		KΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
V_{DD} = 5V ± 5%, V_{SS} = 0V. Voltages are with respect to ground (V_{SS}) unless otherwise stated

Operating Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power suply rejection	PSRR		60		dB	1 KHz
5	Common mode rejection	CMRR		60		dB	-3.0V ≤ V_{IN} ≤ 3.0V
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_C		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \ge 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		KΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

† V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25° C

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ†	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+ 1	dBm	1,2,3,5,6,9
						883	mV_{RMS}	1,2,3,5,6,9
2		Positive twist accept			10		dB	2,3,6,9
3		Negative twist accept			10		dB	2,3,6,9
4		Freq. deviation accept		± 1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject		± 3.5%			Nom.	2,3,5,9
6		Third tone tolerance			-16		dB	2,3,4,5,9,10
7		Noise tolerance			-12		dB	2,3,4,5,7,9,10
8		Dial tone tolerance			+ 22		dB	2,3,4,5,8,9,11

† V_{DD} = 5 V, V_{SS} = 0 , T_A = 25° C and f_C = 3.579545 MHz using test circuit shown in Figure 2

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude
6. Tone pair is deviated by ± 1.5% ± 2Hz
7. Bandwidth limited (3KHz) Gaussian noise
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %
9. For an error rate of better than 1 in 10,000
10. Referenced to lowest level frequency component in DTMF signal
11. Referenced to the minimum valid accept level

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	$\overline{t_{REC}}$	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	t_{DO}	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	μs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12		μs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		μs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	RL = 10KΩ CL = 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	RL = 10KΩ CL = 50 pF
26	CLOCK	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
27		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
28		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
29		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
30		Capacitive load (OSC2)	C_{LO}			30	pF	

†V_{DD} = 5V, V_{SS} = 0V T_A = 25° C and f_C = 3.579545 MHz, using test circuit in Figure 2.

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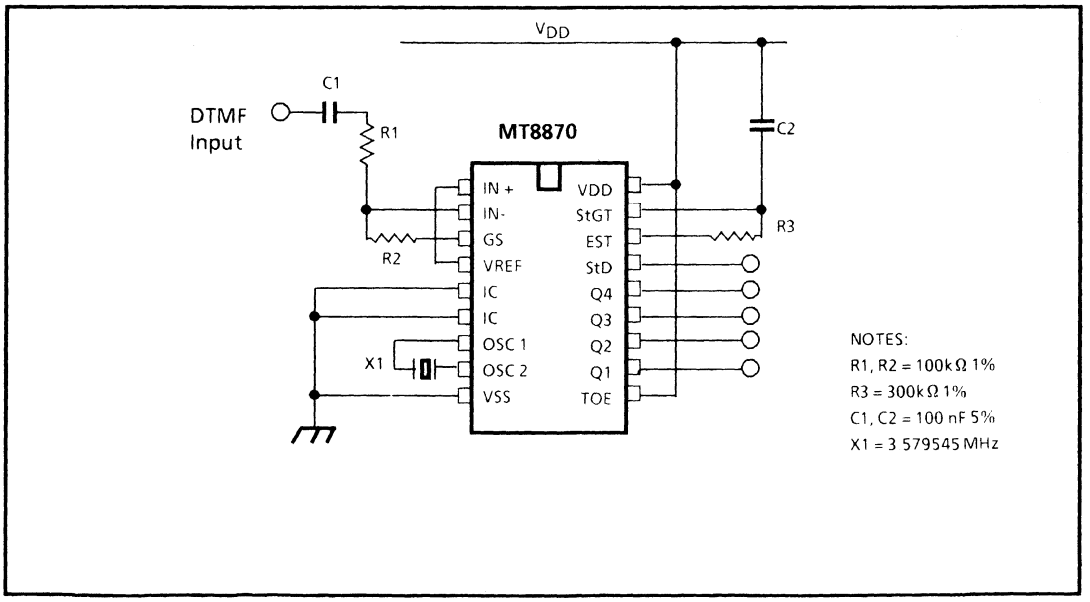
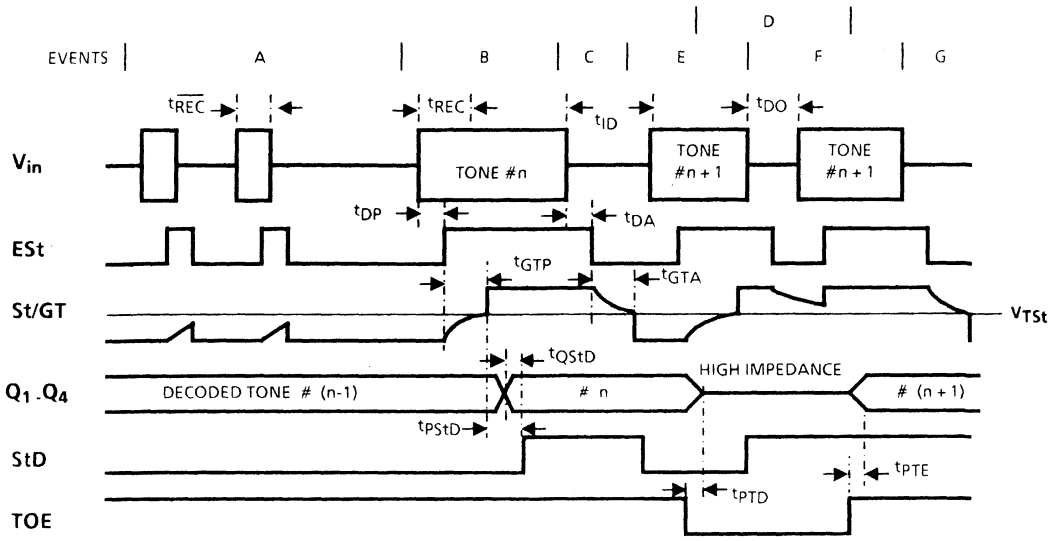


Figure 2. Single Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	Non-inverting op-amp input.
2	IN-	Inverting op-amp input.
3	GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{REF}	Reference voltage output, nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig.2).
5	IC	Internal connection. Must be tied to V_{SS}.
6	IC	Internal connection. Must be tied to V_{SS}.
7	OSC1	Clock input.
8	OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative power supply input.
10	TOE	3- state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull up.
11-14	Q1-Q4	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Fig. 5).
15	StD	Delayed steering output.Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/Gt falls below V_{TSt}
16	ESt	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	St/GT	Steering input/guard time output (bi-directional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply input.



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE
E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE)
F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCED
G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DECTECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4	4-BIT DECODED TONE OUTPUT
StD	DELAYED STEERING OUTPUT. INDICTES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSISTUTING A VALID SIGNAL.
TOE	TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID DTMF SIGNALS
t_{DO}	MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS
t_{DA}	TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS
t_{GTP}	GUARD TIME, TONE PRESENT
t_{GTA}	GUARD TIME, TONE ABSENT

Figure 3. Timing Diagram

Functional Description

The MT8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which seperates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Seperation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band pass filters, the band-widths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig. 4). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Fig. 6) to rise as the capacitor discharges.

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponing 4-bit code (see Fig. 5) into the output latch. At this point the GT output is activated and drives v_c to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to

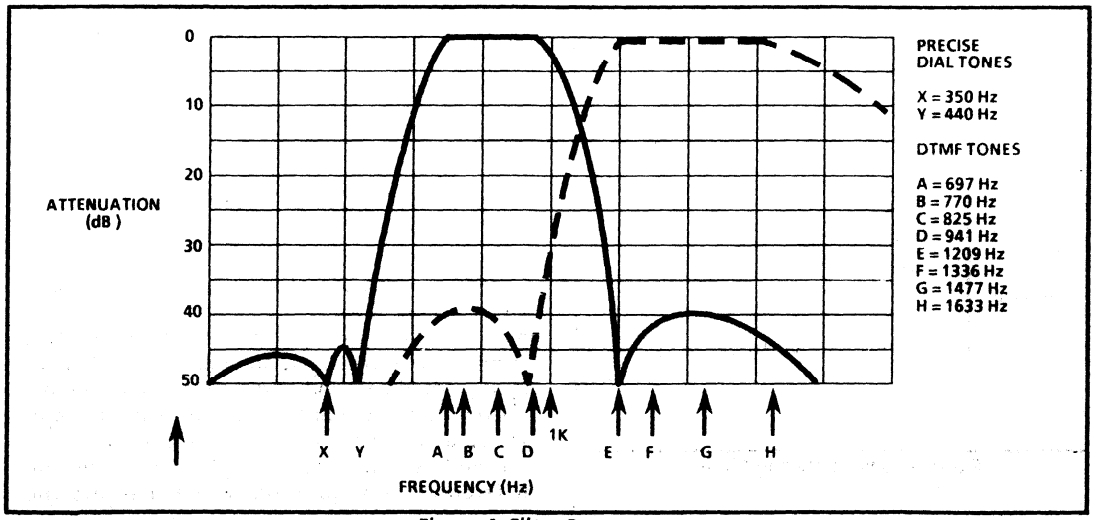


Figure 4. Filter Response

F_{LOW}	F_{HIGH}	NO	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMEDANCE

Figure 5. Functional Decode Table

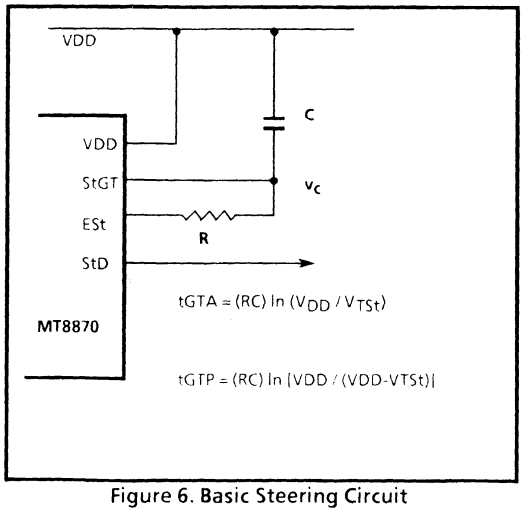


Figure 6. Basic Steering Circuit

validate the interdigit pause between signals. Thus, as well as rejecting signals too short too be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Fig. 6 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independantly the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast aquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 7.

Differential Input Configuration

The input arrangement of the MT8870 provides a differential-input operational amplifier as well as a bias source(V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Fig. 2 with the op-amp connected for unity gain and V_{Ref} biasing the input at $\frac{1}{2}V_{DD}$. Fig. 8 shows the differential configuration, which permits the

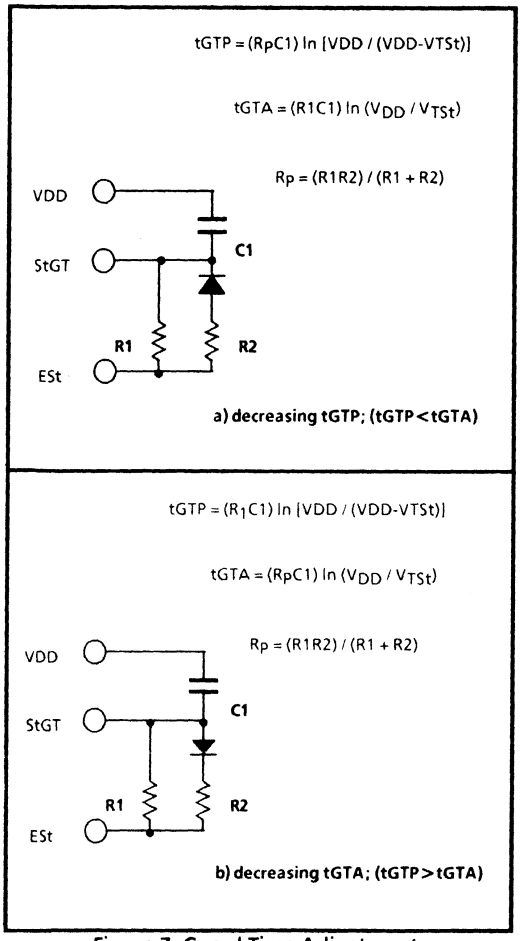


Figure 7. Guard Time Adjustment

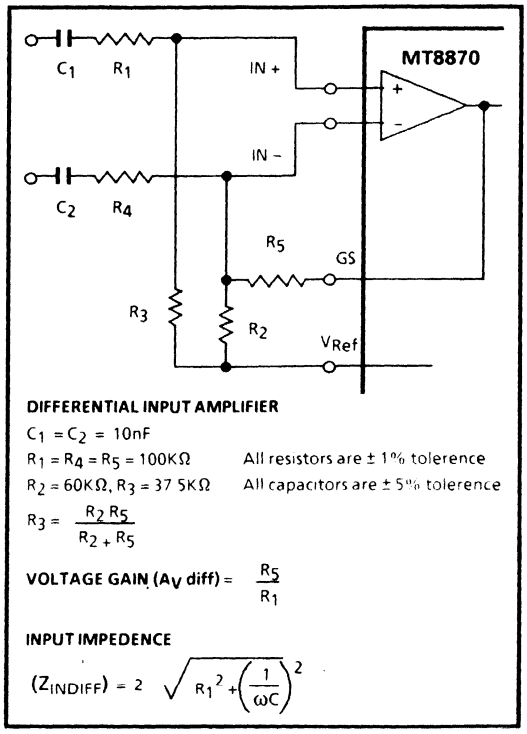


Figure 8. Differential Input Configuration

adjustment of gain with the feedback resistor R_5.

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.58 MHz crystal and is normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible to configure several MT8870 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Fig. 9 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie; precision balancing capacitors are not required.

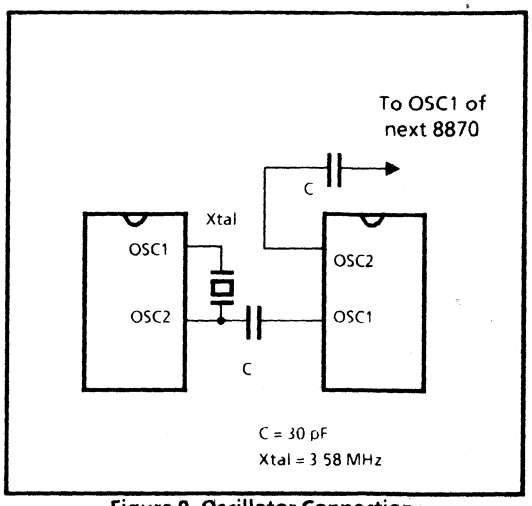


Figure 9. Oscillator Connection

ISO²-CMOS **MT8870-1**
Integrated DTMF Receiver

9161-002-051-NA ISSUE 1 June 1985

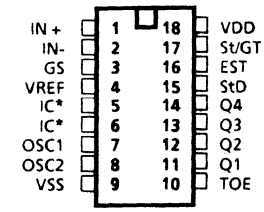
Features

- Complete DTMF receiver
- Low power consumption
- Internal gain setting amplifer
- Adjustable guard time
- Central Office Quality

Applications

- Receiver Systems for British Telecom(BT) or CEPT Spec
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote Control
- Personal Computers

Pin Connections



*connect to VSS

Ordering Information

MT8870BE-1 18 PIN PLASTIC DIP
MT8870BC-1 18 PIN CERDIP

Description

The MT8870-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

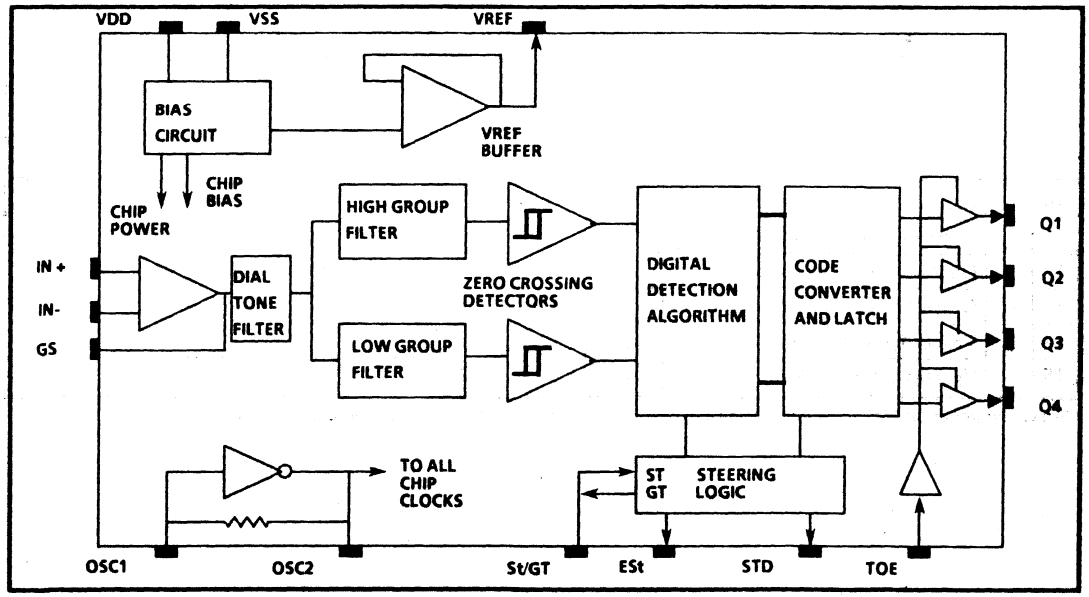


Figure 1. Functional Block Diagram

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}-V_{SS}		6	V
2	Voltage on any pin (other than supply)	V_{MAX}	V_{SS}-0.3	V_{DD} + 0.3	V
3	Current at any pin (other than supply)	I_{MAX}		10	mA
4	Operating temperature	T_A	-40	+ 85	°C
5	Storage temperature	T_{STG}	-65	+ 150	°C
6	Package power dissipation	P_{DISS}		1000	mW

†Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C All leads soldered to board.

Recommended Operating Conditions Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions†
1		Positive supply voltage	V_{DD}		+ 5		V	V_{SS} = 0V
2		Oscillator clock frequency	fc		3.579545		MHz	Colour Burst Crystal
3		Oscillator frequency tolerance	Δfc		± 0.1		%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics V_{DD} = 5V ± 5%, V_{SS} = 0V. Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions†
1	SUPPLY	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2	SUPPLY	Operating supply current	I_{DD}		3.0	9.0	mA	
3	SUPPLY	Power consumption	P_O		15	45	mW	fc = 3.58MHz; V_{DD} = 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5	INPUTS	Low level input voltage	V_{IL}			1.5	V	
6	INPUTS	Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
7	INPUTS	Pull up (source) current	I_{SO}		7.5	15	μA	TOE (pin 10) = 0V
8	INPUTS	Input impedance (IN +, IN-)	R_{IN}		10		MΩ	@ 1 kHz
9	INPUTS	Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			0.03	V	No load
11	OUTPUTS	High level output voltage	V_{OH}	4.97			V	No load
12	OUTPUTS	Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4V
13	OUTPUTS	Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
14	OUTPUTS	V_{Ref} output voltage	V_{Ref}	2.4		2.8	V	No load
15	OUTPUTS	V_{Ref} output resistance	R_{OR}		10		KΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Operating Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power suply rejection	PSRR		60		dB	1 KHz
5	Common mode rejection	CMRR		60		dB	$-3.0V \leq V_{IN} \leq 3.0V$
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_C		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \geq 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		KΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

† $V_{DD} = 5$ V, $V_{SS} = 0$ V, $T_A = 25°C$

‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-31			dBm	1,2,3,5,6,9
				21.8			mV_{RMS}	1,2,3,5,6,9
						+ 1	dBm	1,2,3,5,6,9
						869	mV_{RMS}	1,2,3,5,6,9
2		Input Signal Level Reject		-37			dBm	1,2,3,5,6,9
				10.9			mV_{RMS}	1,2,3,5,6,9
3		Positive twist accept		6	10		dB	2,3,6,9
4		Negative twist accept		6	10		dB	2,3,6,9
5		Freq. deviation accept		± 1.5% ± 2Hz			Nom.	2,3,5,9
6		Freq. deviation reject		± 3.5%			Nom.	2,3,5,9
7		Third tone tolerance		-18.5			dB	2,3,4,5,9,12
8		Noise tolerance			-12		dB	2,3,4,5,7,9,10
9		Dial tone tolerance			+ 22		dB	2,3,4,5,8,9,11

† $V_{DD} = 5$ V, $V_{SS} = 0$, $T_A = 25°C$ and $f_C = 3.579545$ MHz using test circuit shown in Figure 2.

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5% ± 2Hz.
7. Bandwidth limited (3KHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 Input DTMF Tone Level at -25dBm (-28dBm at GS Pin) Interference Frequency Range between 480-3400Hz.

AC Electrical Characteristics†-Voltages are with repsect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	t_{DO}	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	μs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12		μs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		μs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	RL = 10KΩ CL = 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	RL = 10KΩ CL = 50 pF
26	CLOCK	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
27		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
28		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
29		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
30		Capacitive load (OSC2)	C_{LO}			30	pF	

†V_{DD} = 5V, V_{SS} = 0V T_A = 25° C and f_C = 3.579545 MHz, using test circuit in Figure 2.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

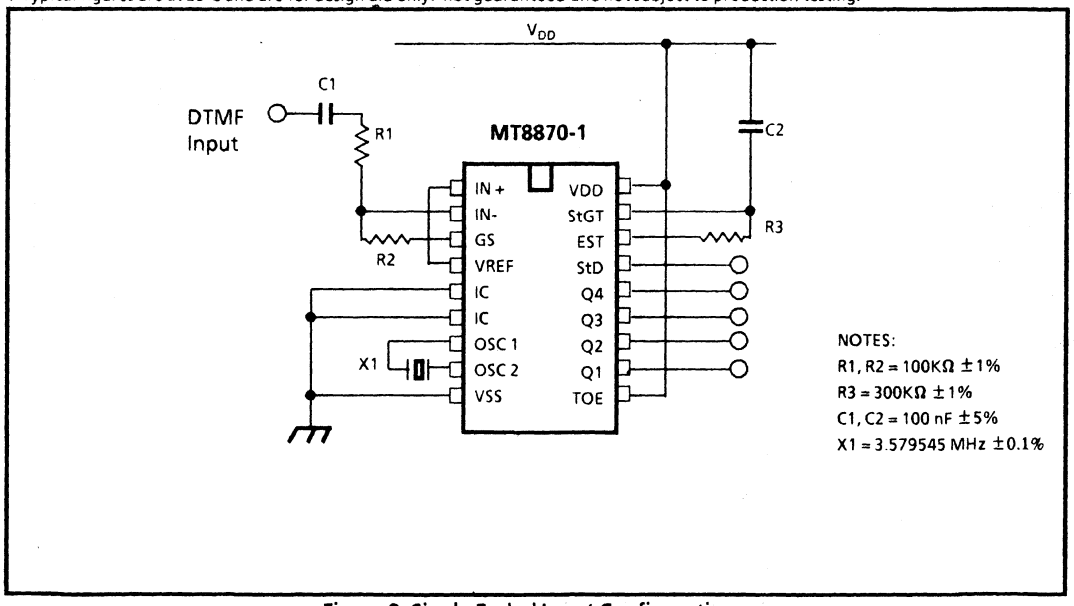
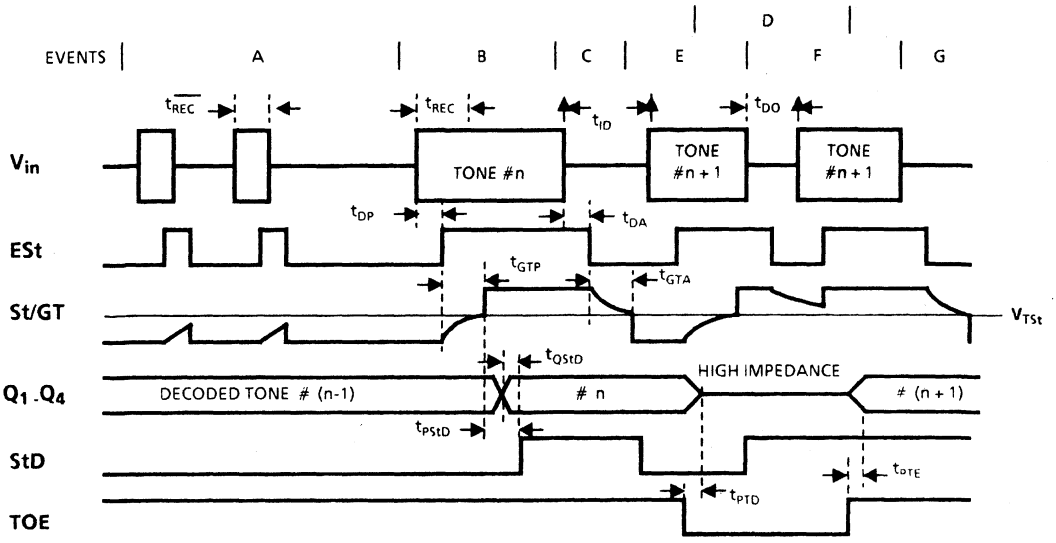


Figure 2. Single Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	Non-inverting op-amp input.
2	IN-	Inverting op-amp input.
3	GS	**Gain select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{REF}	**Reference voltage output,** nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig.2).
5	IC	**Internal connection.** Must be tied to V_{SS}.
6	IC	**Internal connection.** Must be tied to V_{SS}.
7	OSC1	Clock input.
8	OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative power supply input.
10	TOE	**3- state output enable** (input). Logic high enables the outputs Q1-Q4. Internal pull up.
11-14	Q1-Q4	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Fig. 5).
15	StD	**Delayed steering output.**Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/Gt falls below V_{TSt}
16	ESt	**Early steering output.** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	St/GT	**Steering input/guard time output** (bi-directional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply input.



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE
E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE)
F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCED
G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in} DTMF COMPOSITE INPUT SIGNAL.
ESt EARLY STEERING OUTPUT. INDICATES DECTECTION OF VALID TONE FREQUENCIES.
St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4 4-BIT DECODED TONE OUTPUT
StD DELAYED STEERING OUTPUT. INDICTES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSISTUTING A VALID SIGNAL.
TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.

$t_{\overline{REC}}$ MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID} MINIMUM TIME BETWEEN VALID DTMF SIGNALS.
t_{DO} MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.
t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.
t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.
t_{GTP} GUARD TIME, TONE PRESENT.
t_{GTA} GUARD TIME, TONE ABSENT.

Figure 3. Timing Diagram

Functional Description

The MT8870-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band pass filters, the band-widths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig. 4). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Fig. 6) to rise as the capacitor discharges.

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Fig. 5) into the output latch. At this point the GT output is activated and drives v_c to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to

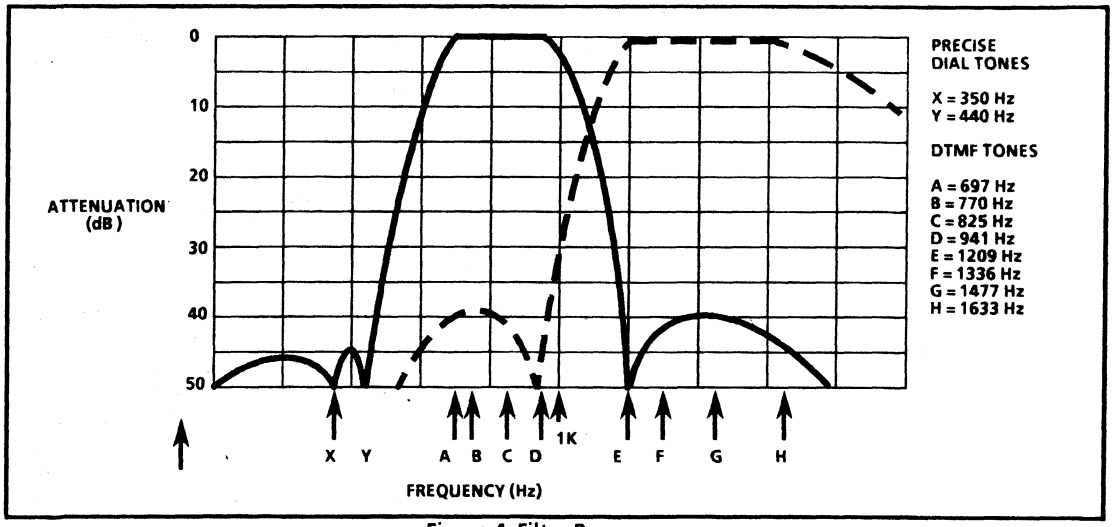


Figure 4. Filter Response

F_{LOW}	F_{HIGH}	NO.	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMEDANCE

Figure 5. Functional Decode Table

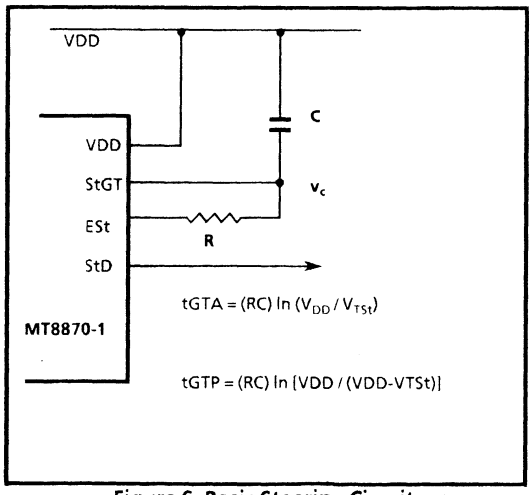


Figure 6. Basic Steering Circuit

validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Fig. 6 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independantly the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 7.

Differential Input Configuration

The input arrangement of the MT8870-1 provides a differential-input operational amplifier as well as a bias source(V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Fig. 2 with the op-amp connected for unity gain and V_{Ref} biasing the input at $\frac{1}{2}V_{DD}$. Fig. 8 shows the differential configuration, which permits the

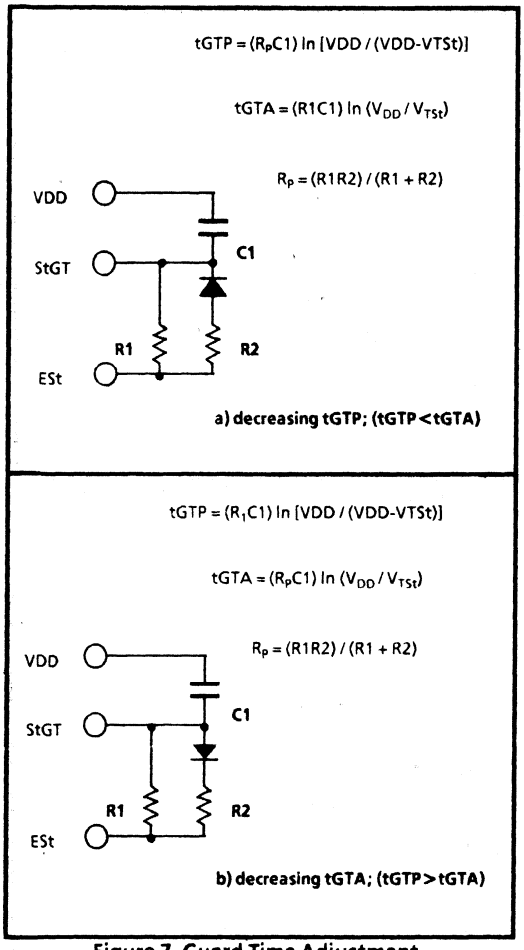


Figure 7. Guard Time Adjustment

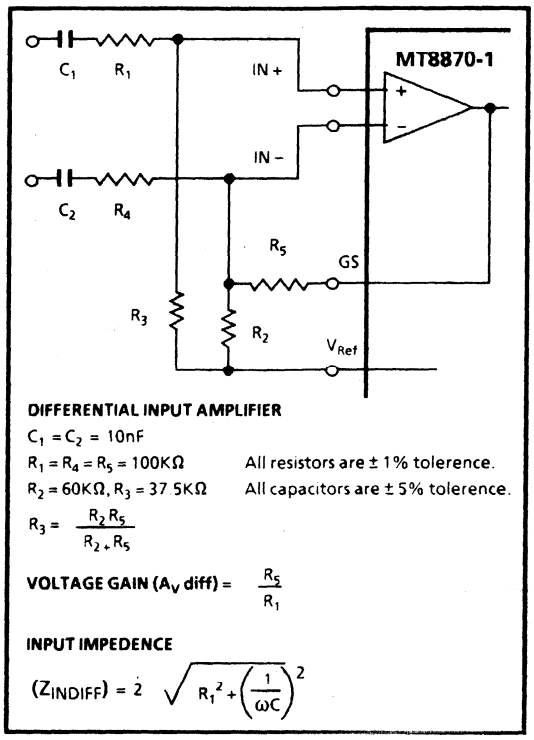


Figure 8. Differential Input Configuration

adjustment of gain with the feedback resistor R_5.

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.58 MHz crystal and is normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible to configure several MT8870-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Fig. 9 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie; precision balancing capacitors are not required.

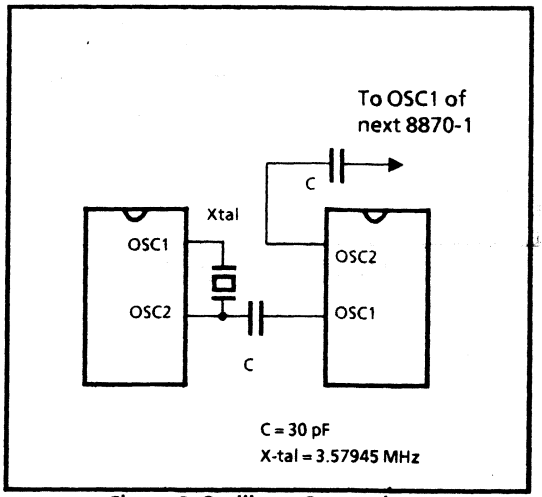


Figure 9. Oscillator Connection

APPLICATION

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 10 illustrates the use of MT8870-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R1 and R2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870-1. As shown in the diagram, the component values of R3 and C2 are the guard time requirement when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 11.

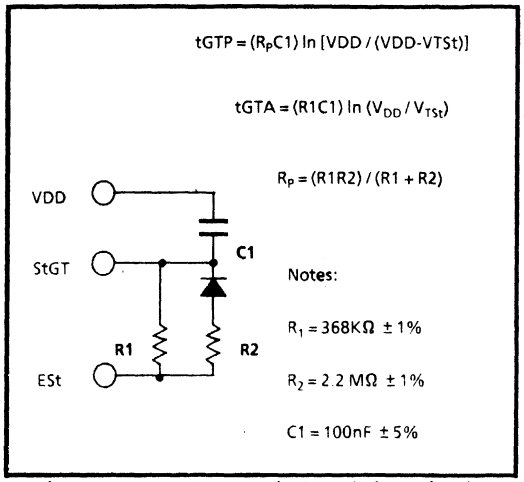


Figure 11. Non-Symmetric Guard Time Circuit

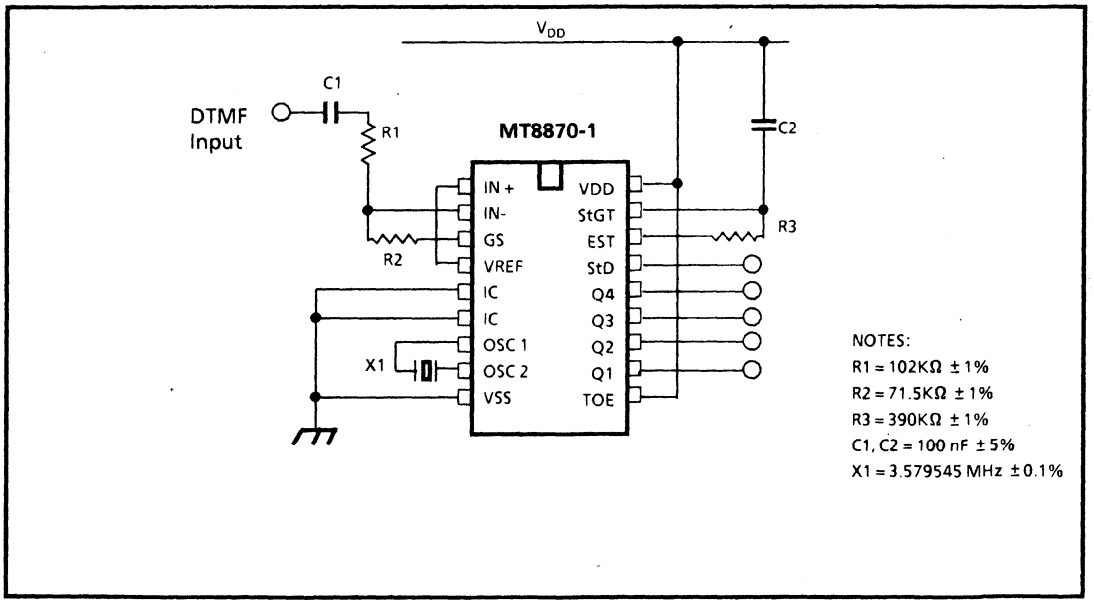


FIGURE 10. Single Ended Input Configuration for BT or CEPT Spec

ISO²-CMOS MT8872
Integrated DTMF Receiver
Preliminary Information

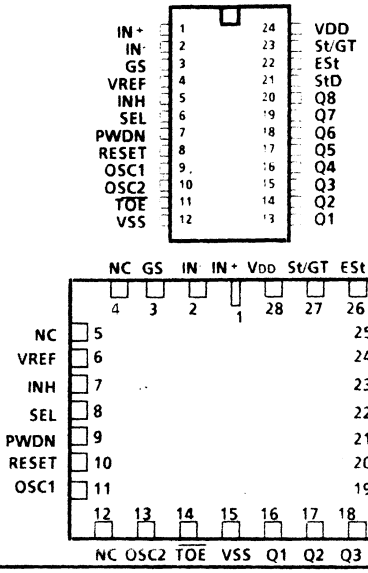
9161-002-063-NA ISSUE 1 June 1986

Features
- Complete DTMF receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality

Applications
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers

Description
The MT8872 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 8-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

Pin Connections



Ordering Information

MT8872BC	24 PIN CERDIP
MT8872BP	28 PIN PLCC
-40°C to +85°C	

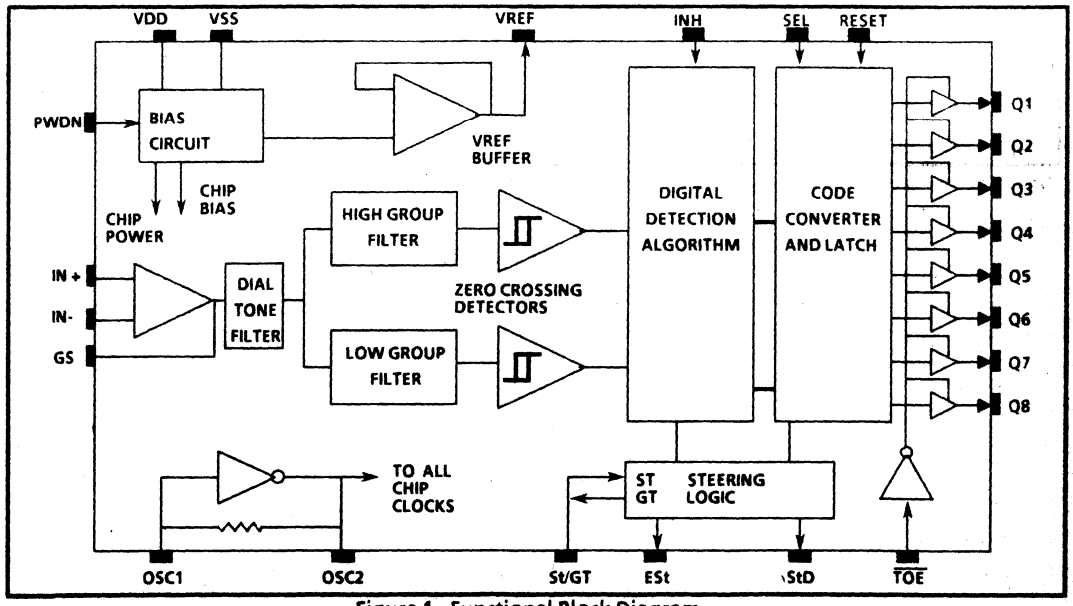


Figure 1- Functional Block Diagram

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD} + 0.3	V
3	Current at any pin	I_I		10	mA
4	Operating temperature	T_O	-40	+ 85	°C
5	Storage temperature	T_{STG}	-65	+ 150	°C
6	Package power dissipation	P_D		1000	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C All leads soldered to board.

DC Electrical Characteristics - V_{DD} = 5V ± 5%, V_{SS} = 0V. Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions*
1	SUPPLY	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2	SUPPLY	Operating supply current	I_{DD}		3.0	9.0	mA	
3	SUPPLY	Power consumption	P_C		15	45	mW	f = 3.5795MHz; V_{DD} = 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5	INPUTS	Low level input voltage	V_{IL}			1.5	V	
6	INPUTS	Input leakage current	I_{IH}/I_{IL}		0.1		µA	V_{IN} = V_{SS} or V_{DD}
7	INPUTS	Pull Down (sink) current	I_{SO}		12	40	µA	$\overline{TOE}$ = V_{DD}
8	INPUTS	Input impedance (IN +, IN-)	R_{IN}		10		MΩ	@ 1 kHz
9	INPUTS	Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			0.03	V	No load
11	OUTPUTS	High level output voltage	V_{OH}	4.97			V	No load
12	OUTPUTS	Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4V
13	OUTPUTS	Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
14	OUTPUTS	V_{Ref} output voltage	V_{REF}	2.4		2.8	V	No load
15	OUTPUTS	V_{Ref} output resistance	R_{OR}		10		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Operating Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power supply rejection	PSRR		60		dB	1 kHz
5	Common mode rejection	CMRR		60		dB	-3.0V ≤ V_{IN} ≤ 3.0V
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_C		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \geq 100k\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		kΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

† V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25° C

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ†	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+ 1	dBm	1,2,3,5,6,9
						883	mV_{RMS}	1,2,3,5,6,9
2		Positive twist accept			10		dB	2,3,6,9
3		Negative twist accept			10		dB	2,3,6,9
4		Freq. deviation accept		± 1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject		± 3.5%			Nom.	2,3,5,9
6		Third tone tolerance			-16		dB	2,3,4,5,9,10
7		Noise tolerance			-12		dB	2,3,4,5,7,9,10
8		Dial tone tolerance			+ 22		dB	2,3,4,5,8,9,11

† V_{DD} = 5 V, V_{SS} = 0 , T_A = 25° C and f_C = 3.579545 MHz using test circuit shown in Figure 2 .

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5% ± 2Hz.
7. Bandwidth limited (3kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	t_{DO}	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	$\overline{TOE} = V_{SS}$
8		Propagation delay (St to StD)	t_{PStD}		12		µs	$\overline{TOE} = V_{SS}$
9		Output data set up (Q to StD)	t_{QStD}		3.4		µs	$\overline{TOE} = V_{SS}$
10		Propagation delay ($\overline{TOE}$ to Q ENABLE)	t_{PTE}		50		ns	R_L = 10kΩ C_L = 50 pF
11		Propagation delay ($\overline{TOE}$ to Q DISABLE)	t_{PTD}		300		ns	R_L = 10kΩ C_L = 50 pF
12	CLOCK	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
13		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
14		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
15		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
16		Capacitive load (OSC2)	C_{LO}			30	pF	

†V_{DD} = 5V, V_{SS} = 0V T_A = 25°C and f_C = 3.579545 MHz, using test circuit in Figure 2.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

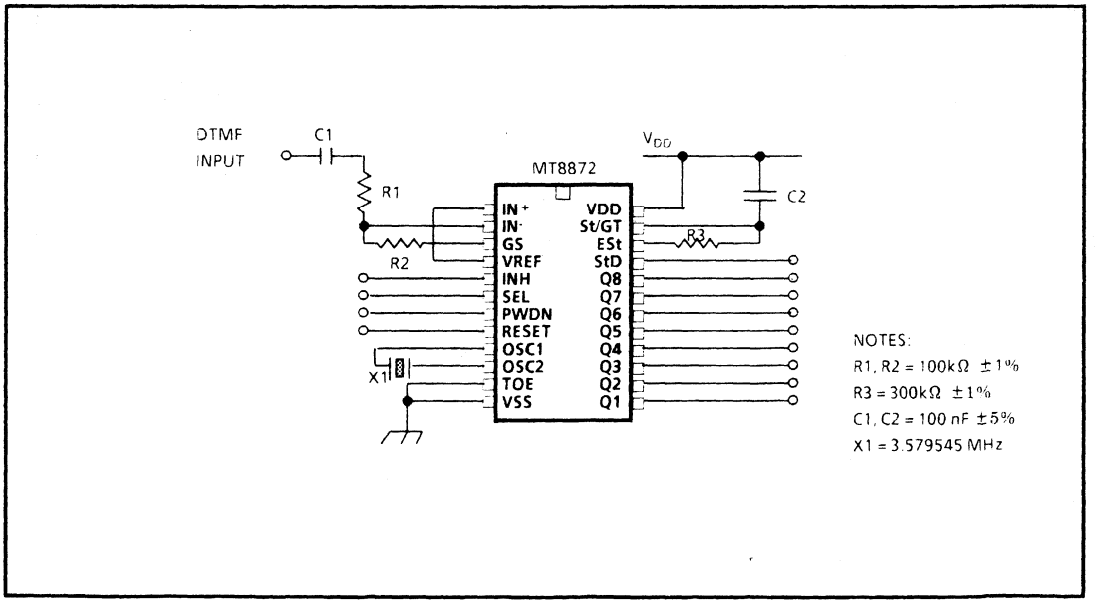


Figure 2- Single Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	**Non-inverting op-amp (Input).**
2	IN-	**Inverting op-amp (Input).**
3	GS	**Gain Select.** Gain access to output front end differential amplifier for connection of feedback register.
4	V_{REF}	**Reference Voltage (Output).** Normally VDD/2 is used to bias inputs at mid-rail.
5	INH	**Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. Internal pull down (see Table 2).
6	SEL	**Output Code Select (Input).** Logic low on this pin selects Q1-Q4, Q5-Q8 to provide two different 4 bit binary output codes. A logic high selects Q1-Q8 to provide a 2 of 8 output code (see Table 1).
7	PDWN	**Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. Internal pull down.
8	RESET	**Reset (Input).** A logic high will reset the data output latches to an "All High" condition.
9	OSC1	**Clock (Input).**
10	OSC2	**Clock (Output).** A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
11	$\overline{TOE}$	**Three State Output Enable (Input).** A logic low enables the data outputs Q1-Q8.
12	V_{SS}	**Negative Power Supply (Input).**
13	Q1	**Data (Outputs)** three-state buffered. Provides 4 bit binary word (SEL Low) or inverted 2-of-8 binary word (SEL High), corresponding to the tone pair decoded when enabled by $\overline{TOE}$.
14	Q2	
15	Q3	
16	Q4	
17	Q5	
18	Q6	
19	Q7	
20	Q8	
21	StD	**Delayed Steering (Output).** Presents a logic high when a received tone pair has been registered and the output latched; returns to a logic low when the voltage on St/GT falls below V_{TST}.
22	ESt	**Early Steering Input (Output).** Presents a logic high once the digital algorithm detects a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
23	St/GT	**Steering Input/Guard Time (Output) bidirectional.** A voltage greater than V_{TST} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant; its state is a function of ESt and the voltage on St.
24	V_{DD}	**Positive Power Supply (Input).**

Functional Description

See MT8870 Data Sheet issue 2 for Reference (note that for the MT8872; $\overline{TOE}$ is active low and output code is 8 bits instead of 4 bits).

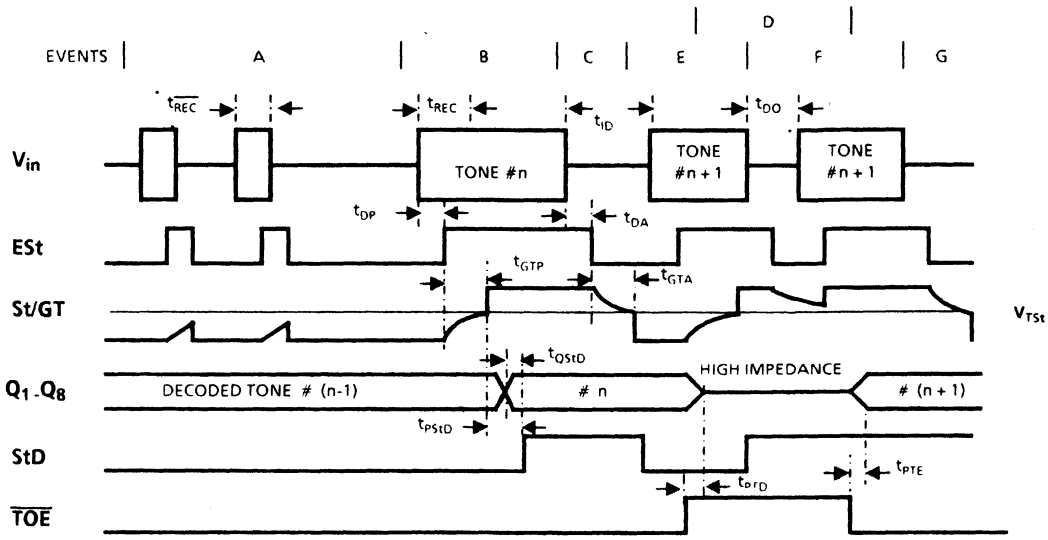
DIGIT	$\overline{TOE}$	SEL	INH	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1
X	H	X	X	Z	Z	Z	Z	Z	Z	Z	Z
1	L	L	L	L	L	L	H	L	L	L	H
2	L	L	L	L	L	H	L	L	L	H	L
3	L	L	L	L	L	H	H	L	L	H	H
4	L	L	L	L	H	L	L	L	H	L	L
5	L	L	L	L	H	L	H	L	H	L	H
6	L	L	L	L	H	H	L	L	H	H	L
7	L	L	L	L	H	H	H	L	H	H	H
8	L	L	L	H	L	L	L	H	L	L	L
9	L	L	L	H	L	L	H	H	L	L	H
0	L	L	L	L	L	L	L	H	L	H	L
*	L	L	L	H	L	H	L	H	L	H	H
#	L	L	L	H	L	H	H	H	H	L	L
A	L	L	L	H	H	L	L	H	H	L	H
B	L	L	L	H	H	L	H	H	H	H	L
C	L	L	L	H	H	H	L	H	H	H	H
D	L	L	L	H	H	H	H	L	L	L	L
1	L	H	L	H	H	H	L	H	H	H	L
2	L	H	L	H	H	L	H	H	H	H	L
3	L	H	L	H	L	H	H	H	H	H	L
4	L	H	L	H	H	H	L	H	H	L	H
5	L	H	L	H	H	L	H	H	H	L	H
6	L	H	L	H	L	H	H	H	H	L	H
7	L	H	L	H	H	H	L	H	L	H	H
8	L	H	L	H	H	L	H	H	L	H	H
9	L	H	L	H	L	H	H	H	L	H	H
0	L	H	L	H	H	L	H	L	H	H	H
*	L	H	L	H	H	H	L	L	H	H	H
#	L	H	L	H	L	H	H	L	H	H	H
A	L	H	L	L	H	H	H	H	H	H	L
B	L	H	L	L	H	H	H	H	H	L	H
C	L	H	L	L	H	H	H	H	L	H	H
D	L	H	L	L	H	H	H	L	H	H	H

Table 1 - Output Coding

X = Any Characters Z = High Impedance L = Logic Low H = Logic High

DIGIT	INH	SEL	ESt
A	H	X	L
B	H	X	L
C	H	X	L
D	H	X	L

Table 2 - Inhibit Function



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.
E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).
F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED
G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_8	8-BIT DECODED TONE OUTPUT
StD	DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.
$\overline{TOE}$	TONE OUTPUT ENABLE (INPUT). A HIGH LEVEL SHIFTS Q_1-Q_8 TO ITS HIGH IMPEDANCE STATE.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.
t_{DA}	TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 3 -Timing Diagram

ISO²-CMOS MT8880
Integrated DTMF Transceiver

Preliminary Information

9161-002-032-NA ISSUE 2 August 1986

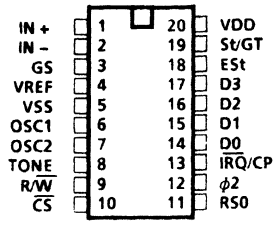
Features

- Complete DTMF transmitter/receiver
- Central Office quality
- Low power consumption
- Microprocessor port
- Adjustable guard time
- Automatic tone burst mode
- Call progress mode

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Pin Connections



Ordering Information

MT8880AE	20 Pin Plastic Dual-in-Line
MT8880AC	20 Pin CERDIP
	-40°C to +85°C

Description

The MT8880 is a monolithic DTMF transceiver with call progress filter. It is fabricated in Mitel's ISO²-CMOS technology which provides low power dissipation and high reliability. The DTMF receiver is based upon the industry standard MT8870 monolithic DTMF receiver; the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones. A standard microprocessor bus is provided and is directly compatible with 6800 series microprocessors.

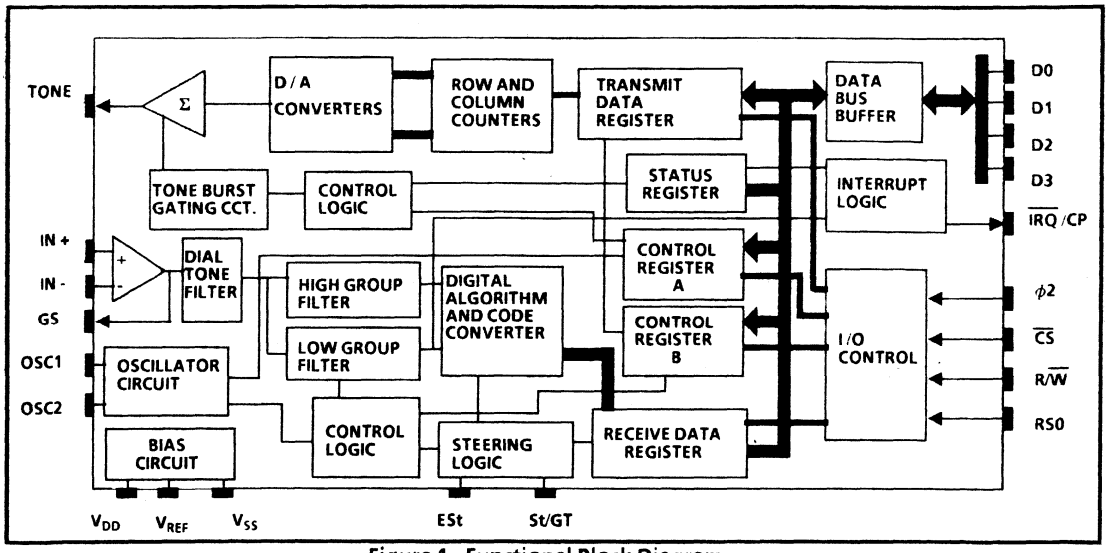


Figure 1- Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current at any pin (Except V_{DD} and V_{SS})			10	mA
5	Storage temperature	T_{ST}	- 65	+ 150	°C
6	Package power dissipation	P_D		1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive power supply	V_{DD}	4.75	5.00	5.25	V	
2	Operating temperature	T_O	- 40		+ 85	°C	
3	$\Phi 2$ clock frequency	f_C	.0005		1	MHz	

‡ Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics -† f_C = 3.579545 MHz, $\phi 2$ = 1 MHz, V_{SS} = 0 V

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
		Operating supply current	I_{DD}		10		mA	
3		Power consumption	P_C		50		mW	
4	INPUTS	High level input voltage (OSC1)	V_{IHO}	3.5			V	
5		Low level input voltage (OSC1)	V_{ILO}			1.5	V	
6		Input impedance (inputs 1,2)			10		MΩ	
7		Steering threshold voltage	V_{TSt}	2.2		2.5	V	V_{DD} = 5 V
8	OUTPUTS	Low level output voltage (OSC2)	V_{OLO}			0.1	V	No load
9		High level output voltage (OSC2)	V_{OHO}	4.9			V	No load
10		Output leakage current (IRQ)	I_{OZ}		1	10	μA	V_{OH} = 2.4 V
11		Vref output voltage	V_{REF}	2.4		2.7	V	No load
12		Vref output resistance	R_{OR}		10		kΩ	
13	DATA BUS	Low level input voltage	V_{IL}			0.8	V	
14		High level input voltage	V_{IH}	2.0			V	
15		Low level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
16		High level output voltage	V_{OH}	2.4			V	I_{OH} = 400 μA
17		Input leakage current	I_{IZ}			10	μA	V_{IN} = 0.4 to 2.4 V

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics

Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated, V_{SS} = 0 V

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power supply rejection	PSRR		60		dB	1 kHz
5	Common mode rejection	CMRR		60		dB	-3.0 V ≤ V_{IN} ≤ 3.0 V
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Unity gain bandwidth	BW		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \geq 100$ kΩ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		kΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

V_{SS} = 0 V, $\Phi 2$ = 1 MHz f_C = 3.579545 MHz.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	RX SIGNAL CONDITION	Valid input signal levels (each tone of composite signal)		- 29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+ 1	dBm	1,2,3,5,6,9
						883	mV_{RMS}	1,2,3,5,6,9
2		Positive twist accept			10		dB	2,3,6,9
3		Negative twist accept			10		dB	2,3,6,9
4		Freq. deviation accept		± 1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject		± 3.5%			Nom.	2,3,5
6		Third tone tolerance			- 16		dB	2,3,4,5,9,10
7		Noise tolerance			- 12		dB	2,3,4,5,7,9,10
8		Dial tone tolerance			+ 22		dB	2,3,4,5,8,9,11
9	CALL PROGRESS	Lower frequency (ACCEPT)	f_{LA}		320		Hz	@ - 25 dBm
10		Upper frequency (ACCEPT)	f_{HA}		510		Hz	@ - 25 dBm
11		Lower frequency (REJECT)	f_{LR}		290		Hz	@ - 25 dBm
12		Upper frequency (REJECT)	f_{HR}		540		Hz	@ - 25 dBm

†Characteristics are over recommended operating conditions unless otherwise stated

‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing

*See "Notes" following Pin Description

AC Electrical Characteristics † - Voltages are with respect to ground (V_{SS}) unless otherwise stated. (See figure 7)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	RX TIMING	Tone present detect time	t_{DP}	5	11	14	ms	
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	
3		Tone duration accept	t_{REC}			40	ms	
4		Tone duration reject	$\overline{t_{REC}}$	20			ms	
5		Interdigit pause accept	t_{ID}			40	ms	
6		Interdigit pause reject	t_{DO}	20			ms	
7		Delay St to b3	t_{PStb3}		13		μs	
8		Delay St to RX_0-RX_3	t_{PStRX}		8		μs	
9	TX TIMING	Tone burst duration	t_{BST}	50		52	ms	DTMF mode
10		Tone pause duration	t_{PS}	50		52	ms	DTMF mode
11		Tone burst duration (extended)	t_{BSTE}	100		104	ms	Call Progress mode
12		Tone pause duration (extended)	t_{PSE}	100		104	ms	Call Progress mode
13	TONE OUT	High group output level	V_{HOUT}	-6.1		-2.1	dBm	R_L = 10kΩ
14		Low group output level	V_{LOUT}	-8.1		-4.1	dBm	R_L = 10kΩ
15		Pre-emphasis	dB_P	0	2	3	dB	R_L = 10kΩ
16		Output distortion	THD		-25		dB	3.4 kHz Bandwidth R_L = 10 kΩ
17		Frequency deviation	f_D		± 0.7	± 1.5	%	f_C = 3.579545 MHz
18		Output load resistance	R_{LT}	10		50	kΩ	
19	MPU INTERFACE	Φ2 cycle period	t_{CYC}		1		μs	
20		Φ2 high pulse width	t_{CH}	450			ns	
21		Φ2 low pulse width	t_{CL}	430			ns	
22		Φ2 rise and fall time	t_R, t_F			25	ns	
23		Address, R/$\overline{W}$ hold time	t_{AH},t_{RWH}	10			ns	
24		Address, R/$\overline{W}$ set- up time (before Φ2)	t_{AS},t_{RWS}	80			ns	
25		Data hold time (read)	t_{DHR}	20			ns	*
26		Φ2 to valid data delay (read)	t_{DDR}			290	ns	200 pF load
27		Data set up time (write)	t_{DSW}	165			ns	
28		Data hold time (write)	t_{DHW}	10			ns	
29		Input Capacitance (data bus)	C_{IN}		5		pF	
30		Output Capacitance ($\overline{IRQ}$/CP)	C_{OUT}		5		pF	
31	DTMF CLK	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
32		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
33		Clock input duty cycle	t_{HLCL}			110	ns	Ext. clock
34		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
35		Capacitive load (OSC2)	C_{LO}			30	pF	

† Timing is over recommended temperature & Power Supply voltages. f_C = 3.579545 MHz

‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing

* The data bus output buffers are no longer sourcing or sinking current by t_{DHR}

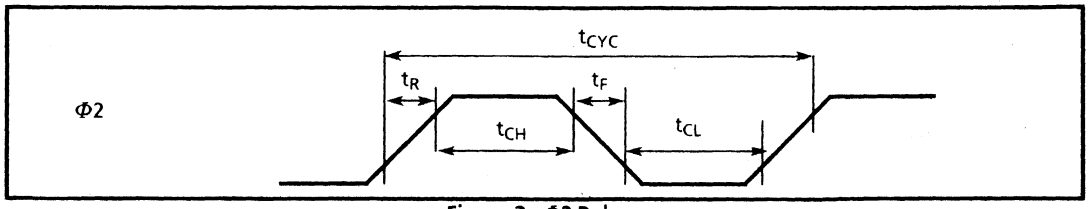


Figure 2 - Φ2 Pulse

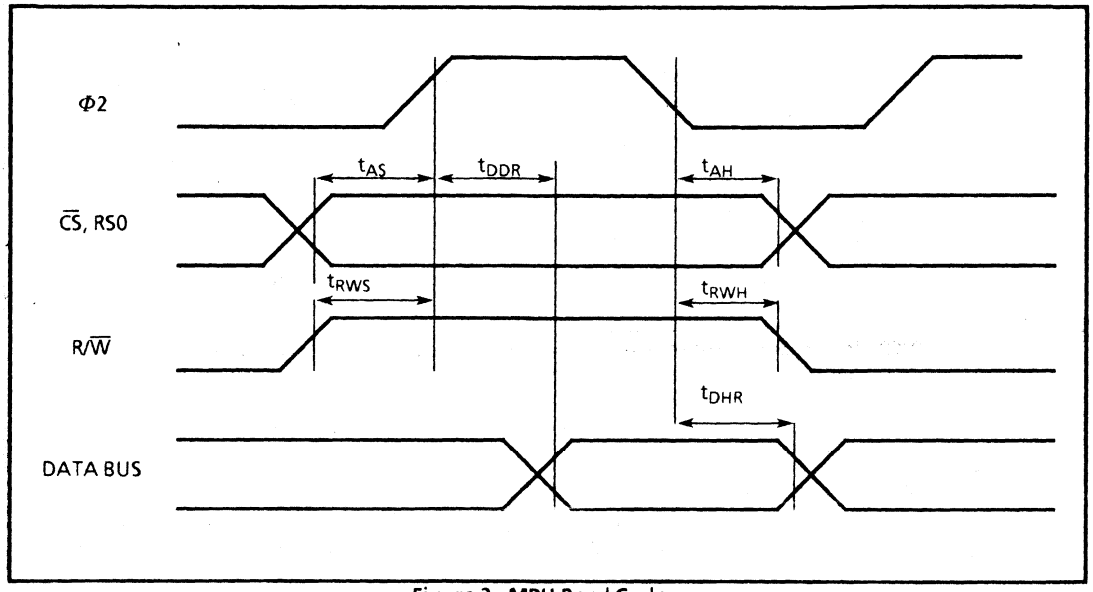


Figure 3 - MPU Read Cycle

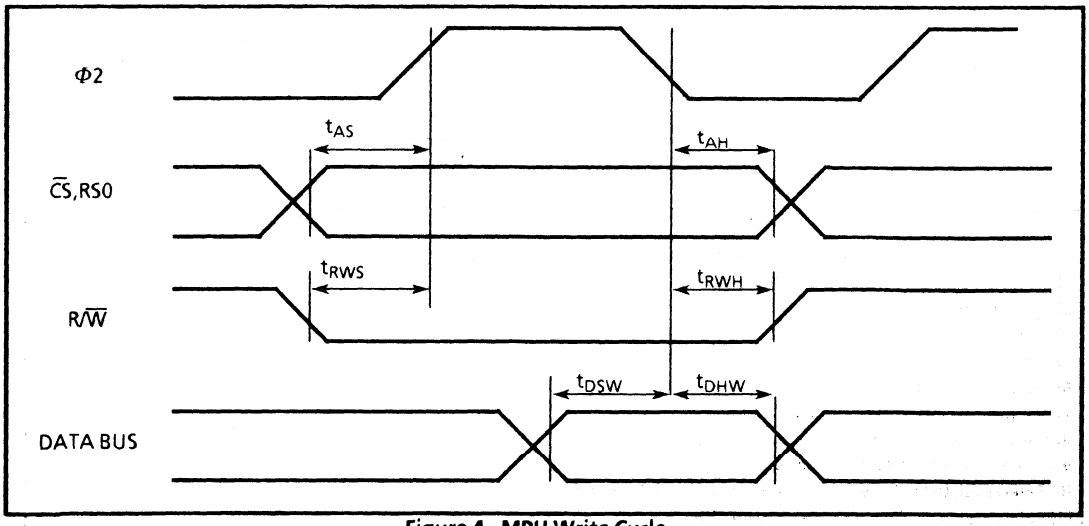


Figure 4 - MPU Write Cycle

Pin Description

Pin #	Name	Description
1	IN +	Non-inverting op-amp input.
2	IN –	Inverting op-amp input.
3	GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{REF}	Reference voltage output, nominally VDD/2 is used to bias inputs at mid-rail (see application diagram).
5	V_{SS}	Negative power supply input.
6	OSC1	DTMF clock/oscillator input.
7	OSC2	Clock output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is clock input.
8	TONE	Dual Tone Multi-Frequency output.
9	R/$\overline{W}$	Read/Write input. Controls the direction of data transfer to and from the MPU and the transceiver registers. TTL compatible.
10	$\overline{CS}$	Chip select, TTL input ($\overline{CS}$ = 0 to select the chip).
11	RS0	Register select input. See register decode table. TTL compatible.
12	$\Phi 2$	System clock input. TTL compatible.
13	I$\overline{RQ}$/CP	Interrupt request to MPU (open drain output). Also, when call progress (CP) mode has been selected and interrupt enabled the I$\overline{RQ}$/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 10.
14-17	D0-D3	Microprocessor data bus (TTL compatible).
18	ESt	Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	St/GT	Steering input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	V_{DD}	Positive power supply input.

NOTES:

1) dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2) Digit sequence consists of all 16 DTMF tones.
3) Tone duration = 40 ms. Tone pause = 40 ms,
4) Nominal DTMF frequencies are used
5) Both tones in the composite signal have an equal amplitude.
6) The tone pair is deviated by ± 1.5 % ± 2 Hz.
7) Bandwidth limited (3 kHz) Gaussian noise.
8) The precise dial tone frequencies are 350 and 440 Hz (± 2 %).
9) For an error rate of less than 1 in 10,000.
10) Referenced to the lowest amplitude tone in the DTMF signal.
11) Referenced to the minimum valid accept level.

Functional Description

The MT8880 Integrated DTMF Transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator which employs a burst counter such that precise tone bursts and pauses can be synthesized. A call progress mode can be selected such that frequencies within the specified pass band can be detected. A standard microprocessor interface allows access to an internal status register, two control registers and two data registers.

Input Configuration

The input arrangement of the MT8880 provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single ended configuration, the input pins are connected as shown in Figure 5.

Figure 6 shows the necessary connections for a differential input configuration.

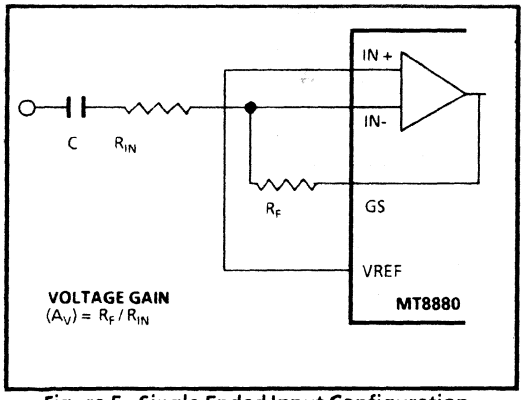


Figure 5 - Single Ended Input Configuration

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the band-widths of which correspond to the low and high group frequencies (see Fig. 10). The low group filter also incorporates notches at 350 Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-

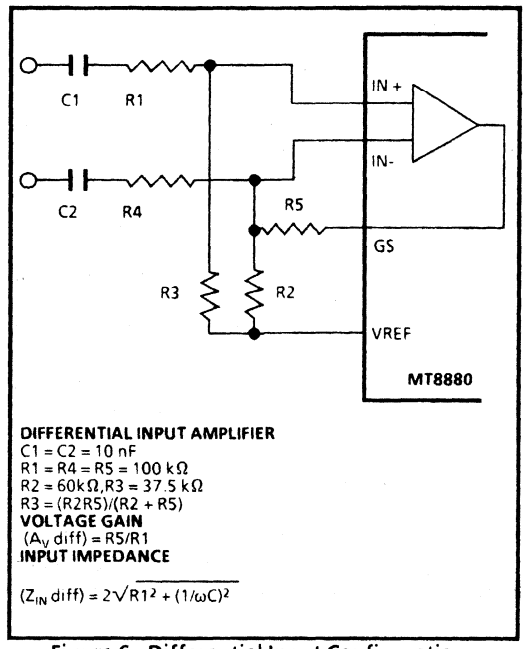


Figure 6 - Differential Input Configuration

gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see Steering Circuit).

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure7) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Figure 9) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. It is possible to monitor the status of the delayed steering flag by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bi-directional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short too be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

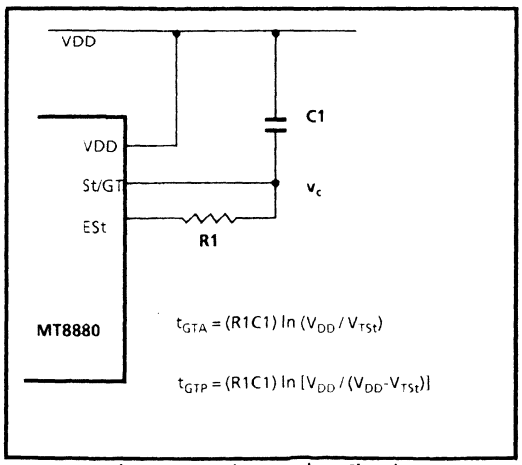


Figure 7. Basic Steering Circuit

Guard Time Adjustment

The simple steering circuit shown in Figure 7 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see AC Electrical Characterstics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 µF is recommended for most applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since

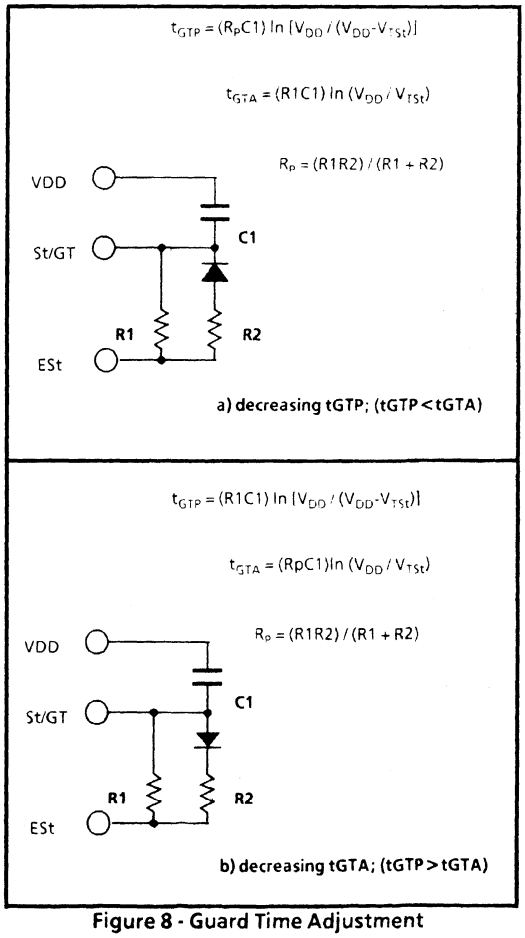


Figure 8 - Guard Time Adjustment

it reduces the probability that tones simulated by speech will maintain signal; condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 8. The receiver timing is shown in Figure 11 with a description of the events in Figure 13.

Call Progress Filter

A call progress mode can be selected allowing the detection of various tones which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 5). Figure 10 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input (IN + and IN-) which are within the 'accept' bandwidth limits of the filter are hard limited by a high gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The square wave output obtained from the schmitt trigger can be analysed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently there will be no activity on $\overline{IRQ}$/CP as a result of these frequencies.

DTMF Generator

The DTMF transmitter employed in the MT8880 is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal data conforming to the encoding format shown in Figure 9 must be written to the transmit data register . Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table in Figure 10, the low group frequencies are 697, 770, 852 and 941 Hz. the high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically the high group to low group amplitude ratio (twist) is 2 dB to compensate for high group attenuation on long loops.

F_{LOW}	F_{HIGH}	DIGIT	D_4	D_3	D_2	D_1
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0 = LOGIC LOW. 1 = LOGIC HIGH

Figure 9 - Functional Encode/Decode Table

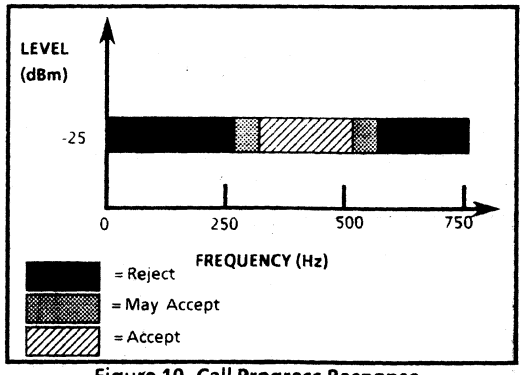


Figure 10- Call Progress Response

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment

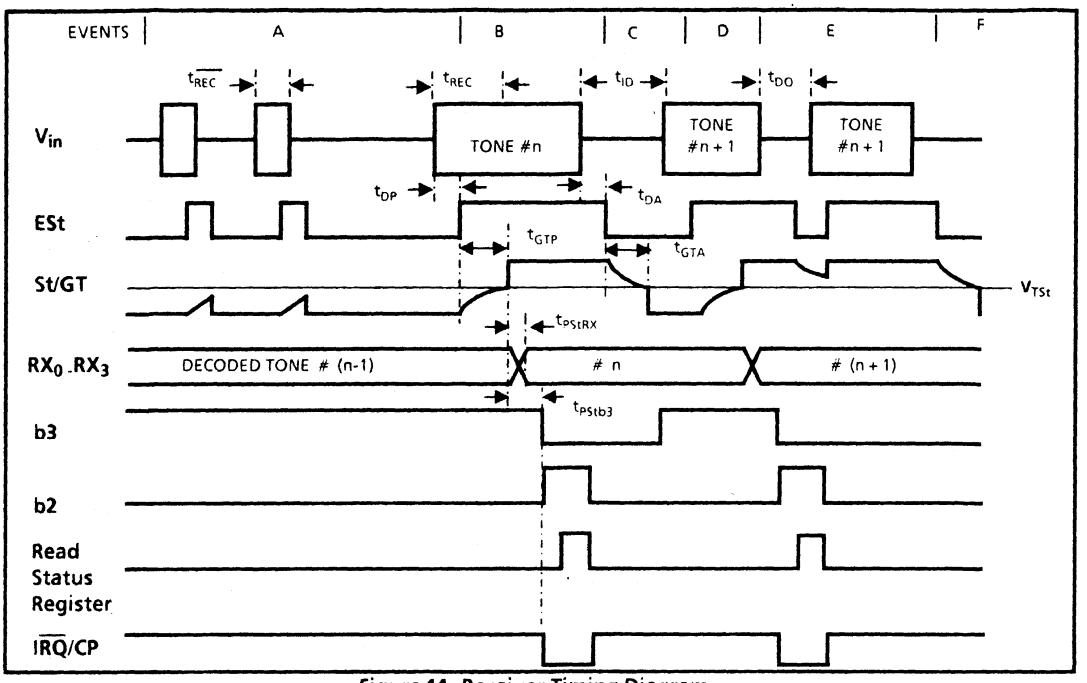


Figure 11- Receiver Timing Diagram

length which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the frequency can also be varied. The divider output clocks another counter which addresses the sinewave lookup ROM.

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones which are then mixed using a low noise summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. Under conditions when there is no tone output signal, the TONE pin assumes a DC level of 2.5 volts (typ). A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 4 kHz. It can be seen from Figure 12 that the distortion products are very low in amplitude.

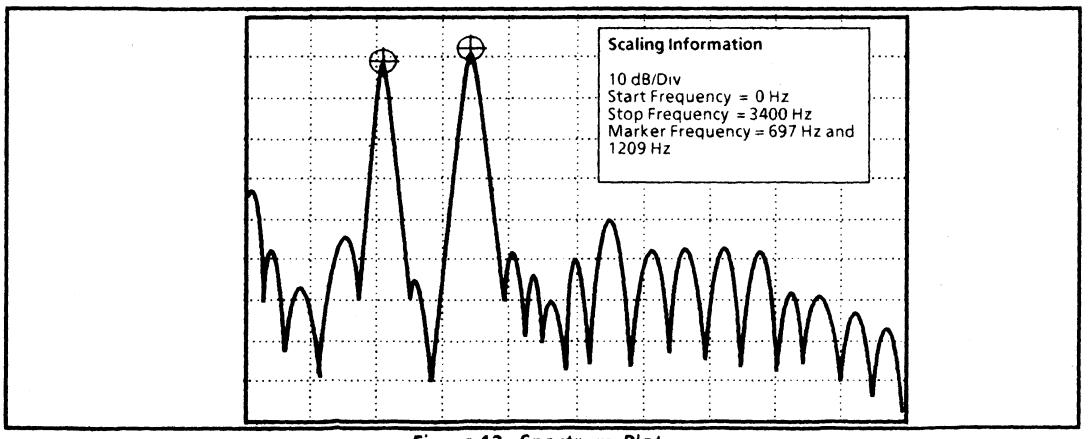


Figure 12 - Spectrum Plot

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms ± 1 ms which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, a secondary burst/pause time is available such that this interval is extended to 102 ms ± 2 ms. The extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In certain applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter. The MT8880 is initialized on power up sequence such that DTMF mode and Burst mode are selected.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgement tone generation and distortion measurements. Refer to Control Register B description for details.

Distortion Calculations

The MT8880 is capable of producing precise tone bursts with minimal error in frequency (see Table 1). The internal summing amplifier is followed by a first-order low pass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1 which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage.

EXPLANATION OF EVENTS

A)	TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED
B)	TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
C)	END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
D)	TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
E)	ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED
F)	END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$\overline{IRQ}$/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 13 - Description of Timing Events

$$THD(\%) = 100 \frac{\left(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + \ldots V^2_{nf}}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

$$THD(\%) = 100 \frac{\left(\sqrt{V^2_{2L} + V^2_{3L} + \ldots V^2_{nL} + V^2_{2H} + V^2_{3H} + \ldots V^2_{nH} + V^2_{IMD}}\right)}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD (%) For a Dual Tone

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+ 0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+ 0.74
H1	1209	1215.9	+ 0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+ 0.73

Table 1 . Actual Frequencies Versus Standard Requirements

The Fourier components of the tone output correspond to V_{2f}.... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 12.

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal having a resonant frequency of 3.579545 MHz. A number of MT8880 devices can be connected as shown in Figure 14 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer (capacitive coupling) with the OSC2 outputs left unconnected.

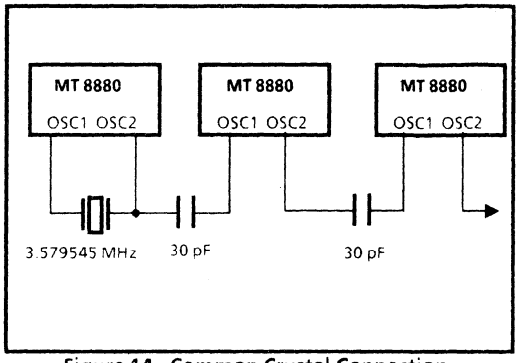


Figure 14 - Common Crystal Connection

Microprocessor Interface

The MT8880 employs a microprocessor interface which allows precise control of transmitter and receiver functions. There are five internal registers associated with the microprocessor interface which can be subdivided into three categories, ie; data transfer, transceiver control and transceiver status.There are two registers associated with data transfer operations. The Receive Data Register contains the output code of the last valid DTMF tone pair to be decoded and is a read only register. The data entered in the Transmit Data Register will determine which tone pair is to be generated (see Figure 10 for coding details). Data can only be written to the transmit register. Transceiver control is accomplished with two Control Registers (CRA and CRB) which occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA . The following write operation to the same address will then be directed to CRB and subsequent write cycles will then be directed back to CRA. Internal reset circuitry will clear the control registers on power up, however, as a precautionary measure the initialization software should include a routine to clear the registers. Assume transmit register is empty after reset. Refer to Tables 3, 4, 5 and Table 6 for details concerning the Control Registers. The $\overline{IRQ}$/CP pin cn be programmed such that it will provide an interrupt request signal upon validation of DTMF signals or when the transmitter is ready for more data (Burst mode only). The $\overline{IRQ}$/CP pin is configured as an open drain output device and as such requires a pull-up resistor (see Figure 15).

RS0	R/$\overline{W}$	FUNCTION
0	0	Write to Transmit Data Register
0	1	Read from Receive Data Register
1	0	Write to Control Register
1	1	Read from Status Register

Table 2 - Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{DTMF}$	TOUT

Table 3- CRA Bit Positions

b3	b2	b1	b0
C/$\overline{R}$	S/$\overline{D}$	TEST	BURST

Table 4- CRB Bit Positions

BIT	NAME	FUNCTION	DESCRIPTION
b0	TOUT	TONE OUTPUT	A logic '1' enables the tone output. This function can be implemented in either the burst mode or non-burst mode.
b1	CP/$\overline{DTMF}$	MODE CONTROL	In DTMF mode (logic '0') the device is capable of generating and receiving Dual Tone Multi-Frequency signals. When the CP (Call Progress) mode is selected (logic '1') a 6th order bandpass filter is enabled to allow call progress tones to be detected. Call progress tones which are within the specified bandwidth will be presented at the $\overline{IRQ}$/CP pin in rectangular wave format if the IRQ bit has been enabled (b2 = 1). Also, when the CP mode and BURST mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 ms (typ) duration. This signal duration is twice that obtained from the DTMF transmitter if DTMF mode had been selected. Note that DTMF signals cannot be decoded when the CP mode of operation has been selected.
b2	IRQ	INTERRUPT ENABLE	A logic '1' enables the INTERRUPT mode. When this mode is active and the DTMF mode has been selected (b1 = 0) the $\overline{IRQ}$/CP pin will pull to a logic '0' condition when either 1) a valid DTMF signal has been received and has been present for the guard time duration or 2) the transmitter is ready for more data (BURST mode only).
b3	RSEL	REGISTER SELECT	A logic '1' selects Control Register B on the next Write cycle to the Control Register address. Subsequent Write cycles to the Control Register are directed back to Control Register A.

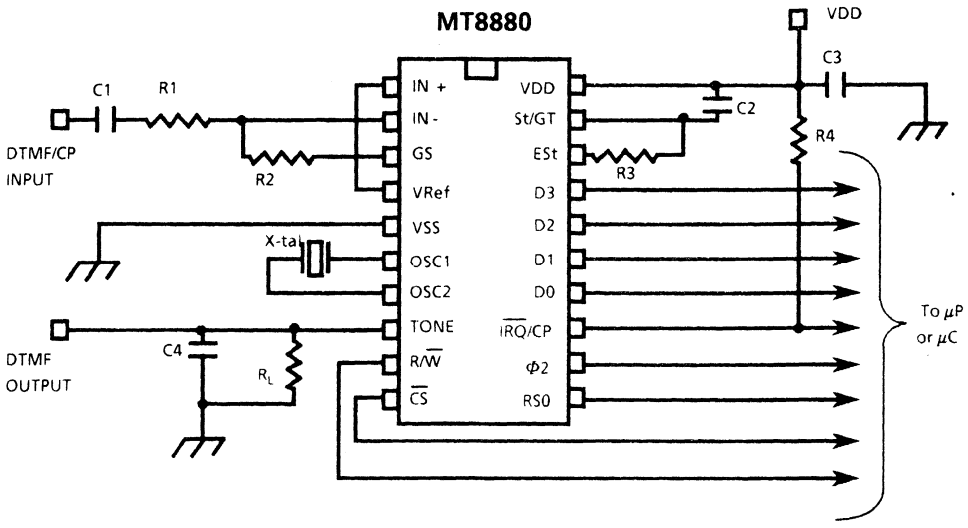
Table 5 - Control Register A Description

BIT	NAME	FUNCTION	DESCRIPTION
b0	BURST	BURST MODE	A logic '0' enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the Transmit Register resulting in a tone burst of a specific duration (see AC Characteristics). Subsequently, a pause of the same duration is induced. Immediately following the pause, the Status Register is updated indicating that the Transmit Register is ready for further instructions and an interrupt will be generated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increased by a factor of two. When the burst mode is not selected (logic '1') tone bursts of any desired duration may be generated.
b1	TEST	TEST MODE	By enabling the test mode (logic '1') the $\overline{IRQ}$/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 7 (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA b1 = 0) before test mode can be implemented.
b2	S/$\overline{D}$	SINGLE/DUAL TONE GENERATION	A logic '0' will allow Dual Tone Multi-Frequency signals to be produced. If single tone generation is enabled (logic '1'), either row or column tones (low group or high group) can be generated depending on the state of b3 in Control Register B.
b3	C/$\overline{R}$	COLUMN/ROW TONES	When used in conjunction with b2 (above) the transmitter can be made to generate single row or single column frequencies. A logic '0' will select row frequencies and a logic '1' will select column frequencies.

Table 6 - Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) and or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 7 - Status Register Description



Notes:

R1, R2 = 100 kΩ 1%
R3 = 374k Ω 1 %
R4 = 3 kΩ 10 %
R_L = 10 k Ω (min)
C1 = 100 nF 5 %
C2 = 100 nF 5 %
C3 = 100 nF 10 % *
C4 = 10 nF 10 %
X-tal = 3.579545 MHz

* Microprocessor based systems can inject undesirable noise into the supply rails. The performance of the MT8880 can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 15 - Application Circuit (Single Ended Input)

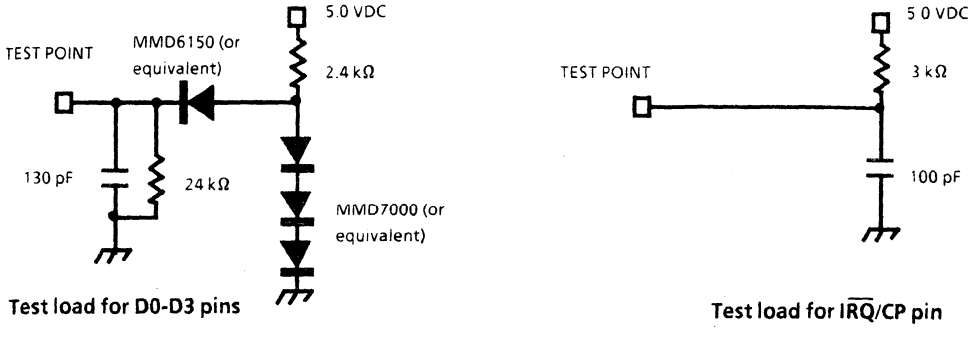


Figure 16- Test Circuits

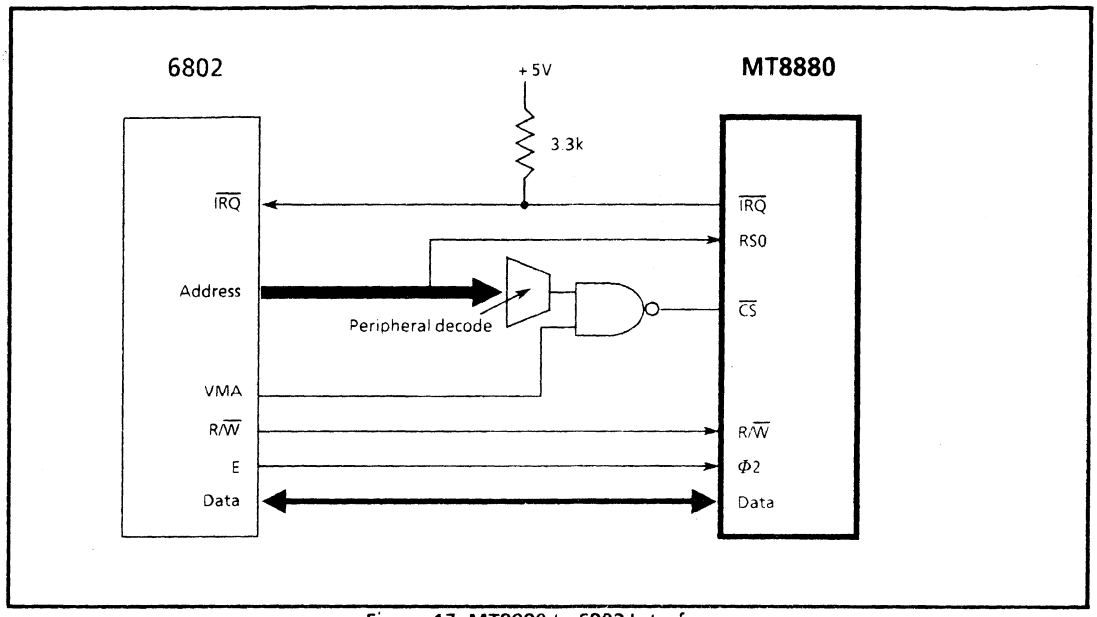


Figure 17- MT8880 to 6802 Interface

CM7291
DTMF Receiver Test Cassette

FEB. 1983

Features

- Provides complete receiver evaluation in less than 90 minutes testing time.
- Utilizes a condensed speech recording equivalent to many hours of receiver exposure to evaluate talk-off rate.
- Checks receiver recognition bandwidths, center frequencies, maximum acceptable amplitude ratio, guard time, dynamic range, and acceptable signal to noise ratio.
- Test equipment requirement consists of a digital counter, an ac voltmeter, and a low cost cassette tape player capable of delivering 2 Vrms at its output terminal. The tape player may require a small amplifier to achieve 2 Vrms.
- Compensation factors allow tape player speed inaccuracies of up to 2% without loss of measurement accuracy.
- Convenient C90 cassette format on low noise tape.

General Description

The Mitel CM7291 Tone Receiver Test Cassette cuts the total evaluation time of DTMF tone receivers to less than 90 minutes. Test equipment requirements are also minimized to a modest test set-up.

Test Content

Side one of the tape contains a series of tests involving recorded tone bursts with the parameters varied in a number of ways. Tests are performed by sending the tone bursts to the receiver, and counting the number of bursts to which the receiver responds. The results from these tests provide direct indications of receiver performance.

Side two of the tape contains a condensed speech recording which is used to evaluate the speech immunity of the receiver. Ideally a receiver's response to the speech recording should be zero, since no intentional tone bursts are present. In practice the number of responses will vary from 2 to 100, depending on the receiver quality and dynamic range.

Prompts and instructions are included on both sides of the tape to aid in receiver testing.

Test Setup

Two test setups using the same test equipment are used. The first, shown in Fig. 1, is used to perform a 1 kHz calibration test. The second, shown in Fig. 2, is used for the receiver dynamic tests.

Calibration Test: The first test on both sides of the tape is a 1 kHz calibration test, and is used to provide a correction factor for the playback inaccuracy of the tape player.

Receiver Test: Once the calibration test has been performed the test setup is changed to that shown in Fig. 2, and remains that way for all other tests.

Receiver Testing

The following describes the recorded contents of both sides of the tape, and the tests provided.

SIDE 1 - TEST 1

Calibration Tone: Consists of a continuous 1 kHz tone, present for 1 minute. Used to provide a correction factor for tape playback speed inaccuracy using equation 1. The correction is employed when checking receiver channel center frequencies in test 3.

$$X(\%) = (f_0 - 1000)/10 \quad \text{..... Eqn 1}$$

Frequency f_0 is measured as follows, using the test setup shown in Fig. 1.

- Set the level of tone at the receiver input to 2 Vrms. This level setting must not be altered for the duration of the tests on side 1.
- Measure the frequency of the tone f_0 at the receiver input.

SIDE 1 - TEST 2

Decode Check: All tone pairs associated with standard 4 x 4 keypad digits (i.e. L1 H1 through L4 H4)

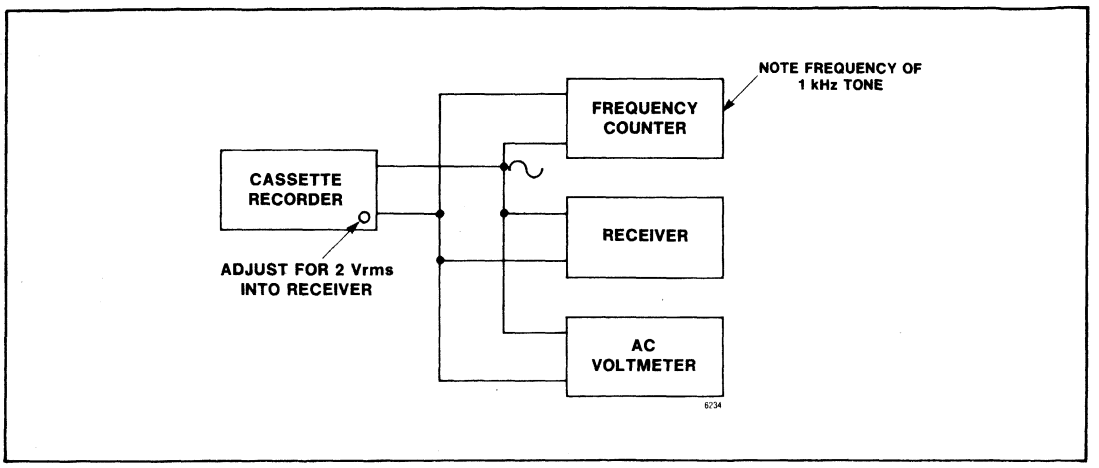


Fig. 1 Test Setup – Calibration Test

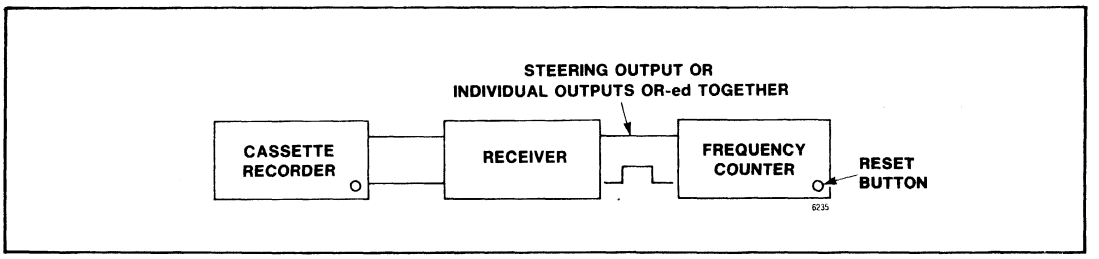


Fig. 2 Test Setup – Receiver Test

are pulsed sequentially using 50 ms bursts at 1 Vrms per frequency. Each tone pair is pulsed 10 times consecutively. The receiver should respond to all tone pairs it is designed to receive.

SIDE 1 - TEST 3

Recognition Bandwidth and Channel Center Frequency Check

This test utilizes the tone pairs L1 H1, L2 H2, L3 H3, and L4 H4 (i.e. digits 1, 5, 9 and 16). Each tone pair requires four tests to complete the check, making 16 sections overall. Each section contains 40 pulses of 50 ms duration, with an amplitude of 0.2 Vrms per frequency.

Four sections covering the tests for one tone pair (1 digit) are:

(a) H frequency at 0% deviation from center, L frequency at +0.1%. L frequency is then incremented in +0.1% steps, up to +4%. The number of tone bursts is noted and designated N^+.

(b) H frequency at 0% deviation, L frequency at −0.1%. L frequency is then incremented in −0.1% steps, up to −4%. The number of tone bursts is noted and designated N^-.

(c) The test in (a) is repeated with the L frequency at 0% and the H frequency varied up to +4%.

(d) The test in (b) is repeated with the L frequency at 0% and the H frequency varied up to −4%.

Receiver Recognition Bandwidth (RRB) is calculated as follows:

$$RRB\% = (N^+ + N^-)/10 \quad \text{..... Eqn 2}$$

Receiver Center Frequency Offset (RCFO) is calculated as follows:

$RCFO\% = X + (N^{+} - N^{-})/20$
(where X is calculated from Eqn 1) ..... Eqn 3

SIDE 1 - TEST 4

Acceptable Amplitude Ratio (Twist)

This test utilizes the tone pairs L1 H1, L2 H2, L3 H3, and L4 H4 (i.e. digits 1, 5, 9 and 16). There are eight sections to the test. Each section contains 200 pulses with a 50 ms duration for each pulse. Initially the amplitude of both tones is 1 Vrms.

Two sections to test one tone pair are:

(a) **Standard Twist:** H tone amplitude is maintained at 1 Vrms, L tone amplitude is attenuated gradually until the amplitude ratio L/H is −20 dB. Note the number of responses from the receiver.

(b) **Reverse Twist:** L tone amplitude is maintained at 1 Vrms, H tone amplitude is attenuated gradually until the amplitude ratio is 20 dB. Note the number of responses from the receiver.

The Acceptable Amplitude Ratio in dB is equal to the number of responses registered in (a) or (b), divided by 10.

SIDE 1 - TEST 5

Dynamic Range

This test utilizes tone pair L1 H1 (digit 1). Thirty-five tone pair pulses are transmitted, with both frequencies starting at 1 Vrms. The amplitude of each is gradually attenuated to −35 dB at a rate of 1 dB per pulse. The Dynamic Range in dBm is equal to the number of responses from the receiver during the test.

SIDE 1 - TEST 6

Guard Time

This test utilizes tone pair L1 H1 (digit 1). Four hundred pulses are transmitted at an amplitude of 1 Vrms per frequency. Pulse duration starts at 49 ms and is gradually reduced to 10 ms. Guard time in ms is equal to (500 – number of responses)/10.

SIDE 1 - TEST 7

Acceptable Signal to Noise Ratio

This test utilizes tone pair L1 H1, transmitted on a noise background. The test consists of three sections in which the tone pair is transmitted 1000 times at an amplitude of 1 Vrms per frequency, but with a different white noise level for each section. The first level is −24 dBV, the second −18 dBV, and the third −12 dBV. The Acceptable Signal to Noise Ratio is the lowest ratio of signal to noise in the test where the receiver responds to all 1000 pulses.

SIDE 2 - TEST 1

Calibration Tone

A repetition of Test 1 - Side 1, at which time the signal level at the receiver input must be recalibrated to 2.0 Vrms. This adjustment is entirely independent of the setting made at Test 1 - Side 1.

SIDE 2 - TEST 2

Talk-Off Test

The test consists of recordings of conversations on telephone trunks make over a long period of time and condensed into a 30 minute period. Receiver immunity to talk-off is determined by the number of responses occurring during this test. A receiver with an acceptable talk-off response should register less than 30.

Summary of Cassette Content

The table below lists the contents of the cassette together with the playing time from the start of the tape. It is recommended that the tape counter reading for each test be recorded in the column provided. This will provide the most convenient method of test location.

TEST	DESCRIPTION			COUNTER	TIME Minutes: Seconds
Introduction					0
Side 1, 1	1 kHz at 2 Vrms				0:20
Side 1, 2	Decode test digits 1 to 16 (10 pulses each)				2:00
Side 1, 3	Recognition bandwidth and centre frequency check (40 pulses each)				3:10
Side 1, 3a	Digit 1	697 Hz	+0.1 to +4%		4:10
Side 1, 3b	Digit 1	697 Hz	−0.1 to −4%		
Side 1, 3c	Digit 1	1209 Hz	+0.1 to +4%		
Side 1, 3d	Digit 1	1209 Hz	−0.1 to −4%		
Side 1, 3e	Digit 5	770 Hz	+0.1 to +4%		
Side 1, 3f	Digit 5	770 Hz	−0.1 to −4%		
Side 1, 3g	Digit 5	1336 Hz	+0.1 to +4%		
Side 1, 3h	Digit 5	1336 Hz	−0.1 to −4%		
Side 1, 3i	Digit 9	852 Hz	+0.1 to +4%		
Side 1, 3j	Digit 9	852 Hz	−0.1 to −4%		
Side 1, 3k	Digit 9	1477 Hz	+0.1 to +4%		
Side 1, 3l	Digit 9	1477 Hz	−0.1 to −4%		
Side 1, 3m	Digit 16	941 Hz	+0.1 to +4%		
Side 1, 3n	Digit 16	941 Hz	−0.1 to −4%		
Side 1, 3o	Digit 16	1633 Hz	+0.1 to +4%		
Side 1, 3p	Digit 16	1633 Hz	−0.1 to −4%		
Side 1, 4	Amplitude ratio (200 pulses each)				12:45
Side 1, 4a	Digit 1	L1/H1	0 to −20 dB		
Side 1, 4b	Digit 1	L1/H1	0 to +20 dB		
Side 1, 4c	Digit 5	L2/H2	0 to −20 dB		
Side 1, 4d	Digit 5	L2/H2	0 to +20 dB		
Side 1, 4e	Digit 9	L3/H3	0 to −20 dB		
Side 1, 4f	Digit 9	L3/H3	0 to +20 dB		
Side 1, 4g	Digit 16	L4/H4	0 to −20 dB		
Side 1, 4h	Digit 16	L4/H4	0 to +20 dB		
Side 1, 5	Dynamic range (35 pulses) Digit 1 −1 to −35 dBV/freq				19:20
Side 1, 6	Guard Time (400 pulses) Digit 1 49 to 10 ms				20:10
Side 1, 7	Signal to Noise (1000 pulses each)				21:50
Side 1, 7a	Digit 1	S/N	24 dB/freq		22:25
Side 1, 7b	Digit 1	S/N	18 dB/freq		24:15
Side 1, 7c	Digit 1	S/N	12 dB/freq		26:05
Side 2	Introduction				0
Side 2, 1	1 kHz at 2 Vrms				0:30
Side 2, 2	Talk-off test (speech)				2:00

ST-BUS Family of ISDN Components

ISO-CMOS ST-BUS™ FAMILY **MT8920**
ST-BUS Parallel Access Circuit
Advance Information

9161-002-058-NA ISSUE 1 MAY 1986

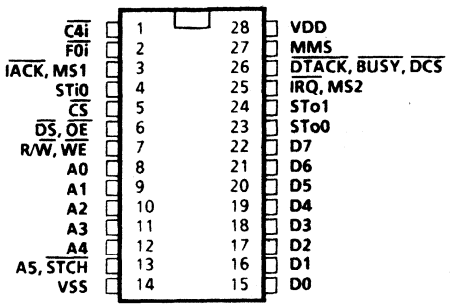
Features

- High speed parallel access to the ST-BUS.
- Five modes of operation
  - Asynchronous µP bus to ST-BUS interface.
  - High speed access - T1 or CEPT trunk format.
  - Parallel bus control mode - T1 or CEPT trunk format.
- Flexible interrupt capabilities - 2 independent interrupt paths with programmed vectoring.
- Selectable loop-around modes with optional frame delay and frame compare.
- Low power ISO-CMOS technology.

Applications

- Interface from parallel environment to digital T1/CEPT trunks.
- Signal processor interface to ST-BUS.
- Computer to DPABX link.
- Messaging in a distributed system.
- Remote access/control over serial bus.

Pin Connections



Ordering Information

MT8920AE	28 Pin Plastic DIP
MT8920AC	28 Pin Ceramic DIP

0°C to 70°C

Description

The ST-BUS Parallel Access Circuit (STPA) provides a method of accessing the ST-BUS from parallel architectures. With five operating modes it offers various system interfaces; a fully asynchronous µP peripheral mode with programmable interrupt vectoring, two high speed modes for parallel access to T1 and CEPT trunks, and two control modes in which the STPA will drive a parallel bus from either the ST-BUS or T1/CEPT digital links. In the high speed mode, the device appears as 24 (T1) or 32 (CEPT) contiguous memory locations and maps these into the proper ST-BUS channels for use with MITEL's digital trunk family. With this mode, fast memory access allows full parallel support of 24 or 32 channels.

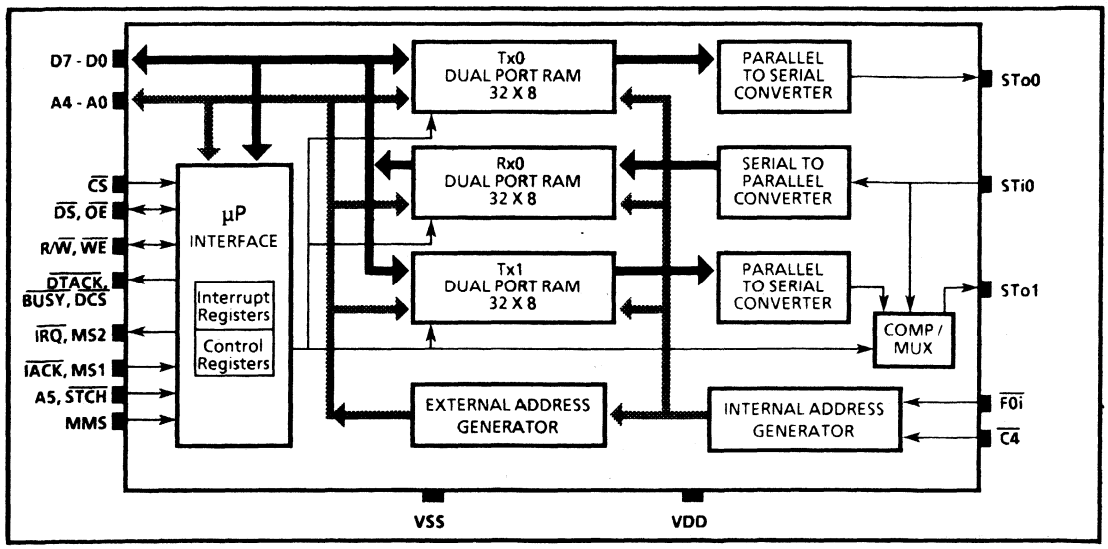


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	- 0.3	7.0	V
2	Voltage on any I/O pin		- 0.3	V_{DD} + 0.3	V
3	Current on any I/O pin	$I_{I/O}$		± 25	mA
4	Storage Temperature	T_{ST}	- 55	125	°C
5	Package Power Dissipation	P_D		1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Input High Voltage	V_{IH}	2.4		V_{DD}	V	for 400mV noise margin
3	Input Low Voltage	V_{IL}	0		0.4	V	for 400mV noise margin
4	Operating Temperature	T_{OP}	0	25	70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current Static	I_{CCS}			10	µA	outputs unloaded
2	Dynamic	I_{CCD}			10	mA	@f_{CK} = 4.096 MHz
3	Input High Voltage	V_{IH}	2.0			V	
4	Input Low Voltage	V_{IL}			0.8	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Fast Access Mode 2 & 3 Timing - (see Fig. 2)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\overline{OE}$ Low to Valid Data	t_{EVD}			80	ns	
2	Address Access Time	t_{AA}			80	ns	
3	Output Disable	t_{OHZ}			40	ns	
4	Address Setup Time	t_{ASF}	20			ns	
5	Data Setup Time	t_{DST}	30			ns	
6	Data Hold Time	t_{DHT}	5			ns	
7	R/$\overline{W}$ High to Address Change	t_{WR}	0			ns	
8	Write Pulse Width	t_{WP}	50			ns	

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

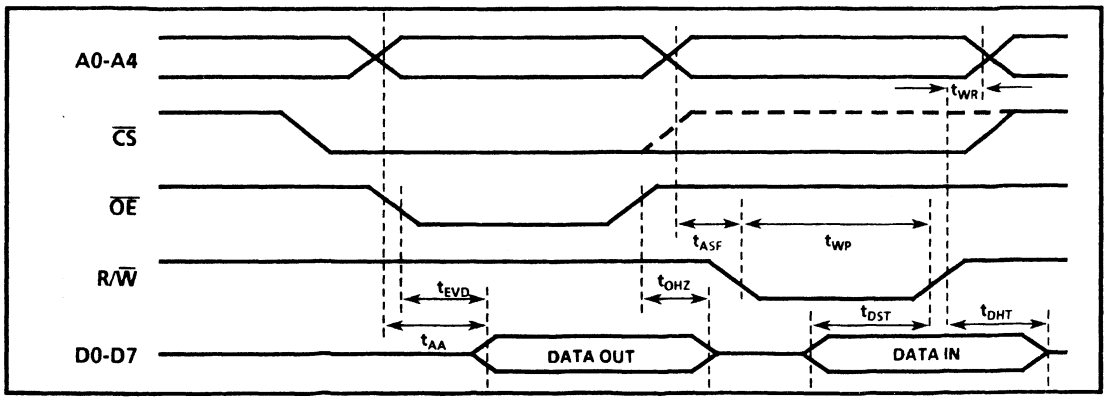


Figure 2. Modes 2 & 3 Timing

Pin Description

Pin #	Name	Type†	Description‡
1	$\overline{C4i}$	I	**4.096 MHz Clock.** The ST-BUS timing clock used to establish bit cell boundaries for the serial bus.
2	$\overline{F0i}$	I	**Framing 0-Type Pulse.** A low going framing pulse used to synchronize the STPA to the 2048 kbit/s ST-BUS stream. The first falling edge of $\overline{C4i}$ subsequent to the falling edge of $\overline{F0i}$ identifies the start of a frame.
3	$\overline{IACK}$	I	**Interrupt Acknowledge (Mode 1).** This active low input signals that the current bus cycle is an interrupt vector fetch cycle. Upon receiving this acknowledgement the STPA will output a user-programmed vector number on D_0 - D_7 indicating the source of the interrupt.
	MS1	I	**Mode Select 1 (Mode 2,3,4,5).** This input is used to select the device operating modes. A low applied to this pin will select modes 4 and 5 while a high will select modes 2 and 3.
4	STi0	I	**ST-BUS Input 0.** This is the input for the 2048 kbit/s ST-BUS serial data stream.
5	$\overline{CS}$	I	**Chip Select.** This active low input is used to select the STPA for a µP access. In modes 4&5 this input signal is internally synchronized to the falling edge of $\overline{C4i}$.
6	$\overline{DS}$	I	**Data Strobe (Mode 1).** This active low input indicates to the STPA that valid data is on the data bus during a write operation or that the STPA must output valid data on the data bus during a read operation.
	$\overline{OE}$	I	**Output Enable (Mode 2,3).** This active low input enables the data bus driver outputs.
	$\overline{OE}$	O	**Output Enable (Mode 4,5).** This active low output indicates that the selected device is to be read and that the data bus is available for data transfer.
7	R/$\overline{W}$	I	**Read/Write (Mode 1,2,3).** This signal defines the data bus transfer as a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$ = 0) cycle.
	$\overline{WE}$	O	**Write Enable (Mode 4,5).** This active low output indicates the data on the data bus is to be written into the selected location of an external device.
8-12	A0-A4	I	**Address Bus (Mode 1,2,3).** These inputs are used to select the internal registers and two-port memories of the STPA.
	A0-A4	O	**Address Bus (Mode 4,5).** These address outputs are generated by the STPA and reflect the position in internal RAM where the information will be fetched from or stored in. Addresses generated in this mode are used to access external devices for direct memory transfer.
13	A5	I	**Address Bit A5 (Mode 1).** This input is used to extend the address range of the STPA. A5 selects internal registers when high and Tx/Rx RAMs when low.
	A5	I	**Address Bit A5 (Mode 2,3).** This input is used to extend the address range of the STPA. A5 selects Tx0/Rx0 RAMs when low and Tx1/Rx0 RAMs when high.
	$\overline{STCH}$	O	**Start of Channel (Mode 4,5).** This signal is a low going pulse which indicates the start of an ST-BUS channel. The pulse is four bits wide and begins at the start of each valid channel.
14	VSS	-	**Power Supply Input.** (Ground).
15-22	D0-D7	B	**Data Bus. Bidirectional Data Bus.** This bus is used to transfer data to or from the STPA during a write or read operation.
23	STo0	O	**ST-BUS Output 0.** This pin supplies the output ST-BUS 2048 kbit/s serial data stream from Tx0 two-port RAM.
24	STo1	O	**ST-BUS Output 1.** In modes 1,2 and 3 this pin supplies the output ST-BUS 2048 kbit/s serial data stream from Tx1 two-port RAM. In modes 4 and 5, information arriving at STi0 is output here with one frame delay.

† Pin types are: I - Input, O - Output, B - Bidirectional.
‡ Pin Descriptions pertain to all modes unless otherwise stated.

Pin Description - cont'd

Pin #	Name	Type†	Description‡
25	$\overline{IRQ}$	O	**Interrupt Request (Mode 1).** This open drain output indicates when an interrupt condition has been raised within the STPA.
	MS2	I	**Mode Select 2 (Mode 2,3,4,5).** This input is used to select the device operating mode. A low applied to this pin will select a 24 (T1) channel mode while a high will select a 32 (CEPT) channel mode.
26	$\overline{DTACK}$	O	**Data Transfer Acknowledge (Mode 1).** This open drain output is supplied by the STPA to acknowledge the completion of data transfers back to the µP. On a read of the STPA, $\overline{DTACK}$ low indicates that the STPA has put valid data on the data bus. On a write, $\overline{DTACK}$ low indicates that the STPA has completed latching the µP's data from the data bus.
	$\overline{BUSY}$	O	**BUSY (Mode 2,3).** This open drain output signals that the controller and the ST-BUS are accessing the same location in the dual-port RAMs. It is intended to delay the controller access until after the ST-BUS completes its access.
	$\overline{DCS}$	O	**Delayed Chip Select (Mode 4,5).** This low going pulse, which is four bit cells long, is active during the last half of a valid channel. This signal is used to daisy-chain together two STPA's in modes 4 and 5 that are accessing devices on the same parallel data bus.
27	MMS	I	**Master Mode Select (Reset).** This pin selects between either mode 1 (MMS = 1), or modes 2,3,4,5 (MMS = 0). If MMS is taken from low to high after power is applied to the STPA , the control registers will be reset.
28	VDD	-	**Power Supply Input.** Positive supply (+ 5v).

† Pin types are: I - Input, O - Output, B - Bidirectional.
‡ Pin Descriptions pertain to all modes unless otherwise stated

Mode	MMS	MS1	MS2	Mode of Operation	Function
1	1	X	X	Asynchronous µP Peripheral	The STPA provides P/S, S/P conversions through a 68000-type interface. Two Tx RAMs and one Rx RAM are available along with full interrupt capability. 32 channel or 24 channel support is available.
2	0	1	0	Fast Access - 24 Channel	The STPA provides a fast access interface to Tx0, Tx1 and Rx0 RAMs in a 24 channel format. This mode is intended for full parallel support of 24 channel T1 trunks including ESF .
3	0	1	1	Fast Access - 32 Channel	The STPA provides a fast access interface to Tx0, Tx1 and Rx0 RAMs in a 32 channel format. This mode is intended for full parallel support of 32 channel CEPT trunks.
4	0	0	0	Parallel Bus Controller - 24 channel	The STPA will synchronously drive the parallel bus using the external address generator and provide all data transfer signals. This mode is intended to support 24 channel devices in the absence of a parallel bus controller.
5	0	0	1	Parallel Bus Controller - 32 channel	The STPA will synchronously drive the parallel bus using the external address generator and provide all data transfer signals. This mode is intended to support 32 channel devices in the absence of a parallel bus controller.

Table 1. STPA Modes of Operation

General Description

The STPA is a monolithic device fabricated in MITEL's low power ISO-CMOS technology that provides a simple means of accessing the ST-BUS from a parallel environment. The device meets the needs of parallel-architecture systems requiring simple, drop-in digital trunk solutions. This device provides a complete parallel interface for use with the entire family of MITEL ST-BUS products and, in particular, MITEL's Digital Trunk products.

In addition to providing an excellent parallel interface for digital trunks, the STPA has incorporated into it many features which make it a versatile device in numerous applications.

A functional block diagram of the STPA is shown in Fig. 1. The device is designed around three 32-byte dual-port memories, two of which supply data to parallel-to-serial shift registers for transmission on the outgoing ST-BUS. The third memory receives data via the serial-to-parallel shift register from the incoming ST-BUS. All three dual-port memories are accessed via the parallel port of the STPA.

The remaining blocks of circuitry consist of a µP interface, internal and external address generators and a comparator/multiplexer circuit. The µP interface includes control registers and interrupt registers. The control registers allow the user to enable interrupts, select modes of interrupt operation, select modes of interrupt service acknowledgement, configure the RAMs as 32 channels or 24 channels, select various loop-around paths, and provide comparisons with delayed frames using the comp/mux circuitry. Two independent sets of interrupt registers allow separate sources of interrupts. Each set of interrupt registers consists of a channel source register, a byte pattern register and a bit mask register. Additional flag registers are used to indicate the cause of an interrupt. When used as a 68000 µP peripheral, user-defined vector numbers can be programmed into a vector register and later fetched by the µP during an interrupt acknowledge cycle.

The internal address generator is used to access the dual-port memories on the ST-BUS side of the device. In a 24 channel mode this circuit accesses only the first 24 consecutive RAM locations and maps these into 24 of the 32 ST-BUS channels. Every fourth channel (ie. 0,4,8,12,16,20,24 and 28) is set to FF_{16}. The external address generator is designed to drive devices on the external parallel address bus and thereby eliminate the need for a separate controller to perform data transfers.

The STPA has five modes of operation. These are selected using the mode select pins MMS, MS1, and MS2 (see Table 1). Many of the µP interface pins are reconfigured for the various modes of operation allowing more flexibility and versatility (see Fig. 3). Following is a brief description of the five operating modes.

Mode 1 - Asynchronous µP Peripheral

In mode 1 the STPA operates as an asynchronous 68000 type microprocessor peripheral. The interface signals presented in this mode include $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$ (Data Strobe), $\overline{DACK}$ (Data Acknowledge), $\overline{IRQ}$, and $\overline{IACK}$ (Interrupt Acknowledge). All three internal dual-port memories (Tx0, Rx0, Tx1) are made available and may be configured as 24 or 32 byte RAMs. Also accessible are the control registers and the interrupt registers. This mode allows the STPA to be used as a signalling and/or link control device, a channel data access device or a messaging device.

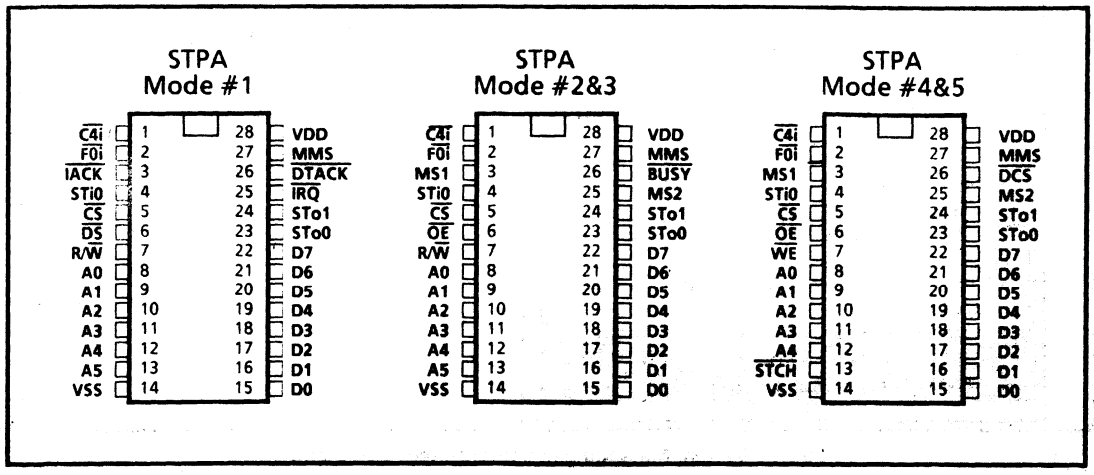


Figure 3. Modes 1-5 Pin Connections

Mode 2 - Fast Access (24 channel)
In mode 2 the STPA operates as a RAM type interface utilizing the signals $\overline{CS}$, $\overline{OE}$, R/$\overline{W}$, and $\overline{BUSY}$. Access times are typically 85 ns for read or write operations. The STPA, in this mode, is configured to interface to ST-BUS devices using 24 data channels such as MITEL's T1 Trunk family. It uses the first 24 locations of the internal dual-port RAMs (Tx0, Rx0, Tx1) as outlined in the general description above. In this mode neither the control registers nor the interrupt registers are accessible.

Mode 3 - Fast Access (32 channel)
Mode 3 is similar to mode 2 except that the STPA is configured to support devices using 32 data channels such as MITEL's CEPT Trunk family.

Mode 4 - Parallel Bus Controller (24 channel)
In this 24 channel mode the STPA outputs all necessary parallel bus signals required to synchronously drive external devices such as RAMs, FIFOs and latches. When channel N is present on the ST-BUS, the STPA generates address N + 1 on the address bus with $\overline{OE}$ low to output data from an external device and latch it into the STPA. During the same channel the STPA will also generate address N – 1 with $\overline{WE}$ low to write from the STPA to an external device.

A read or a write access requires 1/4 of a channel time (1/4 X 3.91 µsec). Therefore, 4 bus accesses are possible per channel time (2 reads and 2 writes). This is made possible through the use of delayed chip select ($\overline{DCS}$). This output, which is active at 1.95 µsec (1/2 X 3.91 µsec) into a channel, can be tied to a second STPA's $\overline{CS}$ input. Using this method two STPAs may be 'daisy-chained' allowing two ST-BUS links to share a common parallel bus.

Mode 5 - Parallel Bus Controller (32 channel)
Mode 5 is identical to mode 4 except that it supports 32 ST-BUS channels.

Applications

This simple yet versatile device is useful in numerous applications allowing users quick and easy access to MITEL's ST-BUS.

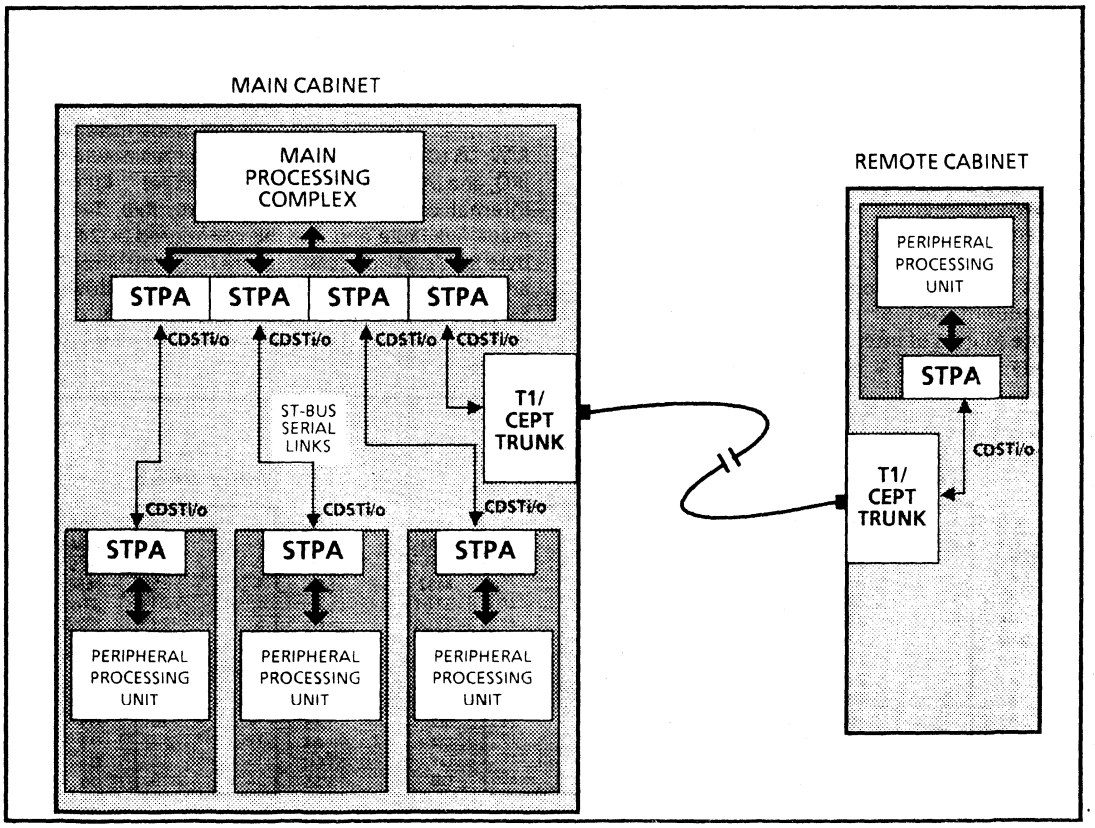


Figure 4. System Messaging in a Distributed Architecture

System Messaging Application

The STPA provides an ideal communications link between a master system controller and a number of distributed processing elements (Fig. 4). In this application, control information is passed back and forth over the 2.048 Mbit/sec serial ST-BUS links. Used in mode 1, the STPA appears as a virtual 32 byte, dual-port memory between the main processing complex and the peripheral units. Messages are simply written to the 32 byte RAM and are transferred serially via the 4-wire bus to the receiving STPA where they can be read by the peripheral processor. In mode 1 the STPA provides a fully asynchronous µP interface ideally suited to 68000 type control devices.

Overhead associated with receiving messages can be minimized by using the STPA's flexible interrupt capabilities. Interrupts can be programmed to trigger on a recurring pattern sent with every message or on a change of state of a particular bit/byte in a predetermined channel location. Upon interruption, the receiving processor would fetch the message, which may be up to 32 bytes long. If the device is used as a 68000 peripheral it may be programmed to supply an interrupt vector number on interrupt acknowledge. Otherwise, interrupts may be acknowledged in a more conventional manner by simply reading the interrupt source registers.

The concept of a serial messaging link can be expanded upon to include communication with remote units or other system cabinets, as shown in Fig. 4. Using MITEL digital trunk modules, the link may be extended over greater distances.

This type of messaging scheme provides many advantages. Foremost, problems associated with routing large busses across backplanes and between shelves is alleviated since the link uses only 4 wires as opposed to 8, 16 or more. Also, messaging does not normally require the available data bandwidth of a parallel bus. In contrast, the ST-BUS provides a more appropriate implementation of such links.

Parallel DPABX to Serial Trunk Interface

The STPA has two modes specifically intended for interfacing parallel DPABX environments to MITEL's family of Digital Trunk devices. These modes of operation support both T1 devices (mode 2) for

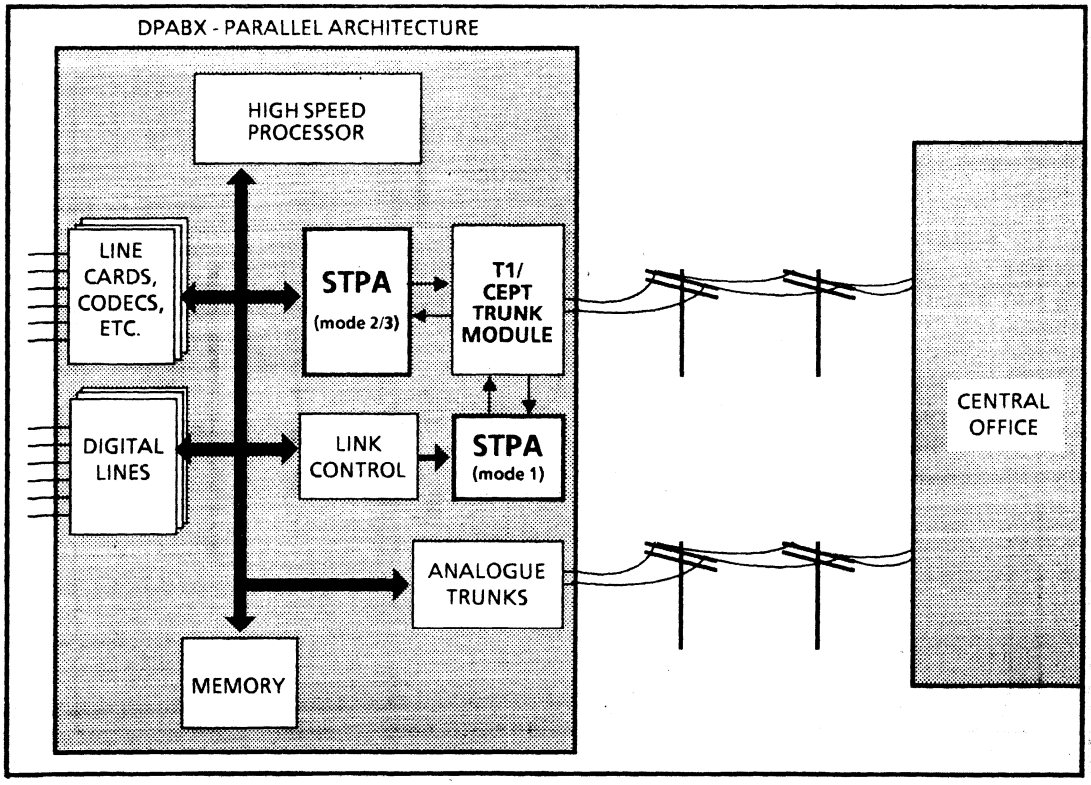


Figure 5. Parallel DPABX to Digital Trunk Interface

North American products and CEPT devices (mode 3) for European products. Read and Write operations are fast, typically in the order of 85 nsec for each. The longest operation occurs when access is requested from the parallel port for the same memory location currently being accessed by the S/P or P/S converters. A read/write operation in this case will take up to a maximum of 244 nsec. At these speeds full parallel support of 24 or 32 channels is possible.

In mode 2 the STPA presents itself to a parallel controller as 24 consecutive memory locations for use in T1 applications. The device then assigns these to the proper ST-BUS channels for use with the MT8975, MH89750, and MH89756 digital T1 trunk interfaces. In mode 3 the device appears as 32 consecutive memory locations corresponding to the 32 channels used by the MT8978, MH89780 and MH89785 CEPT trunk interfaces.

In Figure 5 the link control block is shown as a separate functional unit. This circuit would supply and monitor link and signalling information. It may be implemented using an STPA operating in mode 1 or it may consist of a MITEL MT8980 Digital Crosspoint switch operating in message mode. The MT8980 would allow more than one trunk to be controlled while the STPA would provide interrupt capability for alarms, loss of frame synchronization, etc.

Digital Signal Processor to ST-BUS Interface

Modes 2&3 of the STPA also provide the capability of interfacing other devices to the ST-BUS. Fast access speeds of the STPA now make it possible to easily interface Digital Signal Processing capabilities directly to the ST-BUS. This allows many desireable, yet previously difficult to implement, functions to be designed into systems using a serial bus architecture. Some of the possible functions include;

- Digital Filtering
- Voice Conferencing
- Speech/Data Compression
- Encryption
- Tone Detection and Generation
- Frequency Spectrum Analysis
- Image Processing
- μ-Law to A-Law conversion
- Echo Cancellation
- Modulation
- Speech Synthesis and Recognition

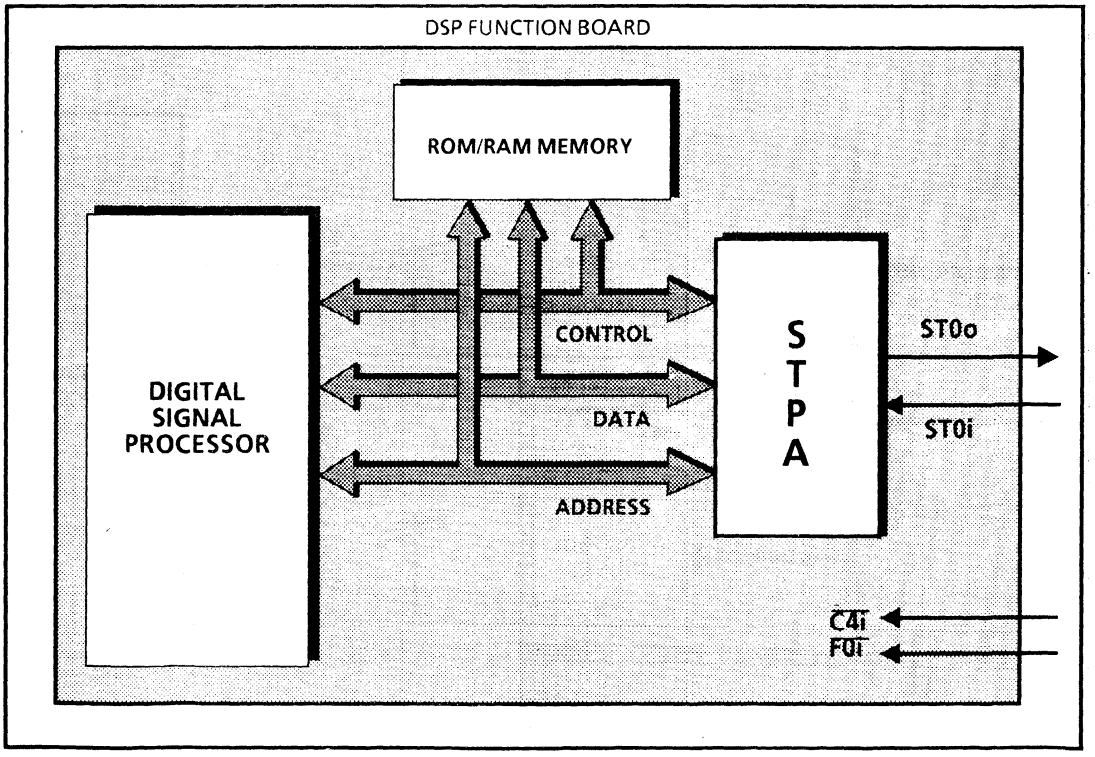


Figure 6. Interfacing DSP to ST-BUS

Figure 6 shows a simplified block diagram of a typical DSP application module. In mode 3 the STPA has a standard RAM-type interface using the signals $\overline{WE}$, $\overline{OE}$, $\overline{CS}$ and $\overline{BUSY}$. Individual channels of the ST-BUS are accessed by reading and writing to the corresponding memory location in the STPA's 32 byte dual-port memories.

In this application, the Signal Processor requires an indication of when new data has arrived in a particular channel. This can be derived from the ST-BUS timing signals $\overline{F0i}$, $\overline{C4i}$ and, if required, the $\overline{STCH}$ signal which is supplied by the STPA to indicate the start of a new channel. Since the STPA uses dual-port memories, the possibility of contention does exist when accessing a particular channel. The $\overline{BUSY}$ signal will indicate such cases and will hold off the access for no longer than 244 nsec.

Remote Control and Sensing Application

The STPA in modes 4 and 5 allows peripheral devices to be driven remotely via the ST-BUS. The STPA, in a sense, provides a remote extension of the central microprocessor's parallel bus. Figure 7 shows a typical application in which an automated plant is controlled from a central computing system. The distance over which the automated assembly line and the controlling system may be separated can be increased using T1 or CEPT trunks or even optical fibre links.

The STPA provides an incrementing address counter and write enable ($\overline{WE}$) and output enable ($\overline{OE}$) signals for accessing all devices on the parallel bus. All devices may be read from and written to once each ST-BUS frame (125 µsec). The STPA may drive up to 32 read/write devices on the bus.

The application in Figure 7 shows a number of different devices common to a typical assembly operation. This example may be extrapolated, however, to any application requiring remote control or sensing in which it is not necessary nor desirable to have a microprocessor at the peripheral location to perform these operations.

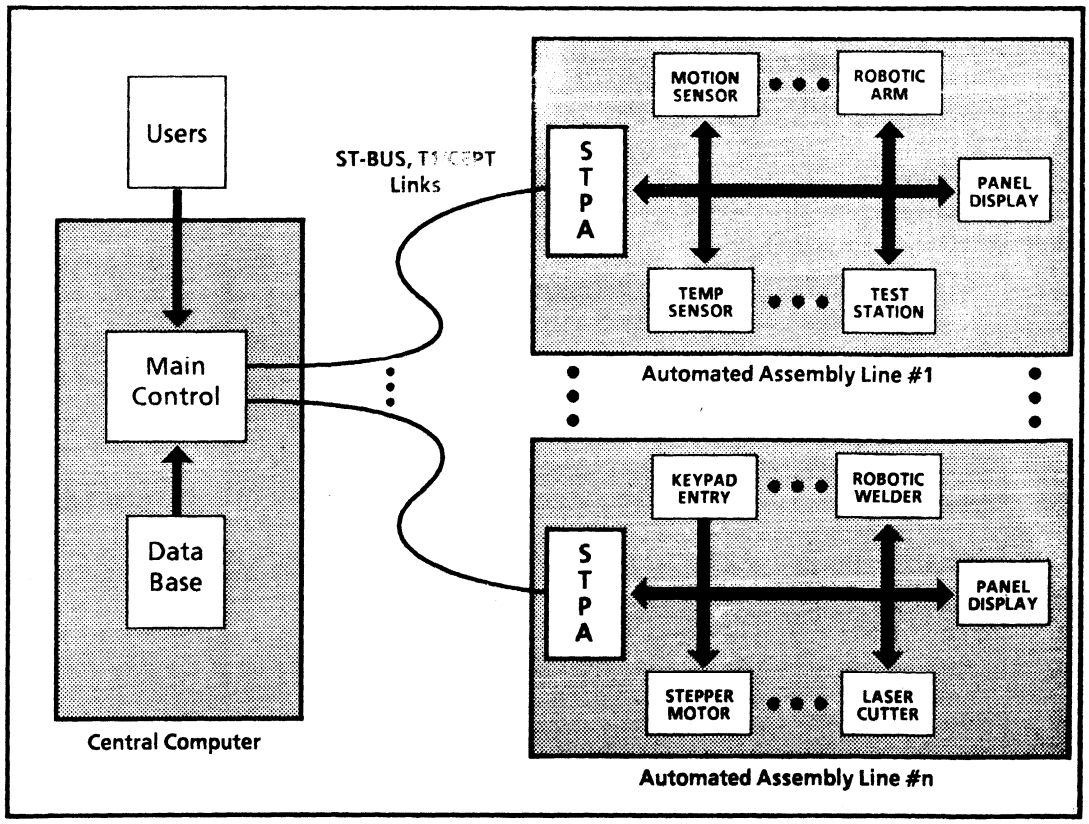


Figure 7. Remote Control/Sensing Application

ST-BUS™ FAMILY MT8930
Subscriber Network Interface Circuit

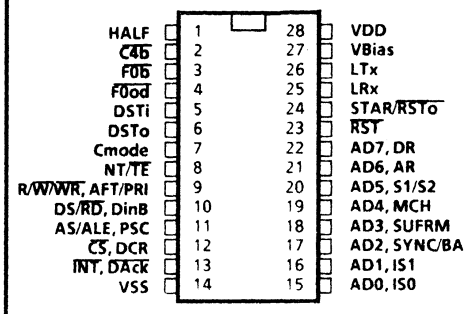
Advance Information

9161-002-073-NA ISSUE 1 June 1986

Features

- CCITT I.430 S and T interface compatible
- Full-duplex 2B + D , 192 kbit/s transmission
- Alternate Space Inversion line code
- Terminal activation/deactivation
- Access contention resolution
- Point-to-point, point-to-multipoint and star configuration compatible
- Master (NT)/Slave (TE) modes of operation
- Complete loopback testing capabilities
- On-chip line data clock generation
- HDLC on chip to format data as per CCITT X.25
- 8 bit Motorola/Intel microprocessor interface
- MITEL ST-BUS™ compatible
- Low power ISO²-CMOS technology
- Single 5 volt power supply

Pin Connections



Ordering Information

MT8930AC 28 Pin CERDIP
0°C to +70°C

Applications

- ISDN S or T interface
- Creates a 2-chip NT1 solution with Mitel MT8972 U-Interface
- Digital sets (TE1) - 4 wire ISDN interface
- Digital PABXs, Digital Line Cards (NT2)
- D-channel controller for ISDN basic access

Description

The MT8930 Subscriber Network Interface Circuit (SNIC) is a device which implements the CCITT I.430 Recommendation for the ISDN S and T reference points. Providing point-to-point and point-to-multipoint digital transmission, the SNIC may be used at either end of the subscriber line (NT or TE). An HDLC transceiver for the D-channel protocol is included and controlled through a Motorola/Intel microprocessor port. A controllerless mode allows simple implementation of an NT1 function in conjunction with the MT8972 DNIC. The MT8930 is fabricated in Mitel's ISO²-CMOS process.

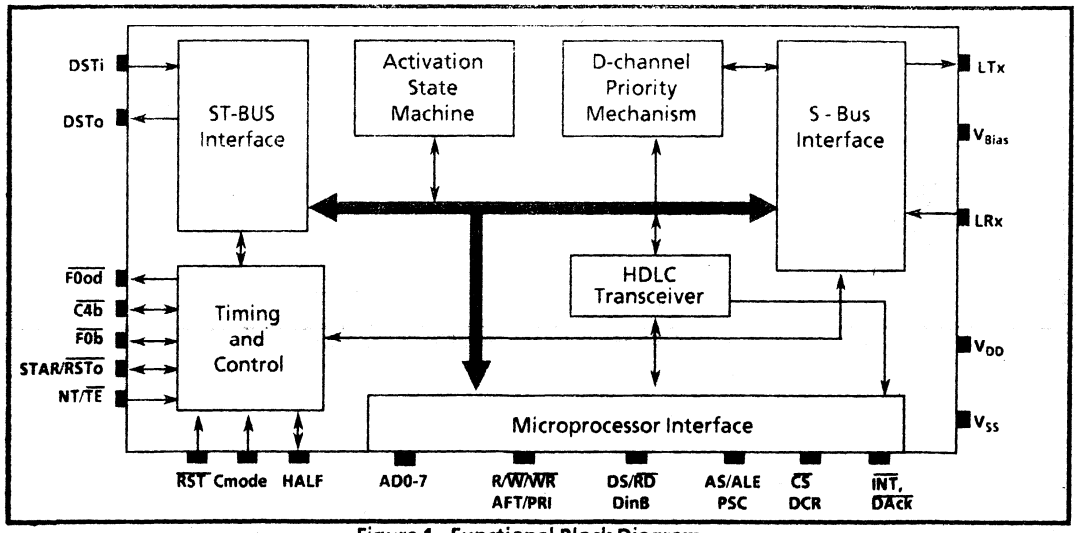


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings*

	Parameters	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any I/O pin	$V_{I/O}$	-0.3	V_{DD} + 0.3	V
3	Current on any I/O pin	$I_{I/O}$		20	mA
4	Storage Temperature	T_{ST}	-55	125	°C
5	Package Power Dissipation	P_D		1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2		Input High Voltage	V_{IH}	2.4		V_{DD}	V	For 400mV noise margin
3		Input Low Voltage	V_{IL}	0		0.4	V	For 400mV noise margin
4		Operating Temperature	T_{OP}	0	25	70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	Supply Current	I_{DD}		8		mA	Outputs unloaded
2		Input High Voltage	V_{IH}	2.0			V	Digital inputs
3		Input Low Voltage	V_{IL}			0.8	V	Digital inputs
4		Output High Current	I_{OH}		15		mA	V_{OH} = 2.4V Digital outputs
5		Output Low Current	I_{OL}		7.5		mA	V_{OL} = 0.4V Digital outputs

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

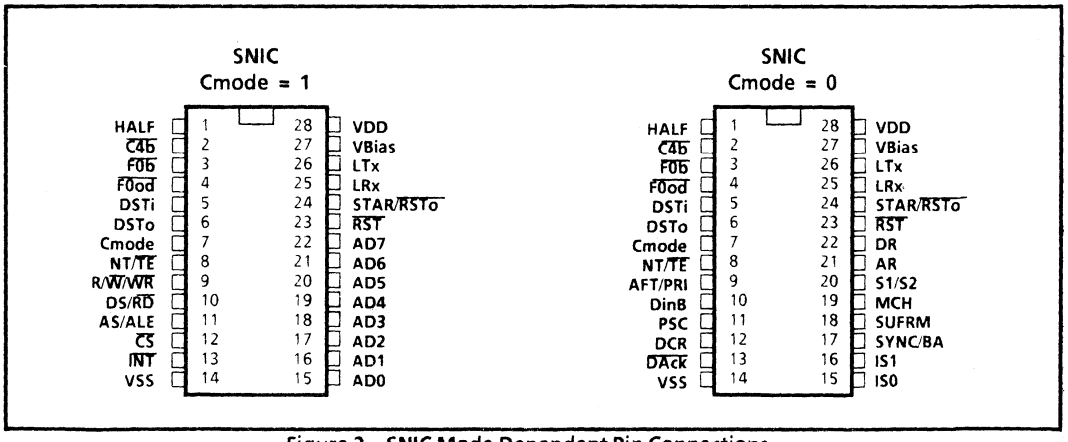


Figure 2 - SNIC Mode Dependent Pin Connections

Pin Description

Pin #	Name	Description
1	HALF	**HALF Input/Output:** in NT mode, this is an input identifying which half of the S-interface frame is currently being written over the ST-BUS. In TE mode, this is an output indicating which half of the received S-interface frame is currently available on the ST-BUS.
2	$\overline{C4b}$	**4.096MHz Clock:** a 4.096MHz ST-BUS Data Clock input in NT mode. In TE mode an output 4.096MHz clock phase-locked to the line data signal.
3	$\overline{F0b}$	**Frame Pulse:** a negative pulse output indicating the beginning of active ST-BUS channel times in TE mode. Frame pulse input in NT mode.
4	$\overline{F0od}$	**Delayed Frame Pulse Output:** a negative pulse output indicating the end of active ST-BUS channel times.
5	DSTi	**Data ST-BUS Input:** a 2048 kbit/s serial PCM/data ST-BUS input with D, C, B1, and B2 channels assigned to the first four timeslots. These channels contain data to be transmitted on the line and chip control information.
6	DSTo	**Data ST-BUS Output:** a 2048 kbit/s serial PCM/data ST-BUS output with D, C, B1 and B2 channels assigned to the first four timeslots and tristated for the remaining time. These channels contain data received from the line and chip status information.
7	Cmode	**Controller Mode Select Input:** when high, microprocessor control is selected. When low the controllerless mode is enabled and the microport pins are redefined as control inputs and status outputs as described below.
8	NT/$\overline{TE}$	**Network Terminator/Terminal Equipment:** ST-BUS operational mode select input. The device is configured as a Network Terminator (NT) when high, or for Terminal Equipment (TE) when low.
9	R/$\overline{W}$/$\overline{WR}$ AFT/PRI	**Read/Write or Write Input (Cmode = 1):** defines the data bus transfer as a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$ = 0) in Motorola bus mode. Redefined to $\overline{WR}$ in Intel bus mode. **Adaptive-Fixed Timing/Priority Select Input (Cmode = 0):** in NT mode, causes the VCO and RX filters/peak detectors to be disabled in favor of fixed timing and thresholds for short passive bus operation (0-fixed, 1-adaptive). Priority input in TE mode. High priority (PRI = 1) is normally reserved for signalling.
10	DS/$\overline{RD}$ DinB	**Data Strobe/Read Input (Cmode = 1):** active high input indicates to the SNIC that valid data is on the bus during a write operation or that the SNIC must output data during a read operation in Motorola bus mode. Redefined to $\overline{RD}$ in Intel µP bus mode. **D-Channel in B1 Timeslot Input (Cmode = 0):** active high input that causes all eight ST-BUS D-channel bits, instead of the usual two bits, to be routed to and from the S-interface B1 timeslot. When asserted, marks are transmitted in the S-interface D-channel.
11	AS/ALE PSC	**Address Strobe/Address Latch Enable Input (Cmode = 1):** Active high input used to strobe address into the SNIC during microprocessor access. Redefined to ALE in Intel microprocessor bus mode. **Parallel/Serial Control Input (Cmode = 0):** determines if the serial C-channel (PSC = 0) or microport pins (PSC = 1) are the source of chip control when controllerless mode is selected. If the ST-BUS is chosen as the source, the dedicated control input pins are ignored but the status output pins remain valid.
12	$\overline{CS}$ DCR	**Chip Select Input (Cmode = 1):** active low input used to select the SNIC for µP access. **D-Channel Request Input (Cmode = 0):** an active high input that in TE mode only causes the SNIC to transmit a "01111110" flag if the number of consecutive marks seen on the received E-channel exceeds the device priority. Otherwise the device waits until the D-channel is clear and then transmits the flag. The $\overline{DAck}$ output signals the successful acquisition of the D-channel. If DCR goes low at any time, marks are transmitted in the D-channel.
13	$\overline{INT}$	**Interrupt Output (Cmode = 1):** (open drain) output indicating either new data available or an asynchronous HDLC event. It can be used by the microprocessor or a DMA controller to synchronize the transfer of data to and from the S-interface. (continued)

Pin Description (continued)

Pin #	Name	Description
13 cont'd	$\overline{DACk}$	**D-Channel Acknowledge (Cmode = 0):** in TE mode only indicates that the SNIC has gained access to the D-channel in response to a DCR and has transmitted an opening flag. The user should immediately begin transmitting the rest of the packet over the ST-BUS D-channel. If this signal goes high in the middle of transmission the channel has been lost and the packet should be retransmitted.
14	V_{SS}	**Ground.**
15-22	AD0-7	**Bidirectional Address/Data Bus (Cmode = 1):** electrically and logically compatible to either Intel or Motorola micro-bus specifications. If DS is low on the falling edge of AS then the chip operates to Motorola specs. If DS is high on the falling edge of AS Intel mode is selected. Taking $\overline{RST}$ low sets Motorola mode.
15-16	IS0-IS1	**Internal State Outputs (Cmode = 0):** Binary encoded state number outputs. IS1 / IS0 / NT State / TE State 0 / 0 / deactivated / deactivated 0 / 1 / pending activation / activation request 1 / 0 / pending deactivation / synchronized 1 / 1 / activated / activated
17	SYNC/BA	**Synchronization/Bus Activity Output (Cmode = 0):** output indicating synchronization to incoming RX frames when part is activated. Active when three successive frames conforming to the 14-bit bipolar violation criteria have been detected. If part is deactivated this pin indicates the presence of bus activity.
18	SUFRM	**Superframe Input/Output (Cmode = 0):** superframe input in NT mode or output in TE mode. Asserting this bit in NT mode forces the F_A, N pair to 1, 0. This bit going high in TE mode indicates that F_A, N = 1, 0 has been received.
19	MCH	**Maintenance Channel Input/Output (Cmode = 0):** an output in NT mode which is valid only in the frame following the transmission of SUFRM. In TE mode, this is the maintenance channel input which is transmitted in the F_A and N bits when SUFRM has been received.
20	S1/S2	**S1, S2 Input/Output (Cmode = 0):** S-bit input in NT mode or S-bit output in TE mode. S1 is read or written when HALF = 0 while S2 is read or written when HALF = 1.
21	AR	**Activate Request Input (Cmode = 0):** asserting AR will initiate the appropriate S-interface activation sequence coded in the NT or TE activation finite state matrix.
22	DR	**Deactivate Request Input (Cmode = 0):** asserting DR high will initiate the appropriate S-interface deactivation sequence coded in the NT or TE activation finite state matrix.
23	RST	**Reset Input:** Schmitt trigger reset input. Sets all control registers to the default conditions, resets activation state machines to the deactivated state, resets HDLC, clears the HDLC FIFOs, and sets microport to Motorola bus mode, if active.
24	STAR/$\overline{RSTo}$	**Star Output/Reset Output:** 192kbit/s RX data output fixed relative to the ST-BUS timebase. A group of NTs can be wire or'ed together to create a Star configuration (Star pin must be tied to V_{DD} with a 10 kΩ resistor). Active low reset output in TE mode indicating 128 consecutive marks have been received. Can be connected directly to $\overline{RST}$ to allow NT to reset all TE's on the bus.
25	LRx	**Receive Line Signal Input:** this is a high impedance input for the psuedo-ternary (ASI) line signal to be connected to the line through a 2:1 ratio transformer. A DC bias level on this input equal to V_{Bias} must be maintained.
26	LTx	**Transmit Line Signal Output:** this is a high impedance current source output designed to drive a nominal 50 ohm line through a 2:1 ratio transformer.
27	V_{Bias}	**Bias Voltage:** analog ground for Tx and Rx transformers. This pin must be decoupled to V_{DD} through a 10μF capacitor with good high frequency characteristics.
28	V_{DD}	**Power Supply Input.**

Functional Description

The MT8930 Subscriber Network Interface Circuit (SNIC) is a multifunction transceiver providing a complete interface to the S/T Reference Point as specified in the CCITT I.430 Recommendations. Implementing both point-to-point and point-to-multipoint voice/data transmission, the SNIC may be used at either end of the digital subscriber loop. A programmable digital interface allows the MT8930 to be configured as a Network Terminator (NT) or as a Terminal Equipment (TE) device.

The SNIC supports 192 kbit/s (2B + D + overhead) full duplex data transmission on a 4-wire balanced transmission line. Transmission capability for both B and D channels, as well as related timing and synchronization functions, are provided on chip. The signalling capability, and procedures necessary to enable customer terminals (TE's) to be activated and deactivated when necessary, form part of the MT8930's functionality. The SNIC handles D-channel resource allocation and prioritization for access contention resolution and signalling requirements in passive bus line configurations. Control and status information allows implementation of maintenance functions and monitoring of the device and the subscriber loop.

An HDLC transceiver is included on the SNIC for link access protocol handling via the D-channel. Depacketized data is passed to and from the transceiver via the microprocessor port. Two 19 byte deep FIFO's, one for transmit and one for receive, are provided to buffer the data. The HDLC block can be set up to transmit or receive to/from either the S-interface port or the ST-BUS port. Further, these transmit and receive destinations and sources can be independently selected, i.e. transmit to S-interface while receiving from ST-BUS. The transmit and receive paths can be separately enabled or disabled. Both one and two byte address recognition is supported by the SNIC. A transparent mode allows data to be passed directly to the D channel without being packetized.

A block diagram of the MT8930 is shown in Figure 1. The SNIC has three interface ports: a 4-wire CCITT compatible S/T interface (subscriber loop interface), a 2048 kbit/s ST-BUS serial port, and a general purpose parallel microprocessor port. This 8-bit parallel port can be configured to be compatible with either Motorola or Intel microprocessor bus signals and timing. In the controllerless mode of operation, the parallel port reverts to hardwire control pins. This allows implementing a simple NT1 function by combining the MT8930 back-to-back with a U-interface device, such as MITEL's MT8972 DNIC.

The three major blocks of the MT8930 consisting of the system serial interface (ST-BUS), HDLC transceiver, and the digital subscriber loop interface (S-interface) are interconnected by high speed data busses. Data sent to and received from the S-interface port (B1, B2 and D channels) can be accessed from either the parallel microprocessor port or the serial ST-BUS port. This is also true for SNIC control and status information (C-channel). Depacketized D-channel information to and from the HDLC section can only be accessed through the parallel microport.

S-Reference Point Interface

The SNIC transmits and receives data at 192 kbit/s with a pseudo-ternary (ASI) line code with 100% pulse width. ASI is essentially the same as AMI, except that spaces as opposed to marks generate the pulse transitions. A binary zero is represented by a positive or negative pulse, while a binary one is represented by no line signal. The SNIC tolerates reversals within either the Rx or Tx pairs between the NT and the TE group. Reversal of the TE transmit pair between two or more TE's will make the S-interface inoperable.

The line interface is made up of three pins, LTx, LRx and V_{Bias} LTx drives the transmit signal onto the transmit side of the 4-wire subscriber line. LRx senses the far-end signal from the receive side of the 4-wire line. Both transmit and receive signals are referenced to an internally generated analog ground which is brought out via the V_{Bias} pin. This pin should be decoupled to V_{DD} with a 10µF capacitor, having good high frequency characteristics.

Line Configurations

The SNIC can be used with both point-to-point and point-to-multipoint wiring configurations. These are described below:

-Point to Point: A maximum 1 km line length with only one transmitter and one receiver active at the interface at any one time (i.e. 2 SNIC's)

-Short Passive Bus: A maximum 150 metre bus made up of no more than 8 simultaneously active TE's with 10 metre connections.

-Extended Passive Bus: A maximum 500 metre line length and a far end grouping of terminals

with a differential distance between TE's of no more than 35 metres.

-Star Configuration: Up to eight SNIC NT devices with physically independent S-buses can be connected in parallel to realize a star configuration. Each branch of the star can be either one of the three basic configurations. Normally the DSTi pins on all NT's are wired together so that the same data is transmitted on all branches of the star. Received data seen on DSTo of each part will reflect data sent by every TE device on every branch. The aggregate data transmission rate remains identical to that of a single bus configuration, as does the D-channel contention mechanism. It is possible for the NT's to transmit different information on each branch of the star by supplying each with a different DSTi stream.

ST-BUS System Serial Interface

The ST-BUS interface is a 2048 kbit/s bidirectional serial port consisting of 32, 8 bit channels per 125 µs frame. The frame pulse defines the frame boundaries, repeating every 125 µs. Each of the 32 channels is 3.9 µs in length with bit periods of 488 ns.

The SNIC transfers PCM/Data transparently between the ST-BUS port (DSTi, DSTo) and the line. The data sent to and received from the ST- BUS port occupies specific channels of the ST-BUS. The D-channel is always passed during channel time 0, followed by the C, B1 and B2 channels in channel times 1, 2, and 3. When Cmode is high, each of the four ST-BUS channels can be separately enabled or disabled through a control register. The DSTo pin is put into a high impedance state during disabled channels. For the DSTi input channels, all 1's are received in disabled B1, B2 and D channels and all 0's in the C-channel when it is disabled. When Cmode is low, all channels are always enabled.

A delayed frame pulse output ($\overline{F0od}$) is generated at the end of the channel time 3. This signal may be connected to the $\overline{F0b}$ inputs of other SNIC's in a daisy chain to perform timeslot assignment without additional circuitry. To facilitate the concatenation of the B1 and B2 channels to implement a 128 kbit/s data stream, the SNIC maintains the temporal association of the B1 and B2 channels on the line.

Microprocessor/Control Interface

The parallel port on the SNIC operates as either a general purpose microprocessor interface or as a hard-wired control port. In microprocessor control mode (Cmode = 1), the interface can act as a Motorola type bus, with Address Strobe, Data Strobe and Read/Write signals active. The Motorola bus mode is selected by keeping DS low on the falling edge of AS. If DS is kept high on the falling edge of AS, then Intel bus mode is selected. In this case, Address Latch Enable, and separate Read and Write inputs are active. Asserting the $\overline{RST}$ input resets the SNIC to Motorola bus mode. When the Cmode pin is low, a controllerless mode is selected and the parallel port reverts to hard-wired control pins. This allows the implementation of a simple NT1 function, without the need for a controlling microprocessor. The SNIC is designed to interface directly with MITEL's MT8972 DNIC, a U-interface device which can be used to complete the NT1 function.

The parallel port on the SNIC controls the HDLC transceiver and can control and monitor all data and C-channel control and status words. A microprocessor can communicate bidirectionally over D, B1, and B2 channels in both ST-BUS or S-interface directions. These operations are completely transparent in that communication defaults to a direct S-interface to ST-BUS connection unless the microprocessor acts on the data once each ST-BUS frame.

Applications

The MT8930 is useful in a wide variety of ISDN applications. As it can be used at both the Network Terminator (NT) and Terminal Equipment (TE) ends of the line, the SNIC finds application on digital subscriber line cards and in digital feature telephone sets. When combined with a U-interface device, such as MITEL's MT8972 (DNIC), the MT8930 can be used to implement an NT1 Network Terminator.

Figure 2 illustrates the use of the SNIC in a voice/data feature telephone set. Also shown is the MT8994, MITEL's single chip digital telephone circuit. These two devices have been designed to connect together implementing a low cost, digital, S-interface telephone set. The MT8994 provides such features as A/D and D/A conversion, handset interface, handsfree operation and tone ringer. PCM encoded voice is passed from the MT8994 to the SNIC via the ST-BUS ports for transmission on one of the B channels. The second B channel is available for transmission of data.

A microcontroller is shown for implementing various features and control functions. Both the MT8930 and MT8994 are controlled and monitored by the microcontroller. Signalling may be performed by scanning the keypad and generating

appropriate messages to be packetized by the HDLC section of the SNIC and transmitted via the D-channel. The microcontroller is responsible for rate converting RS232 data if an R-interface is to be provided by this set. An optional display could be included for additional features such as time/date display and messaging capabilities.

The SNIC can be combined with the MT8972 (DNIC) to implement an NT1 function. This is shown in Figure 3. The controllerless mode of the MT8930 is used to implement a simple NT1, not requiring a microprocessor. The MT8930 is used in NT mode, acting as a master to the S-interface line. The MT8972 operates in slave mode (single port) and derives its timing from the U-interface line originating from the central office. The timing signals from the DNIC are used by the SNIC as well. Communication between the two devices is done via the serial ST-BUS ports.

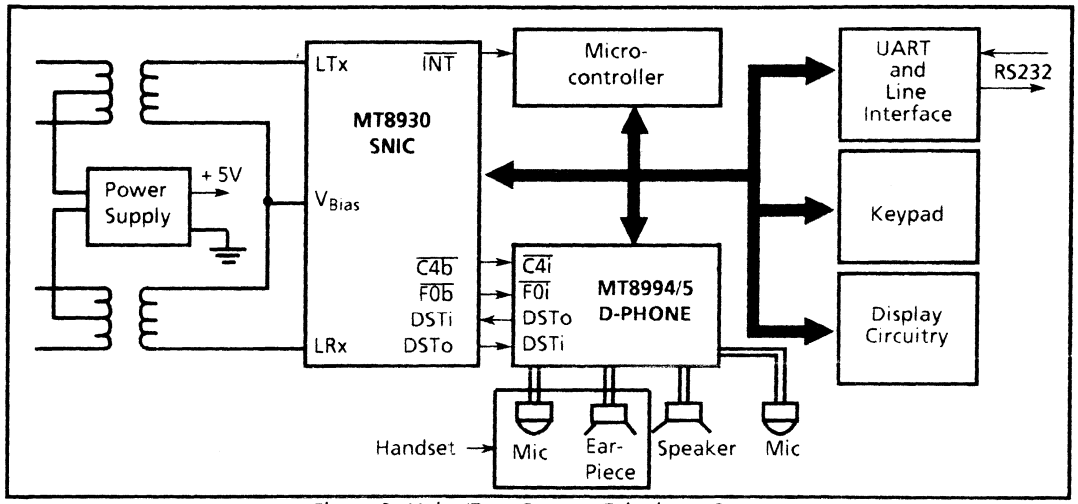


Figure 2 - Voice/Data Feature Telephone Set

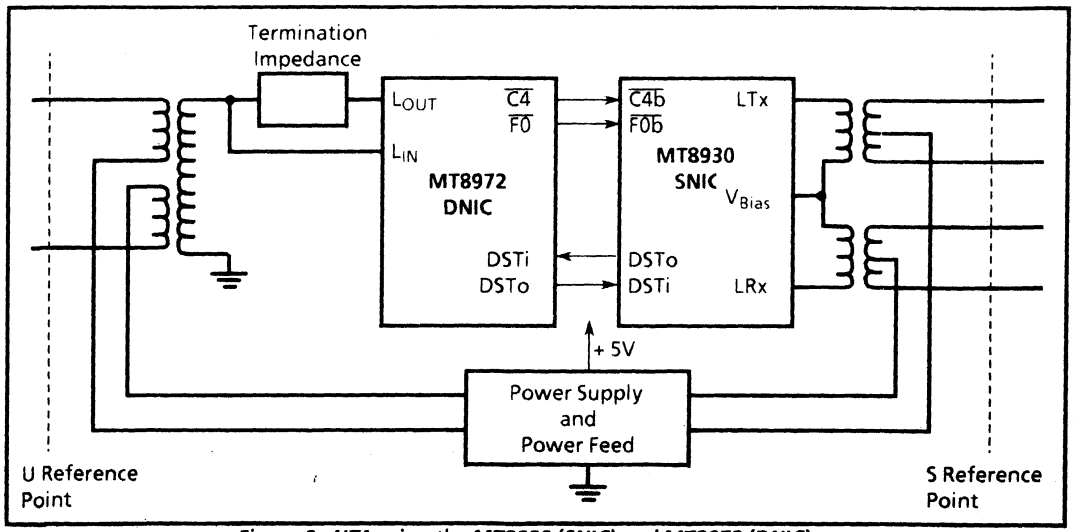


Figure 3 - NT1 using the MT8930 (SNIC) and MT8972 (DNIC)

ISO-CMOS ST-BUS™ FAMILY **MT8940**

T1 / CEPT Digital Trunk PLL

Preliminary Information

9161-002-035-NA ISSUE 2 June 1986

Features

- Provides T1 clock at 1.544 MHz locked to input frame pulse.
- Sources CEPT (30 + 2) Digital Trunk/ST-BUS clock and timing signals locked to internal or external 8 kHz signal.
- TTL compatible logic inputs and outputs.
- Uncommitted 2- input NAND gate.
- Single 5 volt power supply.
- Low power ISO-CMOS™ technology.

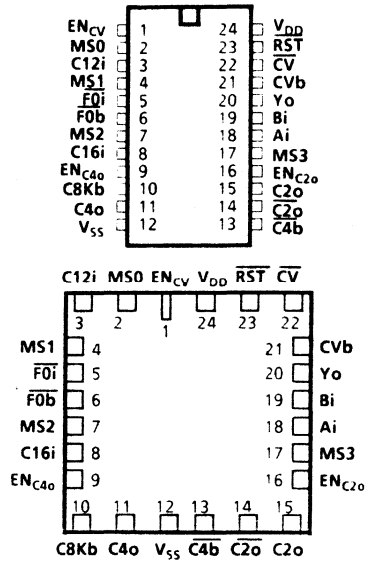
Applications

- Synchronization and timing control for T1 and CEPT digital trunk transmission links.
- ST- BUS clock and frame pulse source.

Description

The MT8940 is a dual digital phase-locked loop providing the timing and synchronization signals for the T1 or CEPT transmission links and the ST-BUS. The first PLL provides the T1 clock (1.544 MHz) synchronized to the input frame pulse at 8 kHz. The timing signals for the CEPT transmission link or the ST-BUS are provided by the second PLL locked to an internal or an external 8 kHz frame pulse signal. The MT8940 is fabricated in MITEL's ISO-CMOS technology.

Pin Connections



Ordering Information

MT8940 AC	24 Pin Ceramic
MT8940 AY	24 Pin LCC

– 40°C to + 85°C

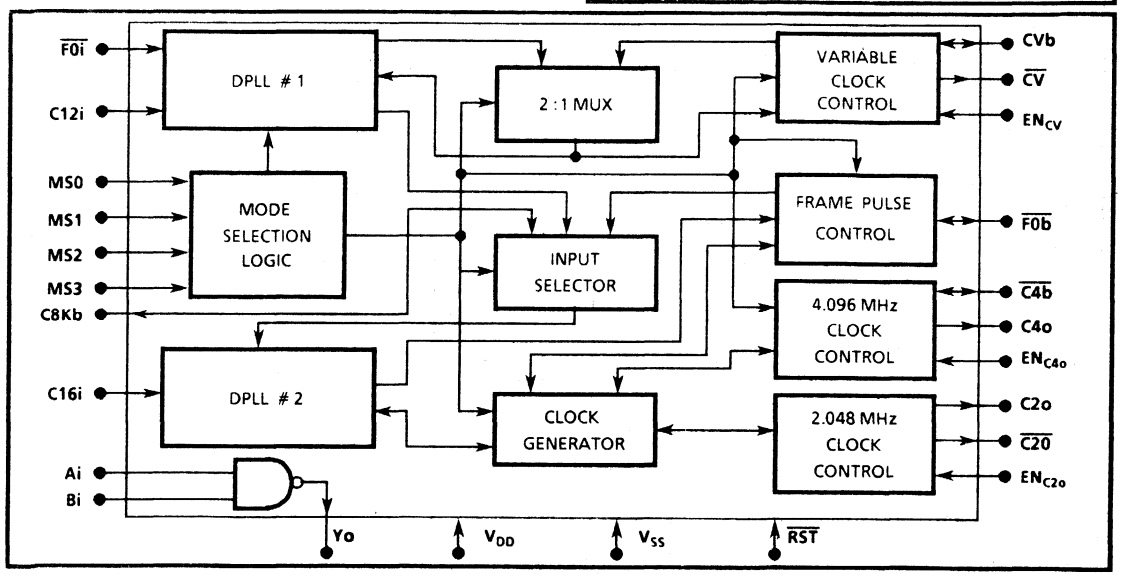


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*- Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD}	-0.3	7.0	V
2	Voltage on any pin		V_I	V_{SS} - 0.5	V_{DD} + 0.5	V
3	Input/Output Diode Current		$I_{IK/OK}$		± 10	mA
4	Output Source or Sink Current		I_O		± 25	mA
5	DC Supply or Ground Current		I_{DD}/I_{SS}		± 50	mA
6	Storage Temperature		T_{ST}	-65	150	°C
7	Package Power Dissipation	Ceramic DIP LCC	P_D P_D		1200 600	mW mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Input HIGH Voltage	V_{IH}	2.4		V_{DD}	V	For 400 mV noise margin
3		Input LOW Voltage	V_{IL}	V_{SS}		0.4	V	For 400 mV noise margin
4		Operating Temperature	T_A	-40	25	85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

V_{DD} = 5.0 V ± 5%; V_{SS} = 0V; T_A = -40 to 85°C. Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Supply current	I_{DD}		8		mA	Under clocked condition, with the inputs tied to the same supply rail as the corresponding pull-up / down resistors.
2	IN	Input HIGH voltage (For all the inputs except pin 23)	V_{IH}	2.0			V	
3	IN	Positive-going threshold voltage (For pin 23)	V_+		2.0		V	
4	IN	Input LOW voltage (For all the inputs except pin 23)	V_{IL}			0.8	V	
5	IN	Negative-going threshold voltage (For pin 23)	V_-		1.6		V	
6	OUT	Output current HIGH (For all the outputs except pin 10)	I_{OH}	-4.6 -14.0	-5.8 -16.8		mA mA	V_{OH} = 4.5 V V_{OH} = 2.4 V
7	OUT	Output current LOW (For all the outputs except pin 10)	I_{OL}	8.9 10.8	11.1 13.4		mA mA	V_{OL} = 0.4 V V_{OL} = 0.5 V
8	OUT	Output current HIGH (pin 10)	I_{OH}		-2.3		mA	Test load circuit 2 (fig. 10) on pin 10 and V_{OH} = 2.4 V
9	OUT	Output current LOW (pin 10)	I_{OL}	4.4	5.5		mA	V_{OL} = 0.4 V
10		Leakage current on bi-directional pins and all inputs except C12i, C16i, $\overline{RST}$	$I_{IZ/OZ}$			± 150	µA	$V_{I/O} = V_{SS}$ or V_{DD}
11		Leakage current on all outputs and C12i, C16i, $\overline{RST}$ inputs	$I_{IZ/OZ}$		± 1	± 10	µA	$V_{I/O} = V_{SS}$ or V_{DD}

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics†

Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figure 2)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DPLL #1	Frame pulse input ($\overline{F0i}$) to CVb output (1.544 MHz) delay.	t_{F15H}	−50		55	ns	
2		CVb output (1.544 MHz) rise time	$t_{r1.5}$		10		ns	Test load circuit 1 (Fig. 10).
3		CVb output (1.544 MHz) fall time	$t_{f1.5}$		12		ns	Test load circuit 1 (Fig. 10).
4		CVb output (1.544 MHz) clock period	t_{P15}		648		ns	
5		CVb output (1.544 MHz) clock width (HIGH)	t_{W15H}		320		ns	
6		CVb output (1.544 MHz) clock width (LOW)	t_{W15L}		306		ns	
7		$\overline{CV}$ delay (HIGH to LOW)	t_{15HL}		5		ns	
8		$\overline{CV}$ delay (LOW to HIGH)	t_{15LH}		−12		ns	

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

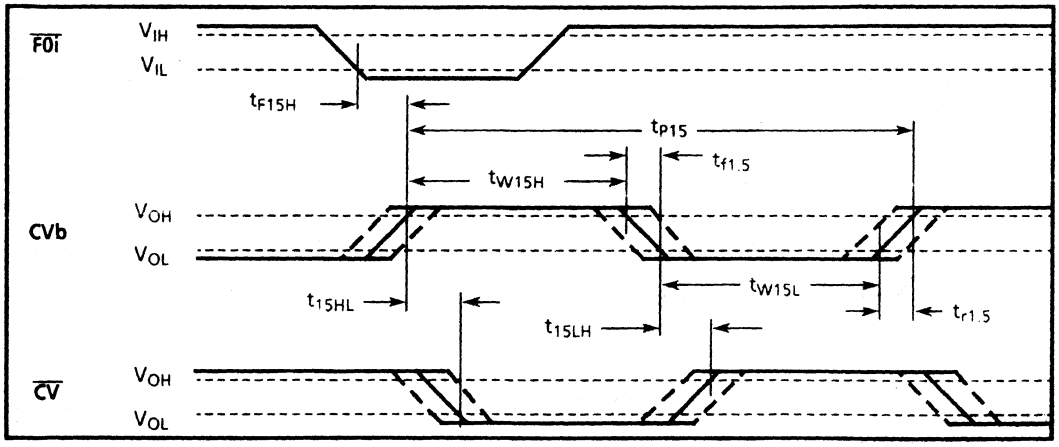


Figure 2. Timing Information for DPLL #1 in NORMAL Mode

AC Electrical Characteristics†

Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figure 3)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DPLL #1	C8Kb output (8 kHz) delay (HIGH to HIGH)	t_{C8HH}		125		ns	Test load circuit 2 (Fig. 10).
2		C8Kb output (8 kHz) delay (LOW to LOW)	t_{C8LL}		50		ns	Test load circuit 2 (Fig. 10).
3		C8Kb output duty cycle			66 50		% %	In Divide -1 Mode In Divide - 2 Mode
4		Inverted clock output delay (HIGH to LOW)	t_{ICHL}		40		ns	
5		Inverted clock output delay (LOW to HIGH)	t_{ICLH}		35		ns	

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

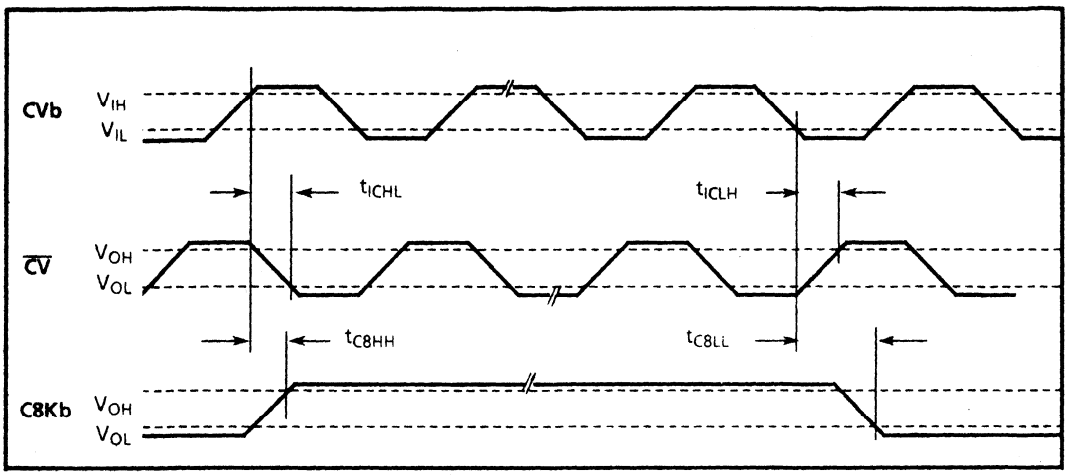


Figure 3. DPLL #1 in DIVIDE Mode

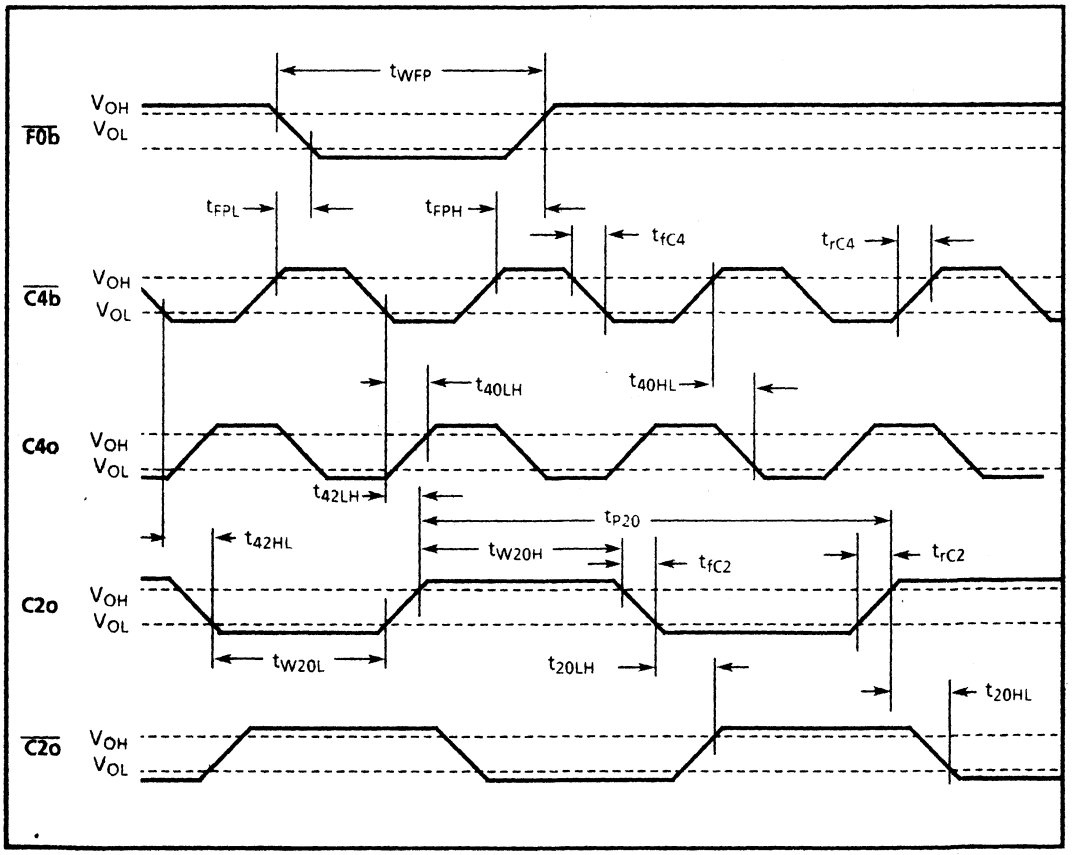


Figure 4. Timing Information on DPLL #2 Outputs

AC Electrical Characteristics † Voltages are with respect to ground (V_{SS}) unless otherwise stated (Ref. Figures 4 and 5)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		$\overline{C4b}$ output delay (HIGH to LOW) from C8Kb input/output	t_{84H}	– 35		40	ns	Test load circuit 2 (Fig. 10) on C8Kb.
2		$\overline{C4b}$ output clock period	t_{P4o}		244		ns	Test load circuit 1 (Fig. 10).
3		$\overline{C4b}$ output clock width (HIGH)	t_{W4oH}		122		ns	
4		$\overline{C4b}$ output clock width (LOW)	t_{W4oL}		107		ns	
5		$\overline{C4b}$ output clock rise time	t_{rC4}		7		ns	Test load circuit 1 (Fig. 10).
6		$\overline{C4b}$ clock output fall time	t_{fC4}		8		ns	Test load circuit 1 (Fig. 10).
7		Frame pulse output delay (HIGH to LOW) from $\overline{C4b}$	t_{FPL}		30		ns	Test load circuit 1 (Fig. 10).
8		Frame pulse output delay (LOW to HIGH) from $\overline{C4b}$	t_{FPH}		25		ns	Test load circuit 1 (Fig. 10).
9	DPLL #2	Frame pulse ($\overline{F0b}$) width	t_{WFP}		244		ns	
10		C4o delay - LOW to HIGH	t_{4oLH}		22		ns	
11		C4o delay - HIGH to LOW	t_{4oHL}		25		ns	
12		$\overline{C4b}$ to C2o delay (LOW to HIGH)	t_{42LH}		– 5		ns	
13		$\overline{C4b}$ to C2o delay (HIGH to LOW)	t_{42HL}		5		ns	
14		C2o clock period	t_{P2o}		488		ns	Test load circuit 1 (Fig. 10).
15		C2o clock width (HIGH)	t_{W2oH}		243		ns	
16		C2o clock width (LOW)	t_{W2oL}		230		ns	
17		C2o clock rise time	t_{rC2}		7		ns	Test load circuit 1 (Fig. 10).
18		C2o clock fall time	t_{fC2}		8		ns	Test load circuit 1 (Fig. 10).
19		$\overline{C2o}$ delay - LOW to HIGH	t_{2oLH}		15		ns	
20		$\overline{C2o}$ delay - HIGH to LOW	t_{2oHL}		5		ns	

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

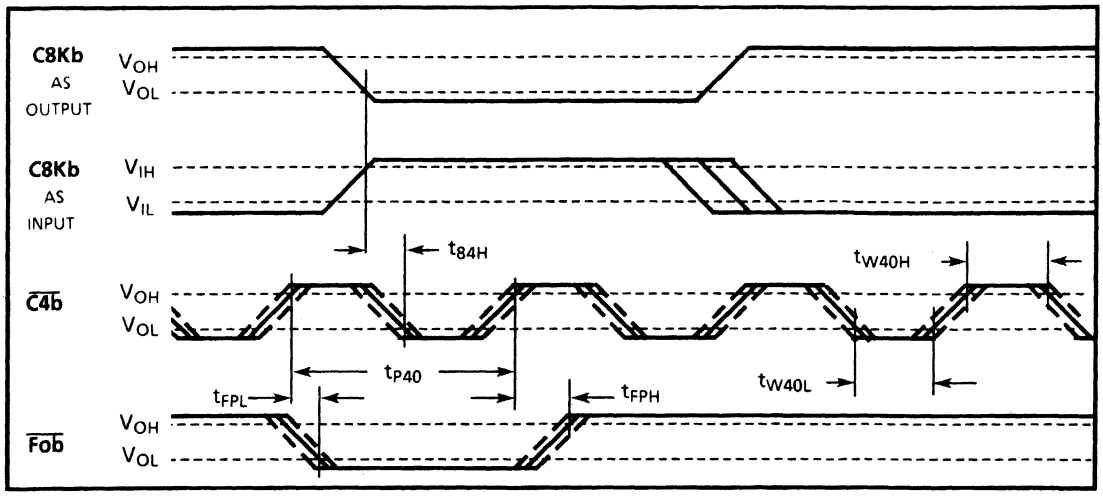


Figure 5. ST-BUS Timings from DPLL #2 and C8Kb Input/Output

AC Electrical Characteristics†

Voltages are with respect to ground (V_{SS}) unless otherwise stated **(Ref. Figure 6)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		$\overline{CV}$/CVb(1.544 MHz) Set-up time	t_{S15}		25		ns	
2		$\overline{CV}$/CVb(1.544 MHz) Hold time	t_{H15}		110		ns	

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

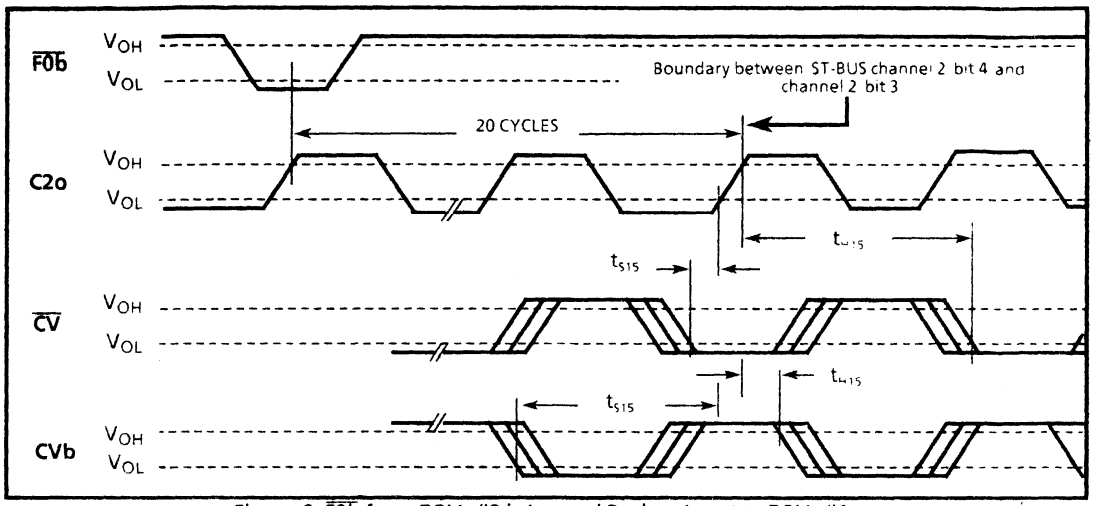


Figure 6. $\overline{F0b}$ from DPLL #2 is Looped Back as Input to DPLL #1 (T1 Line synchronized to ST-BUS)

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated **(Ref. Figure 7)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CLOCKS	Master clocks input rise time	t_r			10	ns	
2		Master clocks input fall time	t_f			10	ns	
3		Master clock period (12.355MHz)	t_{P12}	80.930	80.938	80.946	ns	For DPLL #1, while operating to provide the T1 clock signal.
4		Master clock period (16.388MHz)	t_{P16}	61.018	61.020	61.022	ns	For DPLL #2, while operating to provide the CEPT and ST-BUS timing signals.
5		Duty Cycle of master clocks		45	50	55	%	
6		Lock-in Range (For each PLL)			± 1.04		Hz	With the Master clocks as shown above.

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

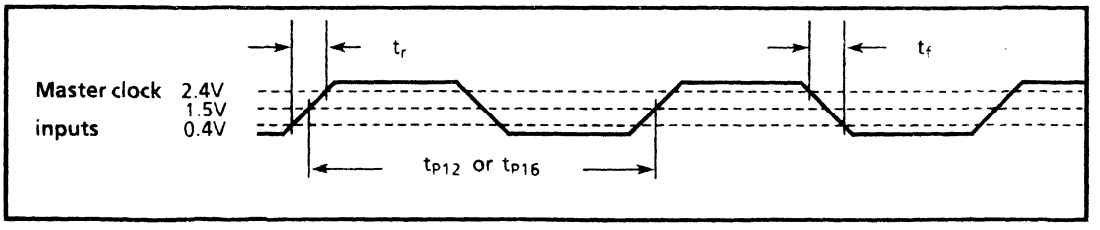


Figure 7. Master Clock Inputs

AC Electrical Characteristics[†] Voltages are with respect to ground (V_{SS}) unless otherwise stated (Ref. Figure 8.)

		Characteristics	Sym	Min	Typ[‡]	Max	Units	Test Conditions
1		$\overline{F0b}$ input pulse width (LOW)	t_{WFP}		244	300	ns	
2		$\overline{C4b}$ input clock period	t_{P4o}		244		ns	
3		Frame pulse ($\overline{F0b}$) set-up time	t_{FS}	50			ns	
4		Frame pulse ($\overline{F0b}$) hold time	t_{FH}	50			ns	

[†] Timing is over recommended temperature & power supply voltages

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

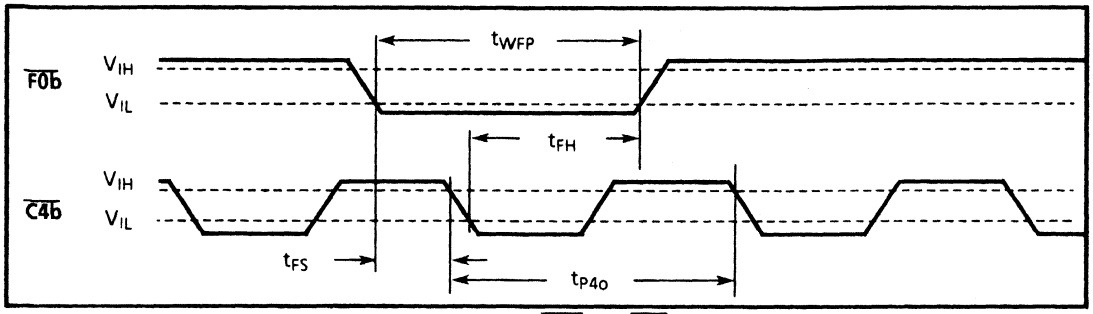


Figure 8. External Inputs on $\overline{C4b}$ and $\overline{F0b}$ for the DPLL #2

AC Electrical Characteristics[†] Voltages are with respect to ground (V_{SS}) unless otherwise stated (Ref. Figure 9)

		Characteristics	Sym	Min	Typ[‡]	Max	Units	Test Conditions
1	OUTPUT	Delay from Enable to Output (HIGH to THREE STATE)	t_{PHZ}		15		ns	Test load circuit 3 (Fig.10).
2	OUTPUT	Delay from Enable to Output (LOW to THREE STATE)	t_{PLZ}		10		ns	Test load circuit 3 (Fig.10).
3	OUTPUT	Delay from Enable to Output (THREE STATE to HIGH)	t_{PZH}		16		ns	Test load circuit 3 (Fig.10).
4	OUTPUT	Delay from Enable to Output (THREE STATE to LOW)	t_{PZL}		38		ns	Test load circuit 3 (Fig.10).

[†] Timing is over recommended temperature & power supply voltages

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

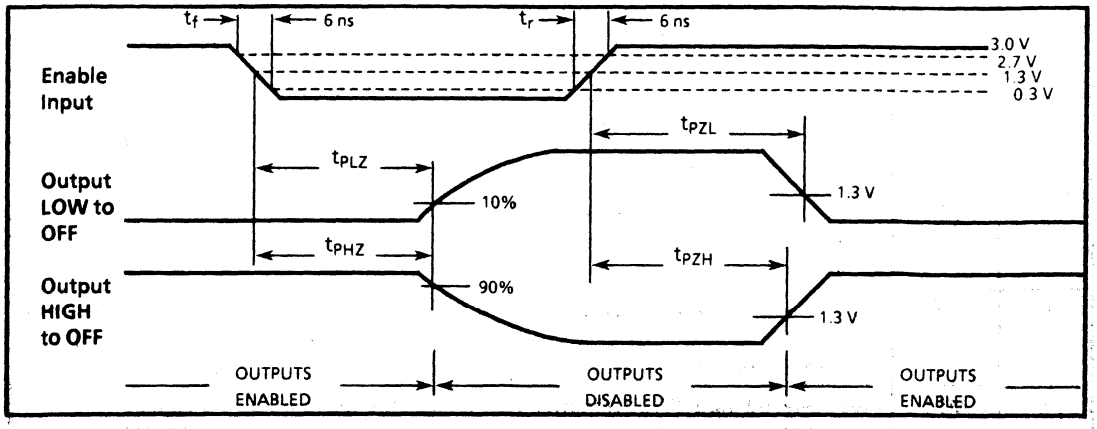


Figure 9. Three State Outputs and Enable Timings

AC Electrical Characteristics† - Uncommitted NAND Gate

Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Propagation delay (LOW to HIGH), input Ai or Bi to output	t_{PLH}		25		ns	Test load circuit 1 (Fig. 10).
2		Propagation delay (HIGH to LOW), input Ai or Bi to output	t_{PHL}		20		ns	Test load circuit 1 (Fig. 10).

† Timing is over recommended temperature & Power Supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

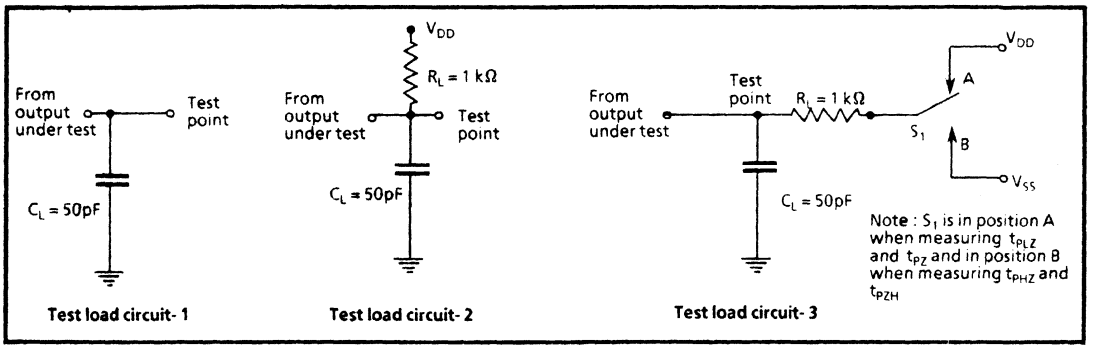


Figure 10. Test Load Circuits

TABLE 1.
Pin Description

Pin No.	Name	Description
1	EN_{CV}	**Variable clock enable (TTL compatible input)** - This input (pulled internally to V_{DD}) directly controls the three states of $\overline{CV}$ (pin 22) under all modes of operation. When HIGH, enables $\overline{CV}$ and when LOW, puts it in high impedance condition. It also controls the three states of CVb signal (pin 21) if MS1 is LOW. When EN_{CV} is HIGH, the pin CVb is an output and when LOW, it is in high impedance state. However, if MS1 is HIGH, CVb is always an input.
2	MS0	**Mode select '0' input (TTL compatible)** - This input (pulled internally to V_{SS}) in conjunction with MS1 (pin 4) selects the major mode of operation for both DPLLs. (Refer to Tables 2 and 3)
3	C12i	**Clock 12.355 MHz input (TTL compatible)** - Master clock input at 12.355 MHz ± 100ppm for DPLL #1.
4	MS1	**Mode select-1 input (TTL compatible)** - This input (pulled internally to V_{SS}) in conjunction with MS0 (pin 2) selects the major mode of operation for both DPLL's. (Refer to Tables 2 and 3)
5	$\overline{F0i}$	**Frame pulse input (TTL Compatible)** - This is the frame pulse input (pulled internally to V_{DD}) at 8 kHz. The DPLL #1 locks on to the falling edge of this input to generate T1 (1.544 MHz) clock.
6	$\overline{F0b}$	**Frame pulse Bi-directional (TTL Compatible input and Totem-pole output)** - Depending on the minor mode selected for the DPLL #2, it provides the 8 kHz frame pulse output or acts as an input (pulled internally to V_{DD}) to an external frame pulse.
7	MS2	**Mode select-2 input (TTL compatible)** - This input (pulled internally to V_{DD}) in conjunction with MS3 (pin 17) selects the minor mode of operation for the DPLL #2. (Refer to Table 4)

TABLE 1. (Continued)
Pin Description

Pin No.	Name	Description
8	C16i	**Clock 16.388 MHz input (TTL compatible)** - Master clock input at 16.388 MHz ± 32 ppm for DPLL #2.
9	EN_{C4o}	**Enable 4.096 MHz clock (TTL compatible input)** - This active high input (pulled internally to V_{DD}) enables C4o (pin 11) output. When LOW, the output C4o is in high impedance condition.
10	C8Kb	**Clock 8 kHz- Bi-directional (TTL compatible input and open drain output with 100K internal resistor to V_{DD})** - This is the 8 kHz input signal on the rising edge of which the DPLL #2 locks during its NORMAL mode. When DPLL #2 is in SINGLE CLOCK mode, this pin outputs the 8 kHz internal signal provided by the DPLL #1 to DPLL #2.
11	C4o	**Clock 4.096 MHz (Three state output)** - This is the inverse of the signal appearing on pin 13 ($\overline{C4b}$) at 4.096 MHz and has a rising edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C4o} (pin 9).
12	V_{SS}	**Ground (0 Volt)**
13	$\overline{C4b}$	**Clock 4.096 MHz- Bi-directional (TTL compatible input and Totem-pole output)** - When the mode select bit MS3 (pin 17) is HIGH, it provides the 4.096 MHz clock output with the falling edge in the frame pulse ($\overline{F0b}$) window. When pin 17 is LOW, $\overline{C4b}$ is an input (pulled internally to V_{DD}) to an external clock at 4.096 MHz.
14	$\overline{C2o}$	**Clock 2.048 MHz (Three state output)** - This is the divide by two output of $\overline{C4b}$ (pin 13) and has a falling edge in the frame pulse($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C2o} (pin 16).
15	C2o	**Clock 2.048 MHz (Three state output)** - This is the divide by two output of $\overline{C4b}$ (pin 13) and has a rising edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C2o} (pin 16).
16	EN_{C2o}	**Enable 2.048 MHz clock (TTL compatible input)** - This active high input (pulled internally to V_{DD}) enables both $\overline{C2o}$ and C2o outputs (pins 14 and 15). When LOW, these outputs are in high impedance condition.
17	MS3	**Mode select 3 input (TTL compatible)** - This input (pulled internally to V_{DD}) in conjunction with MS2 (pin 7) selects the minor mode of operation for the DPLL #2. (Refer to Table 4)
18,19	Ai, Bi	**Inputs A and B (TTL compatible)** -These are the two inputs (pulled internally to V_{SS}) to the uncommitted NAND gate.
20	Yo	**Output Y (Totem pole output)** - Output of the uncommitted NAND gate.
21	CVb	**Variable clock Bi-directional (TTL compatible input and Totem-pole output)** - When acting as an output (MS1-LOW) during the NORMAL mode of DPLL #1, this pin provides the 1.544 MHz clock locked to the input frame pulse $\overline{F0i}$ (pin 5). When MS1 is HIGH, it is an input (pulled internally to V_{DD}) to an external clock at 1.544 MHz or 2.048 MHz to provide the internal signal at 8 kHz to DPLL #2.
22	$\overline{CV}$	**Variable clock (Three state output)**- This is the inverse output of the signal appearing on pin 21, the high impedance state of which is controlled EN_{CV}(pin 1).
23	$\overline{RST}$	**Reset (Schmitt trigger input)**-This input (active LOW) evokes reset condition for the device.
24	V_{DD}	**V_{DD} (+ 5V)** Power supply.

Functional Description

The MT8940 is a dual digital phase-locked loop providing the timing and synchronization signals to the interface circuits for T1 or CEPT (30 + 2) Primary Multiplex Digital Transmission links. As shown in Figure 1, it has two digital phase-locked loops (DPLLs), associated output controls and the mode selection logic circuits. The two DPLLs, although similar in principle, operate independently to provide T1 (1.544 MHz) or CEPT (2.048 MHz) transmission clocks and ST-BUS timing signals.

The principle of operation behind the two DPLLs is shown in Figure 11. A master clock is divided down to 8 kHz where it is compared with the 8 kHz input, and depending on the output of the phase comparison, the master clock frequency is corrected. The MT8940 achieves the frequency correction in both directions by using the master clock at a slightly higher frequency and dividing it unaltered or stretching its period (at two dicrete instants in a frame) before the division depending on the phase comparison output. When the input

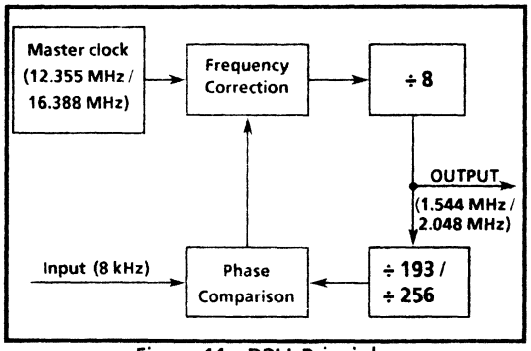


Figure 11. DPLL Principle

frequency is higher, the unchanged master clock is divided, thus effectively speeding-up the locally generated clock and eventually pulling it in synchronization with the input. If the input frequency is lower than the local replica, the period of the master clock is stretched by half a cycle, at two discrete instants in a phase sampling period, thereby introducing a total delay of one master clock period over the sampling duration, and then dividing it to generate the local signal which will subsequently be in synchronization with the input. Once the output is phase-locked to the active edge of the input, the circuit will maintain the locked condition as long as the input frequency is within the lock-in range (± 1.04 Hz) of the DPLLs. The lock-in range is wide enough to meet the CCITT line rate specification (1.544 MHz ± 130ppm and 2.048 MHz ± 50ppm) for the High Capacity Terrestrial Digital Service.

The phase sampling is done once in a frame (8 kHz) and the divisions are set at 8 and 193 for the DPLL #1, which locks on to the falling edge of the input at 8 kHz to generate T1 (1.544 MHz) clock. Although the phase sampling duration is same for the DPLL #2, the divisions are set at 8 and 256 to provide the CEPT/ST-BUS clock at 2.048 MHz synchronized to the rising edge of the input signal (8 kHz). The master clock source is specified to be at 12.355 MHz ± 100 ppm for the DPLL #1 and 16.388 MHz ± 32 ppm for the DPLL #2 over the entire temperature range of operation.

The two DPLLs operate independently depending on the mode selection bits MS0 to MS3. The mode selection logic circuits are common to both the PLLs and control their operation. All the outputs are individually controlled to the high impedance condition by their respective enable controls. The uncommitted NAND gate is available for use in applications involving MITEL's MT8975/MH89750 (T1 interfaces) and MT8978/MH89780 (CEPT interfaces).

Modes of operation

The operation of the MT8940 is categorized into two types; the major modes and the minor modes. The major modes are defined for both DPLLs by the mode select pins MS0 and MS1. The minor modes are selected by the other two mode select pins MS2 and MS3 and applicable only to the DPLL #2. There are no minor modes for the DPLL #1.

Major modes of the DPLL #1

DPLL #1 can be operated in three major modes as selected by MS0 and MS1(Table 2). When MS1 is LOW, the DPLL is in NORMAL mode providing the T1 (1.544 MHz) clock signal locked to the falling edge of the input frame pulse F0i (8 kHz), the necessary master clock input being at 12.355 MHz ± 100 ppm (C12i). In second and third major modes (MS1 is HIGH), the DPLL #1 is set to DIVIDE an external 1.544 MHz or 2.048 MHz signal applied at CVb (pin 21). The division can be set by MS0 to be either at 193 (LOW) or 256 (HIGH). During these modes, the divided output at 8 kHz is connected internally to the DPLL #2 which operates in SINGLE CLOCK mode and also made available on C8Kb (pin 10) for any external use.

Major modes of the DPLL #2

There are four major modes for the DPLL #2 selectable by MS0 and MS1, as shown in Table 3. In all these modes the DPLL #2 provides either the

CEPT Primary Multiplex timing or the ST-BUS clock and framing signals.

MS0	MS1	Mode of operation	Function
X	0	NORMAL	Provides the T1 (1.544 MHz) clock synchronized to the falling edge of the input frame pulse ($\overline{F0i}$)
0	1	DIVIDE-1	DPLL #1 divides the CVb input, the division being at 193. The divided output is connected to DPLL #2.
1	1	DIVIDE-2	DPLL #1 divides the CVb input, the division being at 256. The divided output is connected to DPLL #2.

Note: X: Don't care

Table 2. Major Modes of the DPLL #1

In NORMAL mode, the DPLL #2 provides the CEPT/ST-BUS compatible timing signals locked to the rising edge of the 8 kHz input signal (C8Kb). The 4.096 MHZ (C4o and $\overline{C4b}$) & 2.048 MHz (C2o and $\overline{C2o}$) clocks and 8 kHz frame pulse ($\overline{F0b}$) derived from the 16.388 MHz ±32ppm master clock are provided as the outputs. This mode can also provide the ST-BUS timing and framing signals with the input (C8Kb) tied HIGH and the master clock set at 16.384 MHz. The DPLL makes no correction in this case however, and provides the timing signals compatible to the ST-BUS format without any jitter.

In FREE-RUN mode, the DPLL #2 generates the stand-alone ST-BUS timing and framing signals as in the NORMAL mode with no external inputs except the master clock set at 16.388 MHz ± 32 ppm. Since the master clock source is set at a higher frequency than the nominal value, the DPLL makes the necessary corrections so as to deliver the averaged timing signals compatible to the ST-BUS format.

The operation of DPLL #2 in SINGLE CLOCK-1 and 2 modes are identical functionally, providing the CEPT/ST-BUS compatible timing signals synchronized to the internal 8 kHz signal obtained from DPLL#1 in DIVIDE mode. When SINGLE CLOCK-1 mode is selected for DPLL #2, it automatically selects the DIVIDE-1 mode for DPLL #1 and thus an external 1.544 MHz clock signal applied at CVb (pin 21) is divided by the DPLL #1 to generate the internal signal at 8 kHz which the DPLL #2 locks on to. Similarly when SINGLE CLOCK-2 mode is selected, the DPLL #1 is set to DIVIDE-2 mode, with an external signal at 2.048 MHz providing the internal 8 kHz signal to the DPLL #2. In both these modes, the internal signal is made available on C8Kb (pin 10) for any external use and the DPLL #2 locks on to the falling edge of this internal signal to provide the CEPT/ST-BUS compatible timing signals. This is in contrast to the Normal mode where these timing signals are

MS0	MS1	Mode of operation	Function
0	0	NORMAL	Provides the ST-BUS /CEPT compatible timing signals locked to the rising edge of the 8kHz input signal at C8Kb
1	0	FREE-RUN	Provides the ST-BUS compatible timing and framing signals with no external inputs, except the master clock.
0	1	SINGLE CLOCK-1	Provides the CEPT/ST-BUS compatible timing signals locked to the falling edge of the 8kHz internal signal provided by DPLL #1.
1	1	SINGLE CLOCK-2	Provides the CEPT/ST-BUS compatible timing signals locked to the falling edge of the 8kHz internal signal provided by DPLL #1

Table 3. Major Modes of the DPLL #2

synchronized with the rising edge of the 8 kHz signal on C8Kb.

Minor modes of the DPLL #2

The minor modes for DPLL #2 depend on the status of the mode select bits MS2 and MS3 (pins 7 and 17).
When MS3 is HIGH, the DPLL #2 operates in any of the major modes as selected by MS0 and MS1.

When MS3 is LOW, it overrides the major mode selected and accepts an external clock at 4.096 MHz on $\overline{C4b}$ (pin 13) to provide 2.048 MHz clocks (C2o and $\overline{C2o}$) and 8 kHz frame pulse ($\overline{F0b}$) compatible with the ST-BUS format.

The mode select bit MS2, controls the direction of the signal on $\overline{F0b}$ (pin 6). When MS2 is LOW, the pin $\overline{F0b}$ acts as an input to an external frame pulse at 8 kHz. But this input is effective only if MS3 is also LOW and pin $\overline{C4b}$ is accepting a 4.096 MHz external clock which has a proper phase relation with the external input on $\overline{F0b}$ (Refer Figure 8). Otherwise the input on pin $\overline{F0b}$ will have no bearing on the operation of the DPLL #2, unless it is in FREE-RUN mode as selected by MS0 and MS1. While in FREE-RUN mode, the input on $\overline{F0b}$ is treated the same way as C8Kb input in NORMAL mode, but the frequency of the input on $\overline{F0b}$ should be 16 kHz for the DPLL #2 to lock on to provide the ST-BUS compatible clocks at 4.096 MHz and 2.048 MHz.

When MS2 is HIGH, the pin $\overline{F0b}$ provides the frame pulse output compatible with the ST-BUS format locked on to the internal or external input signal as decided by the other mode select pins MS0, MS1 and MS3.

Table 5 summarizes all the modes the two DPLLs can operate depending on the combination of the four mode select bits. It should be noted however, that each of the major mode selected for the DPLL #2 can have any of the minor modes, although some of the combinations are functionally similar as shown in the Table. But the operation of the DPLL #1 under these conditions are different and hence the status of the mode select bits must be fixed taking into account the required mode of operation for the two DPLLs independently.

MS2	MS3	Functional Description
1	1	Provides the ST-BUS compatible 4.096 MHz and 2.048 MHz clocks and 8kHz frame pulse depending on the major mode selected
0	1	Provides the ST-BUS compatible 4.096 MHz & 2.048 MHz clocks depending on the major mode selected while $\overline{F0b}$ acts as an input. However, the input on $\overline{F0b}$ has no effect on the operation of DPLL #2 unless it is in FREE-RUN mode.
0	0	Overrides the major mode selected and accepts properly phase related external 4.096 MHz clock and 8 kHz frame pulse to provide the ST-BUS compatible clock at 2 048MHz.
1	0	Overrides the major mode selected and accepts an external clock at 4.096 MHz to provide the ST-BUS clock and frame pulse at 2.048 MHz and 8 kHz respectively.

Table 4. Minor Modes of the DPLL #2

MODE #	MS 0	MS 1	MS 2	MS 3	Operating Modes	
					DPLL #1	DPLL #2
0	0	0	0	0	Normal Mode	Properly phase related External 4.096 MHz clock and 8 KHz frame pulse provide the ST-BUS clock at 2.048 MHz.
1	0	0	0	1	Normal Mode	Normal mode (Although $\overline{F0b}$ is an input, it has no effect on the operation).
2	0	0	1	0	Normal Mode	External 4.096 MHz provides the ST-BUS clock and Frame Pulse at 2.048 MHz and 8 kHz respectively.
3	0	0	1	1	Normal Mode: Provides the T1 (1.544 MHz) clock synchronized to the falling edge of the input frame pulse ($\overline{F0i}$).	Normal mode: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz input signal (C8Kb).
4	0	1	0	0	Divide-1 Mode	Same as mode '0'.
5	0	1	0	1	Divide-1 Mode	Single clock-1 mode (Although $\overline{F0b}$ is an input, it has no effect on the operation).
6	0	1	1	0	Divide-1 Mode	Same as mode 2.
7	0	1	1	1	Divide-1 Mode : Divides the CVb input, the division being set at 193. The divided output is connected to the DPLL #2.	Single clock-1 mode: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz internal signal provided by the DPLL #1.
8	1	0	0	0	Normal Mode	Same as mode '0'.
9	1	0	0	1	Normal Mode	$\overline{F0b}$ is an input and DPLL #2 locks on to it only if it is at 16 kHz to provide the ST-BUS control signals.
10	1	0	1	0	Normal Mode	Same as mode 2.
11	1	0	1	1	Normal Mode Provides the T1 (1.544 MHz) clock synchronized to the falling edge of the input frame pulse ($\overline{F0i}$).	Free-Run mode: Provides the ST-BUS timing signals with no external inputs except the master clock.
12	1	1	0	0	Divide-2 Mode	Same as mode '0'.
13	1	1	0	1	Divide-2 Mode	Single clock-2 mode (Although $\overline{F0b}$ is an input, it has no effect on the operation.)
14	1	1	1	0	Divide-2 Mode	Same as mode 2.
15	1	1	1	1	Divide-2 Mode: Divides the CVb input, the division being set at 256. The divided output is connected to the DPLL#2.	Single clock-2 mode: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz internal signal provided by the DPLL #1.

Table 5. Summary of Modes of Operation - DPLL #1 and #2

Applications

A minimum component count approach to provide the timing and synchronization signals to the interface circuits between T1 or CEPT primary multiplex digital link and the ST-BUS is to use the MT8940 as described below. The hardware selectable modes and the independent control over the PLLs add flexibility to the interface circuits built around it. It can reconfigure easily to provide the timing and control signals both at the master and slave ends of the link.

Synchronization and Timing Signals for the T1 Transmission Link

An example of providing the timing signals to MITEL's T1 Interface Hybrid (MH89750) at the master and slave ends of the T1 transmission link is shown in Figures 12 and 13.

At the master end of the link, the DPLL #2 is the source of the ST-BUS signals derived from the 4.096 MHz system clock. The frame pulse output is looped back to the DPLL #1 (in NORMAL mode) which locks on to it to generate the T1 line clock. The timing relation between the 1.544 MHz T1 clock and the 2.048 MHz ST-BUS clock is shown in Figure 6 and meets the requirement of the interface Hybrid. (Ref: MH89750 Data Sheet).
The crystal clock at 12.355 MHz is used by the DPLL #1 to generate the 1.544 MHz clock while DPLL #2 uses the 4.096 MHz system clock to provide the ST-BUS timing signals. The ST-BUS signals can also be obtained from the DPLL #2 in FREE-RUN mode, using a crystal clock at 16.388 MHz instead of 4.096 MHz system clock. The uncommitted NAND gate converts the received signals, RxA and RxB to 'Return to Zero' (RZ) format for the clock extraction circuits in the hybrid. The generated ST-BUS signals can be used to synchronize the system and the switching equipment at the master end.

At the slave end of the link (Figure 13) both the DPLLs are in NORMAL mode with the DPLL #2 providing the ST-BUS timing signals locked to the 8 kHz frame pulse (E8Ko) extracted from the received signal on the T1 line The regenerated frame pulse is looped back to the DPLL #1 to provide the T1 line clock as at the master end.

The 12.355 MHz and 16.388 MHz crystal clock sources are necessary for the DPLL #1 and #2 respectively. The uncommitted NAND gate regenerates the received signal in RZ format as at the master end.

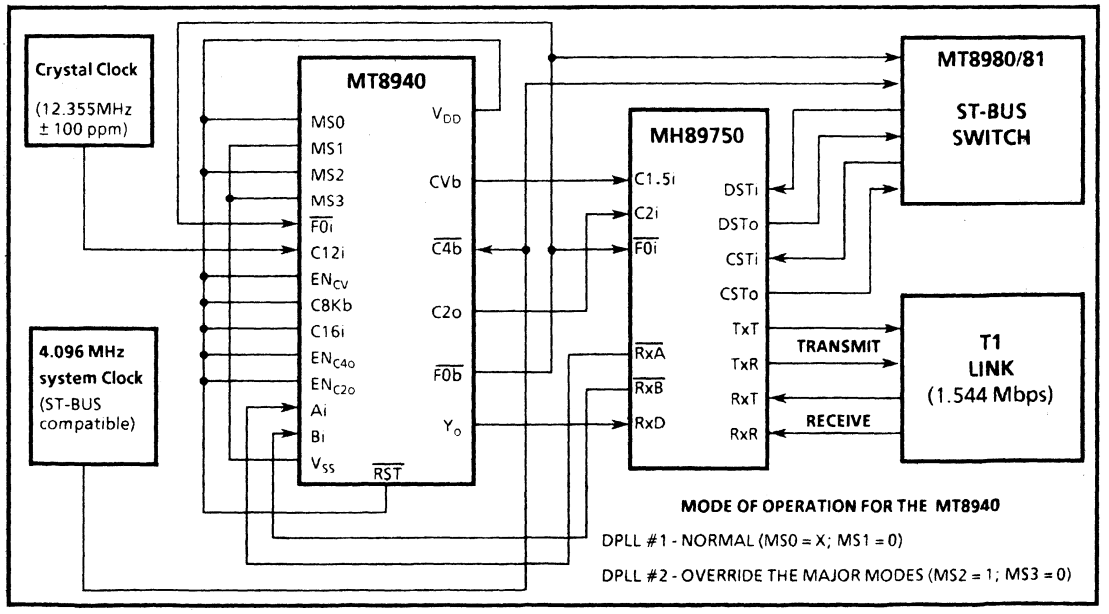


Figure 12. Synchronization at the Master End of the T1 Transmission Link

Synchronization and Timing Signals for the CEPT Transmission Link

The MT8940 can be used to provide the timing and synchronization signals to the MH89780, MITEL's CEPT(30 + 2) digital trunk interface hybrid. Since the operational frequencies of the ST-BUS and the CEPT primary multiplex digital trunk are same, only the DPLL #2 is required to achieve the synchronism between the two.

Figures 14 and 15 show how the MT8940 can be used to synchronize the ST-BUS to the CEPT transmission link at the master and slave ends respectively.

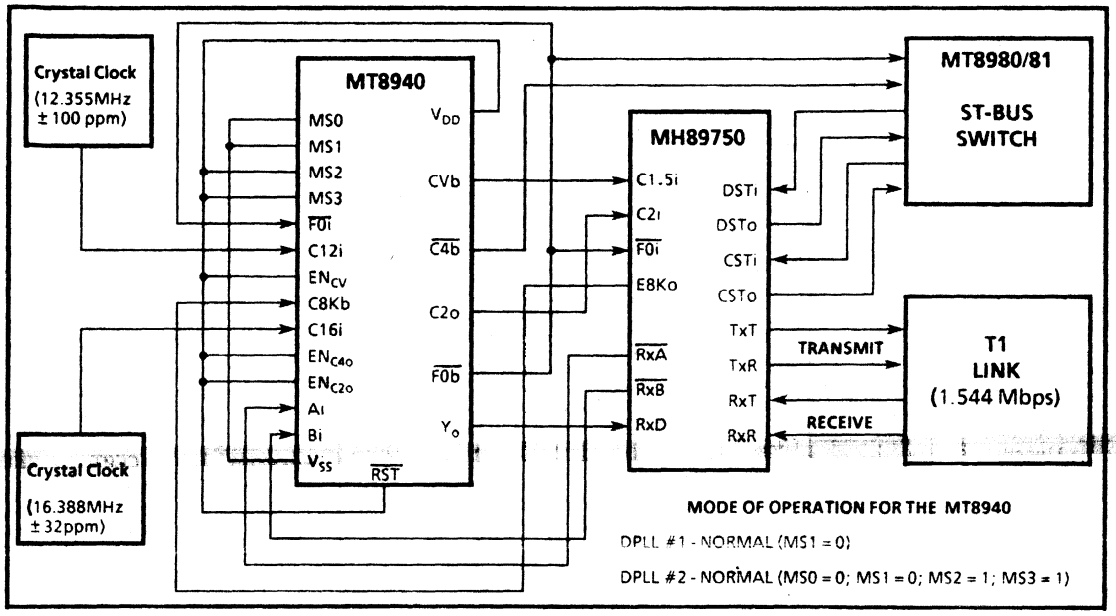


Figure 13. Synchronization at the Slave End of the T1 Transmission Link

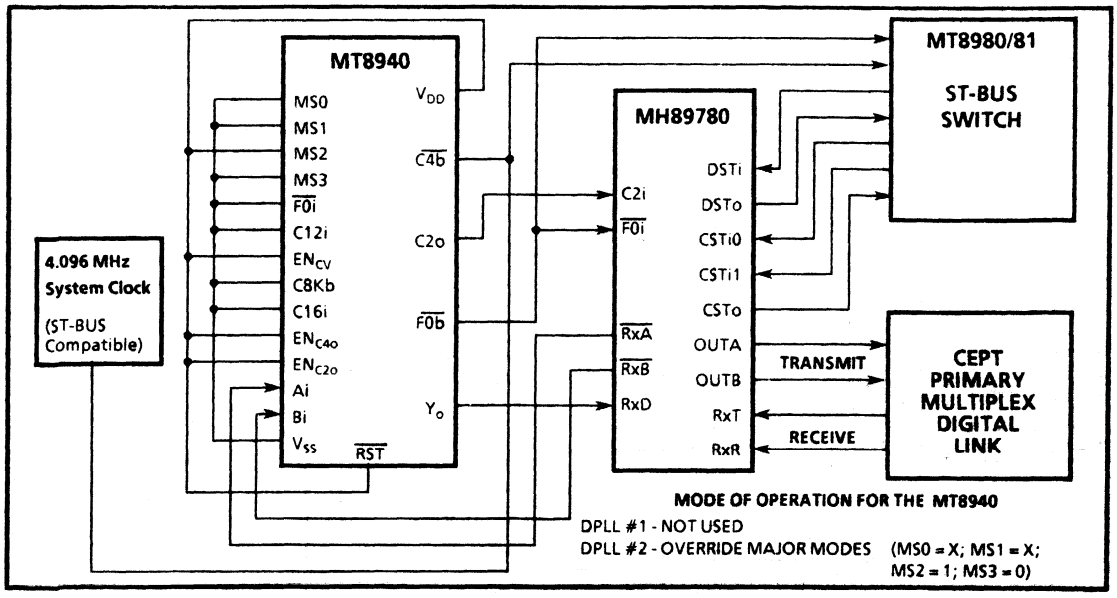


Figure 14. Synchronization at the Master End of the CEPT Digital Transmission Link

Generation of ST-BUS Timing Signals

The MT8940 can source the properly formatted ST-BUS timing and control signals with no external inputs except the crystal clock. This can be used as the standard source in ST-BUS systems and while developing and testing the ST-BUS family components or any other system with similar clock requirements.

The Figure 16 shows two such applications using only the DPLL #2. In one case, it is in FREE-RUN mode with the crystal clock at 16.388 MHz and makes the necessary correction once in two frames (each frame = 125µs) to maintain the frequency standard of the ST-BUS, resulting in jitter on the output. In the other case, the master clock is set at 16.384 MHz (exactly eight times the output frequency) and the DPLL #2 operates in NORMAL mode with C8Kb input tied HIGH. Since it does not require any correction in this case, the output is free from jitter. The DPLL #1 is completely free in both cases and available for any other purpose.

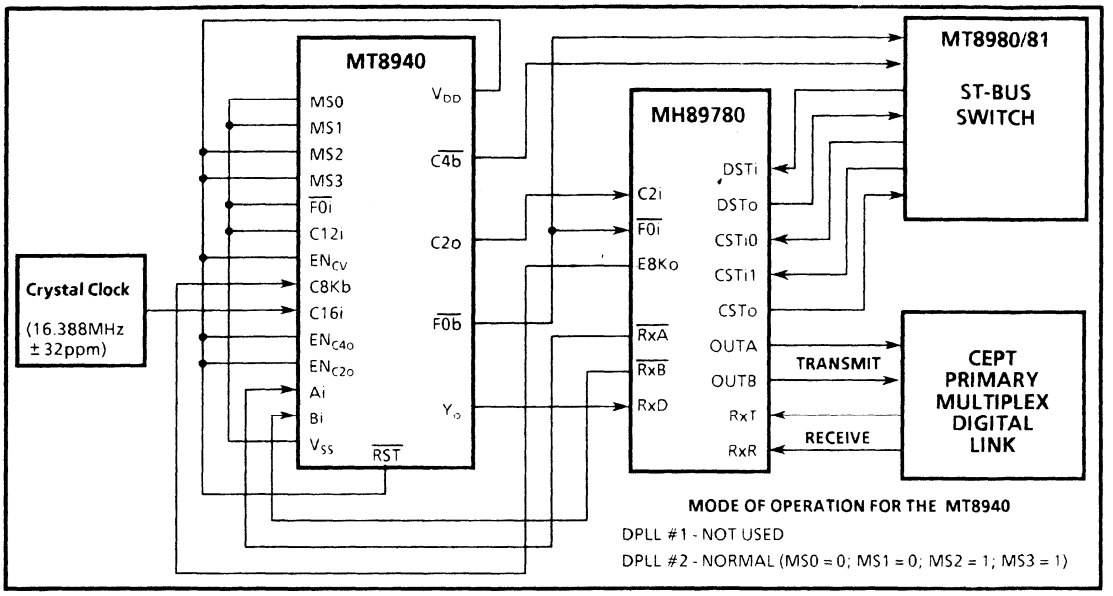


Figure 15. Synchronization at the Slave End of the CEPT Digital Transmission Link

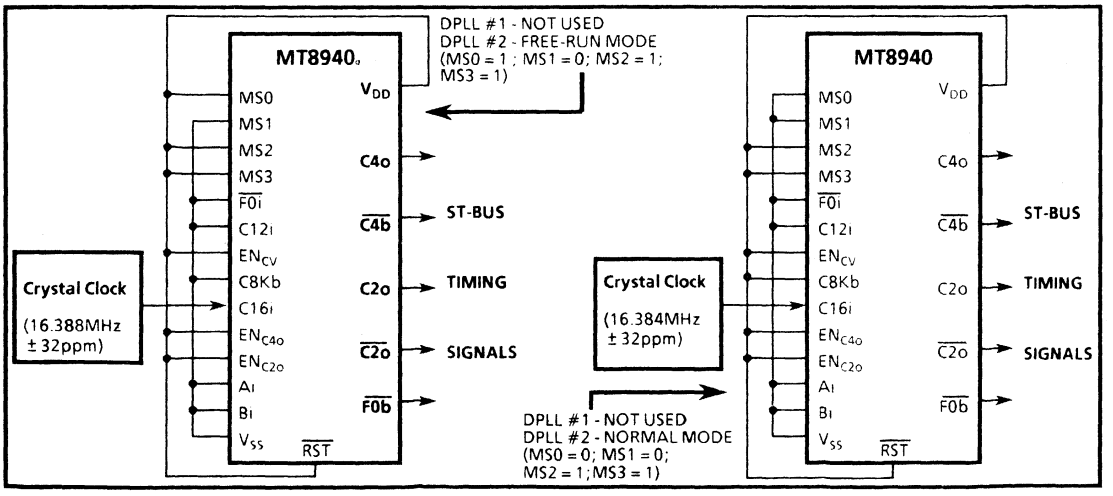


Figure 16. Generation of the ST-BUS Timing Signals

9161-002-048 NA ISSUE 3 AUGUST 1986

Features

- Transparent coding and decoding of 0 to 8, 9.6 and 19.2 Kbps data.
- Coding compatible to PCM voice channels at 56/ 64 Kbps in ST-BUS format.
- Automatic line polarity detection and correction.
- Loopback facility for test purposes.
- Selectable data formats: RZ or NRZ.
- Eight user selectable modes of operation.
- Low power ISO-CMOS technology.

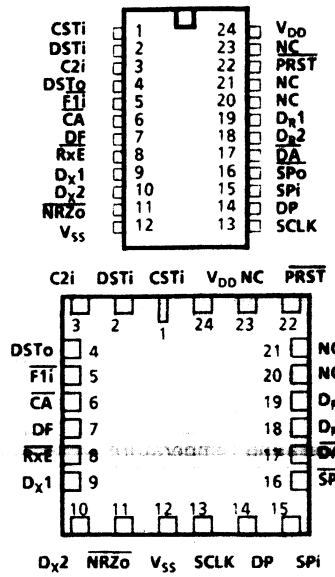
Applications

- Transparent coder/decoder for synchronous and asynchronous data.
- Data Terminal (RS-232C etc.) to ST-BUS Interface
- Data switching on Digital PBXs.
- Channel banks/TDM multiplexers.

Description

The MT8950 is a coder/decoder which uses the Transition Encoded Modulation (TEM) technique for encoding/decoding low speed data to and from a 56/64Kbps channel (equivalent to PCM Voice). The coding and decoding scheme is transparent and can accept either synchronous or asynchronous data upto 8 Kbps (inclusive);at 9.6Kbps and 19.2 Kbps. The MT8950 is fabricated in MITEL's ISO-CMOS Technology.

Pin Connections



Ordering Information

MT 8950 AC 24 Pin Ceramic
MT 8950 AY 24 Pin LCC

0°C to 70°C

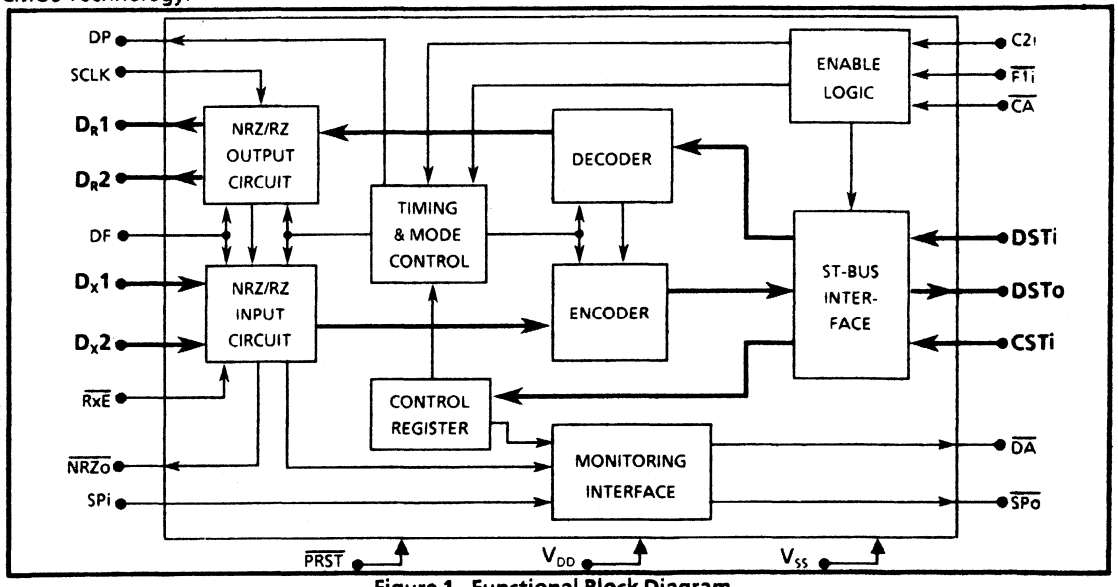


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

- Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.5	7.0	V
2	D.C Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD} + 0.3	V
3	D.C. Output Voltage	V_{OUT}	V_{SS}-0.3	V_{DD} + 0.3	V
4	Input Diode Current ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}		± 10	mA
5	Output Diode Current ($V_O < 0$ or $V_O > V_{DD}$)	I_{OK}		± 20	mA
6	DC Output Current, per pin	I_O		± 25	mA
7	DC Supply or Ground Current	I_{DD}/I_{SS}		± 50	mA
8	StorageTemperature	T_{ST}	-65	150	°C
9	Package Power Dissipation (CERDIP) T_A = 25° C	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recomended Operating Conditions

- Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply voltage	V_{DD}	4.5	5.0	5.5	V	
2	Operating Frequency	f_{CK}		2.048		MHz	
3	Operating Temperature	T_A	0		70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

V_{DD} = 5.0V ± 10%; V_{SS} = 0V; T_A = 0°C to 70°C - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent supply current	I_{QS}			150	µA	All outputs unloaded All inputs @ V_{ss}
2	SUP	Operating supply current	I_{DD}			1.0	mA	All outputs unloaded. Input pins 2 and 3 clocked at 2.048 Mhz. Pins 1,8,15,20,21 @ V_{SS} Pins 5,6,7,9,10,13 and 22 @V_{DD}
3	INPUTS	TTL inputs [1] HIGH voltage LOW voltage	 V_{IH} V_{IL}	 2.0 V_{SS}		 V_{DD} 0.8	 V V	
4	INPUTS	CMOS inputs [2] HIGH voltage LOW voltage	 V_{IH} V_{IL}	 3.5 V_{SS}		 V_{DD} 1.5	 V V	
5	INPUTS	CMOS Schmitt inputs [3] HIGH voltage LOW voltage	 V_{IH} V_{IL}	 3.0 V_{SS}		 V_{DD} 1.0	 V V	
6	INPUTS	SPi Comparator ON Voltage	V_{T+}	2.25	2.5	2.75	V	V_{DD} = 5V
7	INPUTS	SPi Comparator OFF Voltage	V_{T-}	2.0			V	V_{DD} = 5V
8	INPUTS	Input Leakage Current	I_{IN}		± 1	± 10	µA	V_{DD} = 5V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

1. Include DSTi, CSTi, C2i, $F\overline{1}i$ and SCLK
2. Include DF
3. Include $R\overline{xE}$,Dx1, Dx2 and $\overline{PRST}$

DC Electrical Characteristics

V_{DD} = 5.0V ± 10%; V_{SS} = 0V; T_A = 0°C to 70°C - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	OUTPUTS	Output LOW Voltage	V_{OL}			0.05	V	$\|I_O\| < 1.0\ \mu A$ V_{DD} = 5V
2		Output HIGH Voltage	V_{OH}	4.95			V	$\|I_O\| < 1.0\ \mu A$ V_{DD} = 5V
3		Output LOW Current (On all outputs except DSTo)	I_{OL}	2.2	2.8		mA	V_{OL} = 0.4V
4		Output HIGH Current (On all outputs except DSTo)	I_{OH}	-3.5	-4.2		mA	V_{OH} = 2.4V
5		Output LOW Current (On DSTo output)	I_{OL}	8.9	11.1		mA	V_{OL} = 0.4V
6		Output HIGH Current (On DSTo output)	I_{OH}	-14.0	-16.8		mA	V_{OH} = 2.4V
7		Output Leakage Current	I_{OZ}		± 1	± 10	µA	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		C2i Clock Frequency	f_{CK}	2.028	2.048	2.068	MHz	
2		C2i Clock Rise Time	t_{CR}			50	ns	
3		C2i Clock Fall Time	t_{CF}			50	ns	
4		Clock Duty Cycle (C2i & SCLK)			50		%	
5		SCLK Clock Frequency	f_{SCLK}	0	0.6	128	KHz	
6		SCLK Clock Rise Time	t_{SCLKR}			50	ns	
7		SCLK Clock Fall Time	t_{SCLKF}			50	ns	
8		$\overline{F1i}$ and $\overline{CA}$ Rise Time	t_{ER}			100	ns	
9		$\overline{F1i}$ and $\overline{CA}$ Fall Time	t_{EF}			100	ns	
10		$\overline{F1i}$ and $\overline{CA}$ set-up Time	t_{ES}	25			ns	
11		$\overline{F1i}$ and $\overline{CA}$ Hold Time	t_{EH}	-25		25	ns	
12		DSTo Rise Time	t_{OR}			100	ns	Note 1
13		DSTo Fall Time	t_{OF}			100	ns	Note 1
14		Propagation Delay From Clock (C2i) To Output (DSTo) enable.	t_{PZH} t_{PZL}			125	ns	Note 1
15		Propagation Delay From Clock (C2i) To Output (DSTo).	t_{PLH} t_{PHL}			125	ns	Note 1
16		Input Rise Time (DSTi, CSTi)	t_{IR}			100	ns	
17		Input Fall Time (DSTi, CSTi)	t_{IF}			100	ns	
18		DSTi, CSTi Set-up Time	t_{ISH} t_{ISL}	0			ns	
19		DSTi, CSTi Hold Time	t_{IH}	90			ns	
20		$\overline{PRST}$ Low Time		488			ns	

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 1: R_L = 10KΩ to V_{DD}, C_L = 150 pF to V_{SS}

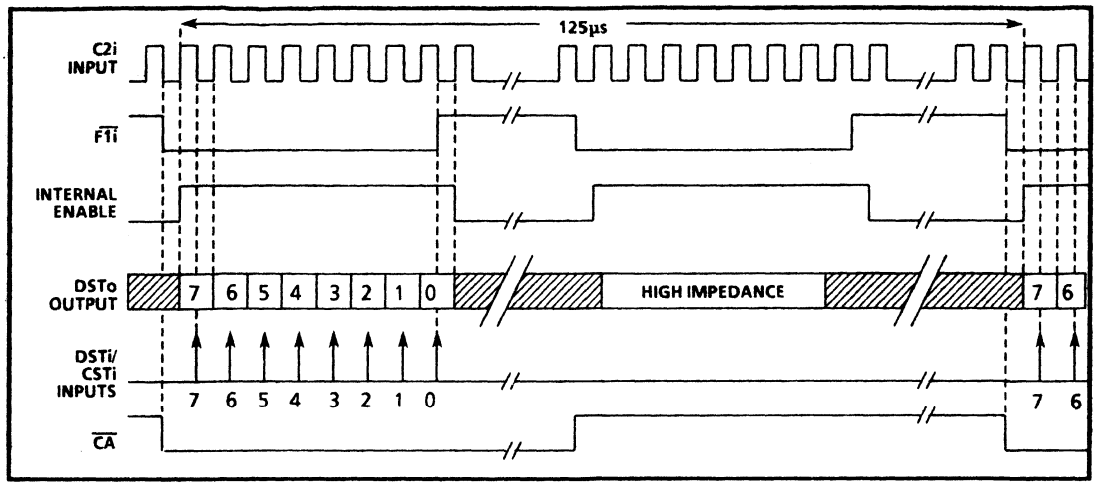


Figure 2. Timing Diagram - 125µs Frame Period

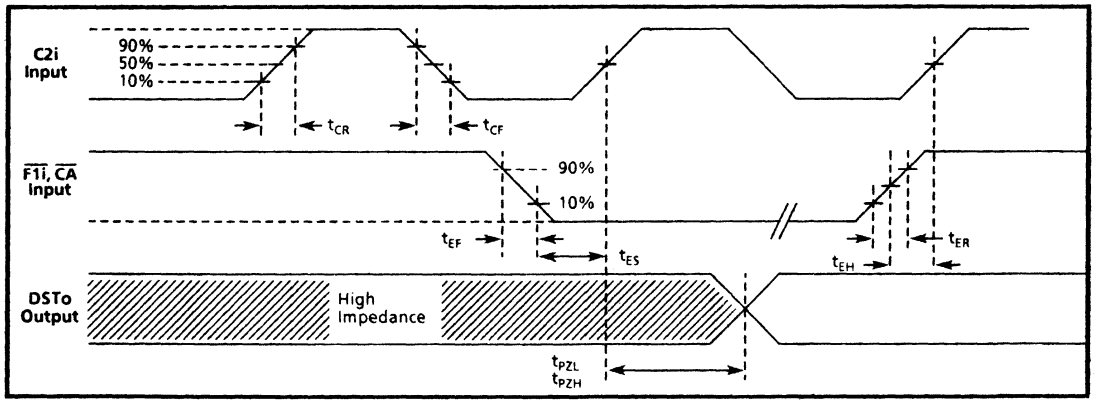


Figure 3. Timing Diagram - ST-BUS Interface Enable

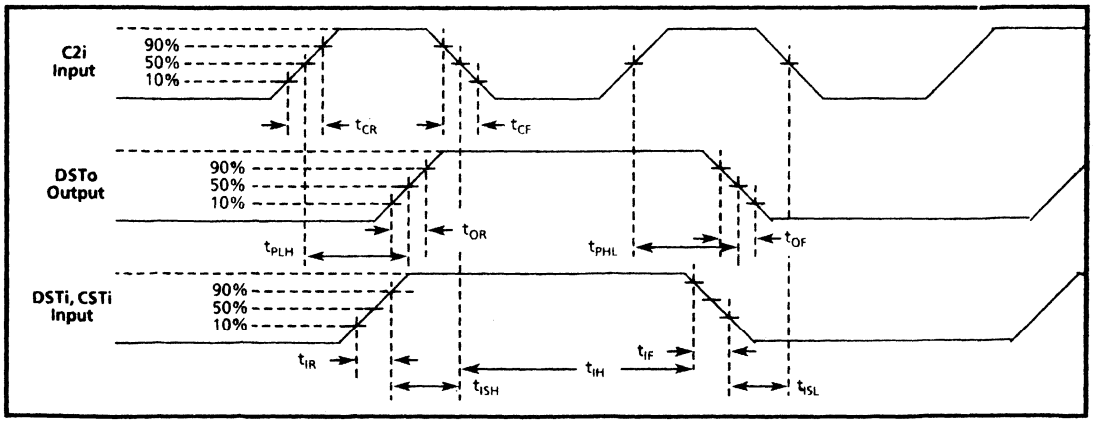


Figure 4. Timing Diagram - ST-BUS Input/Output

Table 1. Pin Description

Pin No.	Name	Description
1	CSTi	**Control ST-BUS In (TTL Input)** - This ST-BUS interface pin accepts a serial input stream which loads the Control Register. The mode of operation of the device, the bits in the Violation word, and, the resetting of Data Activity ($\overline{DA}$) and Scan Point output ($\overline{SPo}$) are controlled by this register. The contents of the register are updated once every ST-BUS frame when the interface is enabled.
2	DSTi	**Data ST-Bus In (TTL Input)** - Accepts the 8 bits of TEM Data when the ST-BUS interface is enabled.
3	C2i	**2.048 MHz Clock (TTL Input)** - This is the input for the 2.048 MHz clock.
4	DSTo	**ST-BUS Output (Three-State Output)** - This is the 2.048 Mbps serial output for theTEM encoded word. It is enabled when both $\overline{F1i}$ and $\overline{CA}$ are low.
5	$\overline{F1i}$	**Framing Type 1 Input (TTL Input)** - This active low input, in conjunction with $\overline{CA}$, enables the ST-BUS interface (DSTi, DSTo and CSTi). It is internally sampled on every positive edge of the C2i clock and provides frame synchronization.
6	$\overline{CA}$	**Control Address (TTL Input)** - This active low input (in conjunction with $\overline{F1i}$) enables the ST-BUS interface.
7	DF	**Data Format Select (CMOS Input)** - When HIGH, the Data Codec accepts and delivers the data in unipolar Return to Zero (RZ) format. When LOW, the data format is unipolar NRZ.
8	$\overline{RxE}$	**Received Energy Signal (Schmitt Input)** - When $\overline{RxE}$ goes LOW it establishes the polarity of the input pins Dx1 and Dx2 in the RZ mode. The input which received the last pulse before $\overline{RxE}$ goes LOW is established as the unipolar MARK input. $\overline{RxE}$ also enables the operation of $\overline{DA}$ and $\overline{SPo}$ outputs. During the loopback modes (Modes 4, 5 and 6) of the codec, $\overline{RxE}$ is forced to the LOW state internally independent of the pin condition. $\overline{RxE}$ should be exerted LOW for the duration of a data call.
9	D_x1	**Data Transmit 1 (Schmitt Input)** - If DF = LOW, accepts data in the NRZ format. (HIGH = MARK, LOW = SPACE) If DF = HIGH, accepts active low unipolar pulses representing the digital data in the RZ format. MARK or SPACE polarity is established by the $\overline{RxE}$ input.
10	D_x2	**Data Transmit 2 (Schmitt Input)** - If DF = LOW, accepts data pulses which are encoded only if there is no activity on the Dx1 pin - the data format and restrictions on the use of this input is explained in the text. If DF = HIGH, accepts active low unipolar pulses representing the digital data in the RZ format. MARK or SPACE polarity is established by the $\overline{RxE}$ input.
11	$\overline{NRZo}$	**Non-Return to Zero Output (Open Drain Output)** - The incoming data, in the RZ format or the NRZ format, is internally converted to inverted NRZ and appears on this open drain output. This output in conjunction with the SPi input can be used for long space detection.

Table 1. Pin Description (continued)

Pin NO	Name	Description
12	V_{SS}	**Ground (0 Volt).**
13	SCLK	**Secondary Clock (TTL Input) -** This is an external clock input that determines the timing of the Violation Word and the synchronization pulses. If these features are not to be utilized, this input can be tied to V_{ss}
14	DP	**Drive Point Output (Totem-pole Output) -** This output is exerted high when the Control Register bits b7,b6 and b5 are set to 110 (decimal 6). The operation of the Codec is normal in every other respect.
15	SPi	**Uncommitted Scan Point Input (Voltage Comparator Input) -** A LOW to HIGH transition on this input causes $\overline{SPo}$ to be set LOW. This is used to detect a long SPACE condition in conjunction with $\overline{NRZo}$ (pin 11).
16	$\overline{SPo}$	**Uncommitted Scan Point Output (Totem-pole Output) -** This output is set LOW when the SPi input undergoes a LOW to HIGH transition. The $\overline{SPo}$ is reset by the presence of a logic "1" in bit b0 of Control Register. This function is active at all times except when $\overline{RxE}$ is false and during power reset conditions.
17	$\overline{DA}$	**Data Activity (Totem-pole Output) -** The NRZ/RZ input circuitry monitors the input signal (after polarity is established) and activates this output when it detects a SPACE on the input. This output is reset by the presence of a logic "1" in bit 1 of the Control Register. The $\overline{DA}$ function is active at all times except when $\overline{RxE}$ is false and during power reset conditions.
18	D_R2	**Data Receive 2 (Totem-pole Output) -** If DF = LOW (NRZ format), outputs the secondary data signal in the NRZ form as explained in the text. If DF = HIGH (RZ format), outputs unipolar, active high MARK pulses.
19	D_R1	**Data Receive 1 (Totem-pole Output) -** If DF = LOW (NRZ format) , outputs the NRZ data signal. (HIGH = MARK, LOW = SPACE) If DF = HIGH (RZ format), outputs unipolar, active low SPACE pulses.
20	NC	**No connection.**
21	NC	**No connection.**
22	$\overline{PRST}$	**Power Reset (CMOS Schmitt Input) -** A LOW level on this input evokes the power reset conditon for the codec.
23	NC	**No connection.**
24	V_{DD}	**Positive Supply Voltage + 5 volts ± 10% .**

Theory of Operation

The MT8950 is an encoder/decoder which operates on low baud rate data (up to 19.2 Kbps) to convert it to the ST-BUS format. The data can subsequently be transparently switched or transmitted in a manner identical to PCM encoded voice. In this respect, the functional characteristics of the device are very similar to many industry standard voice codecs. Asynchronous and synchronous data from 0 to 8Kbps and at 9.6 Kbps is accepted by the codec without any restrictions. Asynchronous data at 19.2 Kbps should have at least two stop bits for the device to encode it properly. The data is encoded by the Codec into an eight bit word which occupies one 64 Kbps channel on the ST-BUS. Conversely it accepts an encoded 8 bit word from an incoming ST-BUS stream and regenerates the original digital signal. Mitel's ST-BUS is a synchronous time division multiplexed serial stream with a bit rate of 2048 Kbps. In a telecommunications environment, it is generally divided into 32 channels made up of 8 bits each, with an effective bandwidth of 64 Kbps per channel. These channels may carry data or PCM encoded voice.

Low Speed Data Format

The Data Codec can accept low speed data in either Non Return to Zero (NRZ) or Return to Zero (RZ) format. The NRZ format requires only one line to carry the data. This format is suitable for interfacing the data codec with RS-232 type terminals and microprocessor peripherals such as UARTS, ACIAs, etc. All signals have to be converted to TTL voltage levels before being input to the codec.

The RZ format requires two separate lines to represent the MARKs and SPACEs in the data as illustrated in Figure 6. This format is useful when the data terminal is located some distance from the codec and the data is to be transmitted over a line as a three level signal (a positive pulse for the beginning of MARKs, negative pulse for the beginning of SPACEs and zero level for no change in the signal). The three level signal is converted to it's TTL-Compatible binary form as shown in Figure 6 before being applied to the codec. A pulse appears on one line of the input indicating the beginning of MARKs. This is followed by a pulse on the second line indicating the beginning of SPACEs. If two or more pulses appear consecutively on the same line before the second line of the pair receives or transmits another pulse, then these pulses can be considered to be violating the normal rule of the RZ format and are called "Violation Pulses". The data codec will accept these violations with the restriction that the time difference between a violation pulse and an actual data transition be at least 125µs. The violation pulses can be on the MARK or SPACE line. In a communications system, these violations can be used to carry other information when no data is being transmitted.

Encoding/Decoding Scheme

The Data Codec uses a Transition Encoded Modulation (TEM) technique to encode low speed data on to a 56 or 64 Kbps equivalent PCM voice channel. This coding algorithm significantly reduces data bit distortion. The timing distortion in the regenerated data is summarized in Table 2. A simple sampling method for encoding the data would require a 256Kbps channel to obtain the same low distortion figures.

If the encoded information is to be transmitted over digital T1/DS1 trunks, the maximum percentage distortion in the regenerated data is effectively doubled. This is due to the fact that the least significant bit in specific channels on these trunks is used to transmit signalling information. Thus the bandwidth per channel is reduced to 56 Kbps.

The encoder stage of the Data Codec observes data transitions in discrete timing windows which are 125µs wide. These timing frames are further divided into 32 timeslots of 3.906µs duration each (see Figure. 5). The position of the first data transition, the total number of transitions, and, the time period between the transitions in this 125µs frame is encoded as an 8 bit word.

Data Rate Bits/Sec	0 - 8000	9600	19200
Asynchronous Restrictions	None	None	Minimum 2 Stop Bits
Synchronous Restrictions	None	None	None
Percentage Distrortion†	± 3.2	± 3.8	± 7.5

Table 2. Summary of Data Codec Capabilities.

† Refers to the maximum distortion in the bit period timing of the regenerated data. (Channel Bandwidth = 64Kbps)

Percentage Distortion = $|T_{BO} - T_{BR}| / T_{BO} \times 100$

where

T_{BO} = Orginal Data Bit Period

T_{BR} = Regenerated Data Bit Period

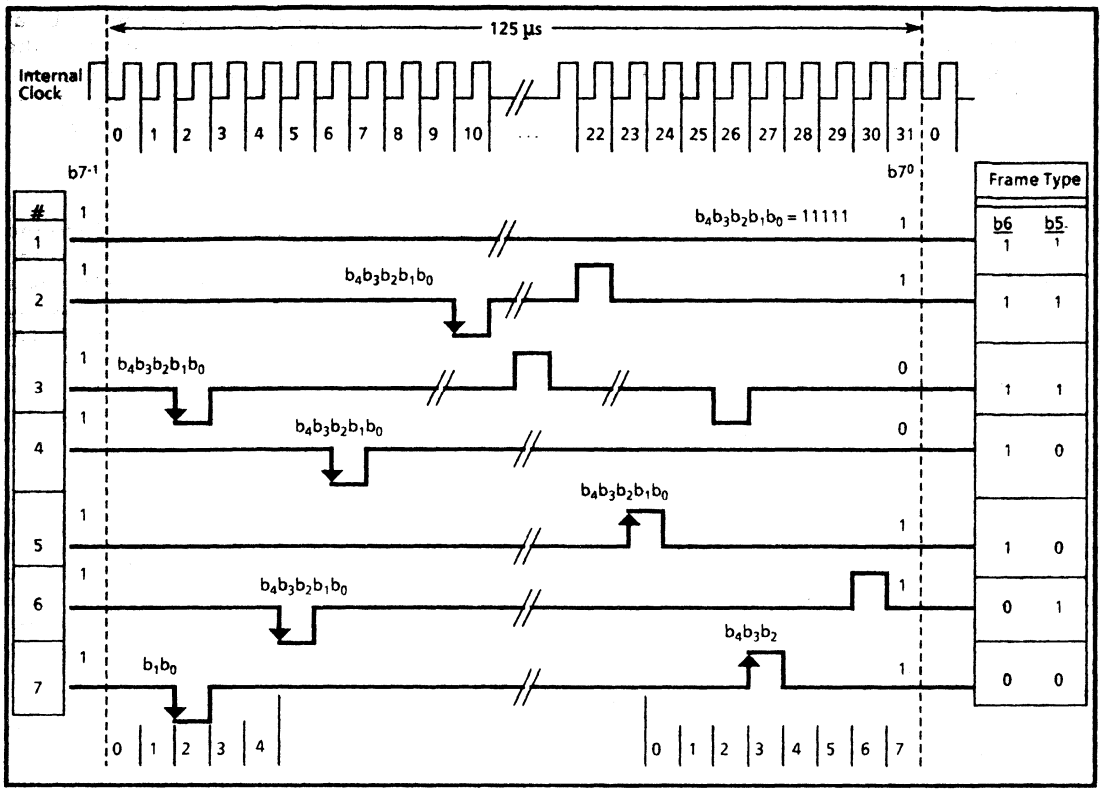


Figure 5. TEM Coding Scheme
(Note: Waveforms shown are bipolar RZ equivalent of separate RZ /NRZ inputs)

#	Frame Description	Level† b7	Frame Type b6 b5	First Transition b4 b3 b2 b1 b0	Notes
1	No Pulse	1/0	1 1	1 1 1 1 1	
2	2 Data Pulses (T = 52 µs)	1/0	1 1	X X X X X	XXXXX ≤ 10001 (17)
3	3 Data Pulses (T = 52 µs)	1/0	1 1	X X X X X	XXXXX ≤ 00100 (4)
4	1 Data Pulse	1/0	1 0	X X X X X	XXXXX = 0 to 31
5	Violation Pulse	1/0	1 0	X X X X X	XXXXX = 0 to 31
6	2 Data Pulses (T = 104 µs) (Time slot 4 to 31)	1/0	0 1	X X X X X	XXXXX > 00011 (3)
7	2 Data Pulses (T = 104 µs) (Time slot 0 to 3)	1/0	0 0	Y Y Y X X	XX = 0 to 3 YYY = 0to 7

Table 3. TEM Coding Summary
† Note: The Level bit (b7) indicates the level (HIGH or LOW) of the input data in timeslot 31 of the current frame.

The first five bits (b0 to b4) indicate the position of the first data transition with respect to the 32 timeslots in the window. Bit 7 in the encoded word represents the absolute value of the data in the 31st timeslot. Bits 5 and 6 in conjunction with bit 7 are used to identify the total number of transitions and the time period between the transitions. Due to the fixed bit rate restrictions above 8Kbps, a maximum of seven frames types are possible as shown in Figure 5. In frame type 7, the first five bits (b0 to b4) are used to represent two transitions instead of the normal first transition. Note that the data transitions in Figure 5. are shown as a three level signal. A positive transition indicates the beginning of one or more continuous MARKs and a negative transition indicates the beginning of one or more continuous SPACEs.

The decoder stage regenerates the original data from the 8 bit TEM word. The absolute values of the data signal in the present and previous frames as given by b7(n) and b7(n-1) are EX-ORed and the result in combination with the remaining bits of the TEM word is used to reproduce the orginal data with an accuracy of ± 3.906µs. Because of the data speed restriction above 8Kbps, the second and third transitions (if any) will be reproduced at intervals which are multiples of 52µs (depending on the input data baud rate).

Functional Description

The functional block diagram of the data codec is shown in Figure 1. The low speed data to be encoded is accepted by the NRZ/RZ input circuitry and relayed to the encoder. The 8 bit encoded word is transmitted within one channel time period on to the ST-BUS serial output stream. At the same time an 8 bit TEM word is loaded into the decoder via the incoming ST-BUS stream. The low speed data is regenerated and output by the NRZ/RZ output circuitry. The data codec can operate in eight modes. The specific mode of operation is selected by programming the internal Control Register using the CSTi serial input.

Transmit Path

The NRZ/RZ input circuitry can be programmed to accept RZ or NRZ data by asserting the appropriate level on the DF pin (HIGH = RZ format; LOW = NRZ format).

In the RZ format, both D_X1 and D_X2 are used for the input data. MARK pulses are received on one line input and SPACE pulses on the other. The MARK and SPACE polarities of the input pins are fixed by the high to low transition of the $\overline{RxE}$ line. The input having the last transition before $\overline{RxE}$ goes low is selected to be the MARK input. Thus to ensure correct polarity selection, the data codec should be receiving MARK pulses before $\overline{RxE}$ is taken low. The $\overline{RxE}$ line must be kept low for the duration of the call. As indicated before, the Data Codec does accept violation pulses. The violation pulses can be input on the MARK or SPACE lines. The time difference between a violation pulse and an actual data pulse must be at least 125µs. Since only one violation pulse is encoded per frame, the minimum time period between consecutive pulses should be 125µs as illustrated in Figure 6.

In the NRZ format, only one line is required for the data. This is input at D_X1 (Pin 9). The second input, D_X2, can be used for transmitting secondary control information. The signal on this input pin is encoded only when there is no activity on the D_X1 line - i.e. during steady MARK or SPACE condition on the data line. To ensure proper encoder function, the signal to the D_X2 line should be applied after at least 125µs have elapsed since the last data transition on D_X1. The acceptable data format for the D_X2 input is illustrated in Figure 7. Each pulse on the line is encoded as a single transition. The minimum time period between consecutive pulses should be 125µs.

The encoding of the NRZ/RZ data to the TEM format is performed by the encoder. The 8 bit TEM words are transmitted on the outgoing ST-BUS channel via DSTo. This is a three state output which is enabled only when both $\overline{CA}$ and $\overline{F1i}$ are low (see Figure. 2).

Receive Path

The 8 bit word generated by a data codec at a remote end is shifted in from the incoming ST-BUS stream via the DSTi input. The word is shifted in at the same time as the outgoing word is shifted out - i.e. when both $\overline{CA}$ and $\overline{F1i}$ are low as illustrated in Figure 2. The NRZ/RZ low speed data is regenerated by the decoder section and output via D_R1 and D_R2.

If the chip is operating in the RZ format, D_R2 transmits MARK pulses and D_R1 transmits SPACE pulses. The format of the output signal is shown in Figure 6. The width of an output pulse is nominally 35µs and cannot be altered by the user. Violation pulses will appear on the line on which they were initially inserted at the remote end.

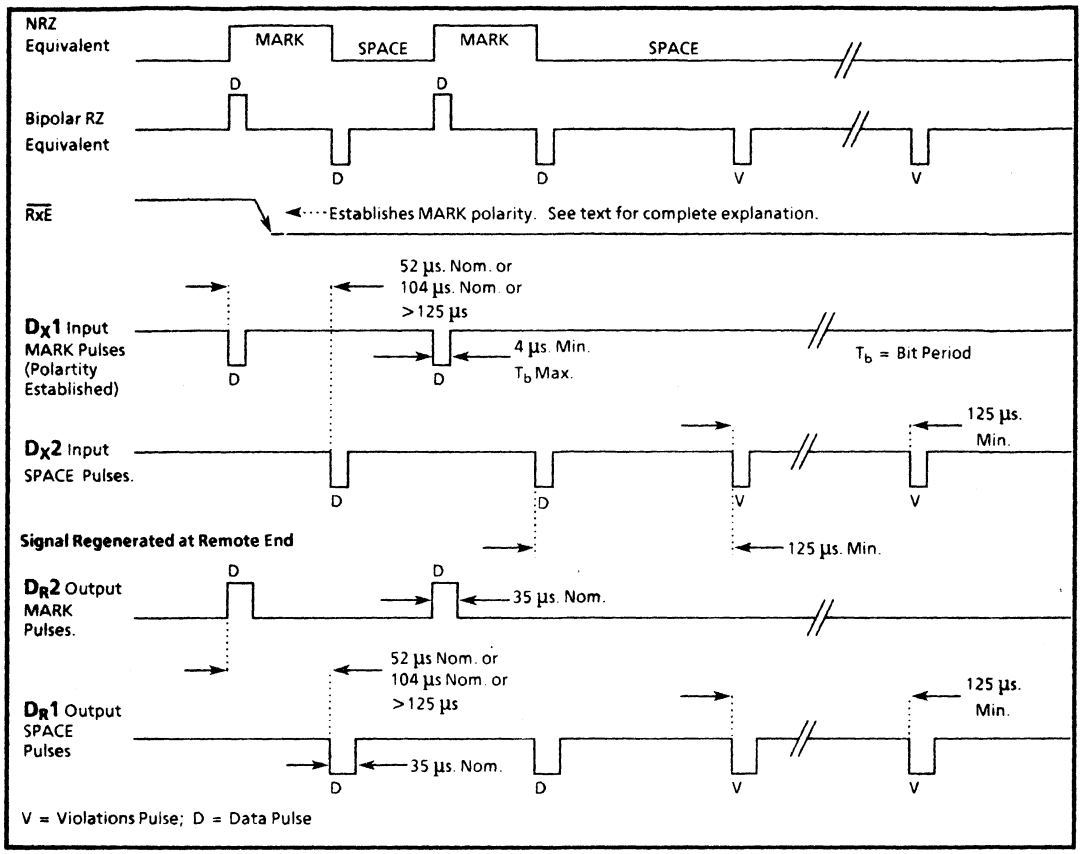


Figure 6. Example Input/output Waveform in the RZ format (DF = HIGH)

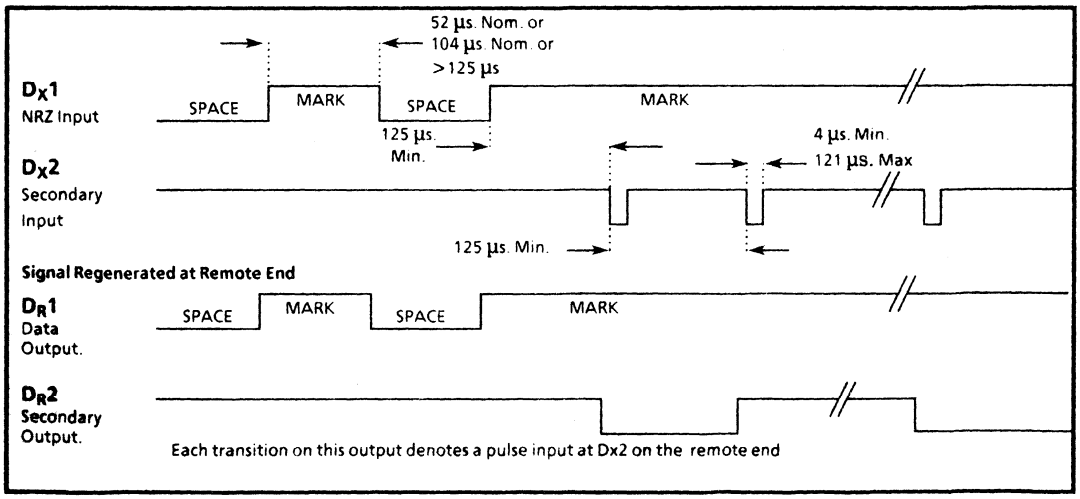


Figure 7. Example Input/Output Waveform in the NRZ format (DF = LOW)

In the NRZ format D_R1 outputs the data. The second output pin D_R2, transmits the secondary signal. Each transition in this signal represents one data pulse encoded by the remote end. An example of the type of waveform observed is illustrated in Figure 7.

The NRZ/RZ output circuitry also transmits synchronizing pulses if the data decoded from DSTi is idling (i.e. no data transitions) for more than six clock periods of the Secondary clock (SCLK). This Secondary clock is typically a 600Hz input to the chip. When the codec is set in the RZ format, these sync pulses will be either MARK or SPACE violation pulses - depending on the last data bit transmitted. If it is operating in the NRZ format, the sync pulses constitute a squarewave with high and low durations of six SCLK periods. This square wave appears at the D_R2 output pin. Synchronization pulses are transmitted until some activity is detected by the decoder or the mode of operation is changed through the Control Register.

Timing Requirements

The data codec derives all the internal timing from the 2.048 MHz clock input (C2i) and the two enable signals $\overline{F1i}$ and $\overline{CA}$. The DSTo output goes from high impedance to the value of bit 7 of the TEM word on the first rising edge of the clock after $\overline{F1i}$ and $\overline{CA}$ are taken low. The 8 bit TEM word from the input ST-BUS stream is clocked into the device on the negative edge of the C2i clock. For proper codec operation, the ST-BUS interface (DSTo, DSTi, and CSTi) should be enabled for only 8 clock periods of the C2i clock in any 125µs period (one ST-BUS frame time) as shown in Figure 2. All data input and output at the ST-BUS interface takes place at 2.048Mbps.

The Secondary clock input (SCLK) is normally a 600Hz clock signal. This clock is internally aligned with the 2.048 Mhz input. It is used to generate the synchronizing pulses and the violation word timing (when the chip is operating in the local carrier mode). Note that the 600Hz frequency is an exact multiple of the most commonly used baud rates i.e. 300, 2400, 4800, 9600, and 19200. In synchronous data transmision schemes, the receiver timing circuitry can be kept in sync using the synchronizing pulses or the violation word when no data is being transmitted. Other clock frequencies can be used for specific applications. If this facility is not to be utilized, the SCLK input can be tied to ground.

Control Interface

An 8 bit word is read into the Control Register via the CSTi input at the same time as the TEM word is being shifted in. The chip functions controlled by the eight bits are summarized in Table 4. and described in subsequent sections.

BIT	FUNCTION
7,6,5	Device mode control bits. These bits select one of eight modes of operation
4,3,2	Violation word control bits
1	Resets the Data Activity Scan point
0	Resets the Uncommitted Scan point

Table 4. Summary of Control Register Function

Modes of Operation

As mentioned earlier, the data codec can operate in eight different modes. The specific mode is selected through bits 7, 6 and 5 in the Control Register. Table 5. summarizes the different modes.

Control Register Bits			Mode of Operation
b7	b6	b5	
0	0	0	Normal
0	0	1	Local Carrier
0	1	0	Local Synchronization
0	1	1	Digital Loopback
1	0	0	Data Loopback
1	0	1	Data Loopback - Local Violation Word
1	1	0	Normal Mode -Drive Point Set HIGH.
1	1	1	Idle

Table 5. Modes of Operation

Mode 0: Normal. This is the normal transparent conversion mode of the data codec. The NRZ/RZ input signal is directly encoded into the TEM format and output as an ST-BUS channel. The TEM word for the input ST-BUS channel is decoded and the regenerated data is output via the NRZ/RZ output circuitry. Synchronizing pulses are also transmitted as explained in the preceding paragraphs.

Mode 1: Local Carrier. In this mode the NRZ/RZ output circuitry transmits an 8 bit word at D_R2 (Pin 18) by modulating the secondary clock (SCLK). If the chip has been selected to operate in the RZ format, this word is transmitted as MARK Violations. The time interval between consecutive pulses specifies the binary value. A logical zero is represented by a time interval of one SCLK period between the pulses. A logic "1" is represented by two clock periods. In the NRZ mode, the time interval between consecutive transitions of the signal carries the information. The modulation scheme is illustrated in Figure 8. The 8 bit word consists of a sync bit followed by seven other bits. Bits 1, 4 and 5 in this word reflect the values of bits 2, 3 and 4 in the Control Register. The remaining four bits in the word are fixed as zeros. The sync bit is identified by a time interval equal to four clock periods of SCLK. The NRZ/RZ input circuitry and the encoder stage operates normally in this mode.

Mode 2: Local Synchronization. In the local sync mode, the NRZ/RZ output circuitry transmits only sync pulses on D_R2. These sync pulses appear as MARK violations in the RZ mode with the time interval between consecutive pulses equal to four SCLK periods. In the NRZ format D_R2 outputs a square wave with a period equal to eight cycles of SCLK. D_R1 output is held at steady MARK. The NRZ/RZ input circuitry and the encoder stage of the chip function normally.

Mode 3: Digital Loopback. In this mode an 8 bit word from the incoming ST-BUS (DSTi) is sampled and one ST-BUS frame later, the same word is looped back to the corresponding outgoing channel of the ST-BUS (DSTo). This allows the user to test the ST-BUS transmission path to and from the data codec.

Mode 4: Data Loopback. This mode permits the user to test the decoding and encoding operation of the codec. A known TEM word is sent to the data codec from the ST-BUS end. This word is decoded and redirected via the output circuitry to the NRZ/RZ input circuit and subsequently to the encoder stage for transmission out on the ST-BUS

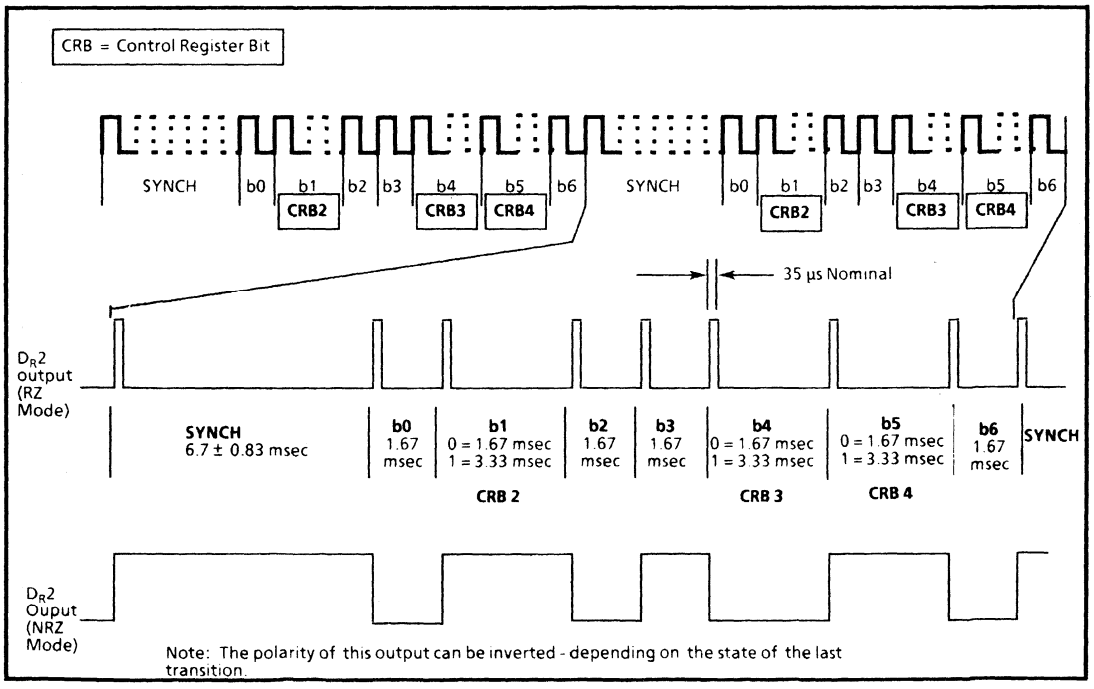


Figure 8. Violation Word Timing in the Local Carrier Mode for a 600Hz input to SCLK

output pin (DSTo). The NRZ/RZ inputs (Pins 9 and 10) are functionally disconnected from the input circuitry. The outputs (pins 18 and 19) are in a non-active state , i.e. D_R1 is steady LOW and D_R2 is steady HIGH.

Mode 5: Data Loopback - Local Violation Word. This mode can be used for testing the operation of the chip in the local carrier mode. The Violation word is generated as in the local carrier mode. However, the modulated signal is not output on D_R2. It is rerouted to the NRZ/RZ input circuit, encoded into the TEM format and output on DSTo.

Mode 6: Normal Mode - Drive Point Activated. The drive point output (Pin 14) is set HIGH in this mode. The codec operation is normal in every other respect. This drive point can be used to control external circuitry. It is reset when the mode of operation is changed.

Mode 7: Idle. In the idle mode D_R1 and D_R2 outputs are in a non-active state, i.e. D_R1 is steady LOW and D_R2 is steady HIGH. The encoder stage and the input circuitry operates normally.

Device Monitoring Features

There are two output pins which can be used to monitor the codec.

1. **Data Activity ($\overline{DA}$):** This output goes from high to low when a SPACE signal, indicating the beginning of data activity, is received by the NRZ/RZ input circuitry. The level on this pin is reset by setting bit 1 of the Control Register to logic "1".

2. **Scan Point output ($\overline{SPo}$):** This output is set LOW whenever SPi input undergoes a low to high transition. It is reset by a logic "1" in bit 0 of the Control Register. The SPi input is generally used in conjunction with pin 11 to detect a long SPACE condition in the data. The external circuitry required to utilize this feature is illustrated in Figure 9. Note that Pin 11 ($\overline{NRZo}$) is an open drain output. The NRZ/RZ data input to the codec is converted to the NRZ format and output on this pin. The RC time constant for the circuit shown in Figure 9 can be set to detect SPACE conditions of varying time durations. The length of the long SPACE detected is given by

$$T_{SP} = 0.7RC$$

Where T_{SP} is the duration of the SPACE in milliseconds. A long SPACE of 150ms is generated when the BREAK key on a data terminal is depressed. To detect this signal, a value of R equal to 210KΩ and C equal to 1.0µF can be used. The $\overline{SPo}$ pin could then be monitored by the system processor to detect a prompt from the peripheral.

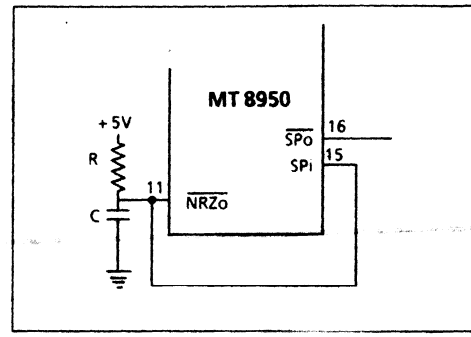


Figure 9. Long Space Detection Circuit

External Power Reset

When the reset input ($\overline{PRST}$) is taken low, the data codec circuit goes into reset mode. The conditions present on the output pins are as follows:

1. DSTo - High Impedance
2. $\overline{SPo}$ - + 5 (unasserted)
3. $\overline{DA}$ - + 5 (unasserted)
4. DP - GND (unasserted)
5. D_R1 - + 5v (inactive)
6. D_R2 - GND (inactive)
7. $\overline{NRZo}$ - GND (Mark condition)

The internal Control Register is loaded with HEX FF.

Applications

A block diagram schematic of a simple Voice-Data integrated switching system is illustrated in Figure 10. The data terminal can access a number of remote devices via the gateway provided by the Data Codec. In this application, the Data Codec function parallels that of the Voice Codec i.e., the Voice Codec converts analog signals into the ST-BUS format while the Data Codec does a similiar conversion for low speed data. The information in the ST-BUS format can be switched via the Digital Switch to any of the other interfaces and subsequently transmitted over the appropriate lines to the remote destination. At the remote end, the orginal signal is regenerated by another codec. The remote equipment can be part of a local area network or it may be accessed through leased T1/CEPT digital lines. In a local area network, the Digital Line Interface Circuit (MT 8970) may be used to provide 256 Kbps full duplex transmission over two pair telephone wiring for distances upto 1.6 kilometers. The MT8970 formats the transmitted signal as three 64Kbps data channels and one 56Kbps channel for synchronization and control information. Thus

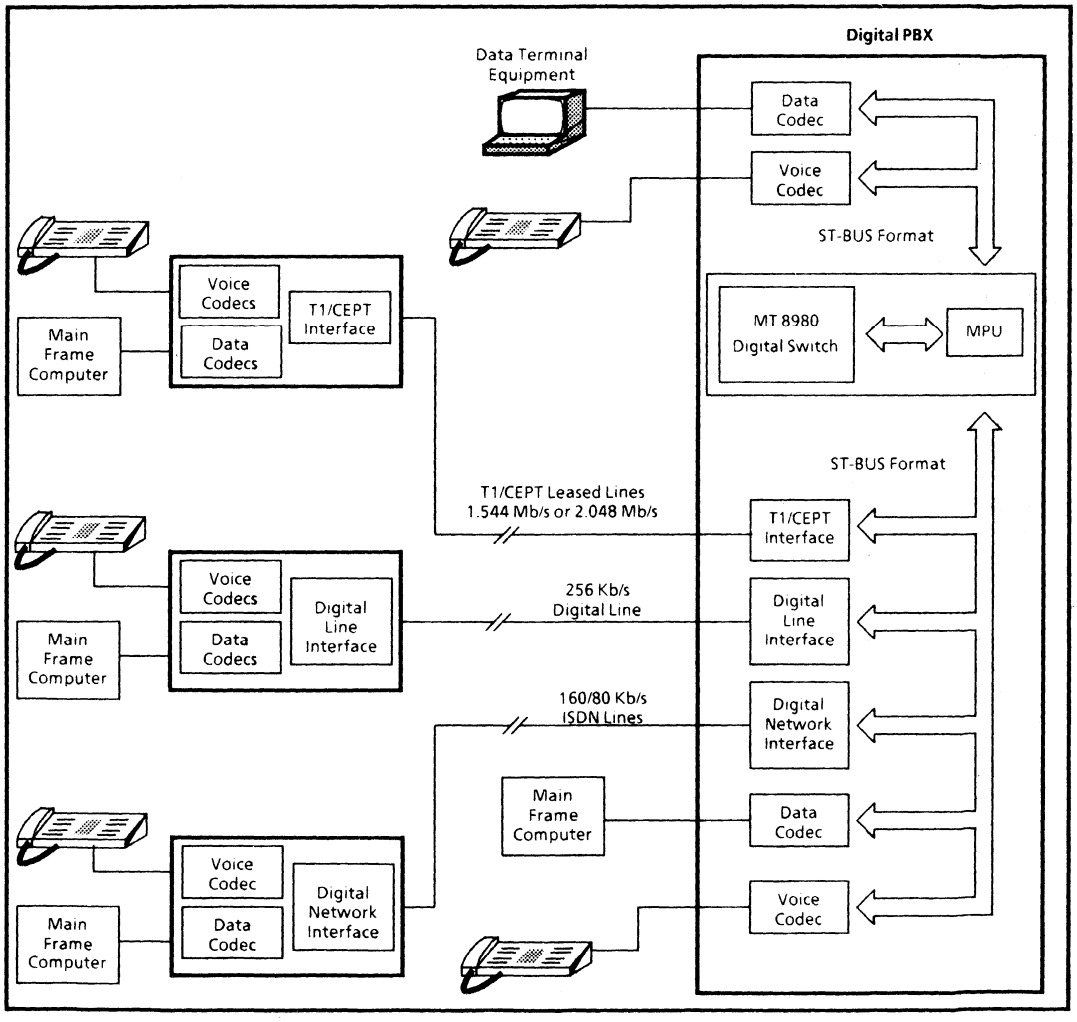


Figure 10. Voice-Data integration using the Data Codec.

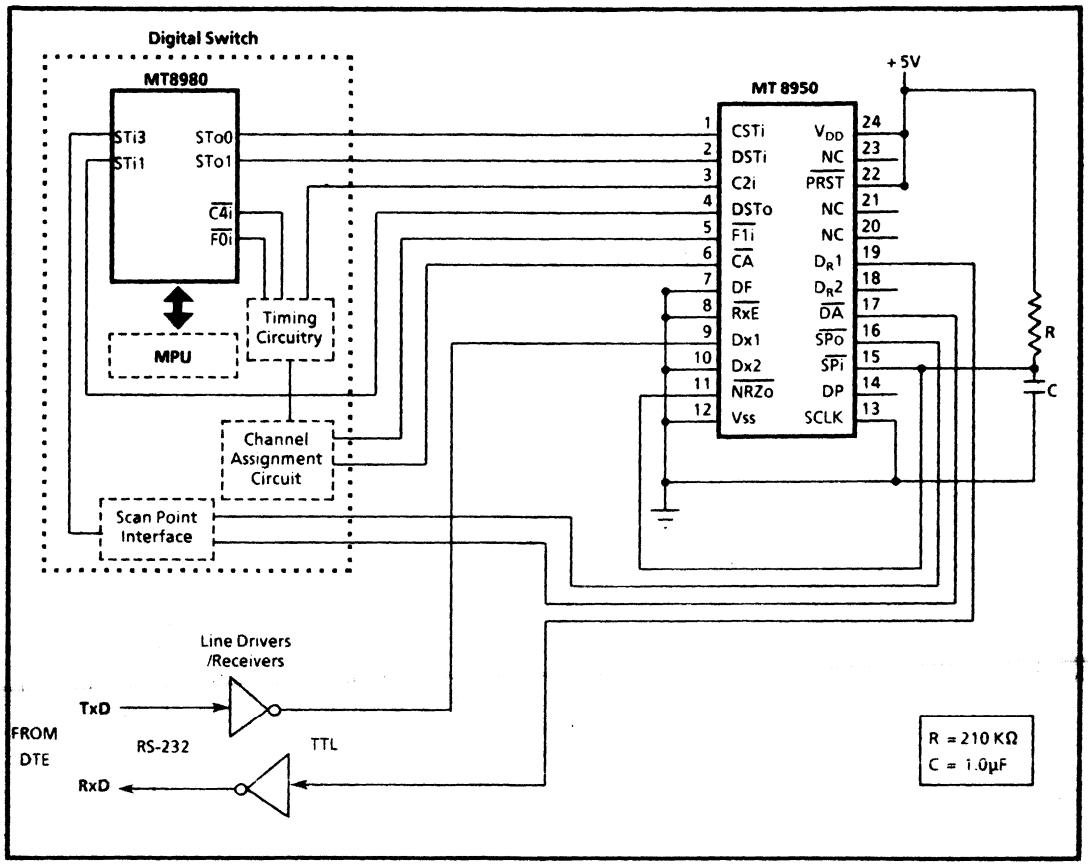


Figure 11. Simplified RS-232 interface using the Data Codec.

upto three data codecs can be interfaced with one 8970. Access to remote equipment via the T1/CEPT leased lines is acquired through the T1/CEPT interfaces (MT8975/8978). Full duplex transmission at 1.544 or 2.048Mbps is possible with these interfaces.

The Digital Network Interface Circuit (DNIC), the MT8972, is capable of providing 160 Kbps full duplex transmission over single telephone pair wiring. This device can support two 64kbps channels, allowing two data codecs to be interfaced to it at the remote end. Simple, low cost data sets can be constructed using the data codec and the DNIC.

A simplified interface for transmitting and receiving RS-232 data signals is illustrated in Figure 11. The Codec is selected to receive and transmit low speed data in the NRZ format. The data transmitted by the terminal equipment in the RS-232 format is inverted and level shifted to TTL-compatible levels before being fed into the D_X1 input on the Codec. The signal is converted into the ST-BUS format and transmitted via the DSTo output in one channel timeslot when the ST-BUS interface is enabled by $\overline{F1i}$ and $\overline{CA}$, as dictated by the system channel assignment scheme. During this same time period the Codec accepts the 8 bit data arriving on the incoming ST-BUS stream which is output at the STo1 pin on the MT8980. The data is decoded and the orginal signal input at the remote end is regenerated and output at the D_R1 pin. This signal is level shifted, inverted and transmitted to the terminal. The codec in this particular application requires no other programming. Loading of the Control Register via the CSTi input is optional. If this input is tied to ground, the Codec will operate in mode 0 (the normal mode). Note that the SCLK input is tied low. Thus synchronization pulses will not be transmitted and the codec cannot be used in the local carrier mode. If this facility is to be used, an appropriate clock can

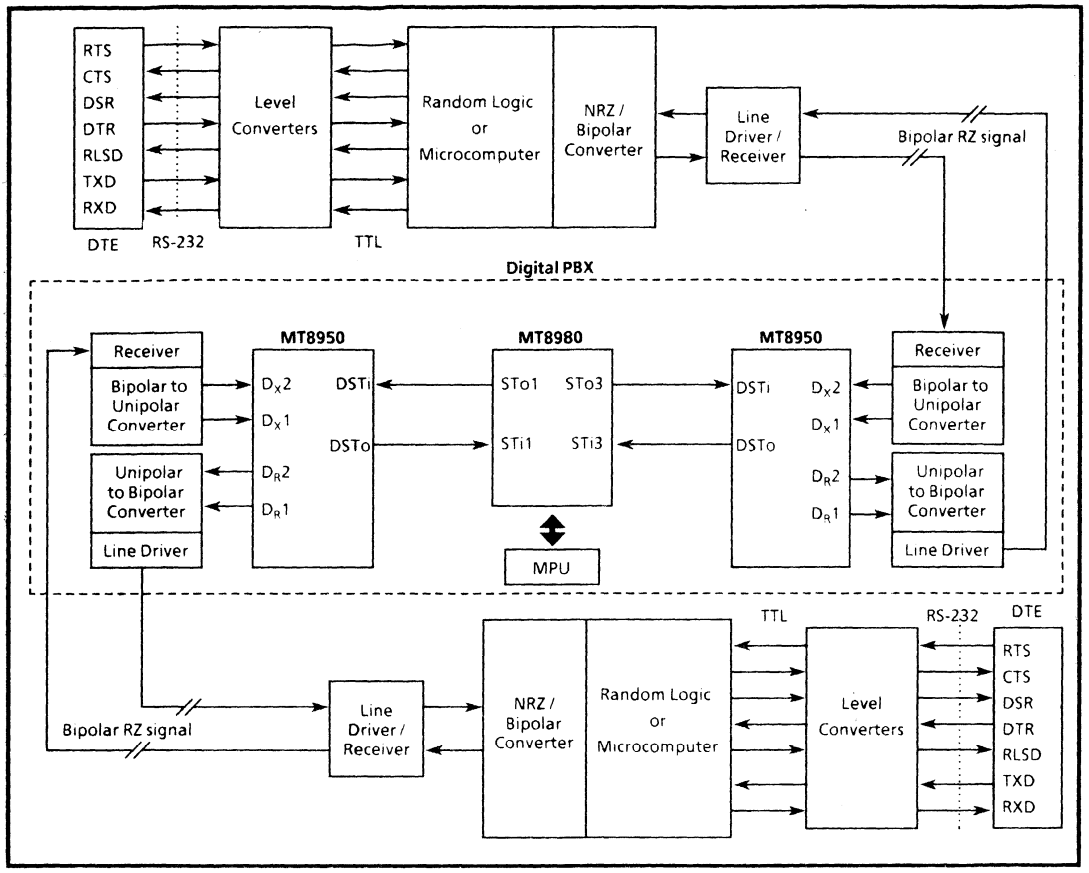


Figure 12. Block diagram illustration of a scheme to submultiplex RS-232 Control Signals.

be input to the device. The long SPACE detection circuitry and the Data Activity output can be used for monitoring the codec if necessary.

Figure 12. shows a block diagram schematic of a circuit which could be used to submultiplex RS-232 control signals with the data. The data and control signals are operated on by the microprocessor or the logic circuitry and subsequently transmitted as a three level signal. The control signals are encoded as bipolar violations. Since the control status does not change very frequently during a call, this information is transmitted only when no data is available. Circuitry near the Codec converts the bipolar signal into a unipolar format and inputs it at D_X1 and D_X2. Conversely, the low speed data from the Codec output at D_R1 and D_R2 is first converted to the bipolar format before being transmitted.The Data Codec is selected to operate in the RZ format. The microprocessor or the random logic circuit examines the received signal for violations. If a stream of violations is detected, then the signal is interpreted to be control information. The detected violations are decoded and the appropriate change in the status of the RS-232 control signals is implemented. If no violations are detected then the incoming signal is considered to be the data and it is rerouted to the RXD pin of the RS-232 connector. The microprocessor could also be used in the initial call set up and for error checking of the received control information. This scheme could be used to provide transparent modem capability to any of the ST-BUS based equipment.

ISO-CMOS ST-BUS™ FAMILY **MT8952B**

HDLC Protocol Controller

Preliminary Information

9161-002-070NA ISSUE 2 AUG 1986

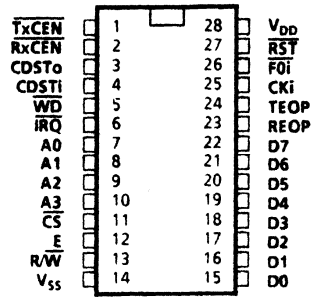
Features

- Formats data as per X.25(CCITT) level-2 standards
- Go-Ahead sequence generation and detection
- Single byte address recognition
- Microprocessor port and directly accessible registers for flexible operation and control
- 19 byte FIFO in both send and receive paths
- Handshake signals for multiplexing data links
- High speed serially clocked output (2.5 Mbps)
- ST-BUS compatibility with programmable channel selection for data and separate time slot for control information
- Independent watch-dog timer
- Facility to disable protocol functions
- Low power ISO-CMOS technology

Applications

- Data link controllers and protocol generators
- Digital sets, PBXs and private packet networks
- D-channel controller for ISDN basic access
- C-channel controller to Digital Network Interface Circuits (typically MT8972)
- Interprocessor communication

Pin Connections



Ordering Information

MT8952BC	28 Pin Cerdip
MT8952BE	28 Pin Plastic

– 40°C to 85°C

Description

The MT8952B HDLC Protocol Controller frames and formats data packets according to X.25 (Level 2) Recommendations from the CCITT. With separate enables for transmit and receive sections and single byte address detection capability, the Protocol Controller can send and receive the packets selectively. It also provides an additional clear channel for control purposes. Further, the protocol functions can be disabled allowing a microprocessor to access the serial bus transparently through the parallel port.

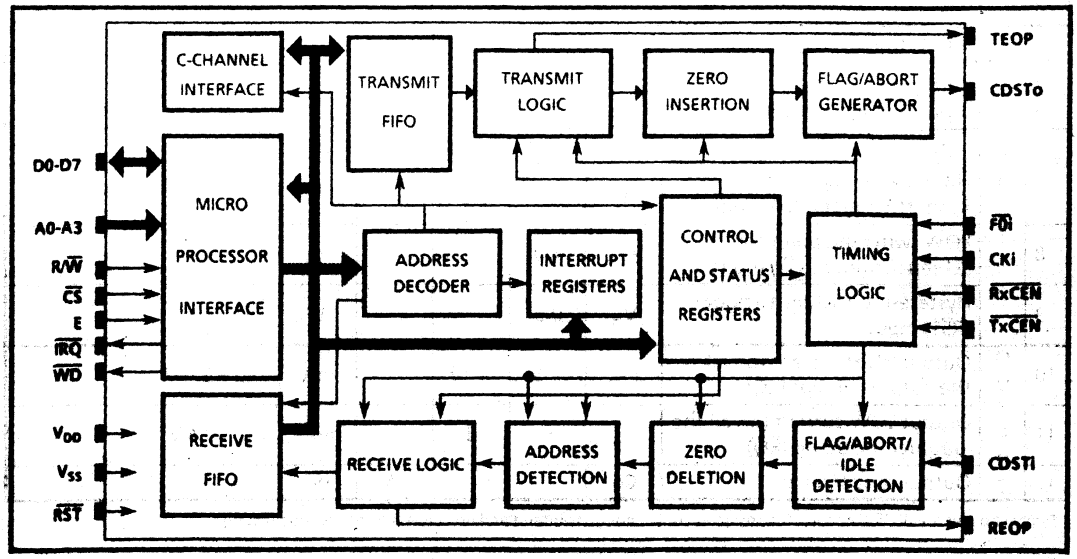


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter		Symbol	Min	Max	Units
1	Supply voltage		V_{DD}	-0.3	7.0	V
2	Voltage on any pin (other than supply pins)		V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current on any pin (other than supply pins)		I_I / I_O		± 25	mA
4	DC Supply or ground current		I_{DD} / I_{SS}		± 50	mA
5	Storage temperature		T_{ST}	-65	150	°C
6	Package power dissipation	Cerdip	P_D		1.0	W
		Plastic	P_D		0.6	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Input HIGH voltage	V_{IH}	2.4		V_{DD}	V	For a Noise Margin of 400 mV
3		Input LOW voltage	V_{IL}	V_{SS}		0.4	V	For a Noise Margin of 400 mV
4		Frequency of operation	f_{CL}			5.0	MHz	When clock input is at twice the bit rate.
5		Operating temperature	T_A	-40	25	85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

V_{DD} = 5V ± 5%, V_{SS} = 0V, T_A = -40 to 85°C

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply current (Quiescent)	I_{DD}			10	µA	Outputs unloaded and clock input (CKi) grounded
2		Supply current (Operational)	I_{DD}			5	mA	At 2.048 Mbps output
3	INPUT	Input HIGH voltage	V_{IH}	2.0			V	
4		Input LOW voltage	V_{IL}			0.8	V	
5		Input leakage current	I_{IZ}			10	µA	
6		Input capacitance	Cin			10	pF	
7		HIGH switching point for Schmitt Trigger ($\overline{RST}$) input	V_{T+}			4.0	V	
8		LOW switching point for Schmitt Trigger ($\overline{RST}$) input	V_{T-}	1.0			V	
9		Hysteresis on Schmitt Trigger ($\overline{RST}$) input	V_H	0.5			V	
10	OUTPUT	Output HIGH current (on all the outputs except $\overline{IRQ}$)	I_{OH}	-5	-12		mA	V_{OH} = 2.4 V
11		Output LOW current (on all the outputs including $\overline{IRQ}$)	I_{OL}	5	8		mA	V_{OL} = 0.4 V
12		Output capacitance	Co			15	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

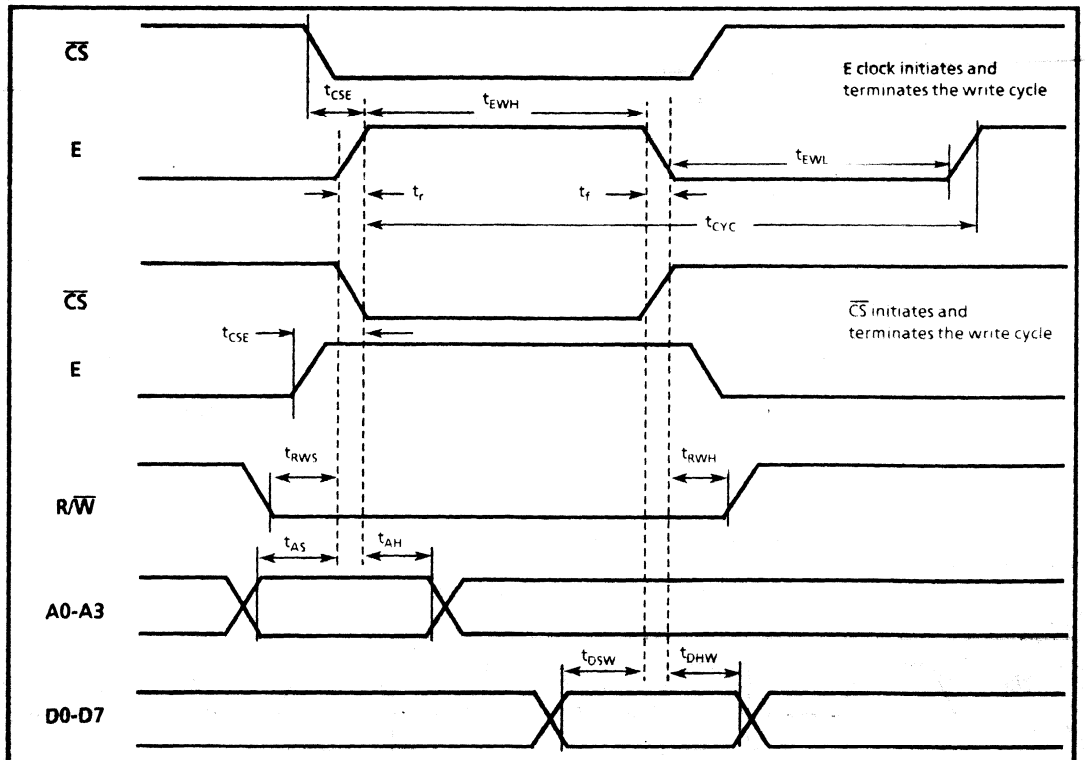
AC Electrical Characteristics† – Microprocessor Interface (Figures 2 and 3)

Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Delay between $\overline{CS}$ and E clock	t_{CSE}	0			ns	
2	Cycle time	t_{CYC}	160			ns	
3	E Clock pulse width HIGH	t_{EWH}	100			ns	
4	E Clock pulse width LOW	t_{EWL}	60			ns	
5	Read/Write set-up time	t_{RWS}	20			ns	
6	Read/Write hold time	t_{RWH}	10			ns	
7	Address set-up time	t_{AS}	20			ns	
8	Address hold time	t_{AH}	40			ns	
9	Data set-up time (write)	t_{DSW}	70			ns	
10	Data hold time (write)	t_{DHW}	10			ns	
11	E clock to valid data delay	t_{DZL} t_{DZH}			125	ns	Test load circuit 1 (fig. 11) C_L = 200pF
12	Data hold time (read)	t_{DLZ} t_{DHZ}	10		60	ns	Test load circuit 3 (fig. 11)

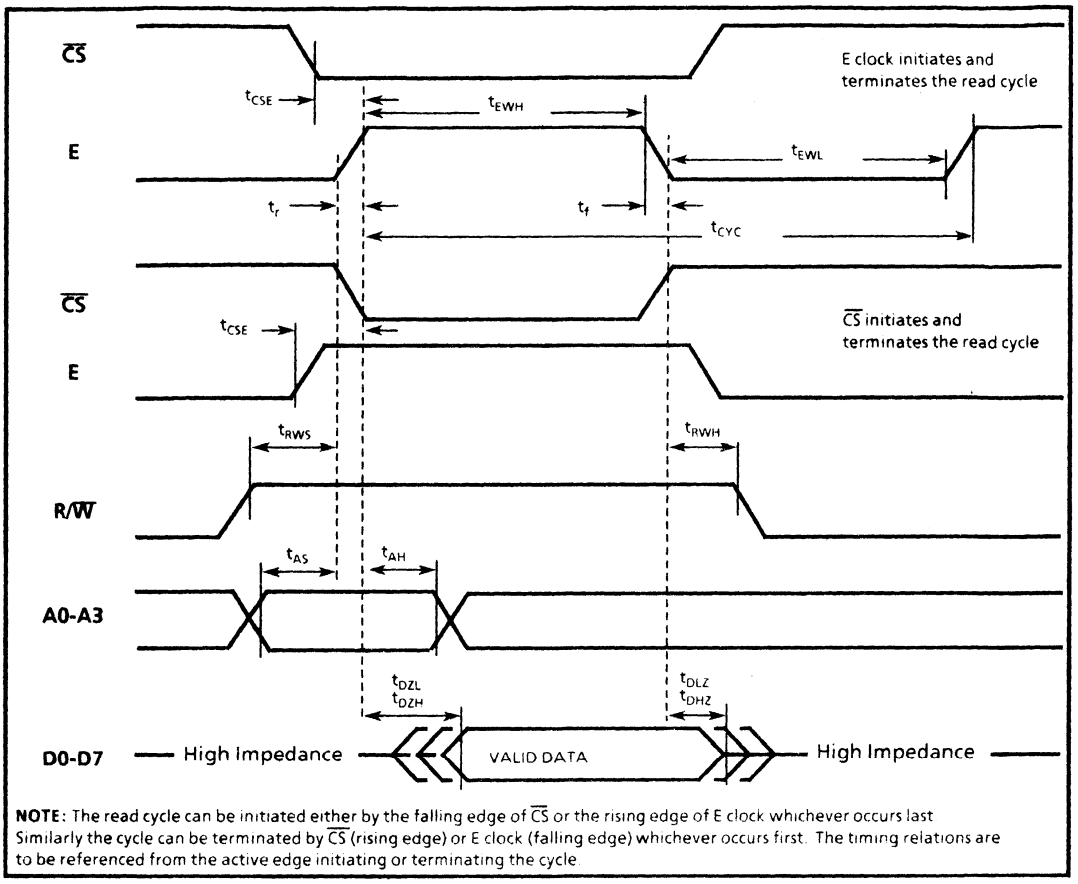
† Timing is over recommended temperature & power supply voltages (V_{DD} = 5V ± 5%, V_{SS} = 0V, T_A = –40 to 85°C)

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



NOTE: The write cycle can be initiated either by the falling edge of $\overline{CS}$ or the rising edge of E clock whichever occurs last. Similarly the cycle can be terminated by $\overline{CS}$ (rising edge) or E clock (falling edge) whichever occurs first. The timing relations are to be referenced from the active edge initiating or terminating the cycle.

Figure 2. Timing Information for MPU Write



NOTE: The read cycle can be initiated either by the falling edge of $\overline{CS}$ or the rising edge of E clock whichever occurs last. Similarly the cycle can be terminated by $\overline{CS}$ (rising edge) or E clock (falling edge) whichever occurs first. The timing relations are to be referenced from the active edge initiating or terminating the cycle.

Figure 3. Timing Information for MPU Read

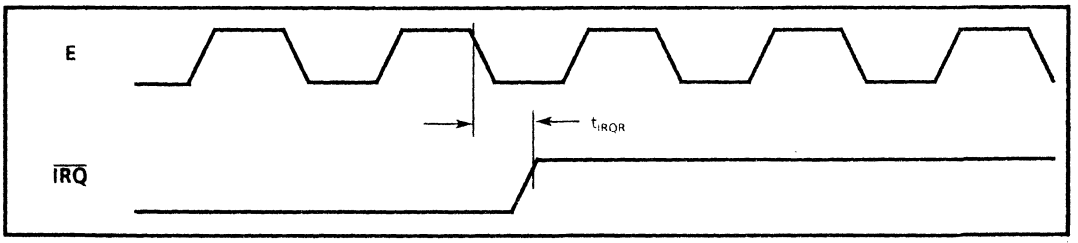


Figure 4. Interrupt Request Release Time

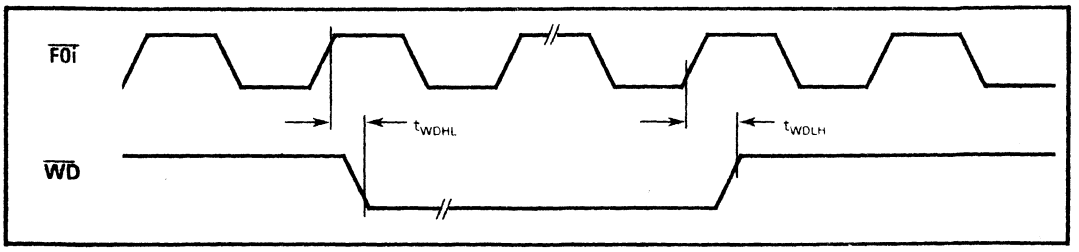


Figure 5. Watchdog Timer Input and Output

AC Electrical Characteristics† – Serial Port, WD Timer and IRQ Release Time (Figures 4, 5, 6, and 7)

Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Interrupt request release time	t_{IRQR}		500		ns	Test load circuit 2 (Fig. 11)
2		$\overline{WD}$ output delay HIGH to LOW	t_{WDHL}		80		ns	Test load circuit 1 (Fig. 11)
3		$\overline{WD}$ output delay LOW to HIGH	t_{WDLH}		80		ns	Test load circuit 1 (Fig. 11)
4		TEOP/REOP output delay	t_{EOPD}			80	ns	Test load circuit 1 (Fig. 11)
5		TEOP/REOP output hold time	t_{EOPH}			80	ns	Test load circuit 1 (Fig. 11)
6		CDSTo delay from CKi	t_{STOD}			120	ns	Test load circuit 1 (Fig. 11)
7		CDSTi set up time	t_{STIS}	30			ns	
8		CDSTi hold time	t_{STIH}	50			ns	

† Timing is over recommended temperature & power supply voltages (V_{DD} = 5V ± 5%, V_{SS} = 0V, T_A = −40 to 85°C)

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

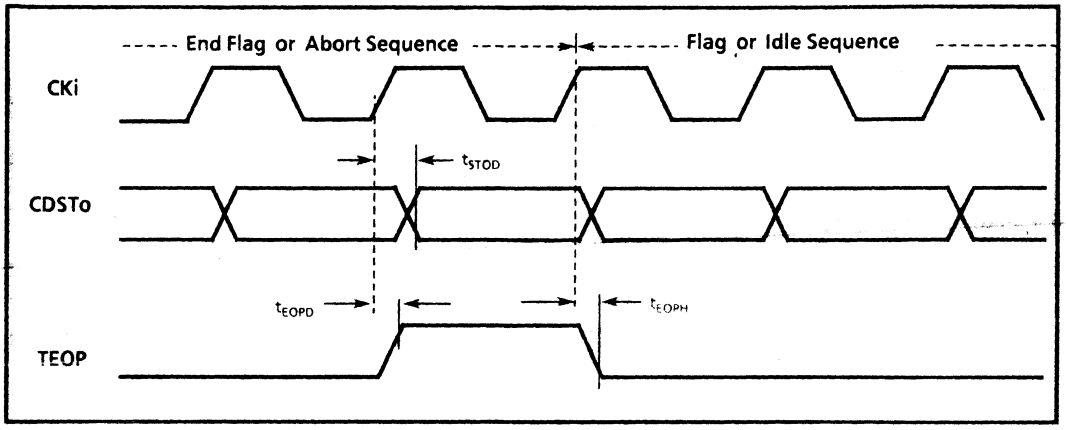


Figure 6. Serial Port Output and TEOP

Note: The frequency of the clock input CKi is assumed to be at the output bit rate. However, it can be at twice the bit rate in the Internal Timing Mode.

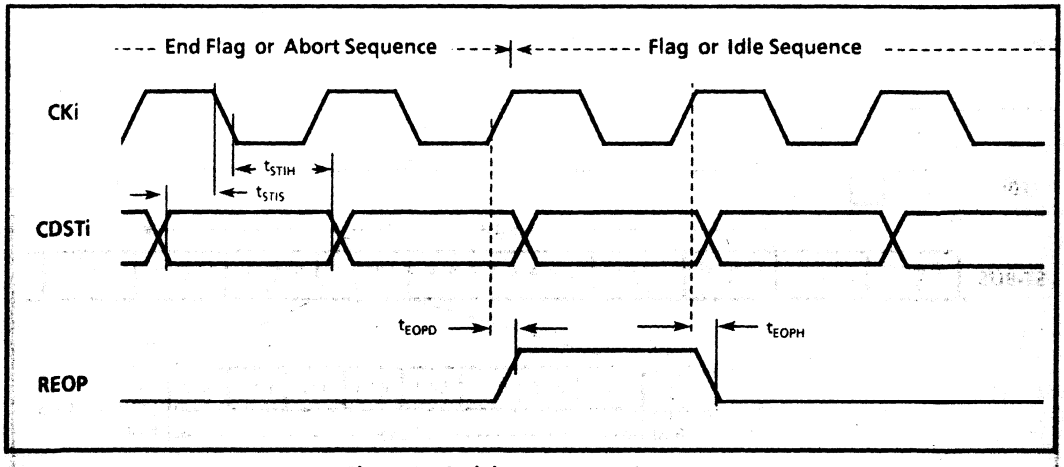


Figure 7. Serial Port Input and REOP

Note: The frequency of the clock input CKi is assumed to be at the output bit rate. However, it can be at twice the bit rate in the Internal Timing Mode.

AC Electrical Characteristics† – Serial Port in External Timing Mode (Figure 8)

Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Clock period on CKi pin	t_{CEX}	400			ns	
2	CKi transition time	t_T		20		ns	
3	$\overline{TxCEN}/\overline{RxCEN}$ set-up time	t_{CENS}	40			ns	
4	$\overline{TxCEN}/\overline{RxCEN}$ hold time	t_{CENH}	40			ns	
5	CDSTi set-up time	t_{STiS}	30			ns	
6	CDSTi hold time	t_{STiH}	50			ns	
7	CDSTo delay	t_{SToZL} t_{SToZL}			120	ns	Test load circuit 1 (Fig. 11) C_L = 150pF
8	CDSTo disable time	t_{SToLZ} t_{SToHZ}			60	ns	Test load circuit 3 (Fig. 11)

† Timing is over recommended temperature & power supply voltages (V_{DD} = 5V ± 5%, V_{SS} = 0V, T_A = -40 to 85°C)

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

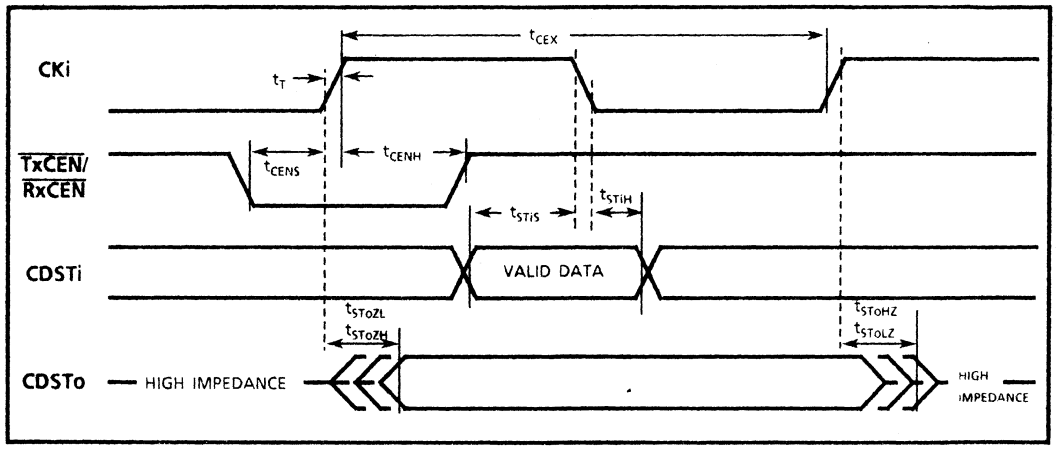


Figure 8. Serial Port Input and Outputs in External Timing Mode

Note: The frequency of the clock input (CKi) should be at the output bit rate in the External Timing Mode.

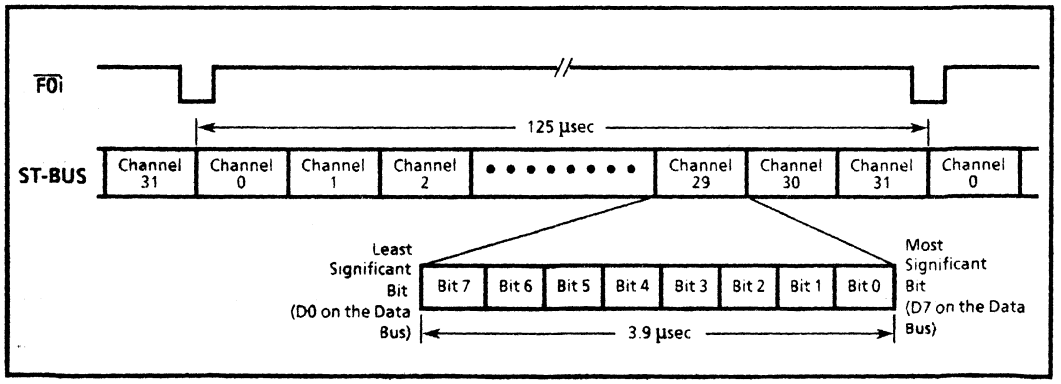


Figure 9. ST-BUS Format

AC Electrical Characteristics† – Serial Port in Internal Timing Mode (Figure 10)

Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Frame Pulse ($\overline{F0i}$) width	t_{F0iW}	100			ns	
2	Frame Pulse ($\overline{F0i}$) set up time	t_{F0iS}	50			ns	See note 3.
3	Frame Pulse ($\overline{F0i}$) hold time	t_{F0iH}	50			ns	See note 3.
4	CDSTo delay from clock input	t_{STOZL} t_{STOZH}			120	ns	Test load circuit 1 (Fig. 11)
5	CDSTi set up time	t_{STiS}	30			ns	
6	CDSTi hold time	t_{STiH}	50			ns	
7	C2i clock period	t_{C2i}	400			ns	
8	$\overline{C4i}$ clock period	t_{C4i}	200			ns	

† Timing is over recommended temperature & power supply voltages (V_{DD} = 5V ± 5%, V_{SS} = 0V, T_A = −40 to 85°C)

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

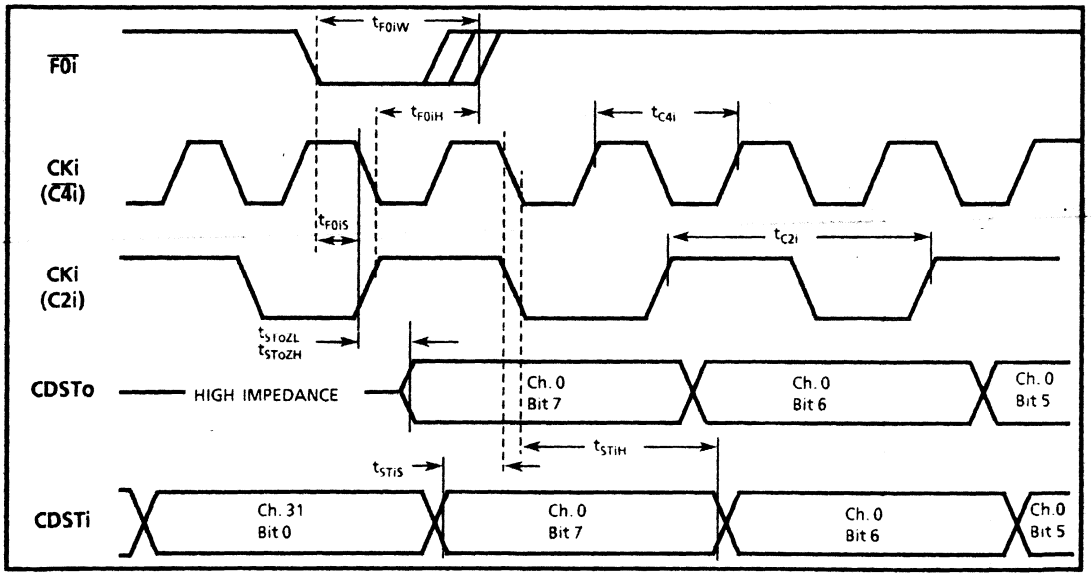


Figure 10. Serial Port Input and Output in ST-BUS Format (Internal Timing Mode)

Note: 1. Channels 0 to 4 can only be active on CDSTi and CDSTo in the Internal Timing Mode.

2. Clock input CKi can be either of the ST-BUS clocks C2i (2.048MHz) or $\overline{C4i}$ (4.096 MHz) in the Internal Timing Mode.

3. The Frame Pulse set up and hold time measurements are to be referenced from the falling edge of $\overline{C4i}$ or the rising edge of C2i depending on the clock selected.

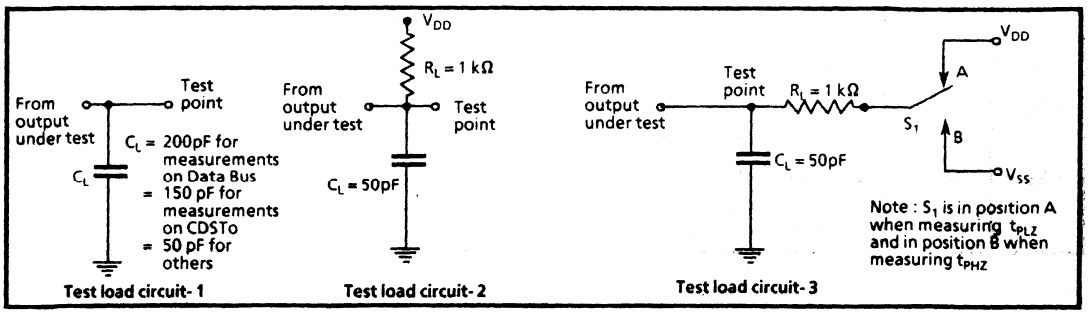


Figure 11. Test Load Circuits

Pin Description

Pin No.	Name	Description
1	$\overline{TxCEN}$	**Transmit Clock Enable** - This active LOW input enables the transmit section in the External Timing Mode. When LOW, CDSTo is enabled and when HIGH, CDSTo is in high impedance state. If the Protocol Controller is in the Internal Timing Mode, this input is ignored.
2	$\overline{RxCEN}$	**Receive Clock Enable** - This active LOW input enables the receive section in the External Timing Mode. When LOW, CDSTi is enabled and when HIGH, the clock to the receive section is inhibited. If the Protocol Controller is in the Internal Timing Mode, this input is ignored.
3	CDSTo	**C and D channel Output in ST-BUS format** - This is the serial formatted data output from the transmitter in NRZ form. It is in ST-BUS format if the Protocol Controller is in Internal Timing Mode with the data in selected time-slots (0,2,3 and 4) and the C-channel information in time-slot No. 1. If the Protocol Controller is in External Timing Mode, the formatted data is output on the rising edge of the clock (CKi) when $\overline{TxCEN}$ is LOW. If $\overline{TxCEN}$ is HIGH, CDSTo is in high impedance state.
4	CDSTi	**C and D channel Input in ST-BUS format** - This is the serial formatted data input to the receiver in NRZ form. It must be in ST-BUS format if the Protocol Controller is in Internal Timing Mode with the input data in selected time-slots (0,2,3 and 4) and the C-channel information in time-slot No.1. If the Controller is in External Timing Mode, the serial input data is sampled on the falling edge of the clock CKi when $\overline{RxCEN}$ is LOW. If $\overline{RxCEN}$ is HIGH, the clock to receive section is inhibited.
5	$\overline{WD}$	**Watch-Dog Timer output** - Normally a HIGH level output, going LOW if the watch dog timer times out or if the external reset ($\overline{RST}$) is held LOW. The $\overline{WD}$ output remains LOW as long as $\overline{RST}$ is held LOW.
6	$\overline{IRQ}$	**Interrupt Request Output (Open Drain)** - This active LOW output notifies the controlling microprocessor of an interrupt request. It goes LOW only when the bits in the Interrupt Enable Register are programmed to acknowledge the source of the interrupt as defined in the Interrupt Flag Register.
7-10	A0-A3	**Address Bus Inputs** - These bits address the various registers in the Protocol Controller. They select the internal registers in conjunction with $\overline{CS}$, R/$\overline{W}$ inputs and E Clock. (Refer to Table 2.)
11	$\overline{CS}$	**Chip Select Input** - This is an active LOW input enabling the Read or Write operation to various registers in the Protocol Controller.
12	E	**Enable Clock Input** - This input activates the Address Bus and R/$\overline{W}$ input and enables data transfers on the Data Bus.
13	R/$\overline{W}$	**Read/Write Control** - This input controls the direction of data flow on the data bus. When HIGH, the I/O buffer acts as an output driver and as an input buffer when LOW.
14	V_{SS}	Ground (0 Volt).
15-22	D0-D7	**Bi-Directional Data Bus** - These Data Bus I/O ports allow the data transfer between the HDLC Protocol Controller and the microprocessor.
23	REOP	**Receive End Of Packet (Output)** - This is a HIGH going pulse that occurs for one bit duration when a closing flag is detected on the incoming packets, or the incoming packet is aborted, or when an invalid packet of 24 or more bits is received.

Pin Description (Continued)

Pin No.	Name	Description
24	TEOP	**Transmit End Of Packet (Output) -** This is a HIGH going pulse that occurs for one bit duration when a packet is transmitted correctly or aborted.
25	CKi	**Clock Input (Bit rate clock or 2 x bit rate clock in ST-BUS format while in the Internal Timing Mode and bit rate Clock in the External Timing Mode) -** This is the clock input used for shifting in/out the formatted packets. It can be at bit rate (C2i) or twice the bit rate ($\overline{C4}$i) in ST-BUS format while the Protocol Controller is in the Internal Timing Mode. Whether the clock should be C2i (typically 2.048 MHz) or $\overline{C4}$i (typically 4.096 MHz) is decided by the BRCK bit in the Timing Control Register. If the Protocol Controller is in the External Timing Mode, it is at the bit rate.
26	$\overline{F0}$i	**Frame Pulse Input -** This is the frame pulse input in ST-BUS format to establish the beginning of the frame in the Internal Timing Mode. This is also the signal clocking the watchdog timer.
27	$\overline{RST}$	**Reset input -** This is an active LOW Schmitt Trigger input, resetting all the registers including the transmit and receive FIFOs and the watchdog timer.
28	V_{DD}	**Supply (5 Volts).**

TABLE 1.

Register Addresses

Address Bits				Registers	
A3	A2	A1	A0	Read	Write
0	0	0	0	FIFO Status	-
0	0	0	1	Receive Data	Transmit Data
0	0	1	0	Control	Control
0	0	1	1	Receive Address	Receive Address
0	1	0	0	C-Channel Control (Transmit)	C-Channel Control (Transmit)
0	1	0	1	Timing Control	Timing Control
0	1	1	0	Interrupt Flag	Watch-Dog Timer
0	1	1	1	Interrupt Enable	Interrupt Enable
1	0	0	0	General Status	-
1	0	0	1	C-Channel Status (Receive)	-

Introduction

The MT8952 HDLC Protocol Controller handles bit oriented protocol structure and formats the data as per the packet switching protocol defined in the X.25 (Level 2) recommendations of the CCITT. It transmits and receives the packeted data (information or control) serially in a format shown in Figure 12, while providing the data transparency by zero insertion and deletion. It generates and detects the flags, various link channel states and the abort sequence. Further, it provides a cyclic redundancy check on the data packets using the CCITT defined polynomial. In addition, it can generate and detect a Go Ahead sequence and recognize a single byte address in the received frame. There is also a provision to disable the protocol functions and provide transparent access to the serial bus through the parallel port.

Frame Format

All frames start with an opening flag and end with a closing flag as shown in Figure 12. Between these two flags, a frame contains the data and the frame check sequence (FCS).

FLAG	DATA FIELD	FCS	FLAG
One Byte	n BYTES ($n \geq 2$)	TWO BYTES	One Byte

Figure 12. Frame Format

Flag:

The flag is a unique pattern of 8 bits (01111110) defining the frame boundary. The transmit section generates the flags and appends them automatically to the frame to be transmitted. The receive section searches the incoming packets for flags on a bit-by-bit basis and establishes frame synchronization. The flags are used only to identify and synchronize the received frame and are not transferred to the FIFO.

Data:

The data field refers to the Address, Control and Information fields defined in the CCITT recommendations. A valid frame should have a data field of at least 16 bits. The first byte in the data field is the address of the frame. If RxAD bit in the Control Register is HIGH, the incoming packet is recognized only if the address byte matches the byte stored in the Receive Address Register or the address byte is the All-Call Address (all ONEs). The LSB of the Receive Address Register is set LOW permanently and the comparison is done only on upper seven bits of the received address byte. The address detection can be limited only to the upper six bits by setting HIGH both RA6/7 and RxAD bits in the Control Register.

Frame Check Sequence (FCS):

The 16 bits following the data field are the frame check sequence bits. The generator polynomial is:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

The transmitter calculates the FCS on all bits of the data field and transmits after the data field and before the end flag. The receiver performs a similar computation on all bits of the received data and FCS fields and the result is compared with $F0B8_{Hex}$. If it matches, the received data is assumed error free. The error status of the received packet is indicated by D7 and D6 bits in the FIFO Status Register.

Zero Insertion and Deletion:

The Protocol Controller, while sending either data from the FIFO or the 16 bits FCS, checks the transmission on a bit-by-bit basis and inserts a ZERO after every sequence of five contiguous ONEs (including the last five bits of FCS) to ensure that the flag sequence is not simulated. Similarly the receiver examines the incoming frame content and discards any ZERO directly following the five contiguous ONEs.

Abort:

The transmitter aborts a frame by sending eight consecutive ONEs. The FA bit in the Control Register along with a write operation to the Transmit Data Register enables the transmission of abort sequence instead of the byte written to the register. On the receive side, a frame abort is defined as seven or more contiguous ONEs occurring after the start flag and before the end flag of a packet. An interrupt can be generated on reception of the abort sequence using FA bit in the Interrupt Flag/Enable Registers.

Interframe Time Fill and Link Channel States

When the HDLC Protocol Controller is not sending packets, the transmitter can be in any of three states mentioned below depending on the status of the IFTF0 and IFTF1 bits in the Control Register. These bits are also used to disable the protocol function to provide the transparent parallel access to the serial bus through the microprocessor port.

Idle state:

The Idle state is defined as 15 or more contiguous ONEs. When the HDLC Protocol Controller is observing this condition on the receiving channel, the Idle bit in the General Status Register is set HIGH. On the transmit side, the Protocol Controller ends the Idle state when data is loaded into the transmit FIFO.

Interframe time fill state:

The Protocol Controller transmits continuous flags ($7E_{Hex}$) in Interframe time fill state and ends this state when data is loaded into the transmit FIFO.

Go Ahead state:

Go Ahead is defined by the 9 bit sequence 011111110 ($7F_{Hex}$ followed by a ZERO), and hence contiguous 7F's appear as Go Aheads. Once the transmitter is in 'Go Ahead' state, it will continue to remain so even after the data is loaded into the FIFO. This state can only be changed by setting the IFTF bits in the Control Register to something other than 'GO Ahead'. The reception of this sequence is indicated by GA bit in the General Status Register and the Protocol Controller can generate an interrupt if enabled to do so by the GA bit in the Interrupt Enable Register.

Transparent Data Transfer State:

The Protocol Controller, in this state, disables the protocol functions defined earlier and provides bi-directional access to the serial bit streams through the parallel port. Like other states, the transparent data transfer can be selected in both timing modes.

Invalid Frames

Any frame shorter than 32 bits between the opening and closing flags (corresponding to 16 bits of data and 16 bits FCS) is considered invalid. The Protocol Controller ignores the frame only if the frame length is less than 24 bits between the flags. For frames of length 24 to 32 bits, it transfers the data field to FIFO and tags it as having bad FCS in the FIFO Status Register.

Functional Description

The functional block diagram of the HDLC Protocol Controller is shown in Figure 1. It has two ports. The serial port transmits and receives formatted data packets and the parallel port provides a microprocessor interface for access to various registers in the Protocol Controller.

The serial port can be configured to operate in two modes depending on the IC bit in the Timing Control Register. It can transmit/receive the packets on selected timeslots in ST-BUS format or it can, using the enable signals ($\overline{TxCEN}$ and $\overline{RxCEN}$), transmit/receive the packets at a bit rate equal to CKi clock input.

The microprocessor port allows parallel data transfers between the Protocol Controller and a 6800/6809 system bus. This interface consists of Data Bus (D0-D7), Address Bus (A0-A3), E Clock, Chip Select ($\overline{CS}$) and $R/\overline{W}$ control. The microprocessor can read and write to the various registers in the Protocol Controller. The addresses of these registers are given in Table 2. The $\overline{IRQ}$ is an open drain, active LOW output indicating an interrupt request to CPU. Control and monitoring of many different interrupts that may originate from the protocol controller is implemented by the Interrupt Flag Register (IFR) and the Interrupt Enable Register (IER). Specific events have been described that set a bit HIGH in the Interrupt Flag Register. Such an event does not necessarily interrupt the CPU. To assert an interrupt (pull $\overline{IRQ}$ output LOW) the bit in IER that coincides with the Interrupt Flag Register must be set HIGH. The IRQ bit in the General Status Register is the complement of $\overline{IRQ}$ pin status. If an interrupt is asserted, this bit will be set HIGH otherwise it will be LOW.

TEOP and REOP Outputs:

The HDLC Protocol Controller provides two separate signals TEOP & REOP indicating the end of packet transmitted and received respectively. TEOP is a HIGH going pulse for one bit duration asserted during the last bit of the closing flag or Abort sequence of the transmit packet. REOP is also a HIGH going pulse occurring for one bit period when a closing flag is received or an incoming packet is aborted or an invalid packet of 24 or more bits is detected. However, REOP is not generated for invalid packets of length less than 24 bits. These 'end of packet' signals are useful in multiplexing several data links on to a single HDLC Protocol Controller.

Timing Modes

There are two timing modes the Protocol Controller can be run in. These timing modes refer only to the configuration of the serial port and are not related to the microprocessor port.

Internal Timing Mode

The Internal Timing Mode is intended for an easy interface to various products using ST-BUS architecture, particularly MITEL's Digital Network Interface Circuit (DNIC - MT8972). The data/packets are shifted in/out serially in ST-BUS format using the timing signals $\overline{F0i}$ and C2i/$\overline{C4i}$. In addition to framing the data, the Protocol Controller reserves one channel (channel-1) on the ST-BUS for carrying control information (C-channel) and this time-slot can not be used for the packetized data. While the Protocol Controller is in the Internal Timing Mode, the clock input CKi can be either at the bit rate or at 2 x bit rate depending on the BRCK bit in the Timing Control Register as shown in Table 2. The Protocol

BRCK bit	CKi input	Output data rate
0	4.096 MHz/$\overline{C4i}$	2.048 Mbps
1	2.048 MHz/C2i	2.048 Mbps

TABLE 2. Output Bit Rate In Internal Timing Mode

Controller uses the ST-BUS timing signals $\overline{F0i}$ and C2i/$\overline{C4i}$, and enables the transmitter and receiver sections in the appropriate timeslots as determined by TCO-TC3 bits in the Timing Control Register. The $\overline{TxCEN}$ and $\overline{RxCEN}$ inputs are ignored in this mode.

C-Channel Interface

This is a seperate control channel (C-channel) interface relevant only in the Internal Timing Mode. The data stored in the C-Channel Control Register is shifted out during the channel-1 timeslot of the outgoing ST-BUS (CDSTo) and the C1EN bit in the Timing Control Register enables the transmission. The transmission of C-Channel is independent of packet/data transmission. The data received on channel-1 of the incoming ST-BUS (CDSTi) is shifted into the C-Channel Status Register independently and it is updated continuously.

Both the C-channel registers are accessible by the accompanying CPU through the parallel port.

External Timing Mode

In the External Timing Mode, the transmit and receive sections are enabled independently by $\overline{TxCEN}$ and $\overline{RxCEN}$ control inputs and the formatted data packets are shifted in/out serially at a rate equal to the clock frequency on CKi. The output is transmitted on the rising edge and the receiver samples the input on the falling edge of the clock. The $\overline{TxCEN}$ and $\overline{RxCEN}$ controls are independent and asynchronous and have effect only after the current bit in the packet is transmitted/received.

Although the protocol controller provides the packetized data on a limited number of channels on the ST-BUS while operating in the Internal Timing Mode, it can packetize the data on any or all the channels of the ST-BUS if it is operated in the External Timing Mode with appropriate enable signals on $\overline{TxCEN}$ and $\overline{RxCEN}$.

Transparent Data Transfer

By setting the IFTF bits in the Control Register appropriately, the protocol functions can be disabled. This provides a bi-directional access to the serial port through the microprocessor interface, with 19 byte deep FIFO in each direction. The transparent data transfer facility functions in bytewide format and is available in both timing modes except when the timing control bits are set for 1bit/frame during the Internal Timing Mode.

The transmit data is shifted out serially on CDSTo and the operation being bytewide, only the least significant bits of each byte loaded are transmitted, if the timing control bits are set to select 2, 6 or 7 bits/frame. When the transmit FIFO is empty, the last byte or the portion the last byte, written to the FIFO is transmitted repeatedly. Similarly the serial data on CDSTi is shifted in and converted to bytewide format. In case the timeslot selected is 2, 6 or 7 bits/frame, the reception involves only the most significant bits of each byte.

It should be noted that none of the protocol related status or interrupt bits are applicable in transparent data transfer state. However, the FIFO related status and interrupt bits are pertinent and carry the same meaning as they do while performing the protocol functions.

Watchdog Timer

This is a fixed eleven stage binary counter with $\overline{F0i}$ as the input and $\overline{WD}$ as the output from the last stage. This counter can be reset either by the external input ($\overline{RST}$) or by writing XXX0 1010 to the Watchdog Timer Register. The $\overline{WD}$ output is normally HIGH and if the WD Timer Register is not written within 2^{10} cycles of $\overline{F0i}$ input after it is reset, the $\overline{WD}$ output will go LOW for a period of 2^{10} cycles of $\overline{F0i}$. Even though the $\overline{F0i}$ input is not

required for formatting data in the External Timing Mode, it is necessary for the operation of the watchdog timer.

Order of Bit Transmission/Reception

The Least Significant Bit (LSB) corresponding to D0 on the data bus is transmitted first on the serial output (CDSTo). On the receiving side, the first bit received on the serial input (CDSTi) is considered as the LSB and placed on D0 of the data bus.

Registers

There are several registers in the HDLC Protocol Controller accessible to the associated microprocessor via the data bus. The addresses of these registers are given in Table 2 and their functional details are given below.

FIFO Status Register (Read) :

This register (Figure 13) indicates the status of transmit and receive FIFOs and the received byte as described below.

D7	D6	D5	D4	D3	D2	D1	D0
Rx Byte Status		Rx FIFO Status		Tx FIFO Status		LOW	LOW

Figure 13. FIFO Status Register

Rx Byte Status: These two bits (D7 and D6) indicate the status of the received byte ready to be read from the receive FIFO. The status is encoded as shown in Table 3.

Rx Byte Status Bits		Status
D7	D6	
0	0	Packet Byte
0	1	First Byte
1	0	Last Byte (Good FCS)
1	1	Last Byte (Bad FCS)

TABLE 3. Received Byte Status

Rx FIFO Status: These bits (D5 and D4) indicate the status of receive FIFO as given by Table 4.

Rx FIFO Status Bits		Status
D5	D4	
0	0	Rx FIFO Empty
0	1	Less than or equal to fourteen bytes
1	0	Rx FIFO Full
1	1	Greater than or equal to fifteen bytes

TABLE 4. Receive FIFO Status

Tx FIFO Status: These two bits (D3 and D2) indicate the status of transmit FIFO as shown in Table 5.

Tx FIFO Status Bits		Status
D3	D2	
0	0	Tx FIFO Full
0	1	Greater than or equal to five bytes
1	0	Tx FIFO Empty
1	1	Less than or equal to four bytes

TABLE 5. Transmit FIFO Status

Receive Data Register (Read) :

Reading the Receive Data Register (Figure 14) puts the first byte from the receive FIFO on the data bus. The first bit of the data received on the serial input (CDSTi) is considered to be the LSB and is available on D0 of the data bus.

Transmit Data Register (Write) :

Writing to Transmit Data Register (Figure 15) puts the data present on the data bus into the transmit FIFO. The LSB (D0) is transmitted first.

D7	D6	D5	D4	D3	D2	D1	D0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Figure 14. Receive Data Register

D7	D6	D5	D4	D3	D2	D1	D0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Figure 15. Transmit Data Register

Control Register (Read/Write) :

The Control Register (Figure 16) is used for general purpose control of the HDLC Protocol Controller. The bits contained in this register and their functions are described below.

D7	D6	D5	D4	D3	D2	D1	D0
TxEN	RxEN	RxAD	RA6/7	IFTF1	IFTF0	FA	EOP

Figure 16. Control Register

TxEN -Transmit Enable: When set HIGH, this bit enables the transmitter and when LOW, disables it setting the serial output (CDSTo) to high impedance state. If the transmitter is disabled during the transmission of a packet using this bit, the Protocol Controller will wait untill the completion of the packet and closing flag is transmitted or the packet is aborted before setting the output (CDSTo) to high impedance state. Thus TxEN bit controls the transmission packet by packet unlike $\overline{\text{TxCEN}}$ input (pin 1) which controls it bit-by-bit. However, if the Protocol Controller is in transparent data transfer state, the transmission will be stopped within two bit periods (maximum) and set the output to high impedance state.

RxEN - Receive Enable: This bit enables the receiver when set HIGH and disables it when LOW. If this bit goes LOW during the reception of the packet, the receiver can only be disabled after the current packet and its closing flag are received or an abort is detected. Thus RxEN bit controls the receiver section packet by packet unlike $\overline{\text{RxCEN}}$ input (pin 2) which controls it bit-by-bit. However, if the Protocol Controller is in transparent data transfer state, the receiver will be disabled immediately.

RxAD - Receive Address Detect: This bit when set HIGH, enables the address detection for the received packets. This causes the receiver to recognize only those packets having a unique address as programmed in the Receive Address Register or if the address byte is the All-Call address (all ONEs). The address comparison is done only on seven bits (compatible to the first byte of the address field defined in LAPD-CCITT) and an All-Call is defined as all ONEs in upper seven bits of the received address field. If RxAD is LOW, the address detection is disabled and every valid packet is recognized.

RA6/7 - Receive Address Six/Seven bits: This bit, when set HIGH, limits the address detection only to the upper six bits of the received address byte (last 6 bits of received address field) and when LOW, allows the address comparison on seven bits. An "all call", in this case is defined as all ONEs in the upper six bits only. RA6/7 is ignored if the address detection is disabled (RxAD = 0).

IFTF0 and IFTF1 - Interframe Time Fill: Setting these bits according to the table below (Table 6) causes the transmitter to be in one of the active or idle states or allows the Protocol Controller to be in the transparent data transfer state.

IFTF Bits		Result
IFTF1	IFTF0	
0	0	Idle state (All ONEs)
0	1	Interframe Time Fill state (Continuous Flags)
1	0	Transparent Data Transfer
1	1	Go Ahead state (Continuous $7F_{HEX}$)

TABLE 6. Interframe Time Fill Bits

FA - Frame Abort: When set HIGH, this bit 'tags' the next byte written to the transmit FIFO and causes an abort sequence (eight ONEs) to be transmitted when it reaches the bottom of the FIFO. The abort sequence will be transmitted instead of the byte that was tagged. The FA bit is cleared to ZERO upon writing the data to the transmit FIFO. As a result, a

'read' of this register bit will not reflect the last data written to it.

EOP - End Of Packet: Writing a ONE to this bit 'tags' the next byte written to the transmit FIFO to indicate that it is the last data byte of the packet. This bit is cleared to ZERO upon writing the data to the transmit FIFO. As a result, a read of this register bit will not indicate the last data written to it.

Receive Address Register (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0

Figure 17. Receive Address Register

The data in this register (Figure 17) defines the unique address for the HDLC Protocol Controller. If address recognition is enabled using the RxAD and RA6/7 bits in the Control Register, an incoming packet is recognized only if its address byte (seven or six most significant bits) matches the corresponding bits in this register or if the address is an "all-call". The LSB of the Receiver Address Register is set LOW permanently and the address comparison is done only on remaining bits of the register.

C-Channel Control Register (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure 18. C-Channel Control Register

The data written to this register (Figure 18) is transmitted on channel-1 slot of the outgoing ST-BUS (CDSTo), when enabled by C1EN bit in the Timing Control Register. This feature can only be used when the HDLC Protocol Controller is in the Internal Timing Mode.

Timing Control Register (Read/Write):

The Timing Control Register (Figure 19) controls the timing mode and other related operations and provides a software reset to the Protocol Controller. The various bits in this register are described below:

D7	D6	D5	D4	D3	D2	D1	D0
RST	IC	C1EN	BRCK	TC3	TC2	TC1	TC0

Figure 19. Timing Control Register

RST - Reset: When this bit is set HIGH, all the registers in the HDLC Protocol Controller are reset and the data in the FIFOs is lost. This is equivalent to the external reset with the exception that the RST bit does not affect itself nor the Watchdog Timer Register and $\overline{WD}$ output.

IC - Internal Control: When this bit is cleared to ZERO, the Protocol Controller is in the External Timing Mode. The transmit and receive sections are enabled by the inputs $\overline{TxCEN}$ and $\overline{RxCEN}$ respectively and $\overline{F0i}$ is used only for the watchdog timer operation. When this bit is a ONE, the Protocol Controller is in the Internal Timing Mode. The transmit and receive sections are enabled by the internally generated timings derived from the inputs CKi and $\overline{F0i}$. The $\overline{F0i}$ input defines the beginning of a frame (Figure 9) and the transmitter and receiver sections are enabled in the time-slots as determined by the bits TCO-TC3. The inputs $\overline{TxCEN}$ and $\overline{RxCEN}$ are ignored in this mode.

C1EN - Channel-1 Enable: When HIGH, it enables the transmission of C-channel information on channel-1 time-slot of the outgoing ST-BUS (CDSTo) and when LOW, puts CDSTo into high impedance state during that period. However, the C-channel information is received independently and the C-channel Status Register is updated continuously. Note that C1EN has relevance only during the Internal Timing Mode.

BRCK- Bit Rate Clock: This bit is used during the Internal Timing Mode to select the clock rate and ignored if the Protocol Controller is in the External Timing Mode. It should be set HIGH if the input clock (CKi) is at the bit rate (C2i) and should be LOW for the clock input at 2 x bit rate ($\overline{C4i}$). In both cases, the clock should be properly phase related to $\overline{F0i}$ as shown in Figure 10.

TC0-TC3 - Timing Control Bits: In the Internal Timing Mode the transmitter and the receiver sections are enabled during the times defined by the Timing Control Bits TC0-TC3 (Table 7). This applies only to the ST-BUS channels 0, 2, 3 and 4 carrying the packets or transparent data (channel-1 pertains to C-channel information). The output CDSTo is put into high impedance state during the remaining time intervals not enabled by these bits.

Timing Control Bits				ST-BUS Channel Number	Bits /Frame
TC3	TC2	TC1	TC0		
X	0	0	0	0	1
X	0	0	1	0	2
0	0	1	0	0	6
1	0	1	0	0	7
X	0	1	1	2	8
X	1	0	0	3	8
X	1	0	1	4	8
X	1	1	0	2 and 3	16
X	1	1	1	2, 3 and 4	24

X : Don't Care

TABLE 7. Timing Control Bits

Interrupt Flag Register (Read):

Reading the Interrupt Flag Register (Figure 20) puts the interrupt status bits on the data Bus. This register is reset when it is read and a particular bit will not be set until its particular condition occurs again. The functional details of each bit are provided below:

D7	D6	D5	D4	D3	D2	D1	D0
GA	EOPD	Tx DONE	FA	Tx 4/19 FULL	Tx URUN	Rx 15/19 FULL	Rx OFLW

Figure 20. Interrupt Flag Register

GA - Go Ahead: This bit when set HIGH, indicates the detection of 'go ahead' sequence on the incoming data stream (CDSTi).

EOPD - End of Packet Detect: A HIGH on this bit confirms the reception of an 'end of packet' flag, an abort sequence or an invalid packet of 24 or more bits on the incoming data stream (CDSTi).

TxDONE - Transmitter Done : This bit, when HIGH, indicates that the packet transmission is complete and the Transmit FIFO is empty. The falling edge of TEOP output causes this interrupt status bit to be set HIGH if the FIFO is empty.

FA - Frame Abort: This bit is set HIGH to indicate that a frame abort has been detected on the incoming data stream.

Tx 4/19 FULL - Transmit FIFO 4/19 full: This bit if set HIGH, indicates that the transmit FIFO has only 4 bytes remaining in it and another 15 bytes could be loaded. This bit has significance only when the transmit FIFO is being depleted and not when it is getting loaded.

Tx URUN - Transmit FIFO underrun: This bit when HIGH, identifies that the transmit FIFO is empty without the Protocol Controller being given the 'end of packet' indication. This indicates that the transmit FIFO has underrun and the Protocol Controller will transmit an abort sequence automatically.

Rx15/19 FULL - Receive FIFO 15/19 full: This bit when HIGH, confirms that the receive FIFO has 15 bytes in it and it can receive four more bytes.

Rx OFLW - Receive FIFO overflow: This bit when set HIGH, indicates that the receive FIFO is full and a 'write' occurred indicating an overflow. The byte causing this and all the subsequent bytes written while the FIFO is in this state are lost.

Watchdog Timer Register (Write):

The Watchdog Timer Register operates in conjunction with the Watchdog Timer and the $\overline{WD}$ output. Writing the code of XXX0 1010 in the register resets the WD timer. If the register is not re-written within 2^{10} cycles of $\overline{F0i}$ after resetting the timer, the $\overline{WD}$ output goes LOW. This register serves the sole purpose of resetting the timer and hence relevant only if it is written with the above data.

Interrupt Enable Register (Read/Write):

This register enables/disables the interrupts as specified in the Interrupt Flag Register (IFR). Setting HIGH the appropriate bits in this register (IER) enables the associated interrupt source. However, the masked bits in the IFR are still valid but they do not cause the $\overline{IRQ}$ output to go LOW. The description of the bits enabling the various interrupts is identical to those of the Interrupt Flag Register.

General Status Register (Read):

This register (Figure 21) contains the general status information on the Protocol Controller.

D7	D6	D5	D4	D3	D2	D1	D0
Rx OFLW	Tx URUN	GA	ABRT	IRQ	IDLE	LOW	HIGH

Figure 21. General Status Register

Rx OFLW - Receive FIFO overflow: This bit, if set HIGH, indicates that the receive FIFO has overflowed. The byte causing this and all the subsequent bytes written while the FIFO is in this state are lost. Note that this bit is the same as the Rx OFLW bit in Interrupt Flag Register (IFR) and can only be cleared by reading the IFR.

Tx URUN - Transmit FIFO Underrun: When HIGH, this bit indicates that the transmit FIFO has underrun. Under this condition the packet being transmitted is aborted. This bit is the same as the Tx URUN bit in the Interrupt Flag Register (IFR) and can only be cleared when the IFR is read.

GA - Go Ahead: This bit is set HIGH if a 'go ahead' is received on the incoming data stream and is cleared when the Interrupt Flag Register is read. This bit is same as the GA bit in the IFR.

ABRT - Abort: The reception of contiguous seven ONEs on incoming data, sets this bit HIGH and reading the General Status Register, clears it.

IRQ - Interrupt Request: This bit refers to the status of the interrupt request output from the Protocol Controller. If HIGH, it indicates that the $\overline{IRQ}$ (pin 6) output is LOW and vice versa.

IDLE - Idle Channel: This bit, if set HIGH, identifies that the receiver is detecting an idle channel at its input (minimum 15 ONEs).

C-Channel Status Register (Read):

D7	D6	D5	D4	D3	D2	D1	D0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Figure 22. C-Channel Status Register

The C-Channel Register (Figure 22) continuously stores the data received during the channel-1 timeslot of the incoming ST- BUS (CDSTi) during the Internal Timing Mode of the Protocol Controller.

Transmit Operation

After a reset, which the external circuitry should provide upon power up, the transmit section is disabled. Before enabling this section, the timing should be set up. On reset, the serial port is set to External Timing Mode. In case this is not desired, the Timing Control Register should be written to with the appropriate data. Once in the correct timing mode, the Transmit Enable (TxEN) bit in the Control Register can be set. Now that the transmitter is enabled it will be in the Idle channel state. If any other channel state or the transparent data transfer facility is required, the IFTF bits in the Control Register should be set accordingly.

Normal Packets:

To start a packet, the data is written into the transmit FIFO starting with the address field. All the data must be written to the FIFO in a bytewide manner. When the data is detected in the transmit FIFO, the protocol controller will proceed in one of the following ways:

If the transmitter is in idle state, the present byte of eight ONEs being transmitted is completed and then followed by a start flag and subsequently the data in the transmit FIFO is transmitted.

If the transmitter is in the interframe time fill state, the flag presently being transmitted is finished and then another start flag is transmitted before transmitting the data from the transmit FIFO.

If the transmitter is in go ahead state, it continues to be in that state even after the data is loaded into the FIFO. Only when the IFTF bits are set to choose something other than go ahead will the data be transmitted.

If the transmitter is in transparent data transfer state, the protocol functions are disabled and the data in the transmit FIFO is transmitted on CDSTo.

To indicate that the particular byte is the last byte of the packet, the EOP bit in the Control Register must be set before the last byte is written into the transmit FIFO. The EOP bit is cleared automatically when the data byte is written to the FIFO. After the transmission of the last byte in the packet, the frame check sequence (16 bits) is sent followed by a closing flag. If there is any more data in the transmit FIFO, another flag is transmitted followed by the new data. In case of no data in the FIFO, the transmitter assumes the selected link channel state.

During the transmission of either the data or the frame check sequence, the Protocol Controller checks the transmitted information on a bit by bit basis and inserts a ZERO after every sequence of five consecutive ONEs.

Transmit Underrun:

A transmit underrun occurs when the last byte loaded into the transmit FIFO was not 'flagged' with the 'end of packet' (EOP) bit and there are no more bytes in the FIFO. In such a situation, the Protocol Controller transmits the abort sequence (eight ONEs) and moves to the selected link channel state.

Abort Transmission:

If it is desired to abort the packet currently being loaded into the transmit FIFO, the next byte written to the FIFO should be 'flagged' to cause this happen. The FA bit of the Control Register must be set HIGH, before writing the next byte into the FIFO. This bit is cleared automatically once the byte is written to the FIFO. When the 'flagged' byte reaches the bottom of the FIFO, a frame abort sequence is sent instead of the byte and the transmitter operation returns to normal.

Go Ahead Transmission:

By setting the IFTF bits in the Control Register appropriately the transmitter can be made to send the Go Ahead sequences when the Protocol Controller is not sending the packets. Since the go ahead is defined as 011111110, contiguous $7F_{Hex}$' s appear as go aheads. As long as the IFTF bits are set to choose go aheads, the transmitter will send them even if data is subsequently loaded into the FIFO. Only when the IFTF bits are set to select something other than go aheads, will the data be transmitted.

C-Channel Transmission:

By setting the C1EN bit in the Timing Control Register HIGH, the information loaded in the C-Channel Control Register can be transmitted over channel-1 timeslot of the outgoing ST-BUS (CDSTo). This is available only during the Internal Timing Mode of the Protocol Controller.

Transparent Data Transfer:

The IFTF bits in the Control Register can be set to provide transparent data transfer disabling the protocol functions. The transmitter no longer generates the Flag, GA, Abort and Idle sequences nor does it insert the zeros and calculate the FCS . It operates in both timing modes in bytewide manner and transmits data serially on CDSTo. If the Protocol Controller is in the Internal Timing Mode and the Timing Control bits are set to select 2, 6 or 7 bits/frame, the corresponding least significant bits of every byte loaded into the transmit FIFO are only transmitted. The transparent data transfer facility is not available when the Timing Control bits are set for 1 bit/frame. In case the FIFO is empty, the last byte or the portion of the last byte, written to the FIFO is transmitted repeatedly. Note that the transparent data transfer can be disabled immediately in software (unlike during the transmission of packets) using TxEN bit in the Control Register.

The operation of the transmitter is similar in the External Timing Mode.

Receive Operation

After a reset on power up, the receive section is disabled. Timing set up considerations are similar to that of the transmit section. Address detection is also disabled when a reset occurs. If address detection is required, the Receiver Address Register is loaded with the desired address and the RxAD bit in the Control Register is set HIGH. The receive section can then be enabled by RxEN bit in the Control Register.

Normal Packets:

After initialization as explained above, the serial data starts to be clocked in and the receiver checks for the idle channel and flags. If an idle channel is detected, the 'Idle' bit in the General Status Register is set HIGH. Once a flag is detected, the receiver synchronizes itself in a bytewide manner to the incoming data stream. The receiver keeps resynchronizing to the flags until an incoming packet appears. The incoming packet is examined on a bit-by-bit basis, inserted zeros are deleted, the FCS is calculated and the data bytes are written into the receive FIFO. However, the FCS and other control characters like the flag, abort etc., never appear in the FIFO. If the address detection is enabled, the first byte following the flag is compared to the byte in the Receive Address Register and to All-Call address. If a match is not found, the entire packet is ignored and nothing is written to the FIFO. If the incoming address byte is valid, the packet is received in normal fashion. All the bytes written to the receive FIFO are flagged with two status bits. The status bits are found in the FIFO status register and indicate whether the byte to be read from the FIFO is the first byte of the packet, the middle of the packet, the last byte of the

packet with good FCS or the last byte of the packet with bad FCS. This status indication is valid for the byte to be read from the receive FIFO.

The incoming data is always written to the FIFO in a bytewide manner. However, in the event of data sent not being a multiple of eight bits, the software associated with the receiver should be able to pick the data bits from the MSB positions of the last byte in the received data written to the FIFO. The Protocol Controller does not provide any indication as to how many bits this might be.

Invalid Packets:

If there are less than 24 data bits between the opening and closing flags, the packet is considered invalid and the data never enters the receive FIFO. This is true even with data and the abort sequence, the total of which is less than 24 bits. The data packets that are at least 24 bits but less than 32 bits long are also invalid, but not ignored. They are clocked into the receive FIFO and tagged as having bad FCS.

Frame Abort:

When a frame abort is received the appropriate bits in the Interrupt Flag and Status Registers are set. The last byte of the packet that was aborted is written to the FIFO with a status of 'packet byte' tagged to it. The CPU determines which packet in the FIFO was aborted, if there is more than one packet in the FIFO, by the absence of 'last byte' status on any of the bytes.

Idle Channel:

While receiving the idle channel, the idle bit in the general status register remains set.

Go Ahead:

The occurrence of this sequence can be used to generate an interrupt as described earlier. The receive circuitry will not recognize a frame abort followed by a flag as go ahead.

C-Channel Reception:

The information contained in channel-1 of the incoming ST-BUS (CDSTi) is shifted into the C-Channel Status Register during the Internal Timing Mode.

Transparent Data Transfer:

By setting the IFTF bits in the Control Register to select the transparent data transfer, the receive section can be made to disable the protocol functions like Flag/Abort/GA/Idle detection, zero deletion, CRC calculation and address comparison. The received data is shifted in from CDSTi and written to receive FIFO in bytewide format. If the Protocol Controller is in the Internal Timing Mode and the Timing Control bits are set to 2, 6 or 7 bits/frame, the respective MSBs of each byte are only to be read from the data bus. The transparent data transfer facility is not available when the Timing Control bits are set to 1 bit/frame. The receive section can be disabled in software immediately using the RxEN bit in the Control Register.

The operation of the receiver is similar in the External Timing Mode.

Receive Overflow:

Receive overflow occurs when the receive section attempts to load a byte to an already full receive FIFO. This status can be used to generate the interrupt as described earlier.

Typical Connection

A typical connection to the HDLC Protocol Controller is shown in Figure 23. The parallel port interfaces with 6800/6809 type processors. The bits A0-A3 are the addresses of various registers in the Protocol Controller. The microprocessor can read and write to these registers treating them as memory locations.

The serial port transmits/receives the packetized data. It can be connected to a digital transmission medium or to a digital network interface circuit. The TEOP and REOP are the 'end of packet' signals on transmit and receive direction respectively. $\overline{FOi}$ and CKi are the timing signals with CKi accepting either the bit rate clock or 2 x bit rate clock in the internal timing mode. $\overline{TxCEN}$ and $\overline{RxCEN}$ are the enable inputs in the External Timing Mode.

$\overline{WD}$ is the of watchdog output going LOW when the timer times out or if the $\overline{RST}$ input is held LOW. This output can be used to reset the associated microprocessor. The $\overline{RST}$ is an active LOW input which resets the entire circuitry.

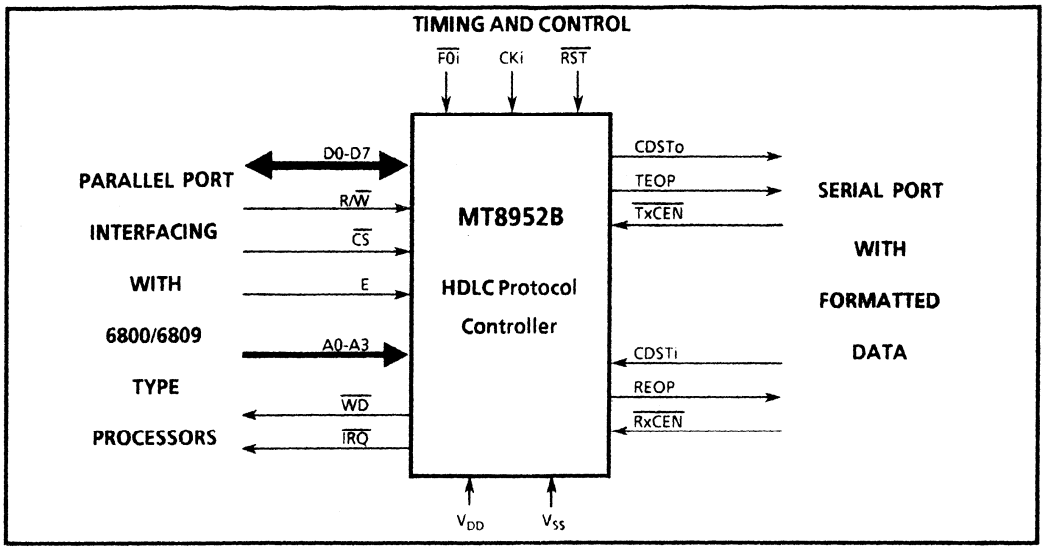


Figure 23. Typical Connection Diagram

Applications

The MT8952B has a number of applications for transferring data or control information over a digital channel while providing built-in error detection capability. In combination with the MT8972 (the Digital Network Interface Circuit), it can be used to transmit digital data over a twisted wire pair.

The block schematic of one such application is shown in Figures 24 and 25. They refer to the primary and secondary ends of a voice/data communication link using the Digital Network

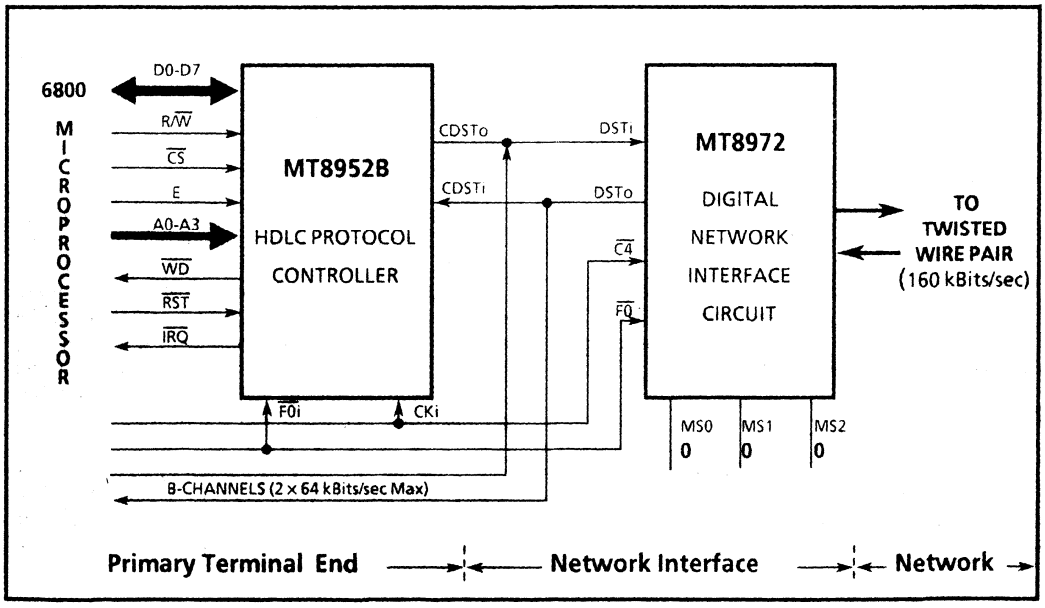


Figure 24. HDLC Protocol Controller at the Primary End of the Link

Interface Circuits (DNIC). Each end is associated with one DNIC which interfaces twisted wire pair to the digital data rate up to 160kbps (2B + D, framing signal and housekeeping information).

Primary End of the Link:

The MT8952B is operating in the internal timing mode with the C-Channel transceiver action enabled. The processor loads the data or control information (D Channel) in the transmit FIFO which is packetized in HDLC format and shifted out serially during the selected channels of the outgoing ST-BUS (CDSTo). The channels and the number of bits per frame (frame period = 125µsec) can be selected by TC0-TC3 bits in the Timing Control Register. Since channel-1 is reserved for the C-Channel information and channels 2 and 3 carry B-channels (64 kbps each), the D channel information can only be sent on channel-0. Similarly the incoming packets on CDSTi are loaded into receive FIFO after the removal of all overhead bits and checked for any errors. The microprocessor will then read the data from the receive FIFO.

The DNIC (MT8972) is selected to operate in single port, master mode with the digital network (DN) option enabled. The B channels, B1 and B2 are shown connected directly to the DNIC. Hence these should be in ST-BUS format enabled at the appropriate timeslot (channels 2 and 3). It can be the outputs of voice codecs (MT896X) providing voice communication or data codecs (MT8950) for communication between RS232-C type terminals. It is possible to use the HDLC protocol on B1 and B2 channels to provide the error detection. This can be done by using a separate MT8952B enabled appropriately to shift out the formatted data during channels 2 and 3 or by multiplexing the same MT8952B between B and D channels.

Secondary End of the Link:

At the secondary end of the communication link, a similar procedure is adopted to transmit/receive the data and control information.

The MT8952B operates in the Internal Timing Mode as at the primary end, but the DNIC (MT8972) is selected to operate in single port, slave mode with the digital network capability enabled.

The other functions and procedures are similar to those at the primary end.

The timing signals like CKi (C2i or $\overline{C4i}$) and $\overline{F0i}$ are provided externally at the primary end and at the secondary end, they are derived from the received data.

Although the above application describes the communication between two stations over a dedicated link, it can be modified to serve a switched communication path by additional control functions and a call set-up procedure many of which can be achieved in software .

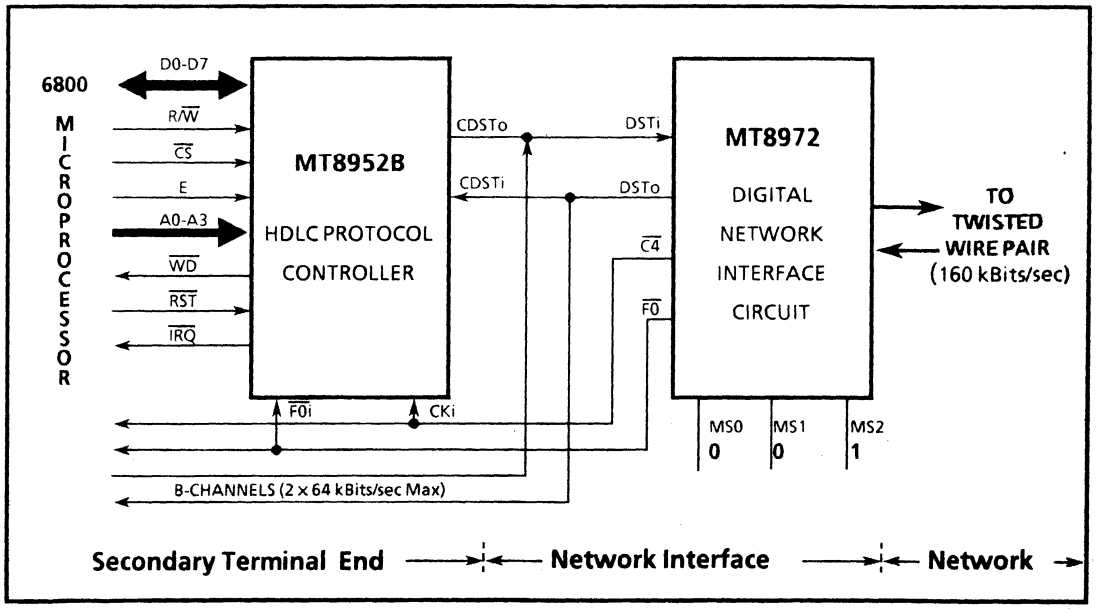


Figure 25. HDLC Protocol Controller at the Secondary End of the Link

Notes:

ISO²-CMOS MT8960/61/62/63/64/65/66/67
Integrated PCM Filter/Codec

9161-002-020 NA ISSUE 6 May 1986

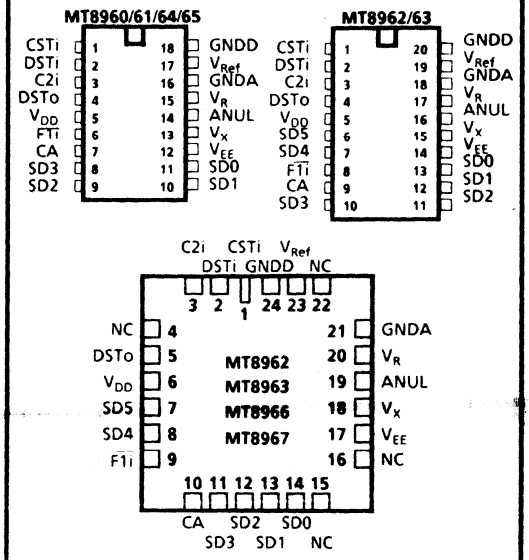
Features

- ST-Bus Compatible
- Transmit/Receive filters & PCM Codec in one I.C.
- Meets AT&T D3/D4 and CCITT G711 and G712
- μ-Law: MT8960/62/64/66
  A-Law: MT8961/63/65/67
- Low power consumption: Op.: 30 mW typ.
  Stby.: 2.5 mW typ.
- Digital Coding Options:
  MT8964/65/66/67 CCITT Code
  MT8960/61/62/63 Alternative Code
- Digitally controlled gain adjust of both filters
- Analog and digital loopback
- Filters and codec independently user accessible for testing
- Power down mode available
- 2.048 MHz master clock input
- Up to 6 uncommitted control outputs
- ± 5V ± 5% power supply

Description

Manufactured in ISO²-CMOS, these integrated filter/codecs are designed to meet the demanding performance needs of the digital telecommunications industry, e.g. PABX, Central Office, Digital telephones.

Pin Connections



Ordering Information

MT8960/61/64/65AC	18 Pin Cerdip
MT8962/63AC	20 Pin Cerdip
MT8962/63/66/67AY	24 Pin LCC

(0°C to + 70°C)

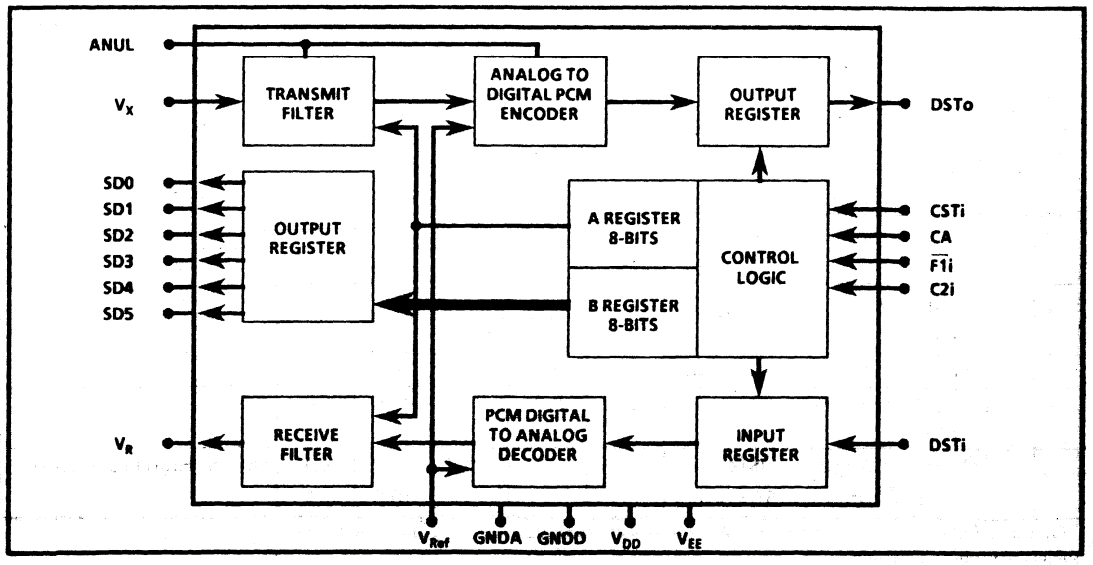


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD}-GNDD	-0.3	+6.0	V
		V_{EE}-GNDD	-6.0	+0.3	V
2	Reference Voltage	V_{Ref}	GNDA	V_{DD}	V
3	Analog Input	V_X	V_{EE}	V_{DD}	V
4	Digital Inputs	Except CA	GNDD-0.3	V_{DD} + 0.3	V
		CA	V_{EE}-0.3	V_{DD} + 0.3	V
5	Output Voltage	SD0-2	GNDD-0.3	V_{DD} + 0.3	V
		SD3	V_{EE}-0.3	V_{DD} + 0.3	V
		SD4-5	V_{EE}-0.3	V_{DD} + 0.3	V
6	Current On Any Pin	I_I		20	mA
7	Storage Temperature	T_S	-55	+ 125	°C
8	Power Dissipation at 25°C (Derate 16 mW/°C above 75°C)	P_{Diss}		500	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to GNDD unless otherwise stated

		Characteristics		Sym	Min	Typ*	Max	Units	Comments
1		Supply Voltage		V_{DD}	4.75	5.0	5.25	V	
				V_{EE}	-5.25	-5.0	-4.75	V	
				V_{Ref}		2.5		V	See Note 1
2		Voltage On Digital Ground		VGNDD	-0.1	0.0	+0.1	Vdc	Ref. to GNDA
					-0.4	0.0	+0.4	Vac	Ref. to GNDA 400ns max. duration in 125µs cycle
3		Operating Temperature		T_O	0		+70	°C	
4		Operating Current	V_{DD}	I_{DD}		3.0	4.0	mA	All digital inputs at V_{DD}
			V_{EE}	I_{EE}		3.0	4.0	mA	or GNDD (or V_{EE} for CA)
			V_{Ref}	I_{Ref}		2.0		µA	Mean current
5		Standby Current	V_{DD}	I_{DDO}		0.25	1.0	mA	All digital inputs at V_{DD}
			V_{EE}	I_{EEO}		0.25	1.0	mA	or GNDD (or V_{EE} for CA)

Note 1: Temperature coefficient of VRef should be better than 100 ppm/°C.

DC Electrical Characteristics - Voltages are with respect to GNDD unless otherwise stated

TA = 0 to 70°C, VDD = 5V ± 5%, VEE = -5V ± 5%, VRef = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Outputs unloaded unless otherwise specified

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	DIGITAL	Input Current	Except CA	I_I			10.0	µA	V_{IN} = GNDD to V_{DD}
			CA	I_{IC}			10.0	µA	V_{IN} = V_{EE} to V_{DD}
2		Input Low Voltage	Except CA	V_{IL}	0.0		0.8	V	
			CA	V_{ILC}	V_{EE}		V_{EE} + 1.2	V	
3		Input High Voltage	All Inputs	V_{IH}	2.4		5.0	V	
4		Input Intermediate Voltage	CA	V_{IIC}	0.0		0.8	V	
5		Output Leakage Current (Tristate)	DSTo	I_{OZ}		±0.1		µA	Output High Impedence
			SD3-5				10.0	µA	

* Typical figures are at 25°C with nominal ± 5V supplies. For design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics (cont'd)

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
6	DIGITAL	Output Low Voltage	DSTo	V_{OL}			0.4	V	I_{OUT} = 1.6 mA
			SD_{0-2}	V_{OL}			1.0	V	I_{OUT} = 1 mA
7		Output High Voltage	DSTo	V_{OH}	4.0			V	I_{OUT} = -100µA
			SD_{0-2}	V_{OH}	4.0			V	I_{OUT} = -1mA
8		Output Resistance	SD_{3-5}	R_{OUT}		1.0	2.0	KΩ	V_{OUT} = + 1V
9		Output Capacitance	DSTo	C_{OUT}		4.0		pF	Output High Impedance
10	ANALOG	Input Current	V_X	I_{IN}			10.0	µA	$V_{EE} \leq V_{IN} \leq V_{CC}$
11		Input Resistance	V_X	R_{IN}		10.0		MΩ	
12		Input Capacitance	V_X	C_{IN}		30.0		pF	f_{IN} = 0 - 4 KHz
13		Input Offset Voltage	V_X	V_{OSIN}		+ 1.0		mV	See Note 2
14		Output Resistance	V_R	R_{OUT}			100	Ω	
15		Output Offset Voltage	V_R	V_{OSOUT}			100	mV	Digital Input = + 0

Note 2: V_{OSIN} specifies the DC component of the digitally encoded PCM word.

AC Electrical Characteristics - Voltages are with respect to GNDD unless otherwise stated

T_A = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V,
Clock Frequency = 2.048 MHz, Outputs unloaded unless otherwise specified.

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	DIGITAL	Clock Frequency	C2i	f_C	2.046	2.048	2.05	MHz	See Note 3
2		Clock Rise Time	C2i	t_{CR}			50	ns	
3		Clock Fall Time	C2i	t_{CF}			50	ns	
4		Clock Duty Cycle	C2i		40	50	60	%	
5		Chip Enable Rise Time	$\overline{F1}$i	t_{ER}			100	ns	
6		Chip Enable Fall Time	$\overline{F1}$i	t_{EF}			100	ns	
7		Chip Enable Setup Time	$\overline{F1}$i	t_{ES}	50			ns	See Note 4
8		Chip Enable Hold Time	$\overline{F1}$i	t_{EH}	25			ns	See Note 4
9		Output Rise Time	DSTo	t_{OR}			100	nS	
10		Output Fall Time	DSTo	t_{OF}			100	nS	
11		Propagation Delay Clock to Output Enable	DSTo	t_{PZL}			122	nS	
				t_{PZH}			122	nS	R_L = 10KΩ to V_{CC}
12		Propagation Delay Clock to Output	DSTo	t_{PLH}			100	nS	C_L = 100 pF
				t_{PHL}			100	nS	
13		Input Rise Time	CSTi	t_{IR}			100	nS	
			DSTi				100	nS	
14		Input Fall Time	CSTi	t_{IF}			100	nS	
			DSTi				100	nS	
15		Input Set Up Time	CSTi	t_{ISH}	25			nS	
			DSTi	t_{ISL}	0			nS	
16		Input Hold Time	CSTi	t_{IH}	60			nS	
			DSTi		60			nS	

* Typical figures are at 25°C with nominal ± 5V supplies. For design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics (cont'd)

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
17	DIGITAL	Propogation Delay SD Clock to SD Output	t_{PCS}			400	nS	CL = 100 pF
18		SD Output Fall Time SD	t_{SF}			200	nS	CL = 20 pF
19		SD Output Rise Time SD	t_{SR}			400	nS	
20		Digital Loopback Time DSTi to DSTo	t_{DL}			122	nS	

(See Figures 2a, 2b, 2c)

Note 3: The filter characteristics are totally dependent upon the accuracy of the clock frequency but, providing $\overline{F1}i$ is synchronized to C2i, the codec function is unaffected by changes in the clock frequency.

Note 4: This gives a 75 nS period, 50 ns before and 25 ns after the 50% point of C2i rising edge, when any change in $\overline{F1}i$ will give an undetermined state to to the internally synchronized enable signal.

AC Electrical Characteristics - Voltages are with respect to GNDD unless otherwise stated

T_A = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V,
Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB, Outputs unloaded unless otherwise specified.

Transmit (A/D) Path

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	ANALOG	Analog Input at V_X equivalent to the overload decision level at the codec	V_{IN}		4.829 5.000		V_{PP} V_{PP}	Level at codec: μ-Law: 3.17 dBm0 A-Law: 3.14 dBm0 See Note 6
2		Absolute Gain	G_{AX}	-0.25		+0.25	dB	0 dBm0 @ 1004 Hz
3		Deviation of Gain Adjustment		-0.1		+0.1	dB	From Nominal Value
4		Gain Variation With Temp	G_{AXT}		0.01		dB	TA = 0°C to 70°C
		With Supplies	G_{AXS}		0.04		dB/V	
5		Gain Tracking (See Figure 5) CCITT G712 Method 1)	GT_{X1}					Sinusoidal Level:
				-0.25		+0.25	dB	+3 to -20 dBm0
								Noise Signal Level:
				-0.25		+0.25	dB	-10 to -55 dBm0
				-0.50		+0.50	dB	-55 to -60 dBm0
		CCITT G712 (Method 2) AT&T	GT_{X2}					Sinusoidal Level:
				-0.25		+0.25	dB	+3 to -40 dBm0
				-0.50		+0.50	dB	-40 to -50 dBm0
				-1.50		+1.50	dB	-50 to -55 dBm0
6		Quantization Distortion (See Figure 6) CCITT G712 (Method 1)	D_{QX1}					Noise Signal Level:
				28.00			dB	-3 dBm0
				35.60			dB	-6 to -27 dBm0
				33.90			dB	-34 dBm0
				29.30			dB	-40 dBm0
				14.20			dB	-55 dBm0

* Typical figures are at 25°C with nominal ± 5V supplies. For design aid only: not guaranteed and not subject to production testing.

Transmit (A/D) Path (cont'd)

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
		Quantization Distortion (cont'd) (See Figure 6)	CCITT G712 (Method 2)	D_{QX2}					Sinusoidal Input Level:
					35.30			dB	0 to -30 dBm0
			AT&T		29.30			dB	-40 dBm0
					24.30			dB	-45 dBm0
7		Idle Channel Noise	C-message	N_{CX}			18	dBrnC0	µ-Law Only
			Psophometric	N_{PX}			-67	dBm0p	CCITT G712
8		Single Frequency Noise		N_{SFX}			-56	dBm0	CCITT G712
9		Harmonic Distortion (2nd or 3rd Harmonic)					-46	dB	Input Signal: 0 dBm0 @ 1.02 KHz
10		Envelope Delay		D_{AX}			270	µS	@ 1004 Hz
11		Envelope Delay Variation With Frequency	1000-2600 Hz	D_{DX}		60		µS	Input Signal:
			600-3000 Hz			150		µS	400-3200 Hz Sinewave
			400-3200 Hz			250		µS	at 0 dBm0
12		Intermodulation Distortion	CCITT G712 50/60 Hz	IMD_{X1}			-55	dB	50/60 Hz @ -23 dBm0 and any signal within 300-3400 Hz at -9 dBm0
	A N A L O G		CCITT G712 2 tone	IMD_{X2}			-41	dB	740 Hz and 1255 Hz @ -4 to -21 dBm0. Equal Input Levels
			AT&T 4 tone	IMD_{X3}			-47	dB	2nd order products
				IMD_{X4}			-49	dB	3rd order products
13		Gain Relative to Gain @ 1004 Hz (See Figure 3)	≤ 50 HZ	G_{RX}			-25	dB	0 dBm0 Input Signal
			60 Hz				-30	dB	
			200 Hz		-1.8		0.00	dB	Transmit
			300-3000 Hz		-0.125		0.125	dB	Filter
			3200 Hz		-0.275		0.125	dB	Response
			3300 Hz		-0.350		0.030	dB	
			3400 Hz		-0.80		-0.100	dB	
			4000 Hz				-14	dB	
			≥ 4600 Hz				-32	dB	
14		Crosstalk D/A to A/D		CT_{RT}			-70	dB	0 dBm0 @ 1.02 KHz in D/A
15		Power Supply Rejection	V_{DD}	$PSSR_1$	33			dB	Input 50 mV_{RMS} at
			V_{EE}	$PSSR_2$	35			dB	1.02 KHz
16		Overload Distortion(See Fig.8)							Input frequency = 1.02KHz

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing

Note 6: 0dBm0 = 1.185 V_{RMS} for the µ-Law codec.
0dBm0 = 1.231 V_{RMS} for the A-Law codec.

AC Electrical Characteristics - Voltages are with respect to GNDD unless otherwise stated

T_A = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V,
Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB, Outputs unloaded unless otherwise specified.

Receive (D/A) Path

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	ANALOG	Analog output at V_R equivalent to the overload decision level at codec	V_{OUT}		4.829 5.000		V_{pp} V_{pp}	Level at codec: μ-Law: 3.17 dBm0 A-Law: 3.14 dBm0 R_L = 10 KΩ See Note 7
2		Absolute Gain	G_{AR}	-0.25		+ 0.25	dB	0 dBm0 @ 1004Hz
3		Deviation of Attenuation Adjustment		-0.10		+ 0.10	dB	From Nominal Value
4		Gain Variation With Temp.	G_{ART}		0.01		dB	TA = 0°C to 70°C
		With Supplies	G_{ARS}		0.04		dB/V	
5		Gain Tracking CCITT G712 (See Figure 5) (Method 1)	GT_{R1}					Sinusoidal Level:
				-0.25		+ 0.25	dB	+ 3 to -10 dBm0
								Noise Signal Level:
				-0.25		+ 0.25	dB	-10 to -55 dBm0
				-0.50		+ 0.50	dB	-55 to -60 dBm0
		CCITT G712 (Method 2) AT & T	GT_{R2}					Sinusoidal Level:
				-0.25		+ 0.25	dB	+ 3 to -40 dBm0
				-0.50		+ 0.50	dB	-40 to -50 dBm0
				-1.50		+ 1.50	dB	-50 to -55 dBm0
6		Quantization Distortion (See Fig. 6) CCITT G712 (Method 1)	D_{QR1}					Noise Signal Level:
				28.00			dB	-3 dBm0
				35.60			dB	-6 to -27 dBm0
				33.90			dB	-34 dBm0
				29.30			dB	-40 dBm0
				14.30			dB	-55 dBm0
		CCITT G712 (Method 2) AT & T	D_{QR2}					Sinusoidal Input Level:
				36 .40			dB	0 to -30 dBm0
				30.40			dB	-40 dBm0
				25.40			dB	-45 dBm0
7		Idle Channel Noise C-message	N_{CR}			12	dBrnC0	μ-Law Only
		Psophometric	N_{PR}			-75	dBm0p	CCITT G712
8		Single Frequency Noise	N_{SFR}			-56	dBm0	CCITT G712
9		Harmonic Distortion (2nd or 3rd Harmonic)				-46	dB	Input Signal 0 dBm0 at 1.02 KHz
10		Intermodulation Distortion CCITT G712 2 tone	IMD_{R2}			-41	dB	
		AT & T 4 tone	IMD_{R3}			-47	dB	2nd order products
			IMD_{R4}			-49	dB	3rd order products

* Typical figures are at 25°C with nominal ± 5V supplies. For design aid only: not guaranteed and not subject to production testing.

Receive (D/A) Path (cont'd)

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
11		Envelope Delay		D_{AR}			210	µS	@ 1004 Hz
12		Envelope Delay	1000-2600 Hz	D_{DR}		90		µS	Input Signal:
		Variation with	600-3000 Hz			170		µS	400 - 3200 Hz digital
		Frequency	400-3200 Hz			265		µS	sinewave at 0 dBm0
13		Gain Relative to	<200 Hz	G_{RR}			0.125	dB	0 dBm0 Input Signal
		Gain @ 1004 Hz	200 Hz		-0.5		0.125	dB	
	A	(See Figure 4)	300-3000 Hz		-0.125		0.125	dB	Receive
	N		3300 Hz		-0.350		0.030	dB	Filter
	A		3400 Hz		-0.80		-0.100	dB	Response
	L		4000 Hz				-14.0	dB	
	O		≥4600 Hz				-28.0	dB	
	G								
14		Crosstalk A/D to D/A		CT_{TR}			-70	dB	0 dBm0 @ 1.02 KHz in A/D
15		Power Supply	V_{DD}	$PSRR_3$	33			dB	Input 50 mV_{RMS} at
		Rejection	V_{EE}	$PSRR_4$	35			dB	1.02 KHz
16		Overload Distortion(See Fig. 8)							Input frequency = 1.02KHz

* Typical figures are at 25°C with nominal ± 5V supplies. For design aid only: not guaranteed and not subject to production testing.

Note 7: 0dBm0 = 1.185 V_{RMS} for µ-Law codec and 0dBm0 = 1.231 V_{RMS} for A-Law codec.

Pin Description

Pin Name	Description
CSTi	**Control ST-Bus In** is a TTL-compatible digital input used to control the function of the filter/codec. Three modes of operation may be effected by applying to this input a logic high (V_{DD}), logic low (GNDD), or an 8-bit serial word, depending on the logic states of CA and $\overline{F1i}$. Functions controlled are : Power-down, Filter gain adjust, Loopback, Chip testing, SD outputs.
DSTi	**Data ST-Bus In** accepts the incoming 8-bit PCM word. Input is TTL-compatible.
C2i	**Clock Input** is a TTL-compatible 2.048 MHz clock.
DSTo	**Data ST-Bus Out** is a 3-state digital output driving the PCM bus with the outgoing 8-bit PCM word.
V_{DD}	**Positive power Supply** (+ 5V).
$\overline{F1i}$	**Synchronization Input** is an active low digital input enabling (in conjunction with CA) the PCM input, PCM output and digital control input. It is internally sampled on every positive edge of the clock, C2i, and provides frame and channel synchronization.
CA	**Control Address** is a 3-level digital input which enables PCM input and output and determines into which control register (A or B) the serial data, presented to CSTi, is stored.
SD3	**System Drive Output** is an open drain output of an N-channel transistor which has its source tied to GNDA. Inactive state is open circuit.
SD4-5	**System Drive Outputs** are open drain outputs of N-channel transistors which have their source tied to GNDD. Inactive state is open circuit.

Pin Description (cont'd)

Pin Name	Description
SD0-2	**System Drive Outputs** are "Totempole" CMOS outputs switching between GNDD and V_{DD}. Inactive state is logic low.
V_{EE}	**Negative power supply** (-5V).
V_X	**Voice Transmit** is the analog input to the transmit filter.
ANUL	**Auto Null** is used to integrate an internal auto-null signal. A capacitor is connected between this pin and GNDA.
V_R	**Voice Receive** is the analog output of the receive filter.
GNDA	**Analog ground** (0V).
V_{Ref}	**Voltage Reference** input to D to A converter.
GNDD	**Digital ground** (0V).

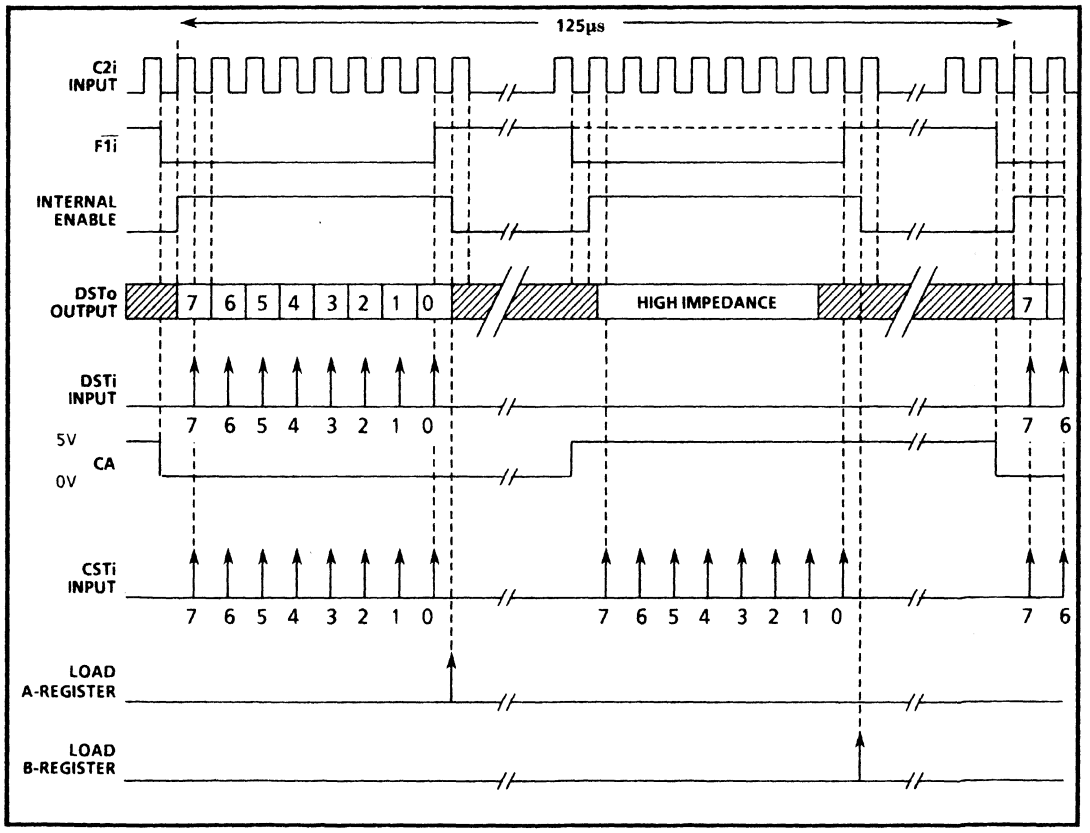


Figure 2a. Timing Diagram - 125µS Frame Period

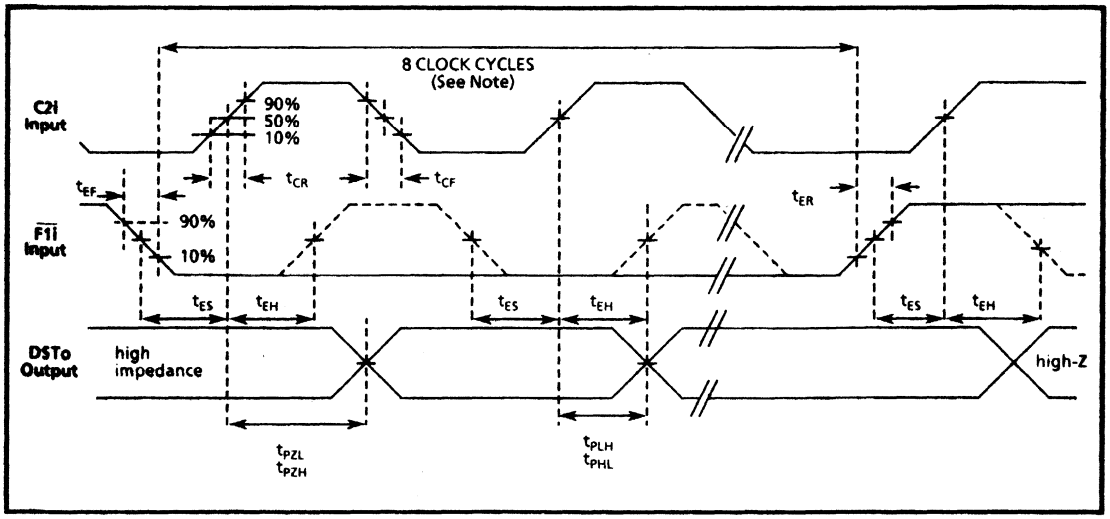


Figure 2b. Timing Diagram - Output Enable

Note: In typical applications, $\overline{F1i}$ will remain low for 8 cycles of C2i. However, the device will function normally as long as t_{ES} and t_{EH} are met at each positive edge of C2i.

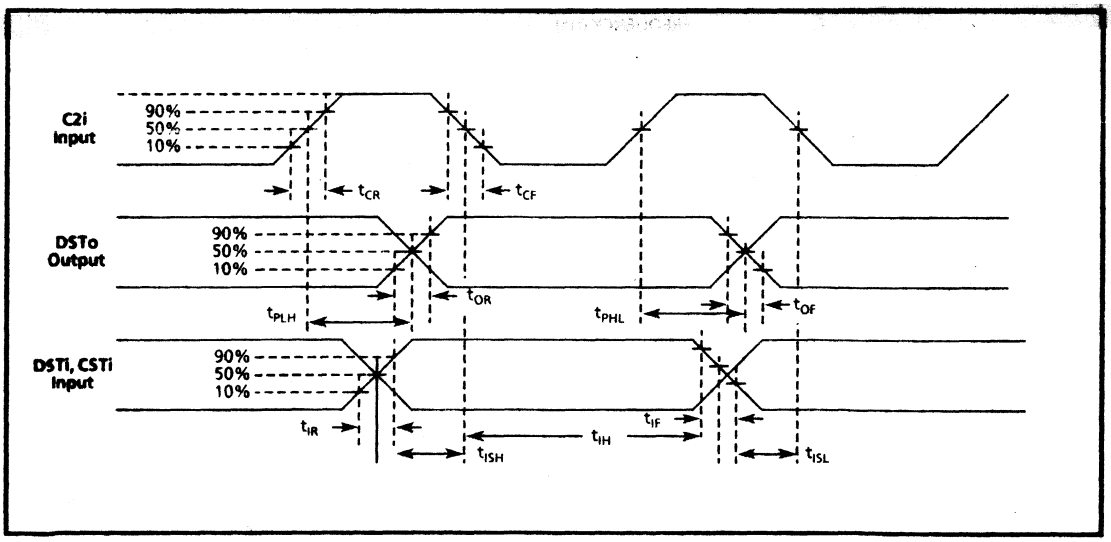


Figure 2c. Timing Diagram - Input/Output

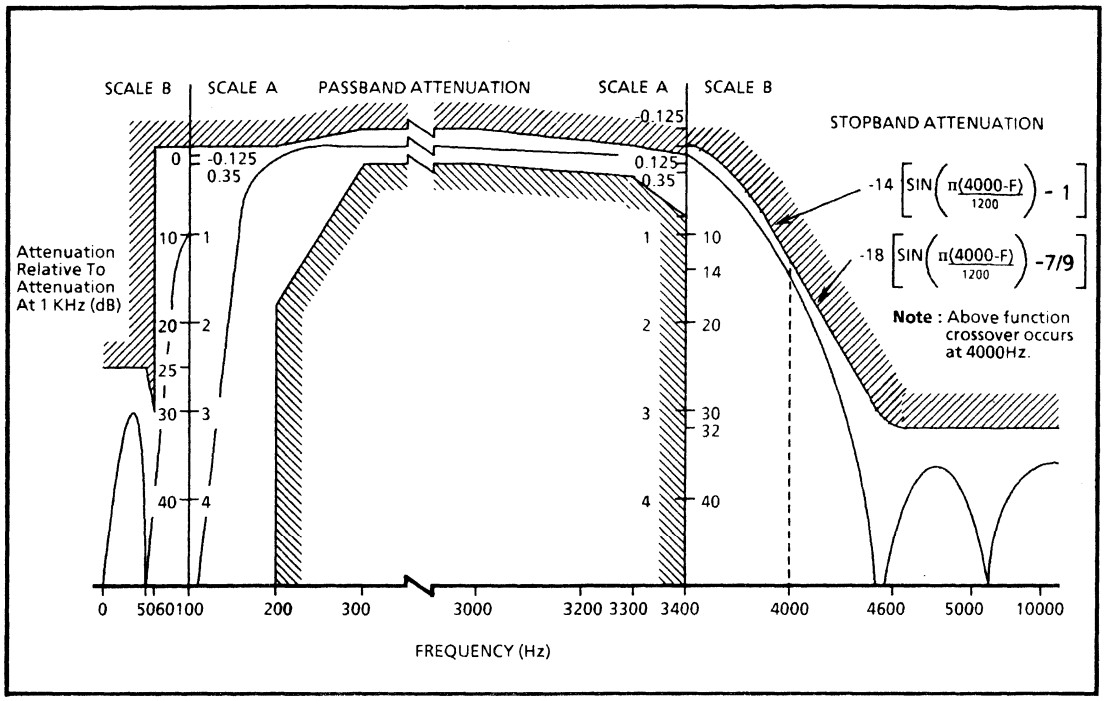


Figure 3. Attenuation vs Frequency for Transmit (A/D) Filter

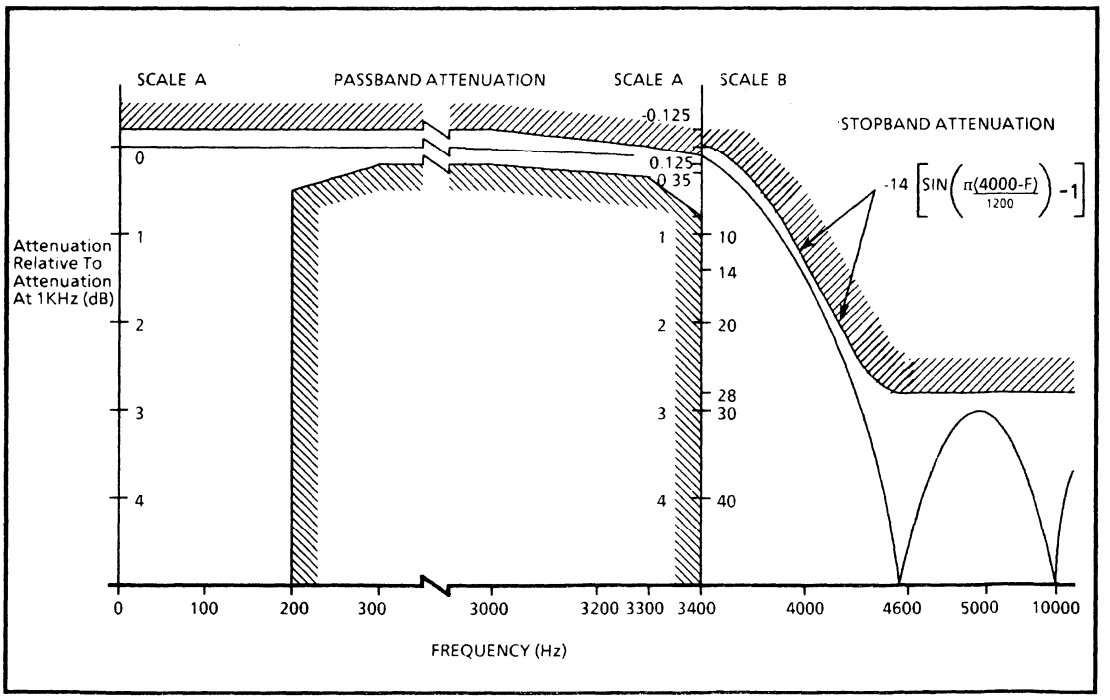


Figure 4. Attenuation vs Frequency for Receive (D/A) Filter

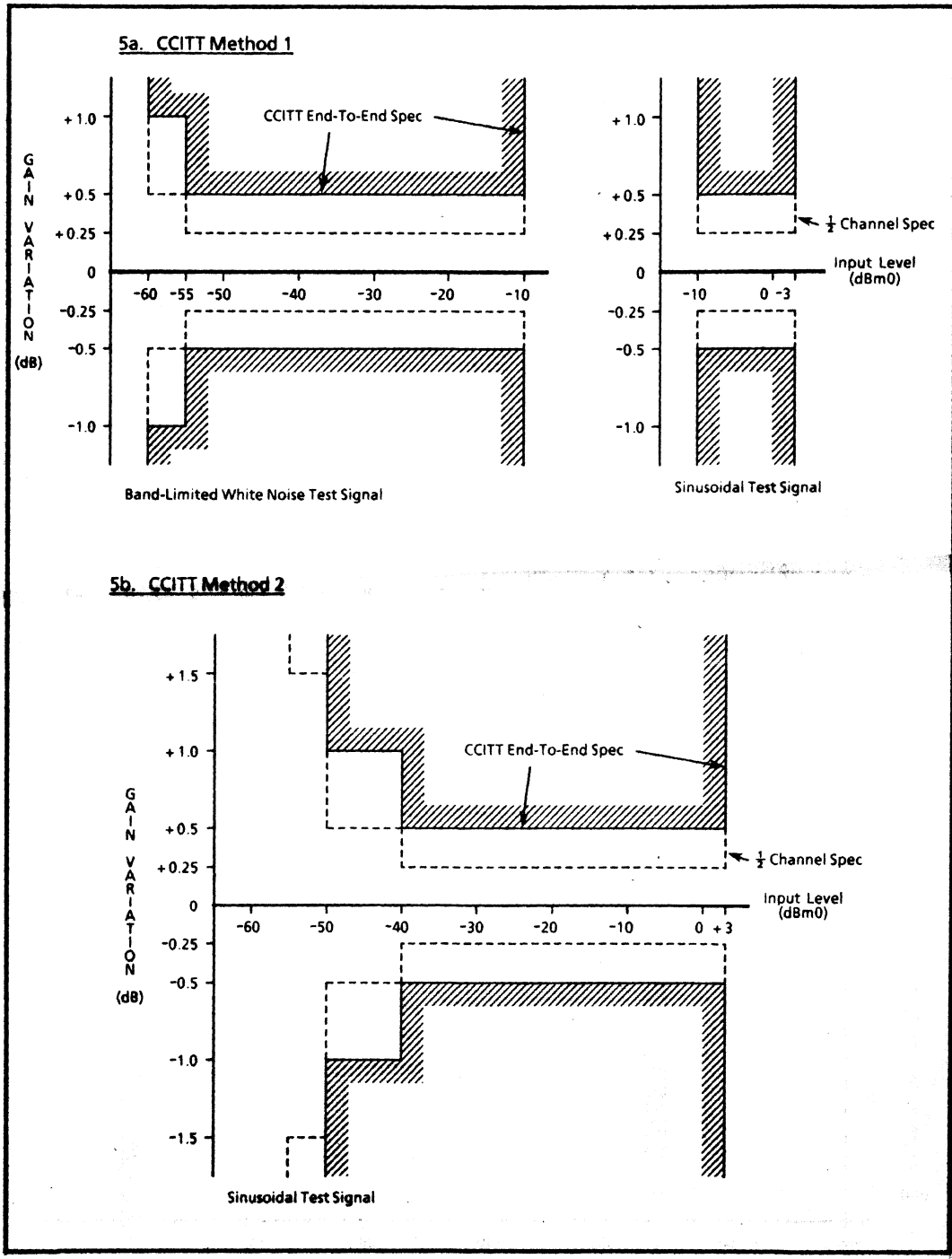


Figure 5. Variation of Gain With Input Level

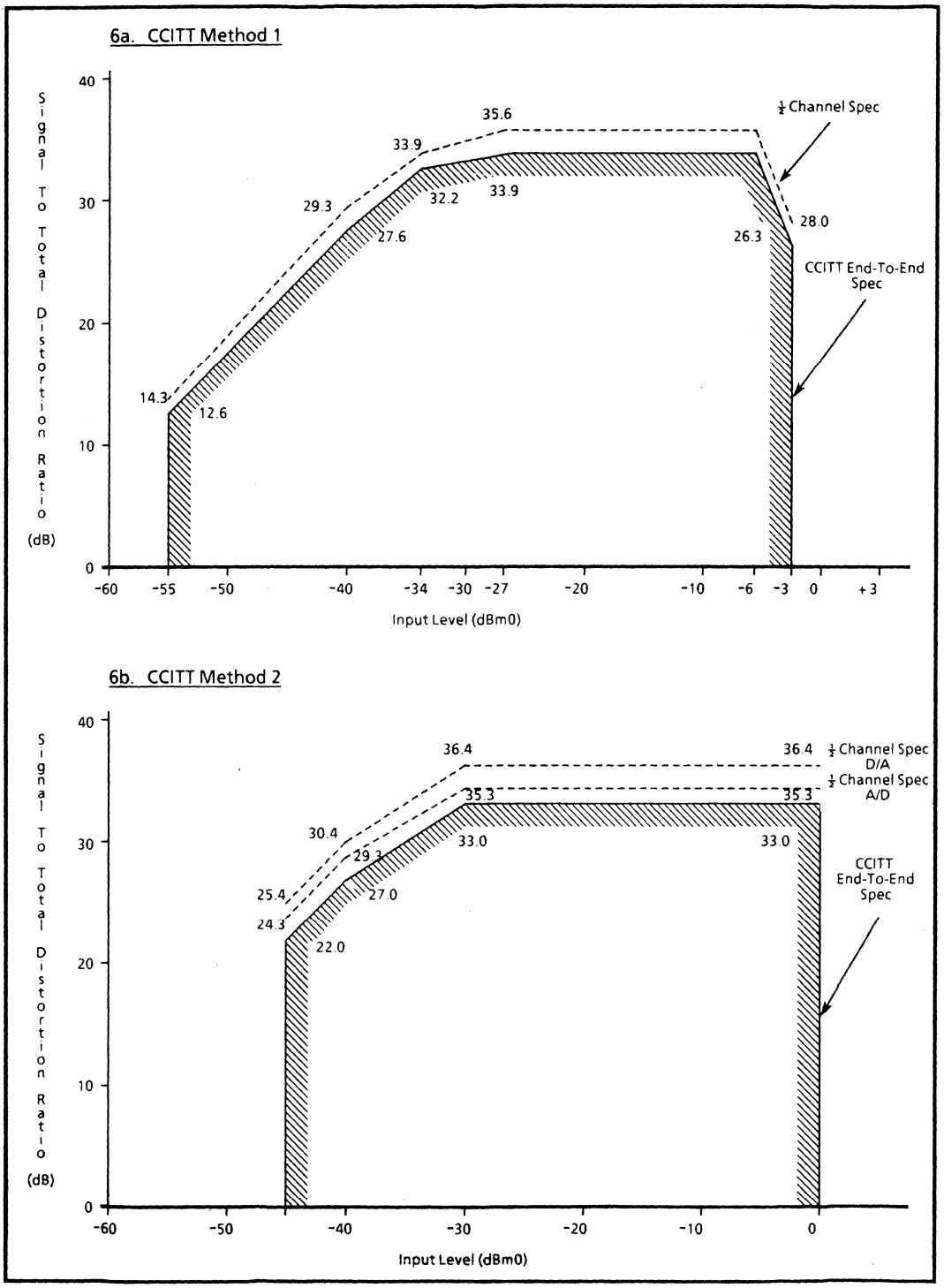


Figure 6. Signal to Total Distortion Ratio vs Input Level

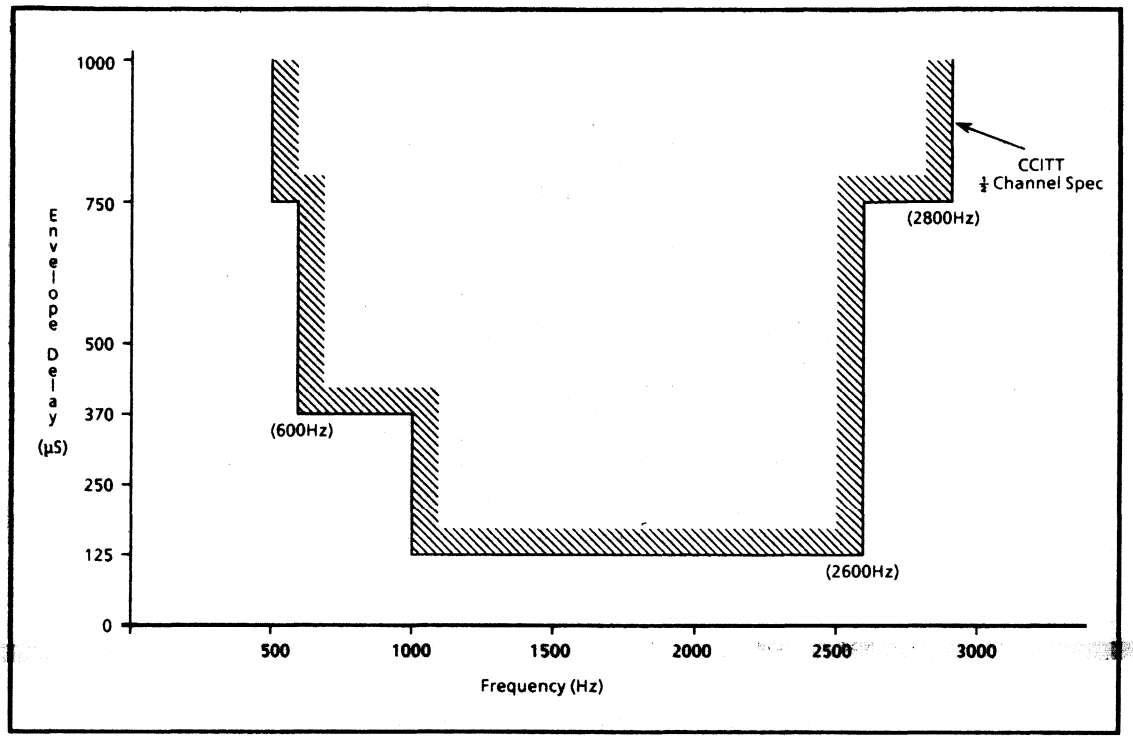


Figure 7. Envelope Delay Variation With Frequency

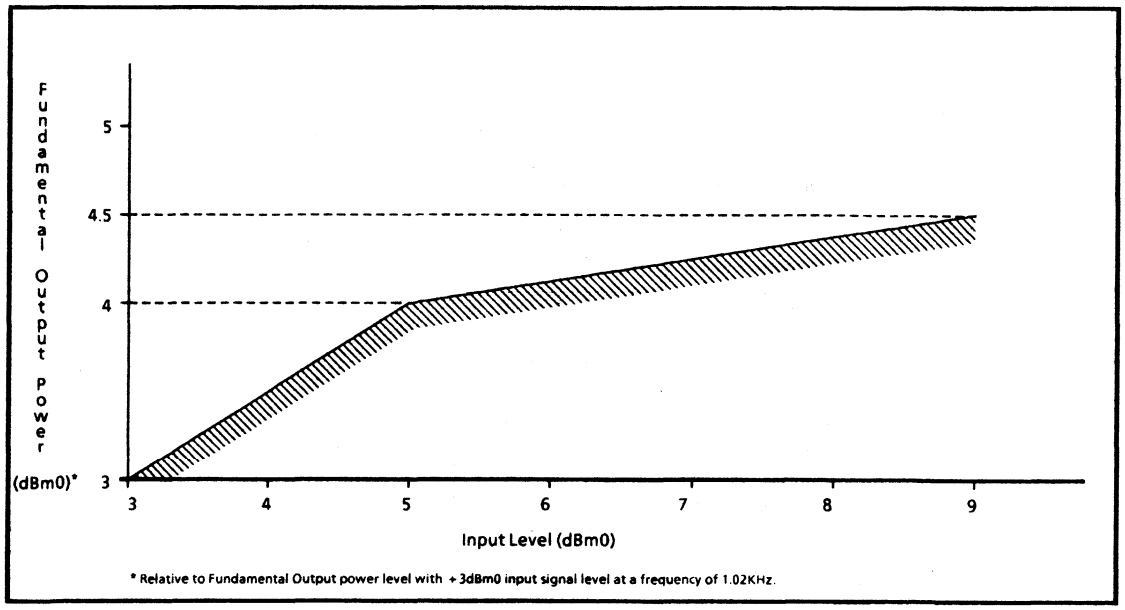


Figure 8. Overload Distortion (End-to-End)

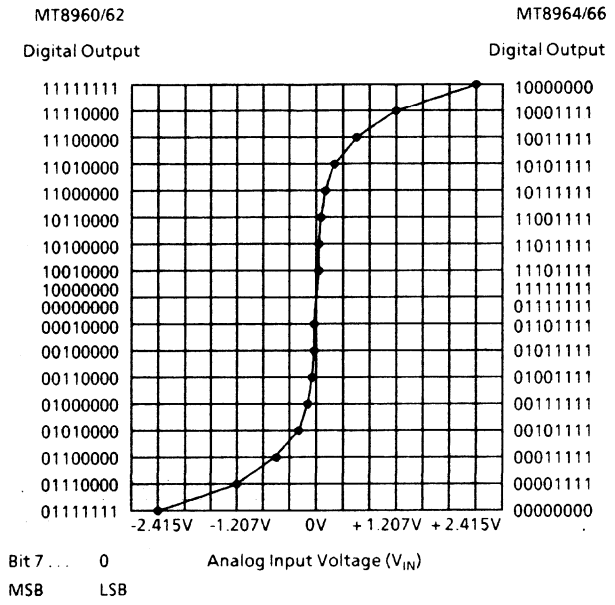


Figure 9. μ-Law Encoder Transfer Characteristic

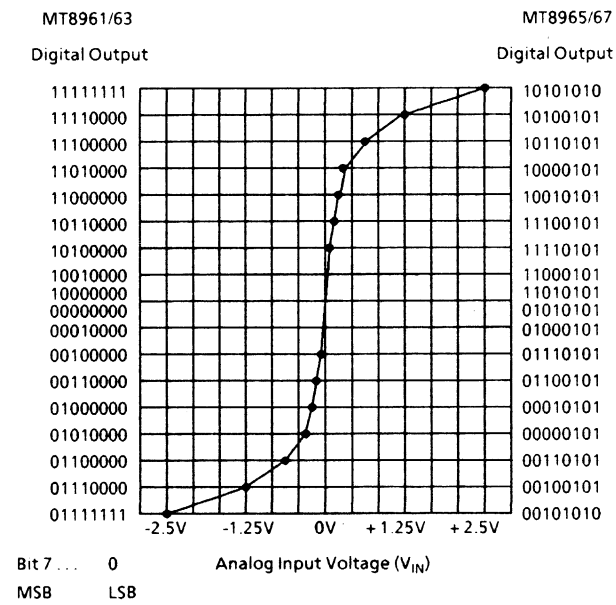


Figure 10. A-Law Encoder Transfer Characteristic

Functional Description

Figure 1 shows the functional block diagram of the MT8960-67. These devices provide the conversion interface between the voiceband analog signals of a telephone subscriber loop and the digital signals required in a digital PCM (pulse code modulation) switching system. Analog (voiceband) signals in the transmit path enter the chip at V_X, are sampled at 8Khz, and the samples quantized and assigned 8-bit digital values defined by logarithmic PCM encoding laws. Analog signals in the receive path leave the chip at V_R after reconstruction from digital 8-bit words.

Separate switched capacitor filter sections are used for bandlimiting prior to digital encoding in the transmit path and after digital decoding in the receive path. All filter clocks are derived from the 2.048 MHz master clock input, C2i. Chip size is minimized by the use of common circuitry performing the A to D and D to A conversion. A successive approximation technique is used with capacitor arrays to define the 16 steps and 8 chords in the signal conversion process. 8 bit PCM encoded digital data enters and leaves the chip serially on DSTi and DSTo pins respectively.

Transmit Path

Analog signals at the input (Vx) are firstly bandlimited to 508 kHz by an RC low-pass filter section. This performs the necessary anti-aliasing for the following first-order sampled data low-pass pre-filter which is clocked at 512 kHz. This further bandlimits the signal to 124 kHz before a fifth-order elliptic low-pass filter, clocked at 128 kHz, provides the 3.4 kHz bandwidth required by the encoder section. A 50/60 Hz third-order high-pass notch filter clocked at 8 kHz completes the transmit filter path. Accumulated DC offset is cancelled in this last section by a switched-capacitor auto-zero loop which integrates the sign bit of the encoded PCM word, fed back from the codec and injects this voltage level into the non-inverting input of the comparator. An integrating capacitor (of value beweeen 0.1 and 1 uF) must be externally connected from this point (ANUL) to the Analog Ground (GNDA).

The absolute gain of the transmit filter (nominally 0 dB at 1 kHz) can be adjusted from 0 dB to 7 dB in 1 dB steps by means of three binary controlled gain pads.

The resulting bandpass characteristics with the limits shown in Figure 3 meet the CCITT and AT & T recommended specifications. Typical atttenuations are 30 dB for 0-60 Hz and 35 dB for 4.6 kHz and above.

The filter output signal is an 8 kHz staircase waveform which is fed into the codec capacitor array, or alternatively, into an external capacitive load of 250 pf when the chip is in the test mode. The digital encoder generates an 8 bit digital word representation of the 8 kHz sampled analog signal. The first bit of serial data stream is bit 7 (MSB) and represents the sign of the analog signal. Bits 4-6 represent the chord which contains the analog sample value. Bits 0-3 represent the step value of the analog sample within the selected chord. The MT8960-63 provide a sign plus magnitude PCM output code format. The MT8964/66 PCM output code conforms to the AT & T D3 specification i.e. true sign bit and inverted magnitude bits. The MT8965/67 PCM output code conforms to the CCITT specifications with alternate mark inversion (even bits inverted). See Figs. 9 and 10 for the digital output code corresponding to the analog voltage, V_{IN}, at V_X input.

The 8 bit digital word is output at DSTo at a nominal rate of 2.048 MHz, via the output buffer as the first 8-bits of the 125 µs sampling frame.

Receive Path

An 8-bit PCM encoded digital word is received on DSTi input once during the 125 µs period and is loaded into the input register. A charge proportional to the received PCM word appears on the capacitor array and an 8 kHz sample and hold circuit integrates this charge and holds it for the rest of the sampling period.

The receive (D/A) filter provides interpolation filtering on the 8 KHz sample and hold signal from the codec. The filter consists of a 3.4 kHz low-pass fifth-order elliptic section clocked at 128 kHz and performs band-limiting and smoothing of the 8 Khz "staircase" waveform. In addition, sinx/x gain correction is applied to the signal to compensate for the attenuation of higher frequencies caused by the capacitive sample and hold circuit. The absolute gain of the receive filter can be adjusted from 0 dB to -7 dB in 1 dB steps by means of three binary controlled gain pads. The resulting low-pass characteristics, with the limits shown in Figure 4, meet the CCITT and AT & T recommended specifications.

Typical attenuation at 4.6 kHz and above is 30 dB. The filter is followed by a buffer amplifier which

will drive 5V peak/peak into a 10k ohm load, suitable for driving electronic 2-4 wire circuits.

V_{Ref}

An external voltage must be supplied to the V_{Ref} pin which provides the reference voltage for the digital encoding and decoding of the analog signal. For V_{Ref} = 2.5V, the digital encode decision value for overload (maximum analog signal detect level) is equal to an analog input V_{IN} = 2.415V (μ-Law version) or 2.5V (A-Law version) and is equivalent to a signal level of 3.17 dBm0 or 3.14 dBm0 respectively, at the codec.

The analog output voltage from the decoder at V_R is defined as:

μ-Law:

$$V_{Ref} X \left[\left(\frac{-0.5}{128}\right)+\left(\frac{2^C}{128}\right)\left(\frac{16.5+S}{33}\right)\right] \pm V_{OFFSET}$$

A-Law:

$$V_{Ref} X \left[\left(\frac{2^{C+1}}{128}\right)\left(\frac{0.5+S}{32}\right)\right] \pm V_{OFFSET} \quad C=0$$

$$V_{Ref} X \left[\left(\frac{2^{C}}{128}\right)\left(\frac{16.5+S}{32}\right)\right] \pm V_{OFFSET} \quad C\neq 0$$

where C = chord number (0-7)
S = step number (0-15)
V_{Ref} is a high impedance input with a varying capacitive load of up to 40 pf.

The recommended reference voltage for the MT8960 series of codecs is 2.5V ± 0.5%. The output voltage from the reference source should have a maximum temperature coefficient of 100 ppm/C°. This voltage should have a total regulation tolerance of ± 0.5% both for changes in the input voltage and output loading of the voltage reference source. A voltage reference circuit capable of meeting these specifications is shown in Figure 11. Analog Devices' AD1403A voltage reference circuit is capable of driving a large number of codecs due to the high input impedance of the VREF input. Normal precautions should be taken in PCB layout design to minimize noise coupling to this pin. A 0.1 μF capacitor connected from V_{Ref} to ground and located as close as possible to the codec is recommended to minimize noise entering through V_{Ref}. This capacitor should have good high frequency characteristics.

Timing

The codec operates in a synchronous manner (see Figure 2a). The codec is activated on the first positive edge of C2i after $\overline{F1i}$ has gone low. The digital output at DSTo (which is a 3 state output driver) will then change from a high impedance state to the sign bit of the encoded PCM word to be output. This will remain valid until the next positive edge, when the next most significant bit will be output.

On the first negative clock edge (after $\overline{F1i}$ signal has been internally synchronized and CA is at GNDD or V_{EE}) the logic signal present at DSTi will be clocked into the input shift register as the sign bit of the incoming PCM word.

The 8 bit word is thus input at DSTi on negative edges of C2i and output at DSTo on positive edges of C2i.

$\overline{F1i}$ must return to a high level after the 8th clock pulse causing DSTo to enter high impedance and preventing futher input data to DSTi. $\overline{F1i}$ will continue to be sampled on every positive edge of C2i. (Note: $\overline{F1i}$ may subsequently be taken low during the same sampling frame to enable entry of serial data into CSTi. This occurs usually mid-frame, in conjunction with CA = V_{DD}, in order to enter an 8-bit control word into Register B. In this case, PCM input and output are inhibited by CA at V_{DD}).

Internally the codec will then perform a decode cycle on the newly input PCM word. The sampled and held analog signal thus decoded will be updated 25 μs from the start of the cycle. After this the analog input from the filter is sampled for 18 μs, after which digital conversion takes place during the remaining 82 μs of the sampling cycle.

Since a single clock frequency of 2.048 MHz is required, all digital data is input and output at this rate. DSTo, therefore, assumes a high impedance state for all but 3.9 μs of the 125 μs frame. Similarly, DSTi input data is valid for only 3.9 μs.

Digital Control Functions

CSTi is a digital input (levels GNDD to V_{DD}) which is used to control the function of the filter/codec. It operates in 3 different modes depending on the logic levels applied to the Control Address input (CA) and chip enable input ($\overline{F1i}$) (See Table 1).

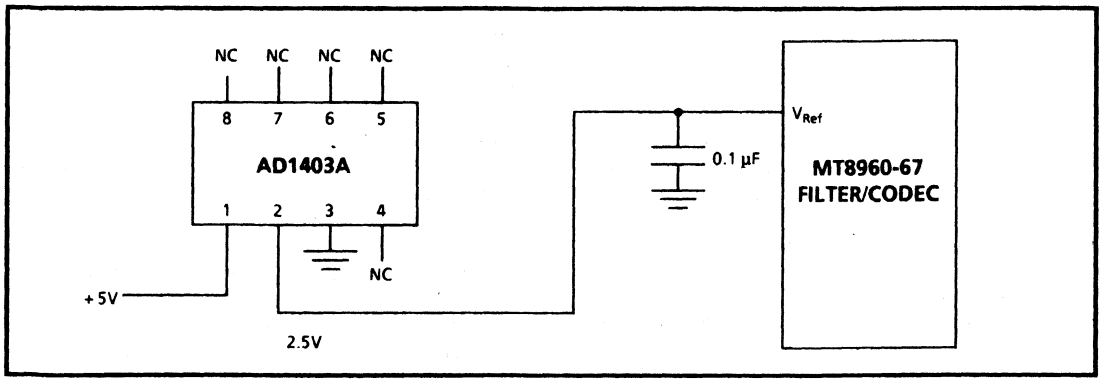


Figure 11. Typical Voltage Reference Circuit

Table 1
DIGITAL CONTROL MODES

MODE	CA	CSTi	FUNCTION
1	V_{EE}	GNDD	Normal chip operation
		V_{DD}	Power Down
2	V_{EE}	Serial Data	8-bit control word into register A. Register B is reset
3	GNDD	Serial Data	8-bit control word into Register A. Register B unaffected
	V_{DD}	Serial Data	8-bit control word into Register B. Register A unaffected
Note 1:	$\overline{F1i}$ at GNDD for each mode of operation.		
Note 2:	PCM input and output inhibited by CA = V_{DD} when in Mode 3.		

Mode 1

CA = -5V (VEE); CSTi = 0V (GNDD)

The filter/codec is in normal operation with nominal transmit and receive gain of 0dB. The SD outputs are in their active states and the test modes cannot be entered.

CA = -5V (V_{EE}); CSTi = +5V (V_{DD})

A state of power-down is forced upon the chip whereby DSTo becomes high impedance, V_R is connected to GNDA and all analog sections have power removed.

Mode 2

CA = -5V (V_{EE}); CSTi receives an 8-bit control word

CSTi accepts a serial data stream synchronously with DSTi (ie, it accepts an 8 bit serial word in a 3.9 µs timeslot, updated every 125 µs, and is specified identically to DSTi for timing considerations). This 8 bit control word is entered into Control Register A and enables programming of the following functions: transmit and receive gain, power-down, loopback. Register B is reset to zero and the SD outputs assume their inactive state. Test modes cannot be entered.

Mode 3

CA = 0V (GNDD); CSTi receives an 8-bit control word

As in Mode 2, the control word enters Register A and the aforementioned functions are controlled. In this mode, however, register B is not reset, thus not affecting the states of the SD outputs.

CA = + 5V (V_{DD}); CSTi receives an 8-bit control word

In this case the control word is transferred into Register B. Register A is unaffected. The input and output of PCM data is inhibited.

The contents of Register B control the six uncommitted outputs SD0-SD5 (four outputs, SD0-SD3, on MT8960/61/64/65 versions of chip) and also provide entry into one of the three test modes of the chip.

Note: For Modes 1 and 2, $\overline{F1i}$ must be at logic low for one period of 3.9 µs, in each 125 µs cycle, when PCM data is being input and output, and the control word at CSTi enters Register A. For Mode 3, $\overline{F1i}$ must be at a logic low for two periods of 3.9 µs, in each 125 µs cycle. In the first period, CA must be at GNDD or V_{EE}, and in the second period CA must be high (V_{DD}).

Control Registers A, B

The contents of these registers control the filter/codec functions as described in Tables 2 and 3.

Bit 7 of the registers is the MSB and is defined as the first bit of the serial data stream input (corresponding to the sign bit of the PCM word).

On initial power-up these registers are set to the power-down condition for a maximum of 25 clock cycles, during which time it is impossible to change the data in these registers.

Chip Testing

By enabling Register B with valid data (8 bit control word input to CSTi when $\overline{F1i}$ = GNDD and CA = V_{CC}) the chip testing mode can be entered. Bits 6 and 7 (most sig. bits) define states for testing the transmit filter, receive filter and the codec function. The input in each case is V_X input and the output in each case is V_R output. (See Table 3 for details)

Loopback

Loopback of the filter/codec is controlled by the control word entered into Register A. Bits 6 and 7 (most sign bits) provide either a digital or analog loopback condition. Digital loopback is defined as follows:

- PCM input data at DSTi is staticized normally in the PCM input register and the output of this register is connected to the input of the 3-state PCM output buffer.
- The digital input to the codec is forced to (-0).
- The output of the PCM encoder is disabled and thus the encoded data is lost. The PCM output at DSTo is determined by the PCM input data.

Table 2

CONTROL STATES - REGISTER A

BIT 2	BIT 1	BIT 0	TRANSMIT (A/D) FILTER GAIN (dB)
0	0	0	0
0	0	1	+ 1
0	1	0	+ 2
0	1	1	+ 3
1	0	0	+ 4
1	0	1	+ 5
1	1	0	+ 6
1	1	1	+ 7
BIT 5	**BIT 4**	**BIT 3**	**RECEIVE (D/A) FILTER GAIN (dB)**
0	0	0	0
0	0	1	-1
0	1	0	-2
0	1	1	-3
1	0	0	-4
1	0	1	-5
1	1	0	-6
1	1	1	-7
BIT 7	**BIT 6**	**FUNCTION CONTROL**	
0	0	Normal operation	
0	1	Digital Loopback	
1	0	Analog Loopback	
1	1	Power-Down	

Analog loopback is defined as follows:

- PCM input data is staticized, decoded and filtered as normal but not output at V_R.
- Analog output buffer at V_R has its input shorted to GNDA and disconnected from the receive filter output.
- Analog input at V_X is disconnected from the transmit filter input.
- The receive filter output is connected to the transmit filter input. Thus the decode signal is fed back through the receive path and encoded in the normal way. The analog output buffer at V_R is not tested by this configuration.

In both cases of loopback, DSTi is the input and DSTo is the output.

Logic Control Outputs SD0-5

These outputs are directly controlled by the logic states of bits 0-5 in Register B. A logic low (GNDD) in Register B causes the SD outputs to assume an inactive state. A logic high (V_{DD}) in Register B causes the SD outputs to assume an active state (see Table 3). SD0-2 switch between GNDD and V_{DD} and may be used to control external logic or transistor circuitry, for example, that employed on the line card for performing such functions as relay drive for application of ringing to line, message waiting indication, etc.

SD3-5 are used primarily to drive external analog circuitry. Examples may include the switching in

TABLE 3
CONTROL STATES - REGISTER B

BITS 0-2		LOGIC CONTROL OUTPUTS SD0-SD2
0		Inactive state - logic low (GNDD)
1		Active state - logic high (V_{DD})
BIT 3		**LOGIC CONTROL OUTPUT SD_3**
0		Inactive state - High Impedance
1		Active state - GNDA
BITS 4,5		**LOGIC CONTROL OUTPUTS SD_4, SD_5**
0		Inactive state - High Impedance
1		Active state - GNDD
BIT 7	**BIT 6**	**CHIP TESTING CONTROLS**
0	0	Normal operation
0	1	Transmit filter testing i.e.:
		Transmit filter input connected to V_X input
		Receive filter and Buffer disconnected from V_R
1	0	Receive filter testing i.e.:
		Receive filter input connected to V_X input
		Receive filter input disconnected from codec
1	1	Codec testing i.e.:
		Codec analog input connected to V_X
		Codec analog input disconnected from transmit filter output
		Codec analog output connected to V_R
		V_R disconnected from receive filter output

or out of gain sections or filter sections (eg. ring trip filter) (Figure 13)

MT8962/8963/8966/8967 provide all six SD outputs.

MT8960/61/64/65 each packaged in an 18-pin DIP provide only four control outputs, SD0-3.

Power-Down

Power-down of the chip is achieved in several ways:

Internal Control:

1) Initial Power-Up. Initial application of V_{DD} and V_{EE} causes power-down for a period of 25 clock cycles and during this period the chip will accept input only from C2i. The B-register is reset to zero forcing SD0-5 to be inactive. Bits 0-5 of Register A (gain adjust bits) are forced to zero and bits 6 and 7 of Register A become logic high thus reinforcing the power-down.

2) Loss of C2i. Power-down is entered 10 to 40 µs after C2i has assumed a continuous logic high (V_{DD}). In this condition the chip will be in the same state as in (1) above.

   Note: If C2i stops at a continuous logic low (GNDD), the digital data and status is indeterminate.

External Control:

1) Register A. Power-down is controlled by bits 6 and 7 (when both at logic logic high) of Register A which in turn receives its control word input via CSTi, when $\overline{F1i}$ is low and CA input is either at V_{EE} or GNDD. Power is removed from the filters and analog sections of the chip. The analog ouput buffer at V_R will be connected to GNDA. DSTo becomes high impedence and the clocks to the majority of the logic are stopped. SD outputs are unaffected and may be updated as normal.

2) CSTi Input. With CA at V_{EE} and CSTi held at continuous logic high the chip assumes the same state as described in External Control (1) above.

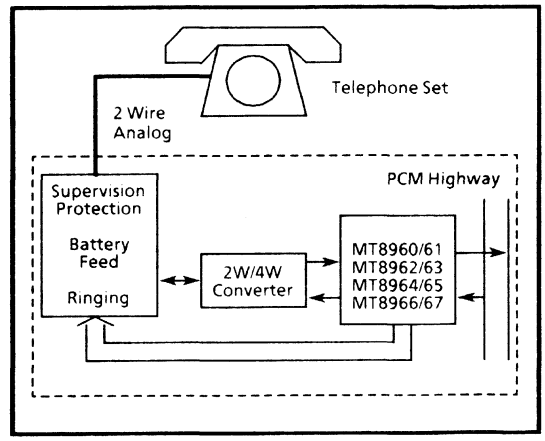


Figure 12. Typical Line Termination

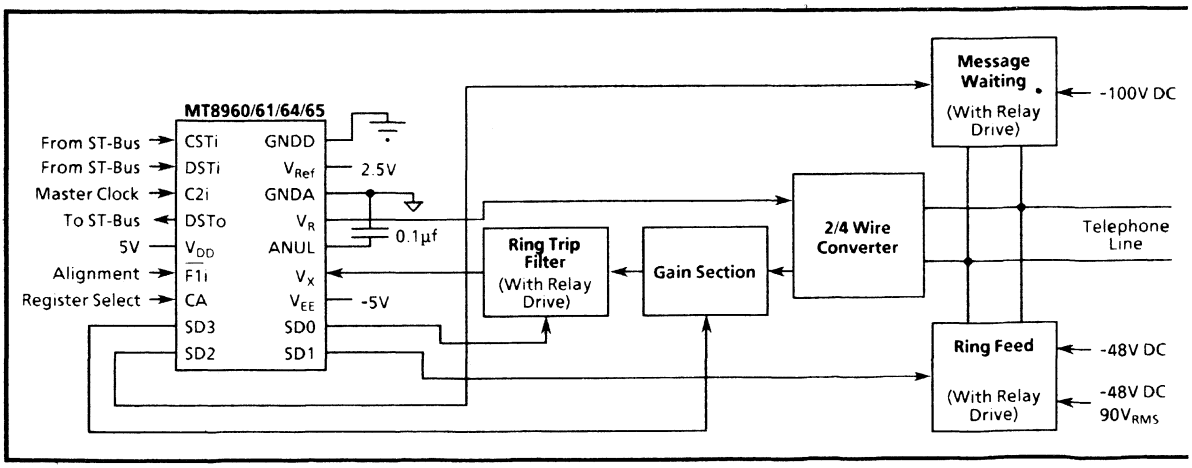


Figure 13. Typical Use of the Special Drive Outputs

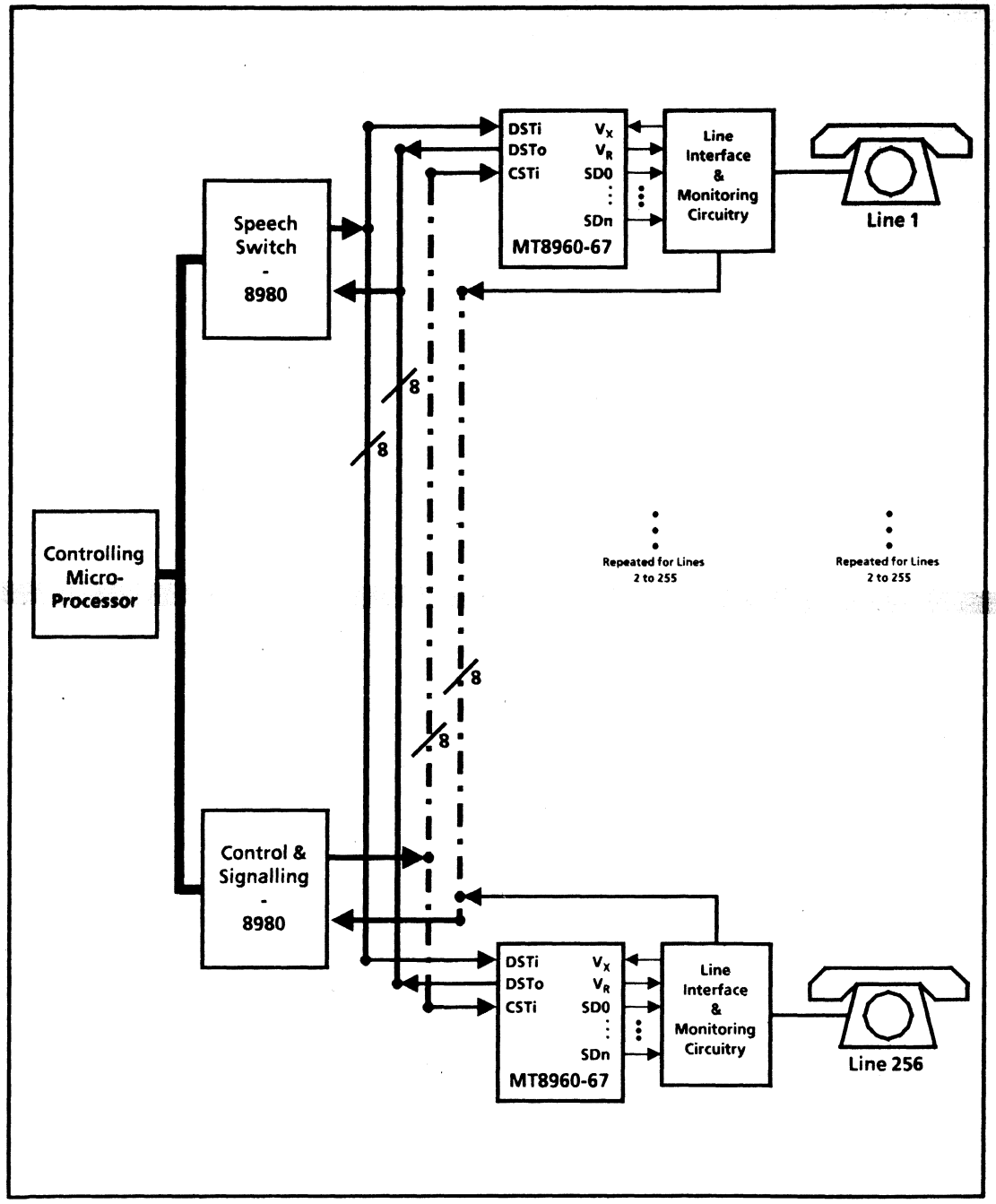


Figure 14. Example Architecture of a Simple Digital Switching System Using The MT8960-67

MITEL

ST-BUS™ FAMILY MH89610

µ-Law Subscriber Line Interface Circuit

Preliminary Information

9161-002-067-NA ISSUE 1 JUNE 1986

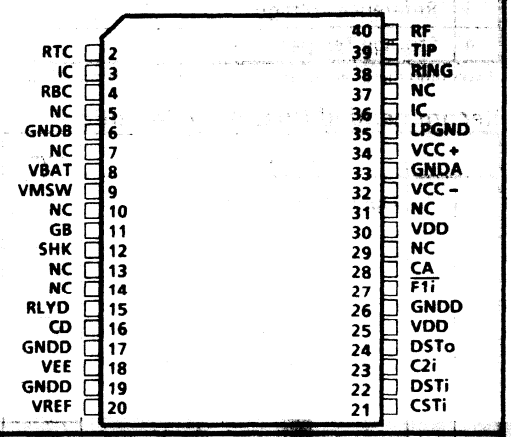
Features

- MITEL ST-BUS™ compatible
- Transformerless 2 to 4 wire conversion
- A/D and D/A conversion
- Conforms with µ-law PCM
- Ground button detection
- Switch hook detection
- Message waiting lamp control
- Ring trip filter
- Ring relay driver
- 600 ohms input impedance
- Audio transmit and receive gain control
- Analog and digital loopback

Applications

- Digital PBX Subscriber Line Card
- Control System
- Key Telephone System

Pin Connections



Ordering Information

MH89610AT	40 Pin DIL Lead Frame Hybrid Package with Plastic Lid
MH89610AS	40 pin DIL C-Clip Lead with a Socket Assembly

0°C TO 70°C

Description

The Mitel MH89610 is an on-premise SLIC interface between digital equipment (PABX) and the subscriber loop. In conjunction with a minimum number of external components, it performs the BORSCHT functions associated with the analog line circuit. The device is fabricated using thick film hybrid and ISO²-CMOS technology to provide those functions requiring high power dissipation, low power consumption and optimum circuit packing density.

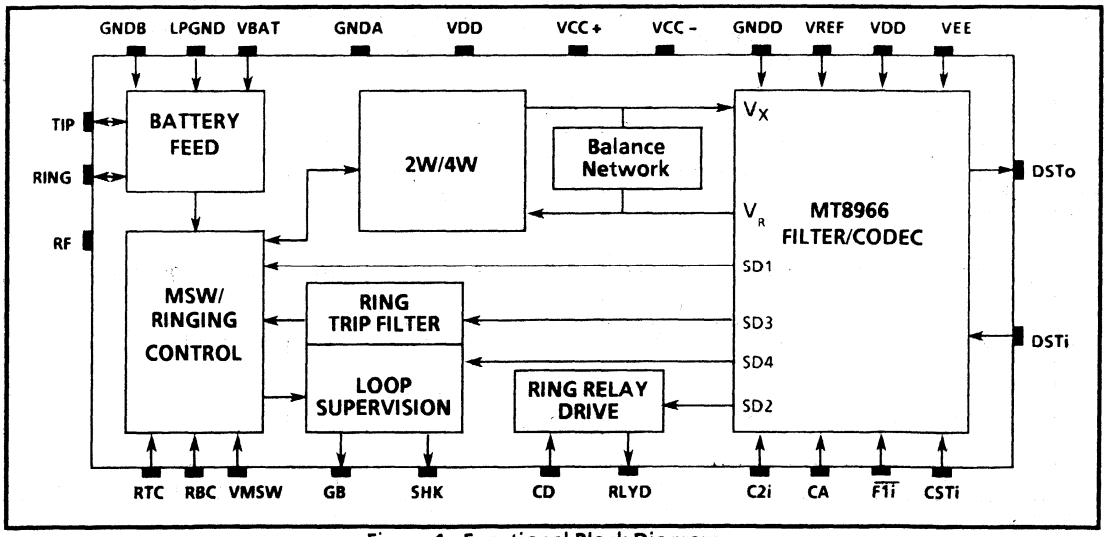


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to GNDD unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD}	-0.3	+6.0	V
		V_{EE}	-6.0	-0.3	V
		V_{CC+}		+18.0	V
		V_{CC-}	-18.0		V
2	Clamp Diode Reverse Breakdown Voltage	V_{CD}	70		V
3	Reference Voltage	V_{REF}	GNDA	V_{DD}	V
4	Storage Temperature	T_{STG}	-20	+85	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to GNDD unless otherwise stated.

		Characteristics		Sym	Min	Typ‡	Max	Units	Comments
1		Operating Supply Voltage		V_{DD}	4.75	5.0	5.25	V	
				V_{EE}	-5.25	-5.0	-4.75	V	
				V_{Ref}	2.4825	2.5	2.5125	V	See Note 1
				V_{cc+}	11.4	12.0	12.6	V	
				V_{cc-}	-12.6	-12.0	-11.4	V	
2		Operating Current	V_{DD}	I_{DD}	2.2	4.8	10.0	mA	
			V_{EE}	I_{EE}	-10.0	-3.5	-2.0	mA	
			V_{Ref}	I_{Ref}		2.0		µA	
			V_{cc+}	I_{cc+}	1.0	3.5	5.0	mA	
			V_{cc-}	I_{cc-}	-5.0	-2.3	-1.0	mA	
3		Power Consumption		P_C			223 523	mW mW	Stand-by Active
4		Operating Temperature		T_O	0		70	°C	

Note 1: Temperature coefficient of V_{Ref} should be better than 100 ppm/°C.
‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics for Digital Interface - Voltages are with respect to GNDD unless otherwise stated.

T_O = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Outputs unloaded unless otherwise specified

		Characteristics		Sym	Min	Typ†	Max	Units	Test Conditions
1	DIGITAL	Input Current	Except CA	I_I			10.0	µA	V_{IN} = GNDD to V_{DD}
			CA	I_{IC}			10.0	µA	V_{IN} = V_{EE} to V_{DD}
2		Input Low Voltage	Except CA	V_{IL}	0.0		0.8	V	
			CA	V_{ILC}	V_{EE}		V_{EE} + 1.2	V	
3		Input High Voltage	All Inputs	V_{IH}	2.4		5.0	V	
4		Input Intermediate Voltage	CA	V_{IIC}	0.0		0.8	V	
5		Output Leakage Current	DSTo	I_{OZ}	-1.0	±0.1	1.0	µA	Output High Impedance
6		Output Low Voltage	DSTo	V_{OL}			0.4	V	I_{OUT} = 1.6mA
7		Output High Voltage	DSTo	V_{OH}	4.0			V	I_{OUT} = -100µA
8		Output Capacitance	DSTo	C_{OUT}		4.0		pF	Output High Impedance

† Typical figures are at 25°C with nominal ±5V supplies and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - TIP/RING Line State Outputs

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Output High Voltage GB SHK		 10.4 2.7	 10.7 3.80	 12.0 5.0	 V V	 No Load No Load
2	Output Low Voltage GB SHK		 -12.0 -5.0	 -11.4 -3.30	 -10.0 -2.80	 V V	 No Load No Load
3	Output Short Circuit Current GB SHK		 0.67	 0.71 -18.0		 mA mA	

* Typical figures are at 25°C with nominal ±5V and ±12V supplies and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Audio Transmission

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Ringing Voltage (RMS) Frequency	V_R		90 20		V Hz	
2	**Battery Feed Voltage**	V_{BAT}		**-27**		**V**	
3	Operating Loop Resistance	R_{LOOP}		400		Ω	
4	Operating Loop Current	I_{LOOP}	13.6	20	44	mA	
5	Message Waiting Output Voltage	V_{MSWO}	-109	-107	-103	V_{DC}	on External Tip/Ring V_{MSW} = -140 V_{DC}
6	Ground Button Detection Resistance Threshold	R_{GB}			800	Ω	
7	Switch Hook Detect Time with Ring Trip Filter Activated		25	38	40	ms	
8	Tip Feed Voltage	V_{TF}	-1.52	-1.50	-1.48	V_{DC}	V_{BAT} = -27 V_{DC}
9	Ring Feed Voltage	V_{RF}	-23.98	-23.66	-23.51	V_{DC}	V_{BAT} = -27 V_{DC}
10	Transhybrid Loss (single frequency) into 600Ω		 -30	-29 -41 -26		dB dB dB	0.2kHz 1.0kHz 3.0kHz
11	Single Frequency 2-Wire return loss		20 25 25	28 44 44		dB dB dB	0.2kHz 1.0kHz 3.0kHz
12	Single Frequency Signal Balance		-45 -40 -32	-53 -44 -35		dB dB dB	0.2kHz 1.0kHz 3.0kHz
13	Single Frequency Longitudinal Balance		57 53	63 64		dB dB	0.2 - 1.0kHz 1.0 - 3.0kHz

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics for Digital Interface - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Outputs unloaded unless otherwise specified.

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	DIGITAL	Clock Frequency	C2i	f_C	2.046	2.048	2.05	MHz	See Note 2
2		Clock Rise Time	C2i	t_{CR}			50	ns	
3		Clock Fall Time	C2i	t_{CF}			50	ns	
4		Clock Duty Cycle	C2i		40	50	60	%	
5		Chip Enable Rise Time	$\overline{F1i}$	t_{ER}			100	ns	
6		Chip Enable Fall Time	$\overline{F1i}$	t_{EF}			100	ns	
7		Chip Enable Setup Time	$\overline{F1i}$	t_{ES}	50			ns	See Note 3
8		Chip Enable Hold Time	$\overline{F1i}$	t_{EH}	25			ns	See Note 3
9		Output Rise Time	DSTo	t_{OR}			100	ns	
10		Output Fall Time	DSTo	t_{OF}			100	ns	
11		Propagation Delay Clock to Output Enable	DSTo	t_{PZL}			122	ns	
				t_{PZH}			122	ns	R_L = 10kΩ to V_{CC}
12		Propagation Delay Clock to Output	DSTo	t_{PLH}			100	ns	C_L = 100 pF
				t_{PHL}			100	ns	
13		Input Rise Time	CSTi	t_{IR}			100	ns	
			DSTi				100	ns	
14		Input Fall Time	CSTi	t_{IF}			100	ns	
			DSTi				100	ns	
15		Input Set Up Time	CSTi	t_{ISH}	25			ns	
			DSTi	t_{ISL}	0			ns	
16		Input Hold Time	CSTi	t_{IH}	60			ns	
			DSTi		60			ns	
17		Digital Loopback Time DSTi to DSTo		t_{DL}			122	ns	

* Typical figures are at 25°C with nominal ±5V supplies and are for design aid only: not guaranteed and not subject to production testing. (See Figures 2a, 2b, 2c)

Note 2: The filter characteristics are totally dependent upon the accuracy of the clock frequency but providing $\overline{F1i}$ is synchronized to C2i, the codec function is unaffected by changes in the clock frequency.

Note 3: This gives a 75 ns period, 50 ns before and 25 ns after the 50% point of C2i rising edge, when any change in $\overline{F1i}$ will give an undetermined state to the internally synchronized enable signal.

AC Electrical Characteristics- Transmit (A/D) Path - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70° C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{REF} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Absolute Gain	G_{AX}	-3.25	-3.0	-2.75	dB	0dB gain in Codec (Gain is selectable from -4 to +3dB, in 1dB step via Codec). See Note 4
2	Max. Analog Input Level at Tip/Ring before overload	V_{IN}		6.17		dBm	0dB gain in Codec
				-0.83		dBm	7dB gain in Codec
3	Gain Tracking	GT_X					Sinusoidal input level @ 1020Hz
	AT &T		-0.25		+0.25	dB	+3 to -40 dBm0
	CCITT G.712		-0.50		+0.50	dB	-40 to -50 dBm0
	(Method 2)		-1.50		+1.50	dB	-50 to -55 dBm0
4	Quantization Distortion	D_{QX}					Sinusoidal input level @ 1020Hz
	AT & T		35.3			dB	0 to -30 dBm0
	CCITT G.712		29.3			dB	-40 dBm0
	(Method 2)		24.3			dB	-45 dBm0
5	Idle Channel Noise	N_{CX}					C-Message
				15	18	dBrnC0	7dB gain in Codec
6	Frequency Response w.r.t. 1020Hz, +4dBm Sinusoidal level on Tip/Ring	G_{RX}		-52	-30	dB	60Hz (See Fig. 4)
				-2.5		dB	140Hz
			-0.25		+0.25	dB	300-3000Hz
				-1.0		dB	3400Hz
				-4.0		dB	3600Hz

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 4: 0dBm on Tip/Ring will appear as -3dBm0 on DSTo of the hybrid. This implies -3dB gain.

AC Electrical Characteristics- Receive (D/A) Path - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70° C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{REF} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Absolute Gain	G_{AR}	-3.25	-3.0	-2.75	dB	0dB gain in Codec (Gain is selectable from -4 to +3dB, in 1dB steps via Codec). See Note 5
2	Maximum Analog Output Level at Tip/Ring	V_{OUT}		6.17		dBm	0dB gain in Codec
3	Gain Tracking	GT_R					Sinusoidal input level @ 1020Hz :
	AT &T		-0.25		+0.25	dB	+3 to -40 dBm0
	CCITT G.712		-0.50		+0.50	dB	-40 to -50 dBm0
	(Method 2)		-1.50		+1.50	dB	-50 to -55 dBm0
4	Quantization Distortion	D_{QR}					Sinusoidal input level @ 1020Hz:
	AT & T		36.4			dB	0 to -30 dBm0
	CCITT G.712		30.4			dB	-40 dBm0
	(Method 2)		25.4			dB	-45 dBm0
5	Idle Channel Noise	N_{CR}					C-Message
				9.3	12	dBrnC0	0dB gain in Codec
6	Frequency Response w.r.t. 1020Hz, +0dBm0 Sinusoidal level on Tip/Ring	G_{RR}	-0.25		+0.25	dB	300Hz to3000Hz (See Fig.5)
				-0.8		dB	3400Hz
				-3.6		dB	3600Hz

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 5 : 0dBm0 into DSTi of the hybrid will appear -3dBm at Tip/Ring. This implies a -3dB gain.

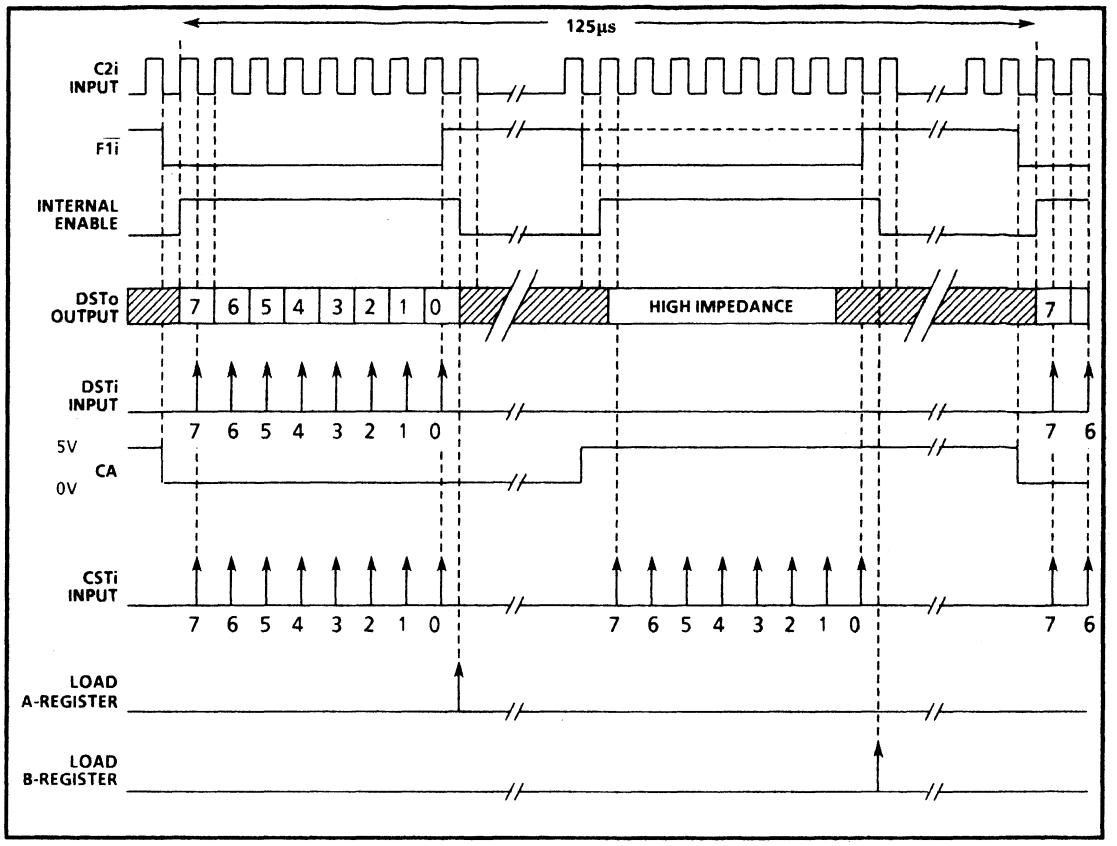


Figure 2a - Timing Diagram - 125µs Frame Period

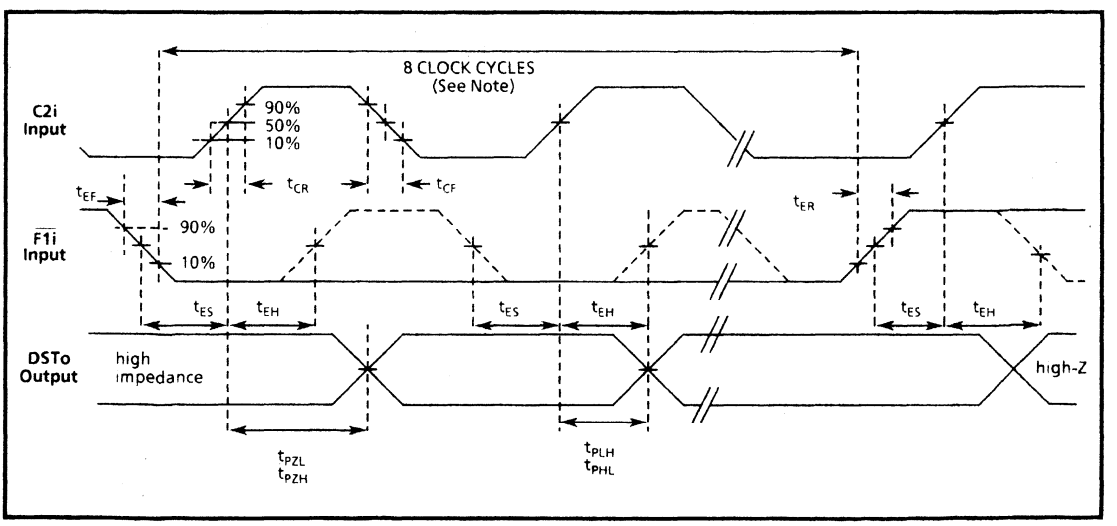


Figure 2b -Timing Diagram - Output Enable

Note: In typical applications, $\overline{F1i}$ will remain low for 8 cycles of C2i. However, the device will function normally as long as t_{ES} and t_{EH} are met at each positive edge of C2i.

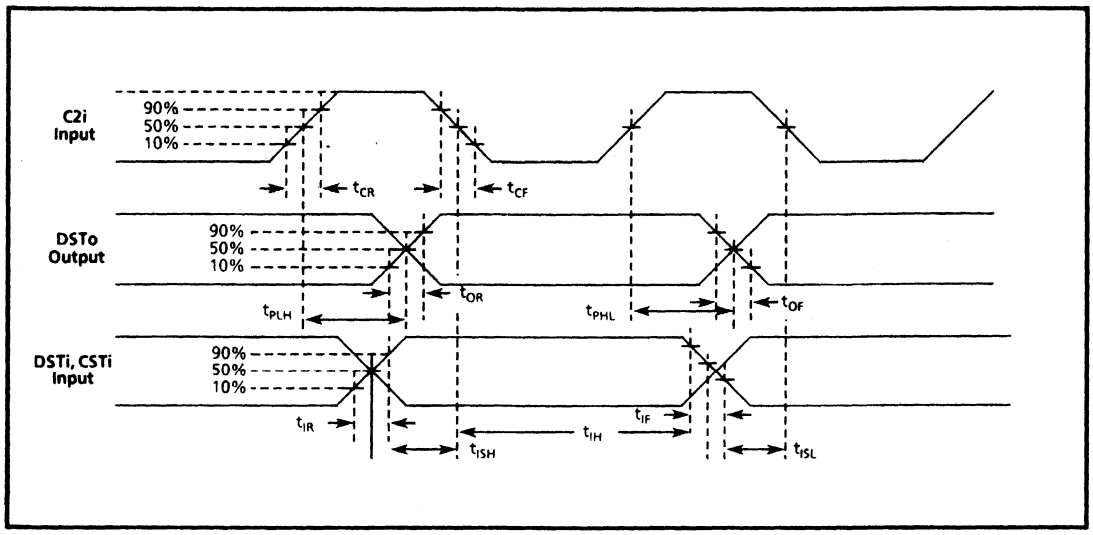


Figure 2c -Timing Diagram - Input/Output

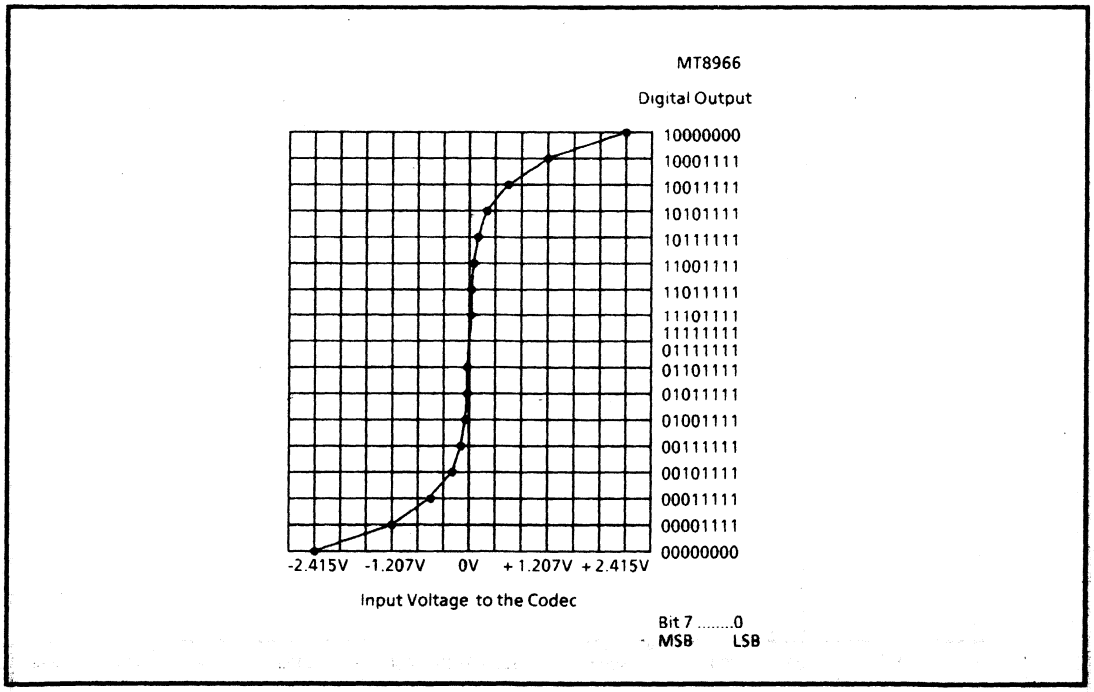


Figure 3 - μ-Law Encoder Transfer Characteristic

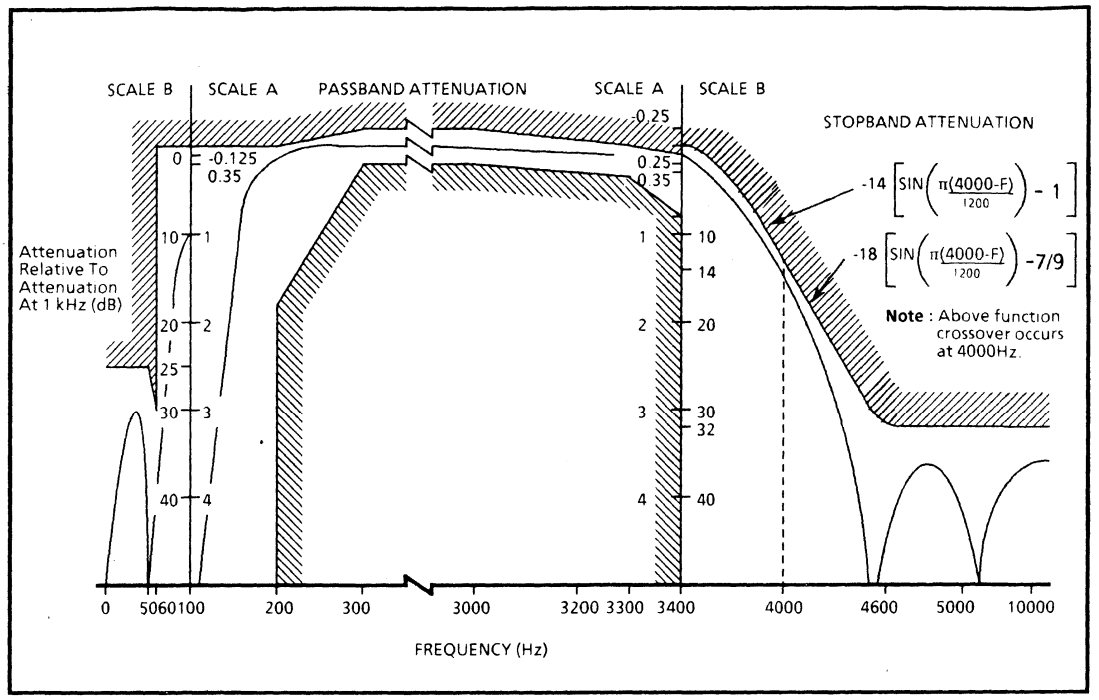


Figure 4 - Attenuation vs. Frequency for Transmit (A/D) Filter

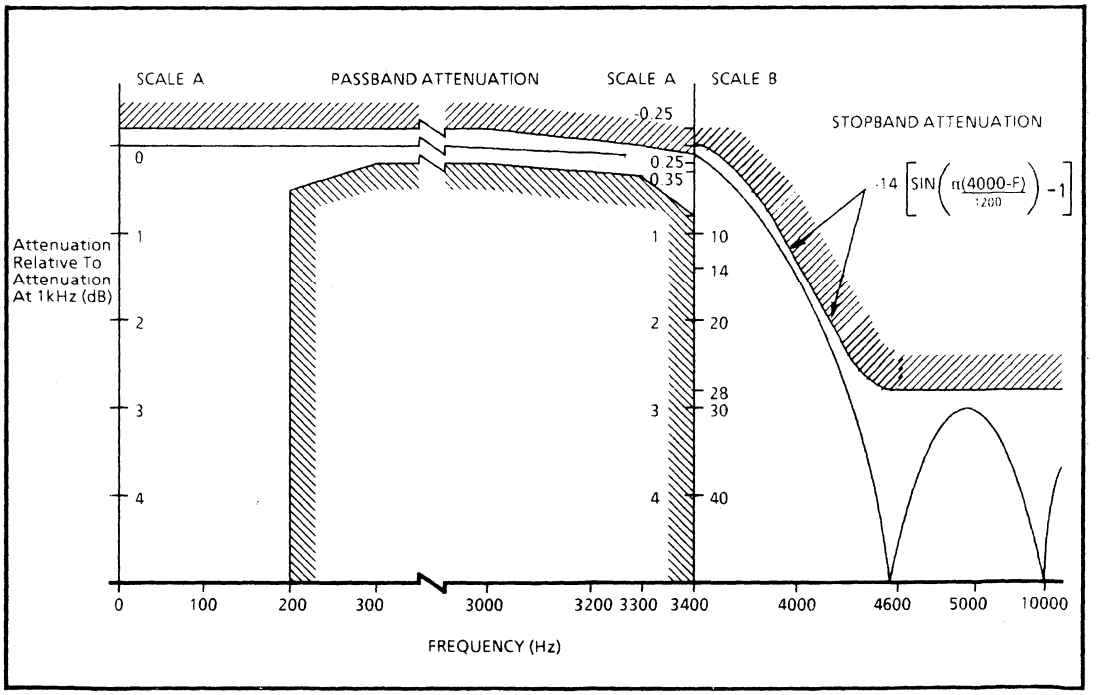


Figure 5 - Attenuation vs. Frequency for Receive (D/A) Filter

Pin Description

Pin #	Name	Description
2	RTC	**Ring Trip Contact** .Connects to the external ring relay contact which is normally open.When the external relay is energized,the contact is closed to provide the ringing signal from the external ring source to the subscriber set. Refer to Fig. 8.
3	IC	**Internal Connection** . Leave open circuit.
4	RBC	**Ring Break Contact** . Connects to the external ring relay contact which is normally closed to provide DC path to the RTC (pin 2). When the external relay is energized,the contact is open to prevent high ringing voltage being applied to the internal circuitry. Refer to Fig. 8.
5	NC	**No Connection.**
6	GNDB	**Battery Ground (Input)** is the battery voltage ground reference and should be 27 volts higher than V_{BAT} (pin 8)
7	NC	**No Connection.**
8	V_{BAT}	**Negative Battery feed supply voltage** (-27 volts).
9	V_{MSW}	**Message Waiting Signalling Supply Voltage** (-140 volts) .
10	NC	**No Connection.**
11	GB	**Ground Button Detect (Output)**. Digital output of an internal op-amp (LM358 ± 12V) connects with a 15kΩ resistor in series. Refer to Figure 6. Upon detection of a grounded Ring lead at the subscriber set, the output will go high.
12	SHK	**Switch Hook Detect (Output)**. Digital output of an internal op-amp (LM1458 ± 5V). **Refer to Figure 7.This output goes high when the loop current exceeds 13.6** mA,indicating that the subscriber set is Off-Hook.
13	NC	**No Connection.**
14	NC	**No Connection.**
15	RLYD	**Ring Relay Drive (Output).** Open collector. Controlled by codec register B, Bit 2.
16	CD	**Clamp Diode** - Normally connects to relay positive supply (+ $12V_{DC}$)
17	GNDD	**Digital Ground.**
18	V_{EE}	**Negative power supply voltage** to the codec (-5V).
19	GNDD	**Digital Ground.**
20	V_{REF}	**Voltage Reference (Input)** to the codec (2.5 V ± 0.5%) .
21	CSTi	**Control ST-Bus (Input).** A TTL compatible digital input used to control the function of the filter/codec. Three modes of operation may be selected by applying a logic high (V_{DD}), logic low (GNDD) or an 8- bit serial word, to this input depending on the logic states of CA and $\overline{F1i}$. See Table 1
22	DSTi	**Data ST-Bus (Input)** . Accepts the incoming 8-bit PCM word. Input TTL compatible.
23	C2i	**Clock (Input).** A TTL compatible 2.048 MHz clock.
24	DSTo	**DataST-Bus (Output)**. A tristate digital output drives the PCM bus with the outgoing 8-bit PCM word.
25	V_{DD}	**Positive Power Supply Voltage** to the codec (+ 5V).
26	GNDD	**Digital Ground.**
27	$\overline{F1i}$	**Framing Signal Type 1 (Input).** Active low digital input enabling (in conjunction with CA) the PCM input, PCM output and digital control input. It is internally sampled on every positive edge of the C2i clock and provides frame and channel synchronization.
28	CA	**Control Address (Input).** A three level digital input which enables PCM input and output and determines into which control register (A or B) the serial data, presented at CSTi, is stored.

Pin Description

Pin #	Name	Description
29	NC	**No Connection.**
30	V_{DD}	**Positive Power Supply Voltage** for the analog circuitry (+ 5V).
31	NC	**No Connection.**
32	V_{CC} -	**Negative Power Supply Voltage** for the analog circuitry (-12V).
33	GNDA	**Analog Ground.**
34	V_{CC} +	**Positive Power Supply Voltage** for the analog circuitry (+ 12V).
35	LPGND	**Loop Ground (Input)** is the system ground reference with respect to V_{BAT} (Pin 8).
36	IC	**Internal Connection.** Leave open circuit.
37	NC	**No Connection.**
38	RING	Connects to the "**RING**" lead of the telephone line.
39	TIP	Connects to the "**TIP**" lead of the telephone line.
40	RF	**Ring Feed** . Connects to the "**RING**" lead (Pin 38).

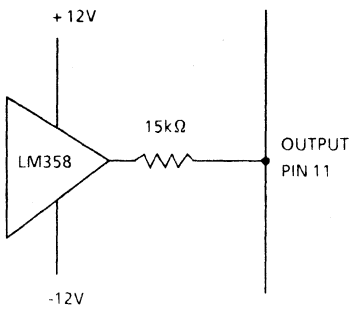


Figure 6 - Output Equivalent Circuit Pin 11

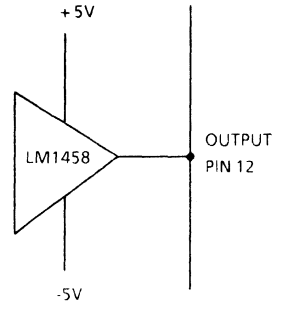


Figure 7-Output Equivalent Circuit Pin 12

Functional Description

Mitel MH89610 provides the SLIC functions of Battery Feed, Ringing, Supervision, Coding, Hybrid and Testing. In addition to these performances, it also provides Switch Hook detection,Ground Button detection and Message Waiting Signalling.

The hybrid function is accomplished by using transformerless 2 wire to 4 wire conversion, between 2W subscriber loop and the 4W internal transmit and receive pairs, which are connected to filter/codec.

Incoming analog (voiceband) signals ,applied differentially across the Tip and Ring from the subscriber loop, are passed through a differential op-amp to achieve maximum longitudinal balance . The output of the op-amp is transmitted to both the filter/codec for A/D conversion and to Tip and Ring Drivers for AC 600 ohms impedance correction. The analog signal entering the filter/codec, is sampled at 8kHz, μ-law companded and assigned an 8-bit digital word. This 8-bit digital word is then serially output at DSTo pin at a nominal rate of 2.048 MHz, via the output buffer as the 8 bits of the 125μs sampling frame. Figure 3 shows the digital output code of the codec on the module.

The 8-bit PCM encoded digital word from the digital network side is serially transmitted to DSTi input of the SLIC where it is decoded and reconstructed into staircase analog signals by the filter/codec. After bandpass filtering in the filter/codec, the audio signals are buffered by the audio Tip Driver to the output of Tip and Ring. A maximum transhybrid loss is provided to ensure that the incoming received signal is not coupled to the transmit pair.

All functions of the SLIC interface are controlled by the System Drive (SD) output of the codec . (see Digital Control Functions for details). The SD control is provided over a dedicated 32 channels ST-BUS serial data link (CSTi). Each SLIC interface requires two channels of data to load the Internal Register A and B of the codec. In total, up to 16 SLIC can be concatenated into one serial bit stream of 32 channels.

Battery Feed

The Battery Feed circuit of MH89610 has a relatively low DC resistance and high AC impedance. It accomplishes this with positive feedback circuits which have different gain for AC and DC signals. The loop current is sourced from a matched pair of resistors connected between V_{BAT}(-27 V_{DC}) and the ground. Because the internal biasing on the line circuit, the effective battery voltage is -22.2 V_{DC} on external Tip and Ring.

Ringing and Ring Trip Detection

The most practical means of detecting an Off-hook condition is by superimposing the ringing voltage on a DC battery supply. This permits an Off-Hook condition to be detected even during ringing cycle by simply observing the DC level.

Ring Trip Detection is achieved by monitoring the status of the switch-hook (SHK) under processor control. During ringing, the bit 3 of the codec register B should be set at 1 so that a time constant of 100 ms is introduced to prevent pre-trip due to a large AC component. If a valid Off-hook condition is detected, the bit 3 of the control register B should be disabled to remove the time constant and set to 0.

Supervision (SHK) and Dial Pulse Detection

One of the key supervisory function of the SLIC is to detect the On-hook or Off-hook condition of the subscriber set, so that dial tone and servicing can be supplied. When a minimum of 13.6 mA DC loop current is detected, the SHK output will go high to indicate an Off-hook condition. Since the dial pulses are periodical interruptions of the DC loop current, the SHK output can be monitored as dial pulses collection,by using external hardware or software debouncing.

Ground Button Detection

The Ground Button Detect pin goes high when the Ring lead to ground voltage exceeds a threshold voltage. If the ring lead at the subscriber set is grounded with a resistance less than 800 ohms,the output of GB will go high. Whether the subscriber set is On-hook or Off-hook, a grounded ring lead will result in output high on both GB and SHK.

Message Waiting Signalling

The Message Waiting feature is a signal to subscriber set. When it is active, it is powered by V_{MSW} of -140 V_{DC} to turn on a neon lamp in the subscriber set to indicate a message is waiting. Owing to the internal voltage drop, the effective voltage across the Ring and Tip lead is about -107 V_{DC}. See Table 3 for details.

Filter/Codec Timing:

The codec operates in a synchronous manner (see Figure 2a). It is activated on the first positive edge of C2i after $\overline{F1i}$ has gone low. The digital output at DSTo (which is a three state output driver) will then change from a high impedance state to the sign bit of the encoded PCM word to be output. This will remain valid until the next positive edge, when the next most significant bit will be output.

On the first negative clock edge (after $\overline{F1i}$ signal has been internally synchronized and CA is at GNDD or V_{EE}) the logic signal present at DSTi will be clocked into the input shift register as the sign bit of incoming PCM word.

The 8-bit word is thus input at DSTi on negative edges of C2i and output at DSTo on positive edges of C2i.

$\overline{F1i}$ must return to a high level after the 8th clock pulse causing DSTo to enter high impedance and preventing further input data to DSTi. $\overline{F1i}$ will continue to be sampled on every positive edge of C2i. (Note: $\overline{F1i}$ may subsequently be taken low during the same sampling frame to enable entry of serial data into CSTi. This occurs usually mid-frame, in conjunction with CA = V_{DD}, in order to enter an 8-bit control word into Register B. In this case, PCM input and output are inhibited by CA at V_{DD}).

Internally the codec will then perform a decode cycle on the newly input PCM word. The sampled and held analog signal, thus decoded, will be updated 25µs from the start of the cycle. After this, the analog input from the filter is sampled for 18µs, after which digital conversion takes place during the remaining 82µs of the sampling cycle.

Since a single clock frequency of 2.048MHz is required, all digital data is input and output at this rate. DSTo, therefore, assumes a high impedance state for all but 3.9µs of the 125µs frame. Similarly, DSTi input data is valid for only 3.9µs.

Digital Control Functions:

CSTi is a digital input (levels GNDD to V_{DD}) which is used to control the function of the filter/codec. The codec operates in three different modes depending on the logic levels applied to Control Address input (CA) and codec enable input ($\overline{F1i}$) (see Table 1).

MODE	CA	CSTi	FUNCTION
1	V_{EE}	GNDD	Normal operation.
		V_{DD}	Power down.
2	V_{EE}	Serial Data	8-bit control word into Register A. Register B is reset.
3	GNDD	Serial Data	8-bit control word into Register A. Register B unaffected.
	V_{DD}	Serial Data	8-bit control word into Register B. Register A unaffected.

Table 1 - Digital Control Modes

Note 1: $\overline{F1i}$ at GNDD for each mode of operation.
Note 2: PCM input and output inhibited by CA = V_{DD} when in Mode 3.

Mode 1

CA = -5V (V_{EE}); CSTi = 0V (GNDD)
The filter/codec is in normal operation with nominal transmit and receive gain of 0dB. The SD outputs are in their active states and the test modes cannot be entered.

CA = -5V (V_{EE}); CSTi = + 5V (V_{DD})
A state of power-down is forced upon the codec whereby DSTo becomes high impedance, transmit filter (V_R) is connected to GNDA and all analog sections have power removed.

Mode 2

CA = -5V (V_{EE}); CSTi receives an 8-bit control word. CSTi accepts a serial data stream synchronously with DSTi (i.e., it accepts an 8-bit serial word in a 3.9µs timeslot, updated every 125µs, and is specified identically to DSTi for timing considerations). This 8 -bit control word is entered into Control Register A and enables programming of the following functions: transmit and receive gain, power-down, loopback. Register B is reset to zero and the SD outputs assume their inactive state. Test modes cannot be entered.

Mode 3

CA = 0V (GNDD); CSTi receives an 8-bit control word. As in Mode 2, the control word enters Register A and the aforementioned functions are controlled. In this mode, however, register B is not reset, thus not affecting the states of the SD outputs.

CA = + 5V (V_{DD}); CSTi receives an 8-bit control word. In this case the control word is transferred

into Register B. Register A is unaffected. The input and output of PCM data is inhibited.

The contents of Register B control four codec outputs, SD4-SD1, which in turn control the output function of the SLIC (see Table 3) and also provide entry into one of the three test modes of the codec.

Note: for Modes 1 and 2, $\overline{F1i}$ must be at logic low for one period of 3.9µs, in each 125µs cycle, when PCM data is being input and output, and the control word at CSTi enters Register A. For Mode 3, $\overline{F1i}$ must be at a logic low for two periods of 3.9µs, in each 125µs cycle. In the first period, CA must be at GNDD or V_{EE}, and in the second period CA must be high (V_{DD}).

7	6	5	4	3	2	1	0
Functional Control		Receive (D/A) Filter Gain			Transmit (A/D) Filter Gain		

BIT 2	BIT 1	BIT 0	TRANSMIT (A/D) FILTER GAIN (dB)
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	+4
1	0	1	+5
1	1	0	+6
1	1	1	+7
BIT 5	**BIT 4**	**BIT 3**	**RECEIVE (D/A) FILTER GAIN (dB)**
0	0	0	0
0	0	1	-1
0	1	0	-2
0	1	1	-3
1	0	0	-4
1	0	1	-5
1	1	0	-6
1	1	1	-7
BIT 7	**BIT 6**	**FUNCTIONAL CONTROL**	
0	0	Normal Operation	
0	1	Digital Loopback	
1	0	Analog Loopback	
1	1	Power Down	

Table 2 - Control States - Register A

Control Registers A & B:

The contents of these registers control the filter/codec functions as described in Tables 2 and 3.

Bit 7 of the registers is the MSB and is defined as the first bit of the serial data stream input (corresponding to the sign bit of the PCM word).

On initial power-up these registers are set to the power-down condition for a maximum of 25 clock cycles, during which time it is impossible to change the data in these registers.

Loopback:

Loopback of the filter/codec is controlled by the control word entered into Register A. Bits 6 and 7 (most significant bits) provide either a digital or analog loopback condition.

Digital loopback is defined as follows:

1) PCM input data at DSTi is loaded into the PCM input register and the output of this register is connected to the input of the 3-state PCM output buffer.

2) The digital input to the codec is forced to (-0).

3) The output of the PCM encoder is disabled and thus the encoded data is lost. The PCM output at DSTo is determined by the PCM input data.

Analog loopback is defined as follows:

1) PCM input data is decoded and filtered as normal but not output at V_R of the codec.

2) Analog output buffered at V_R has its input shorted to GNDA and disconnected from the receive filter output.

3) Analog input to the codec at V_X is disconnected from the transmit filter input.

4) The receive filter output is connected to the transmit filter input. Thus the decode signal is fed back through the receive path and encoded in the normal way. The analog output buffer at V_R is not tested by this configuration.

In both cases of loopback, DSTi is the input and DSTo is the output.

Power-Down

Power-down of the codec is achieved in several ways:

Internal Control

1) Initial Power-Up. Initial application of V_{DD} and V_{EE} causes power-down for a period of 25 clock

7	6	5	4	3	2	1	0
CODEC TESTING		-	Self Test	Ring Trip Filter	Ring Relay	MSW	-

BIT	NAME	DESCRIPTION
0	-	Unused.
1	MSW	A logic '1' will activate a transistor switch on the hybrid to apply -140 VDC to the Ring lead of an idle line to turn on a neon lamp in the subscriber set, which can be interrupted at a rate controlled by software.
2	Ring Relay	When '1', the ring relay will connect the ring source to apply ringing voltage to the line through the ring feed resistor.Upon a valid off-hook detection,this bit should be set to 0.
3	Ring Trip Filter	A logic '1' will introduce a 100 ms time constant to prevent pre-trip on switch hook during the first ringing cycle. It should be set simultaneouly with the activation of ring relay and should remain in circuit until the ringing cycle is complete or until a valid ring trip occurs.
4	Self Test	A logic'1',the SHK output will be forced to high within 2 ms as an Off-hook condition. Primarily, this is used to test an idle line for maintenance purpose.
5	-	Unused.
6,7	Codec Testing	These two bits are used during manufacturing process in testing the codec and must be set to 0 for normal operation.

Table 3 - Control States- Register B

cycles and during this period the codec will accept input only from C2i. The register B is reset to zero forcing SD1-4 to be inactive. Bits 0-5 of Register A (gain adjust bits) are forced to zero and bits 6 and 7 of Register A become logic high, thus reinforcing the power-down.

2) Loss of C2i. Power-Down is entered 10 to 40µs after C2i has assumed a continuous logic low (GNDD), the digital data and status is indeterminate.

External Control

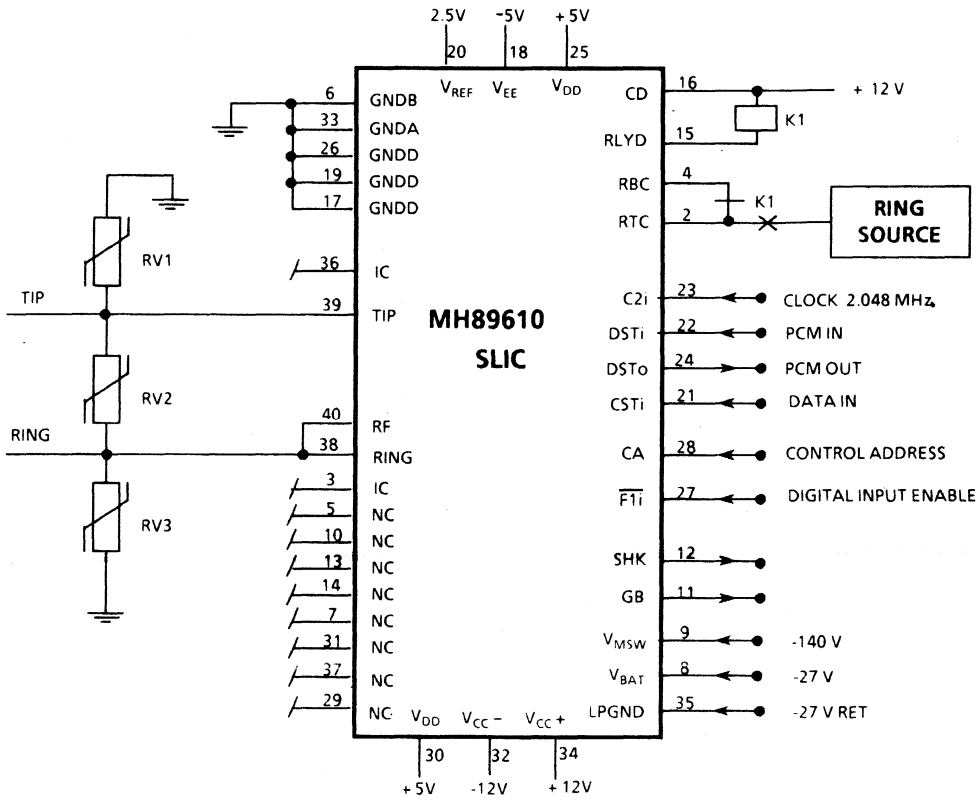
1) Register A. Power-down is controlled by bits 6 and 7 (when both at logic high) of Register A which in turn receives its control word input via CSTi, when $\overline{F1i}$ is low and CA input is either at V_{EE} or GNDD. Power is removed from the filters and analog sections of the codec. The analog output buffer at V_R will be connected to GNDA. DSTo becomes high impedance and the clocks to the majority of the logic are stopped. SD outputs are unaffected and may be updated as normal.

2) CSTi Input. With CA at V_{EE} and CSTi held at continuous logic high, the codec assumes the same state as described in External Control (1) above.

Application

The diagram in Figure 8 illustrates the use of Mitel MH89610 to interface to a subscriber set. Three external varistors are required for overvoltage and line fault protection. When the ring relay (K1) is enabled, it will close one set of contacts to apply ringing voltage to the input of RTC. At the same time, the other set of contacts is open to prevent high ringing voltage being applied at the input of RBC. If an off-hook condition is detected, the ringing voltage can be removed by disabling the ring relay.

Figure 9 shows an external circuit to convert the GB and SHK output into +5V logic output. A typical digital switching system is shown in Figure 10 using the SLIC to interface a subscriber set.



Components List:

RV1,RV2,RV3 = Varistor, V150LA1,430V,8Joules
K1 = Relay,12V 1FORMC Sealed,BR211NADO12M

Figure 8 - Application Circuit

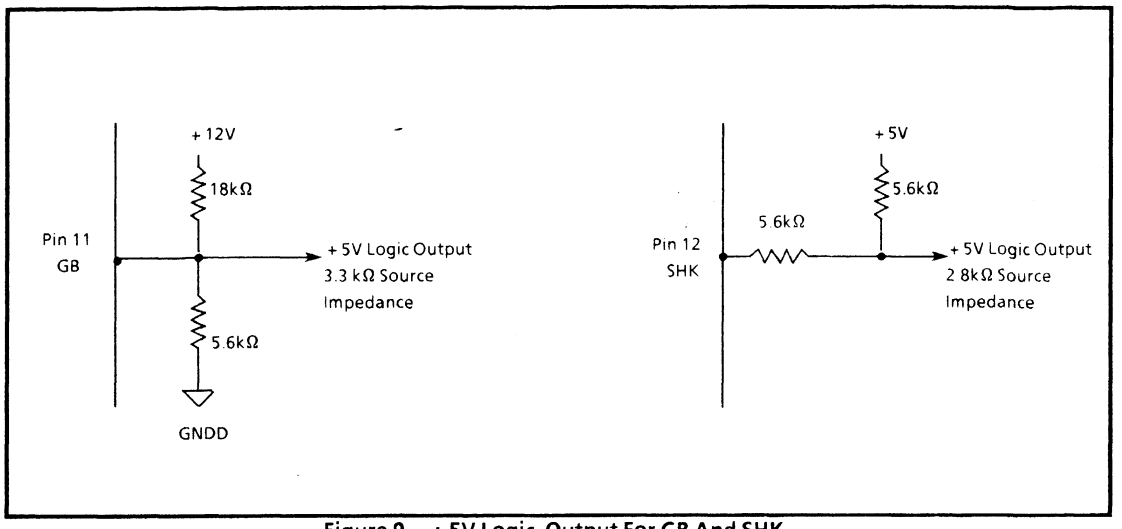


Figure 9 - +5V Logic Output For GB And SHK

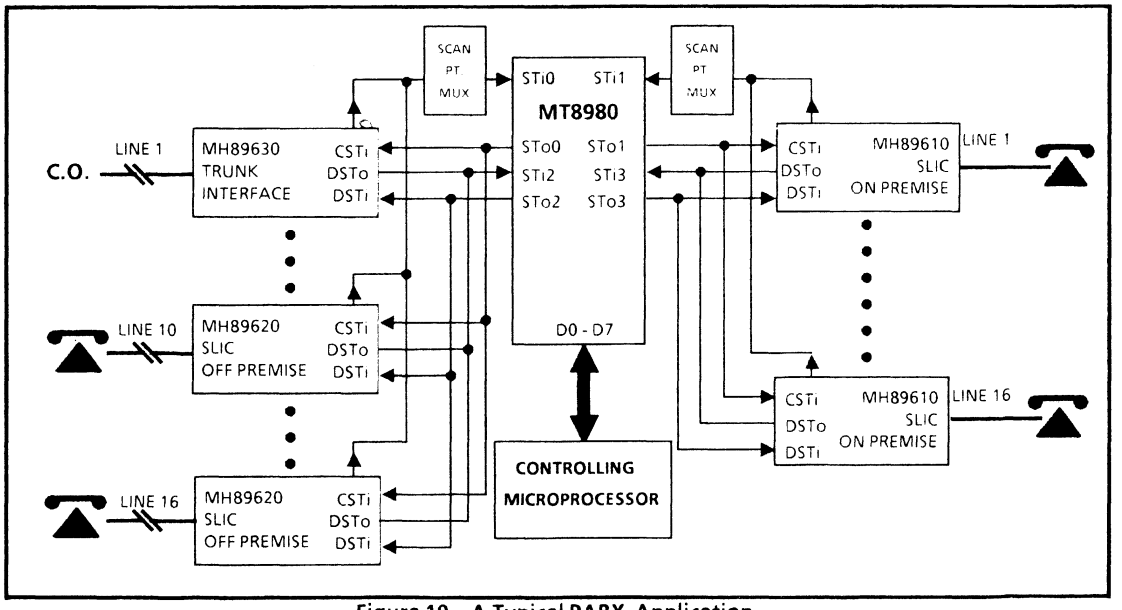


Figure 10 - A Typical PABX Application

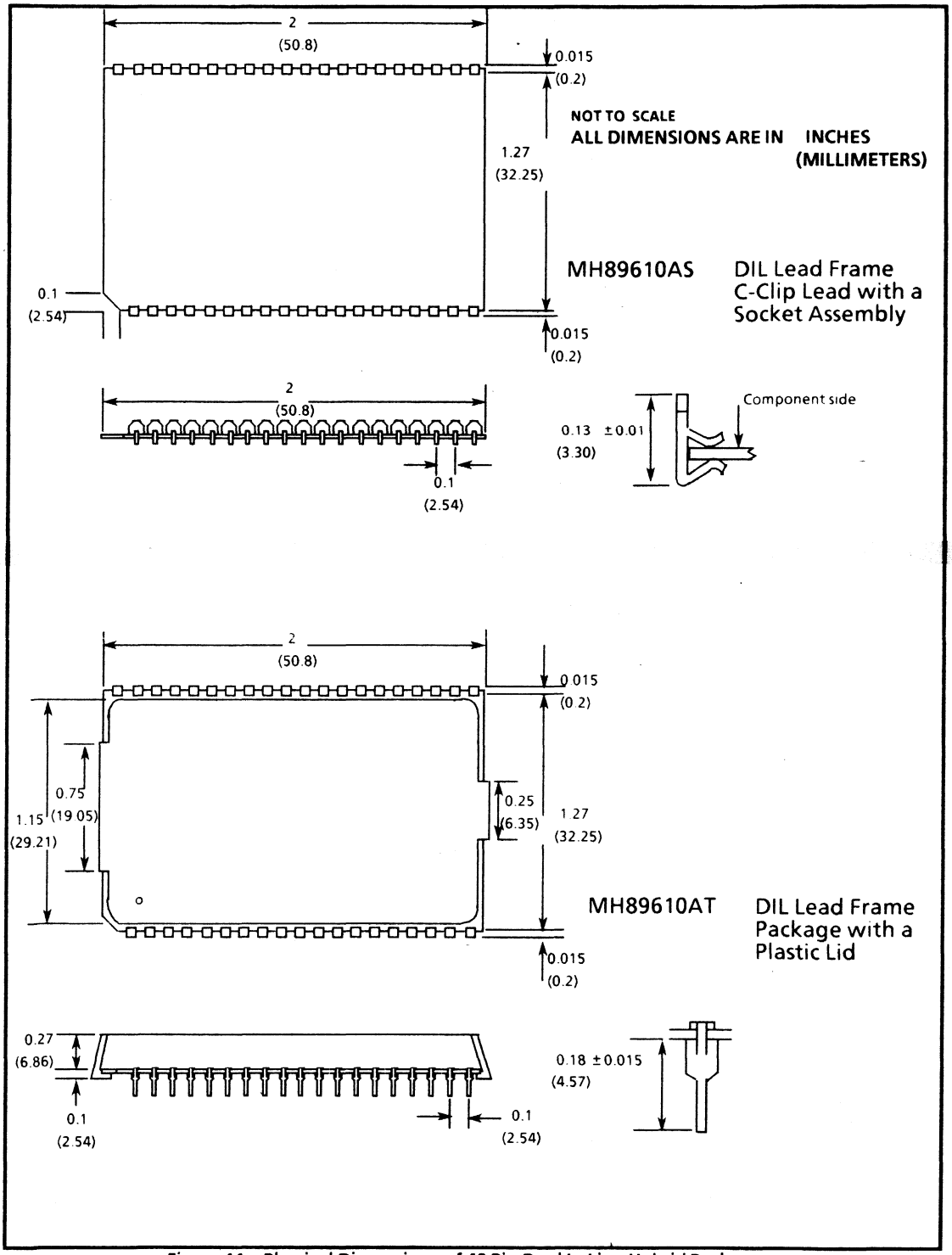


Figure 11 - Physical Dimensions of 40 Pin Dual In Line Hybrid Package

ST-BUS™ FAMILY MH89615
A-Law Subscriber Line Interface Circuit

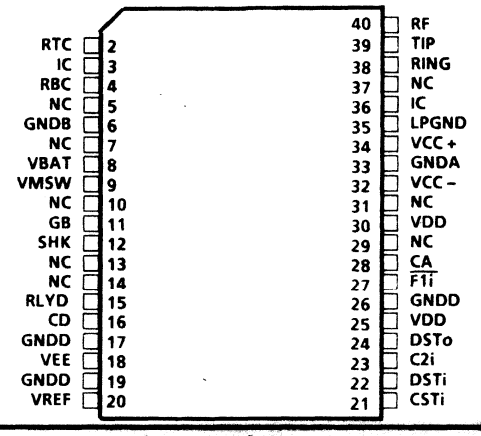
Preliminary Information

9161-002-077-NA ISSUE 1 AUGUST 1986

Features

- MITEL ST-BUS™ compatible
- Transformerless 2 to 4 wire conversion
- A/D and D/A conversion
- Conforms with A-law PCM
- Ground button detection
- Switch hook detection
- Message waiting lamp control
- Ring trip filter
- Ring relay driver
- 600 ohms input impedance
- Audio transmit and receive gain control
- Analog and digital loopback

Pin Connections



Ordering Information

MH89615AT	40 Pin DIL Lead Frame Hybrid Package with Plastic Lid
MH89615AS	40 pin DIL C-Clip Lead with a Socket Assembly

0°C TO 70°C

Applications

- Digital PBX Subscriber Line Card
- Control System
- Key Telephone System

Description

The Mitel MH89615 is an on-premise SLIC interface between digital equipment (PABX) and the subscriber loop. In conjunction with a minimum number of external components, it performs the BORSCHT functions associated with the analog line circuit. The device is fabricated using thick film hybrid and ISO²-CMOS technology to provide those functions requiring high power dissipation, low power consumption and optimum circuit packing density.

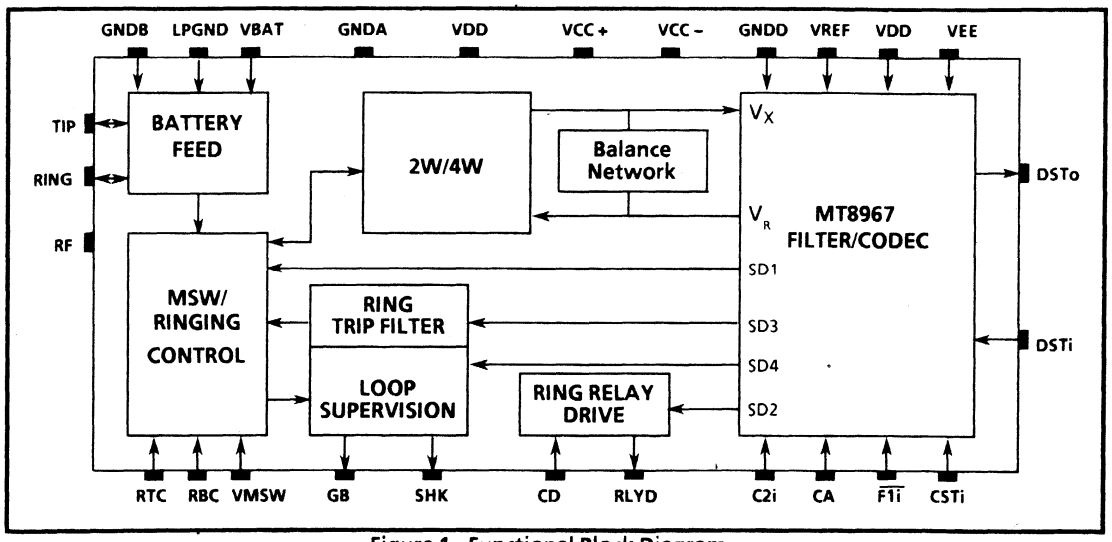


Figure 1- Functional Block Diagram

Refer to the MH89610 Data Sheet for the functional description. Contact your Mitel representative for more information.

ST-BUS™ FAMILY MH89620
μ-Law Subscriber Line Interface Circuit

Preliminary Information

9161-002-068-NA ISSUE 1 JULY 1986

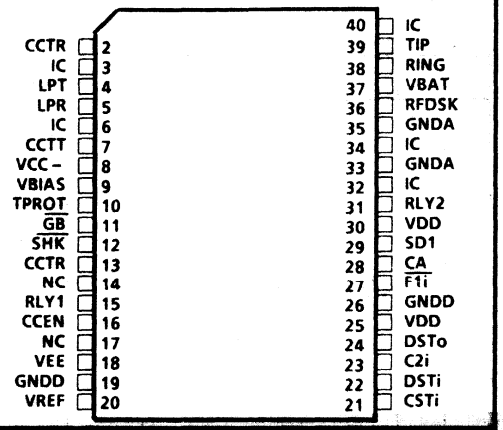
Features

- MITEL ST-BUS™ compatible
- Transformerless 2 to 4 wire conversion
- A/D and D/A conversion
- Conforms with μ-law PCM
- Ground button detection
- Switch hook detection
- Software selectable control
  - -600Ω or AT & T compromise network
  - -Audio transmit and receive gain control
- Ring trip filter
- Ring relay driver
- Two uncommitted control outputs
- Analog and digital loopback

Applications

- Digital PBX Subscriber Line Card
- Control System
- Key Telephone System

Pin Connections



Ordering Information

MH89620AT	40 Pin DIL Lead Frame Hybrid Package with Plastic Lid
MH89620AS	40 pin DIL C-Clip Lead with a Socket Assembly

0°C TO 70°C

Description

The Mitel MH89620 is an off-premise SLIC interface between digital equipment (PABX) and a subscriber loop. It provides a selectable software control balancing network and a maximum longitudinal balance for long loops. With a few external components, it performs the BORSCHT function asssociated with analog line circuit requirement. The device is fabricated using thick film hybrid and ISO²-CMOS technology to achieve high power dissipation, low power consumption, and optimum circuit packing density.

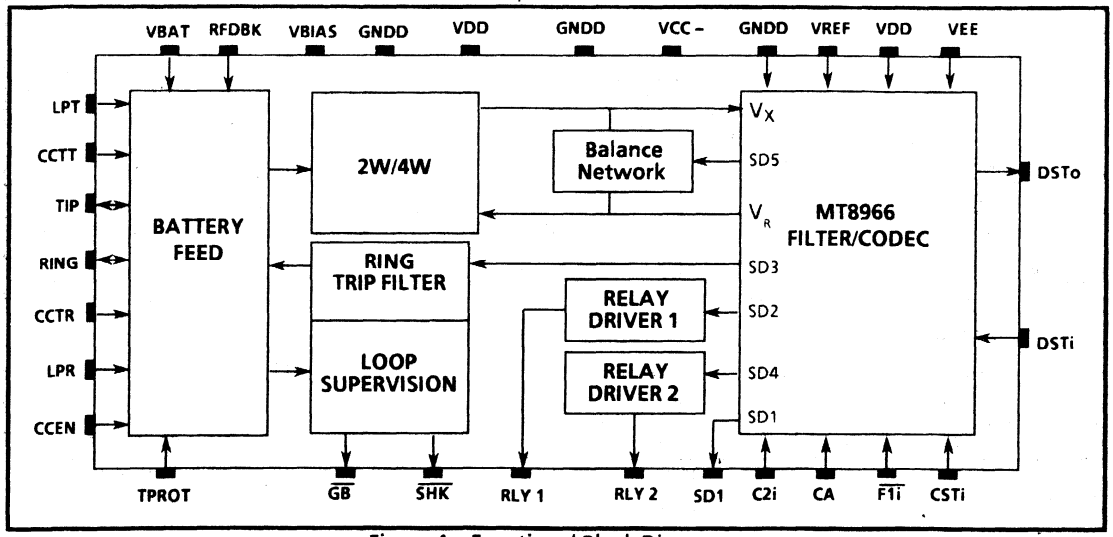


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings*

- Voltages are with respect to GNDD unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD} V_{EE} V_{CC-}	-0.3 -6.0 -31.0	+6.0 -0.3	V V V
2	Reference Voltage	V_{REF}	GNDA	V_{DD}	V
3	Storage Temperature	T_{STG}	-20	+85	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

- Voltages are with respect to GNDD unless otherwise stated.

		Characteristics		Sym	Min	Typ†	Max	Units	Comments
1		Operating Supply Voltage		V_{DD}	4.75	5.0	5.25	V	
				V_{EE}	-5.25	-5.0	-4.75	V	
				V_{Ref}	2.4825	2.5	2.5125	V	See Note 1
				V_{cc-}		-27		V	
				V_{BAT}		-48		V	
2		Operating Current	V_{DD}	I_{DD}		4.3		mA	$R_{Loop} = 600\Omega$
			V_{EE}	I_{EE}		-2.0		mA	$R_{Loop} = 600\Omega$
			V_{Ref}	I_{Ref}		2.0		µA	
			V_{BAT}	I_{BAT}		-40		mA	$R_{Loop} = 600\Omega$
			V_{cc-}	I_{cc-}		-2.0		mA	$R_{Loop} = 600\Omega$
3		Power Consumption		P_C			572 2600	mW mW	Stand-by Active ($R_{Loop} = 343\Omega$ and with external line drivers)
4		Operating Temperature		T_O	0		70	°C	

Note 1: Temperature coefficient of V_{Ref} should be better than 100 ppm/°C.

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics for Digital Interface

- Voltages are with respect to GNDD unless otherwise stated T_O = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0 5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Outputs unloaded unless otherwise specified

		Characteristics		Sym	Min	Typ†	Max	Units	Test Conditions
1		Input Current	Except CA	I_I			10.0	µA	V_{IN} = GNDD to V_{DD}
			CA	I_{IC}			10.0	µA	V_{IN} = V_{EE} to V_{DD}
2		Input Low Voltage	Except CA	V_{IL}	0.0		0.8	V	
			CA	V_{ILC}	V_{EE}		V_{EE} + 1 2	V	
3	D	Input High Voltage	All Inputs	V_{IH}	2.4		5.0	V	
4	I	Input Intermediate Voltage	CA	V_{IIC}	0.0		0.8	V	
5	G	Output Leakage Current	DSTo	I_{OZ}	-1.0	± 0.1	1.0	µA	Output High Impedance
6	I	Output Low Voltage	DSTo	V_{OL}			0.4	V	I_{OUT} = 1.6mA
7	T	Output High Voltage	DSTo	V_{OH}	4.0			V	I_{OUT} = -100µA
8	A L	Output Capacitance	DSTo	C_{OUT}		4.0		pF	Output High Impedance

†Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - TIP/RING Line State Outputs

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Output High Voltage $\overline{GB}$, $\overline{SHK}$		2.7	3.5	5.0	V	No Load
2	Output Low Voltage $\overline{GB}$, $\overline{SHK}$		-5.0	-3.7	-2.7	V	No Load
3	Output Short Circuit Current $\overline{GB}$, $\overline{SHK}$			10.0		mA	

* Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Audio Transmission

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Ringing Voltage (RMS) Frequency	V_R		90 20		V Hz	
2	Battery Feed Voltage	V_{BAT}		-48	-60	V	
3	Operating Loop Resistance	R_{LOOP}		1600		Ω	
4	Operating Loop Current	I_{LOOP}		20	53	mA	
6	Ground Button Detection Resistance Threshold	R_{GB}			800	Ω	
10	Transhybrid Loss into 600Ω		-19 -21 -19			dB dB dB	0.2kHz 1.0kHz 3.0kHz
10	Transhybrid Loss into AT&T Compromise Balance Network		-19 -21 -19			dB dB dB	0.2kHz 1.0kHz 3.0kHz
11	2-Wire return loss		20 25 25			dB dB dB	0.2kHz 1.0kHz 3.0kHz
12	Signal Balance		-46 -46 -46			dB dB dB	0.2kHz 1.0kHz 3.0kHz
13	Longitudinal Balance		58 53			dB dB	0.2 - 1.0kHz 1.0 - 3.0kHz

‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics for Digital Interface - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Outputs unloaded unless otherwise specified.

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	DIGITAL	Clock Frequency	C2i	f_C	2.046	2.048	2.05	MHz	See Note 2
2		Clock Rise Time	C2i	t_{CR}			50	ns	
3		Clock Fall Time	C2i	t_{CF}			50	ns	
4		Clock Duty Cycle	C2i		40	50	60	%	
5		Chip Enable Rise Time	$\overline{F1i}$	t_{ER}			100	ns	
6		Chip Enable Fall Time	$\overline{F1i}$	t_{EF}			100	ns	
7		Chip Enable Setup Time	$\overline{F1i}$	t_{ES}	50			ns	See Note 3
8		Chip Enable Hold Time	$\overline{F1i}$	t_{EH}	25			ns	See Note 3
9		Output Rise Time	DSTo	t_{OR}			100	ns	
10		Output Fall Time	DSTo	t_{OF}			100	ns	
11		Propagation Delay Clock to Output Enable	DSTo	t_{PZL}			122	ns	
				t_{PZH}			122	ns	R_L = 10kΩ to V_{CC}
12		Propagation Delay Clock to Output	DSTo	t_{PLH}			100	ns	C_L = 100 pF
				t_{PHL}			100	ns	
13		Input Rise Time	CSTi	t_{IR}			100	ns	
			DSTi				100	ns	
14		Input Fall Time	CSTi	t_{IF}			100	ns	
			DSTi				100	ns	
15		Input Set Up Time	CSTi	t_{ISH}	25			ns	
			DSTi	t_{ISL}	0			ns	
16		Input Hold Time	CSTi	t_{IH}	60			ns	
			DSTi		60				
17		Digital Loopback Time DSTi to DSTo		t_{DL}			122	ns	

* Typical figures are at 25°C with nominal ±5V supplies and are for design aid only: not guaranteed and not subject to production testing. (See Figures 2a, 2b, 2c)

Note 2: The filter characteristics are totally dependent upon the accuracy of the clock frequency but providing $\overline{F1i}$ is synchronized to C2i, the codec function is unaffected by changes in the clock frequency.

Note 3: This gives a 75 ns period, 50 ns before and 25 ns after the 50% point of C2i rising edge, when any change in $\overline{F1i}$ will give an undetermined state to to the internally synchronized enable signal.

AC Electrical Characteristics- Transmit (A/D) Path - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70° C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{REF} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Absolute Gain	G_{AX}	-0.26	-0.12	0.38	dB	0dB gain in Codec . See Note 4
2	Max. Analog Input Level at Tip/Ring before overload	V_{IN}		3.29		dBm	0dB gain in Codec
				-3.71		dBm	7dB gain in Codec
3	Gain Tracking	GT_X					Sinusoidal input level @ 1020Hz
	AT &T		-0.25		+ 0.25	dB	-0 to -10 dBm
	CCITT G.712 (Method 2)		-0.50		+ 0.50	dB	-50 dBm
4	Quantization Distortion	D_{QX}					Sinusoidal input level @ 1020Hz
	AT & T		35.3			dB	-10 dBm
	CCITT G.712 (Method 2)		-29.3			dB	-40 dBm
5	Idle Channel Noise	N_{CX}			18	dBrnC0	C-Message 7dB gain in Codec
6	Frequency Response w.r.t. 1020Hz, + 4dBm Sinusoidal level on Tip/Ring	G_{RX}			-30	dB	60Hz (See Fig. 4)
			-2.0			dB	220Hz
			-0.25		+ 0.25	dB	300-3000Hz
				-1.0		dB	3400Hz

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 4: 0dBm on Tip/Ring will appear as -0.12dBm0 on DSTo of the hybrid. This implies -0.12dB gain.

AC Electrical Characteristics- Receive (D/A) Path - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70° C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{REF} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
	Absolute Gain	G_{AR}	-0.62	-0.12	0.38	dB	0dB gain in Codec . See Note 5
2	Maximum Analog Output Level at Tip/Ring	V_{OUT}		3.29		dBm	0dB gain in Codec
3	Gain Tracking	GT_R					Sinusoidal input level @ 1020Hz :
	AT &T		-0.25		+ 0.25	dB	+ 3 to -10 dBm0
	CCITT G.712 (Method 2)		-1.50		+ 1.50	dB	-55 dBm0
4	Quantization Distortion	D_{QR}					Sinusoidal input level @ 1020Hz:
	AT & T		35.6			dB	-10 dBm0
	CCITT G.712 (Method 2)		-29.3			dB	-40 dBm0
5	Idle Channel Noise	N_{CR}			13	dBrnC0	C-Message 0dB gain in Codec
6	Frequency Response w.r.t. 1020Hz, + 0dBm0 Sinusoidal level on Tip/Ring	G_{RR}			0.25	dB	220 Hz
			-0.63		+ 0.25	dB	300Hz to3000Hz (See Fig.5)
			-0.25		+ 0.25	dB	3200Hz
			-0.60				

*Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 5 : 0dBm0 into DSTi of the hybrid will appear -0.12dBm at Tip/Ring. This implies a -0.12dB gain.

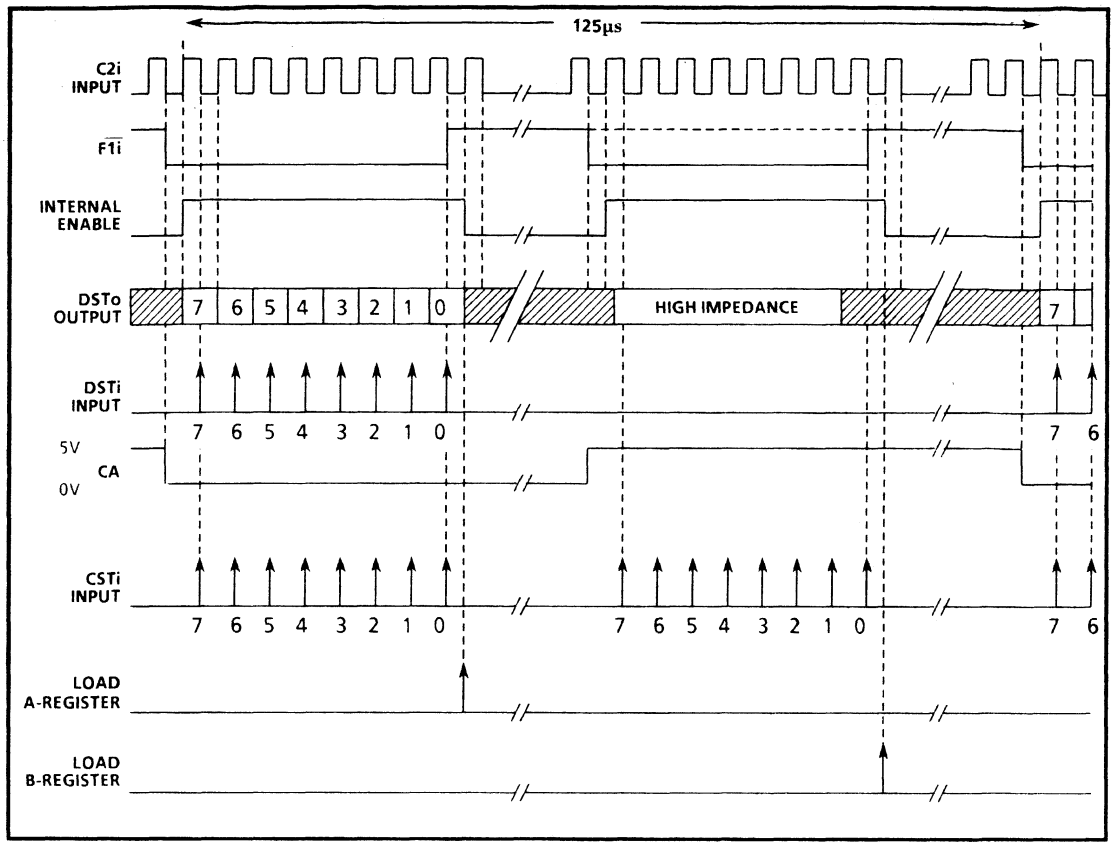


Figure 2a - Timing Diagram - 125µs Frame Period

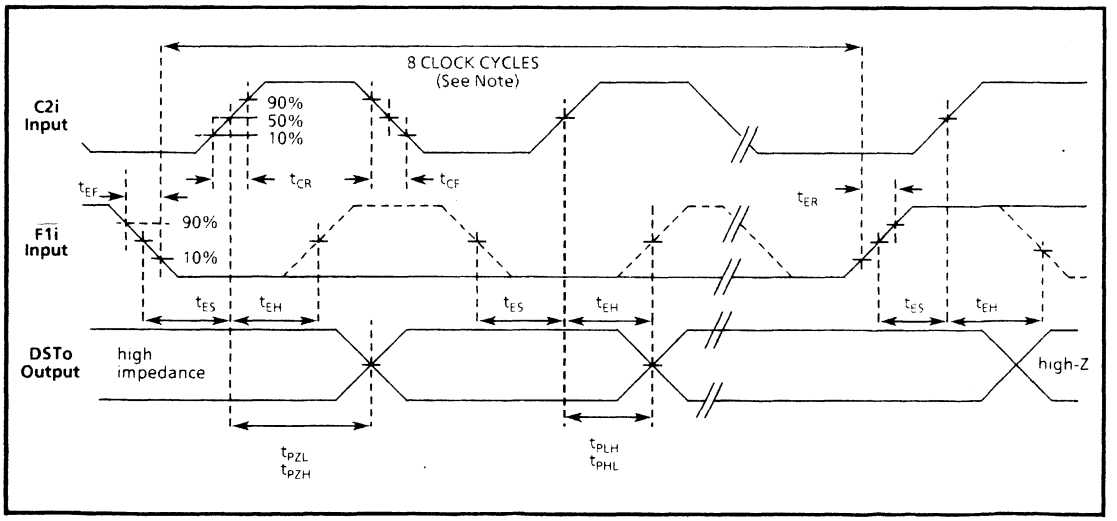


Figure 2b -Timing Diagram - Output Enable

Note: In typical applications, $\overline{F1i}$ will remain low for 8 cycles of C2i. However, the device will function normally as long as t_{ES} and t_{EH} are met at each positive edge of C2i.

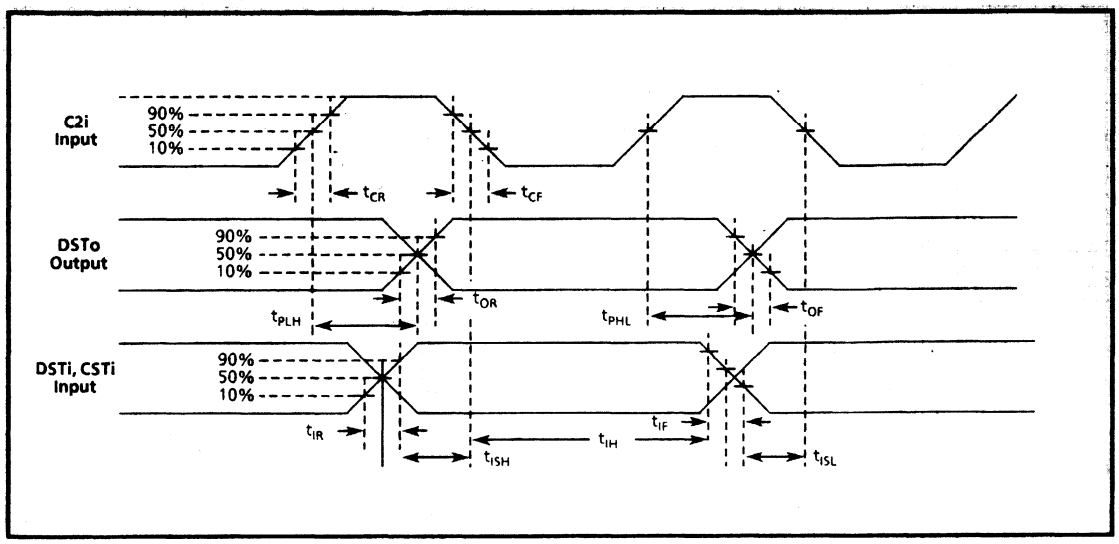


Figure 2c - Timing Diagram - Input/Output

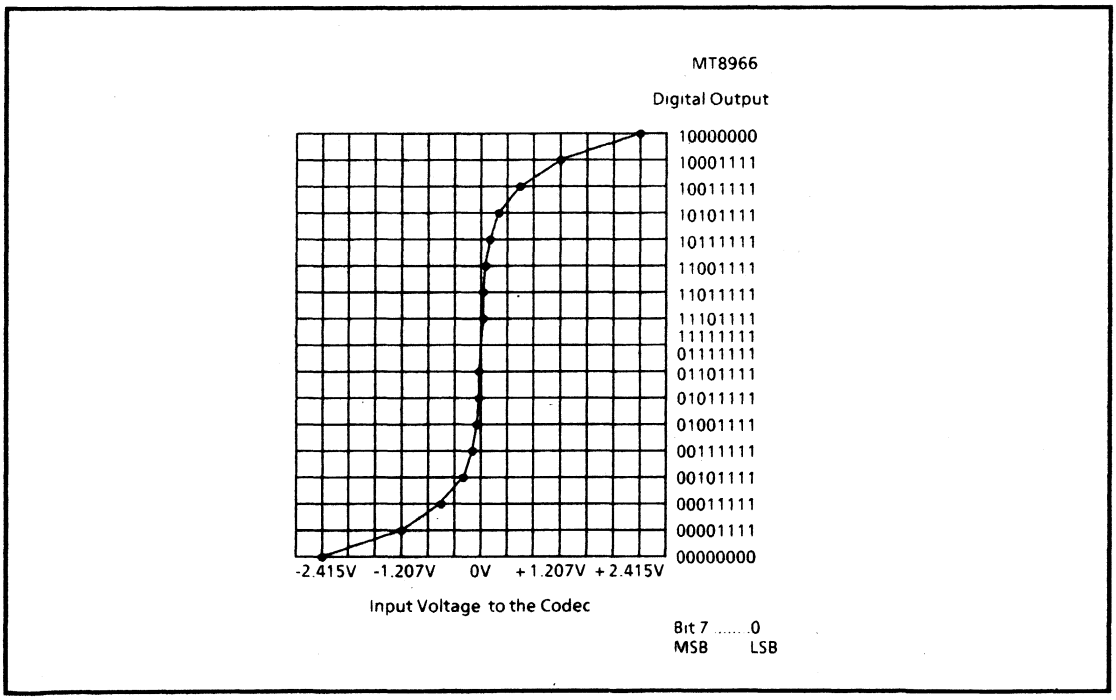


Figure 3 - μ-Law Encoder Transfer Characteristic

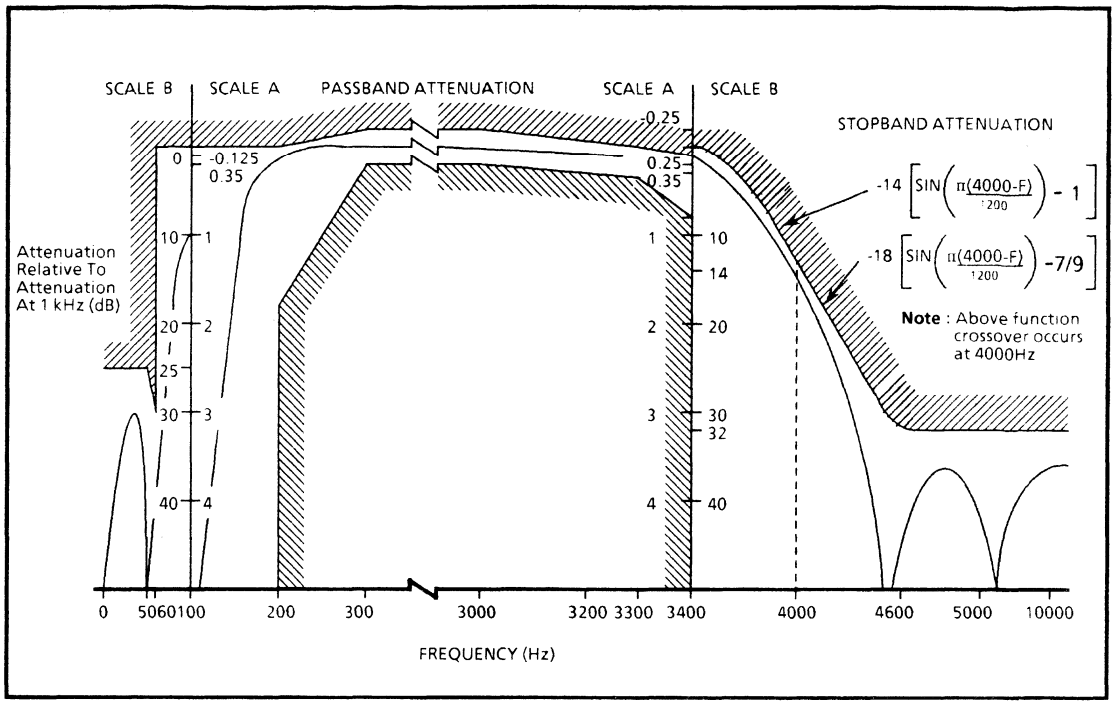


Figure 4 - Attenuation vs. Frequency for Transmit (A/D) Filter

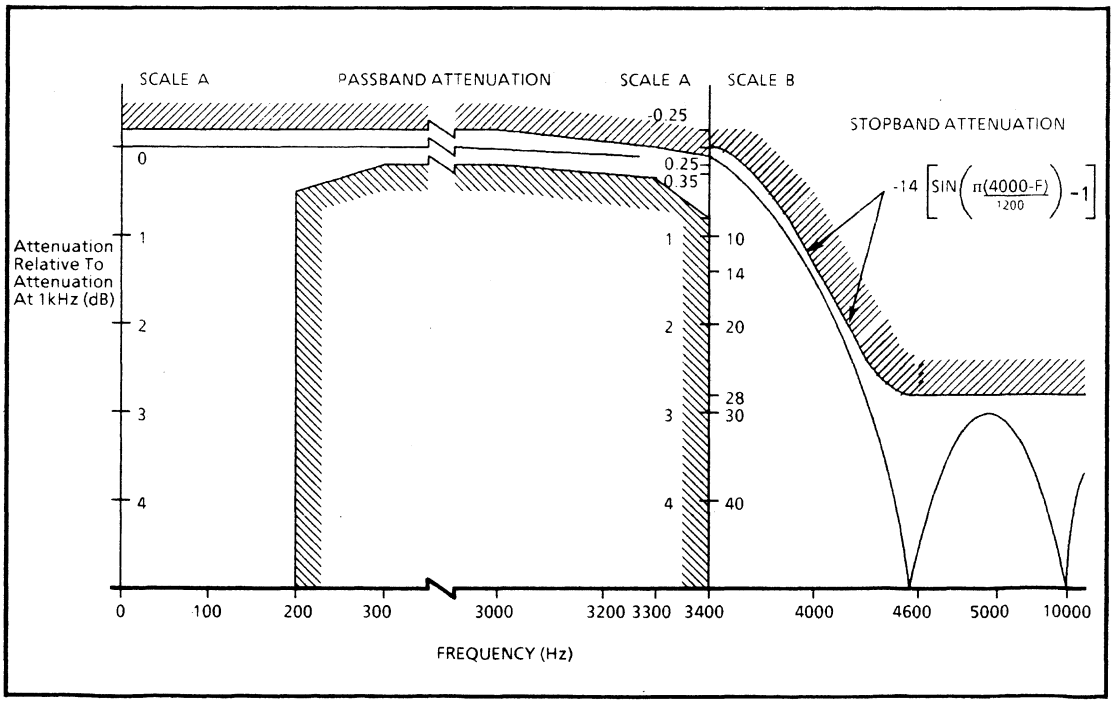


Figure 5 - Attenuation vs. Frequency for Receive (D/A) Filter

Pin Description†

Pin #	Name	Description
2	CCTR	**Circuit Ring (Input).** Analog signal input from the Ring lead. Connect this pin to the external feed resistor (R2) which is in series with Ring lead.
3	NC	**Internal Connection.** Leave open circuit.
4	LPT	**Loop Tip (Input).** Differential analog signal from the Tip lead.
5	LPR	**Loop Ring (Input).** Differential analog signal from the Ring lead.
6	NC	**Internal Connection.** Leave open circuit.
7	CCTT	**Circuit Tip (Input).** Analog signal input from the Tip lead. Connect this pin to the external feed Resistor (R1) which is in series with Tip lead.
8	V_{CC-}	**Negative Analog Power Supply Voltage** (– 27V).
9	V_{Bias}	**Bias Voltage.** Internal bias voltage reference. Connect from V_{Bias} with a coupling capacitor (C2) in series to GNDA.
10	TPROT	**Tip Protect (Input).** Connect this pin to pin 7 with a coupling capacitor (C1).
11	$\overline{GB}$	**Ground Button Detect (output).** Digital output of an internal op-amp (MC3403, ± 5V). Upon detection of a grounded Ring lead at the subscriber set,the output will go low.
12	$\overline{SHK}$	**Switch Hook Detect (output).** Digital output of an internal op-amp (MC3403, ± 5V). When the loop current exceeds a threshold, the output will go low to indicate that the subscriber set is Off-Hook.
13	CCTR	**Circuit Ring (Input).** Connect this pin to pin 2.
14	NC	**Internal Connection.** Leave open circuit.
15	RLY 1	**Relay Drive 1 (Output).** Open collector, controlled by codec register B, bit 2.
16	CCEN	**Circuit Centre.** Mid-reference of CCTT and CCTR. Connect this pin to pin 2 (CCTR) in series with a Zener diode (D10) and a resistor (R11).
17	NC	**No Connection.**
18	V_{EE}	**Negative Power Supply Voltage** to the codec (-5V).
19	GNDD	**Digital Ground.**
20	V_{Ref}	**Voltage Reference (Input)** to the codec (2.5 V ± 0.5%).
21	CSTi	**Control ST-BUS (Input).**TTL-Compatible digital input used to control the function of the filter/codec. Three modes of operation may be selected by applying a logic high (V_{DD}), logic low (GNDD) or an 8-bit serial word, to this input depending on the logic states of CA and $\overline{F1i}$.
22	DSTi	**Data ST-BUS (Input).** Accepts the incoming 8-bit PCM word. Input TTL-compatible.
23	C2i	**Clock (Input).** TTL-Compatible 2.048 MHz clock.
24	DSTo	**Data ST-BUS (Output).** A tristate digital output drives the PCM bus with the outgoing 8-bit PCM word.
25	V_{DD}	**Positive Power Supply Voltage** to the codec (+ 5V).
26	GNDD	**Digital Ground**
27	$\overline{F1i}$	**Framing Signal Type 1 (Input).** Active low digital input enabling (in conjunction with CA) the PCM input, PCM output and digital control input. It is internally sampled on every positive edge of the C2i clock and provides frame and channel synchronization.
28	CA	**Control Address (Input).** A three level digital input which enables PCM input and output and determines into which control register (A or B) the serial data, presented at CSTi, is stored.
29	SD1	**System Drive 1 (Output).** "Totem-pole" CMOS output which switches between GNDD and V_{DD}. Inactive state is logic low. Controlled by codec register B,bit 1.
30	V_{DD}	**Positive Power Supply Voltage** to the codec (+ 5V).

†Components designation refers to Figure 6 unless otherwise stated

Pin Description†

Pin #	Name	Description
31	RLY 2	**Relay Drive 2 (Output).** Open Collector,controlled by codec register B,bit 4.
32	IC	**Internal Connection.** Leave open circuit.
33	GNDA	**Analog Ground.**
34	IC	**Internal Connection.** Leave open circuit.
35	GNDA	**Analog Ground**
36	RFDBK	**Ring Feedback (Input)** . Ring feedback signal is used to activate the protection circuit against high ringing voltage.
37	V_{BAT}	**Negative Battery Feed Supply Voltage** (-48Volts).
38	RING	Connect this pin in series with a resistor (R6) to the external push-pull amplifiers (Q3,Q4) .
39	TIP	Connect this pin in series with a resistor (R5) to the external push-pull amplifiers (Q1,Q2) .
40	IC	**Internal Connection.** Leave open circuit.

†Components designation refers to Figure 6 unless otherwise stated.

MODE	CA	CSTi	FUNCTION
1	V_{EE}	GNDD	Normal operation.
		V_{DD}	Power down.
2	V_{EE}	Serial Data	8-bit control word into Register A. Register B is reset.
3	GNDD	Serial Data	8-bit control word into Register A. Register B unaffected.
	V_{DD}	Serial Data	8-bit control word into Register B. Register A unaffected.

Table 1 - Digital Control Modes

Note 1: $\overline{F1i}$ at GNDD for each mode of operation.
Note 2: PCM input and output inhibited by CA = V_{DD} when in Mode 3.

7	6	5	4	3	2	1	0
Functional Control		Receive (D/A) Filter Gain			Transmit (A/D) Filter Gain		

BIT 2	BIT 1	BIT 0	TRANSMIT (A/D) FILTER GAIN (dB)
0	0	0	0
0	0	1	+ 1
0	1	0	+ 2
0	1	1	+ 3
1	0	0	+ 4
1	0	1	+ 5
1	1	0	+ 6
1	1	1	+ 7
BIT 5	**BIT 4**	**BIT 3**	**RECEIVE (D/A) FILTER GAIN (dB)**
0	0	0	0
0	0	1	-1
0	1	0	-2
0	1	1	-3
1	0	0	-4
1	0	1	-5
1	1	0	-6
1	1	1	-7
BIT 7	**BIT 6**	**FUNCTIONAL CONTROL**	
0	0	Normal Operation	
0	1	Digital Loopback	
1	0	Analog Loopback	
1	1	Power Down	

Table 2 - Control States - Register A

Functional Description

The MH89620 is an Off-Premise subscriber line interface which provides the SLIC function of Battery Feed, Ringing, Supervision, Coding, Hybrid and Testing.

The hybrid function performs transformerless 2 to 4 wire conversion between the 2 wire line and the transmit and receive pairs, connected to the filter/codec.

All functions of SLIC interface are controlled by the System Drive (SD) output of the codec (MT8966). The SD control is provided over a dedicated 32 channels of ST-BUS serial data link (CSTi). All SLIC interface functions are controlled by internal register A & B of the codec (refer to Tables 1,2 & 3).

Application

Figure 6 illustrates the use of Mitel MH89620 to interface a subscriber set. The external line buffers on the Tip and Ring lead are composed of simple push-pull amplifiers. Four external varistors are used for protection against lightning, overvoltage and static discharge. When the ring relay (K1) is enabled, it will close one set of contacts to apply ringing voltage from the source to the Ring lead. At the same time, the other set of contacts is open to prevent high ringing voltage being applied to the device. If an Off-Hook condition is detected, the ringing voltage can be removed by disabling the relay.

7	6	5	4	3	2	1	0
CODEC TESTING		BALANCE NETWORK	RLY 2	RING TRIP FILTER	RLY 1	SD1	-

BIT	NAME	DESCRIPTION
0	-	Unused
1	SD1	A logic "0", the output will be inactive - logic low. A logic "1", the output will be active - logic high.
2	RLY1	When "1", the output will be open collector which can be used to control an uncommitted external relay.
3	RING TRIP FILTER	A logic "0" will introduce a 60 ms time constant to prevent pre-trip on Switch Hook during the first ringing cycle. It should be set simultaneously with the activation of ring relay and should remain in circuit until the ringing cycle is complete or until a valid ring trip occurs.
4	RLY2	When "1", the output will be open collector which can be used to control an uncommitted external relay.
5	Balance Network	A logic '0' will select the 600Ω transhybrid balance network. For a long loop, the AT&T compromise network should be selected to improve transhybrid loss.
6, 7	Codec Testing	These two bits are used during manufacturing process in testing the codec and must be set to ' 0' for normal operation.

Table 3 -Control States - Register B

Component List:

†R1, R2 = Resistor 1W, 0.5%, ABS 0.1% Ratio, 200Ω

†R3, R4 = Resistor 1W, 0.5%, 10Ω

R5, R6 = Resistor $\frac{1}{4}$W, 5%, 100Ω

R7, R8 = Resistor $\frac{1}{2}$W, 5%, 1kΩ

R9 = Resistor $\frac{1}{4}$W, 5%, 510Ω

R10 = Resistor $\frac{1}{4}$W, 5%, 51kΩ

R11 = Resistor $\frac{1}{4}$W, 5%, 150kΩ

R12 = Resistor $\frac{1}{4}$W, 5%, 7.5kΩ

C1 = Cap Cer., 4.7pF, 10%, 50V

C2 = Cap Elec., 10µF, 20%, 5V

†Resistors can be made by Mitel as a custom device.

Q1 = NPN 60V, 1A, 2W, T0202, 2N6551

Q2 = PNP 60V, 0.5A, 0.6W, T092, 2N3645

Q3 = NPN 140V, 0.6A, 0.6W, T092, 2N5832

Q4 = PNP 80V, 1A, 2W, T0202, 2N6555

D1 - D5 = Diode Rect., 200V, 1A, IN4003

D6 - D9 = Diode SW., 75V, 0.2A, 0.5W, IN4148

D10 = Zener Diode, 82V, 1W, IN4762

RV1, RV2 = Varistor, 1100V, 135 Joules, SIOV-SIOK680

RV3, RV4 = Varistor, 39V, 1.3 Joules, SIOV-SIOK50

K1 = Relay E/M, 12V, 2 Form C Dip Sealed

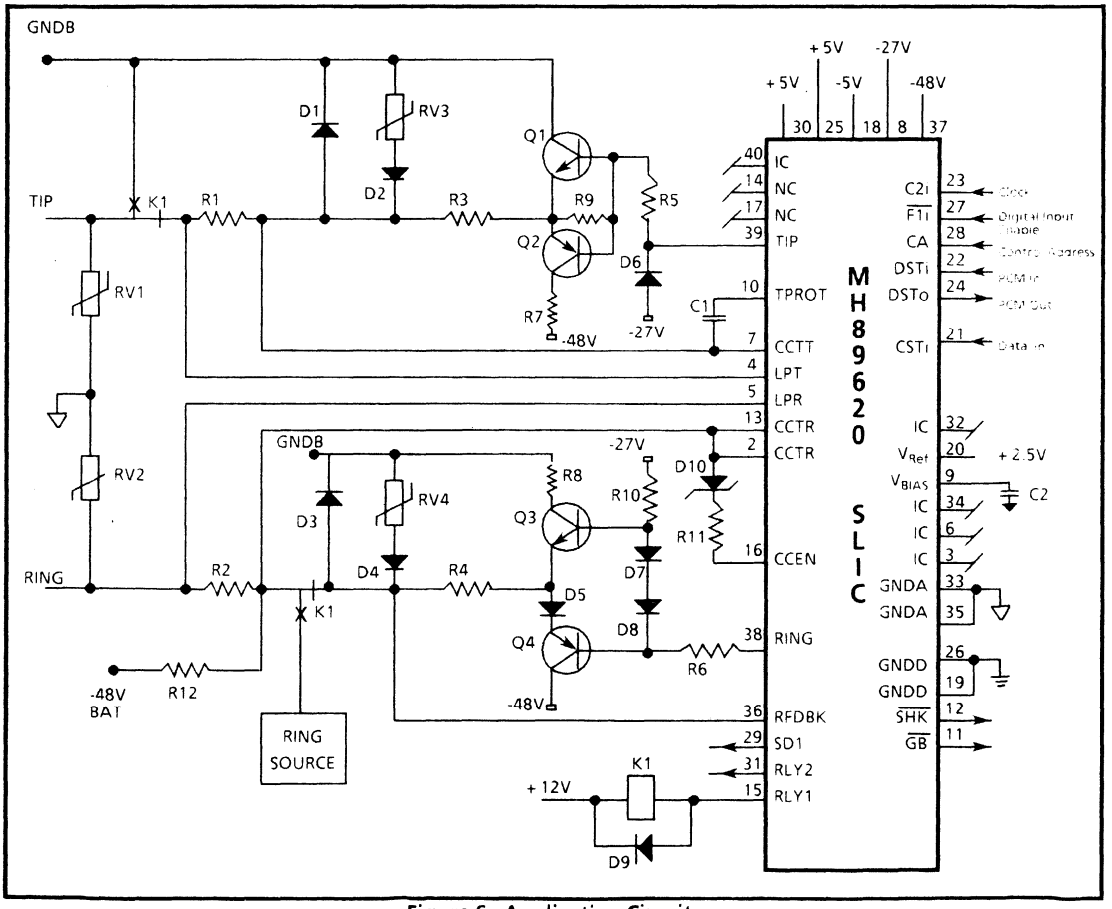


Figure 6 - Application Circuit

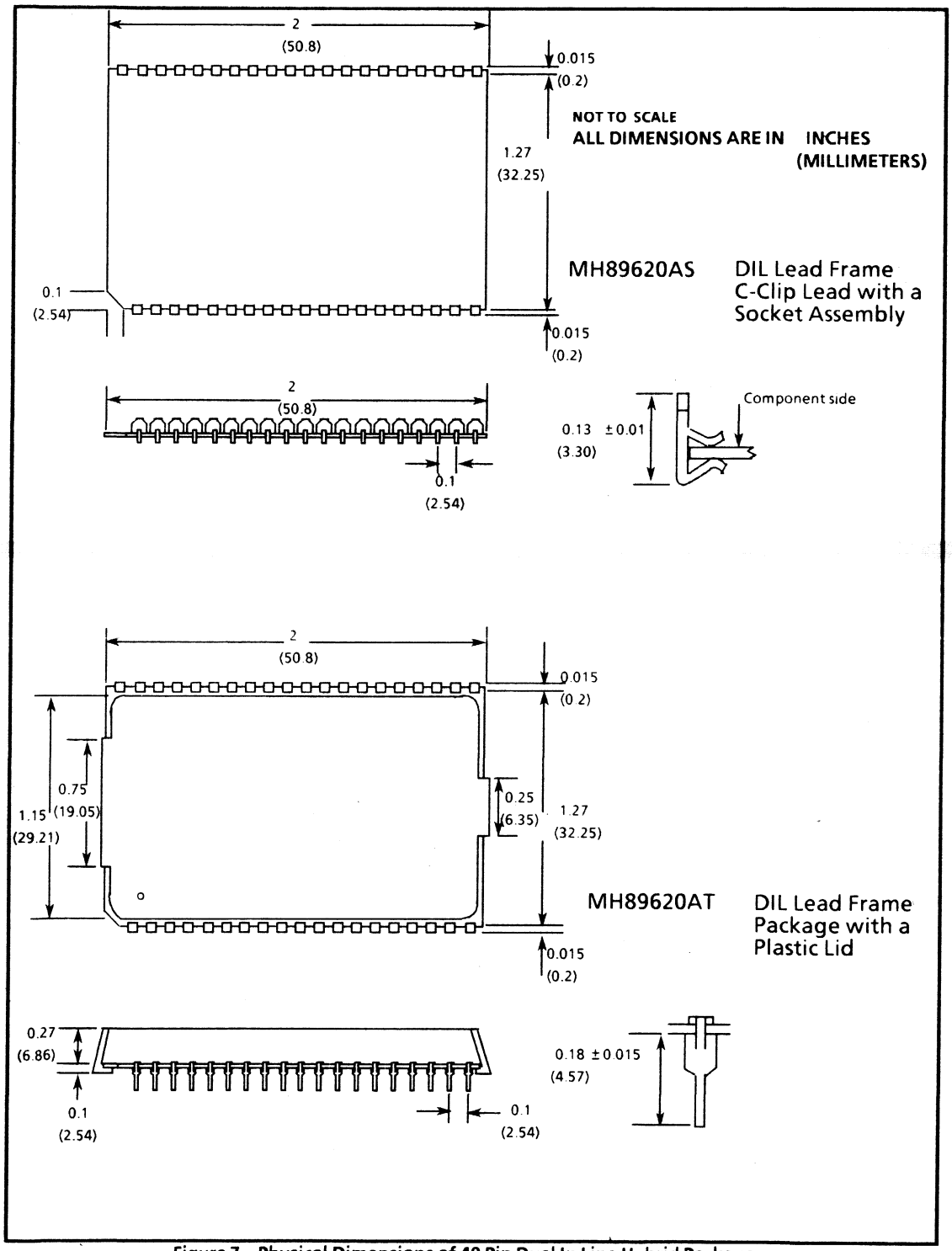


Figure 7 - Physical Dimensions of 40 Pin Dual In Line Hybrid Package

ST-BUS™ FAMILY **MH89625**

A-Law Subscriber Line Interface Circuit

Preliminary Information

9161-002-079-NA ISSUE 1 AUGUST 1986

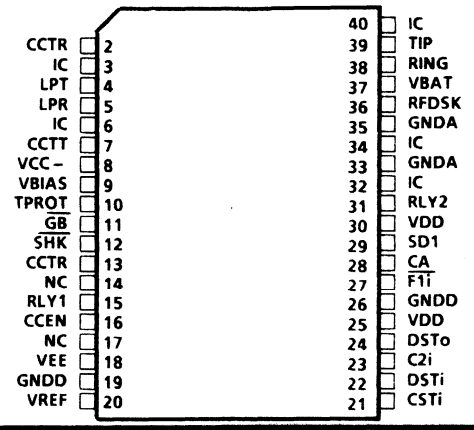
Features

- MITEL ST-BUS™ compatible
- Transformerless 2 to 4 wire conversion
- A/D and D/A conversion
- Conforms with A-law PCM
- Ground button detection
- Switch hook detection
- Software selectable control
  - -600Ω or an alternative complex impedance balance network.
  - -Audio transmit and receive gain control
- Ring trip filter
- Ring relay driver
- Two uncommitted control outputs
- Analog and digital loopback

Applications

- **Digital PBX Subscriber Line Card**
- Control System
- Key Telephone System

Pin Connections



Ordering Information

MH89625AT	40 Pin DIL Lead Frame Hybrid Package with Plastic Lid
MH89625AS	40 pin DIL C-Clip Lead with a Socket Assembly

0°C TO 70°C

Description

The Mitel MH89625 is an off-premise SLIC interface between digital equipment (PABX) and a subscriber loop. It provides a selectable software control balancing network and a maximum longitudinal balance for long loops. With a few external components, it performs the BORSCHT function asssociated with analog line circuit requirement. The device is fabricated using thick film hybrid and ISO²-CMOS technology to achieve high power dissipation, low power consumption, and optimum circuit packing density.

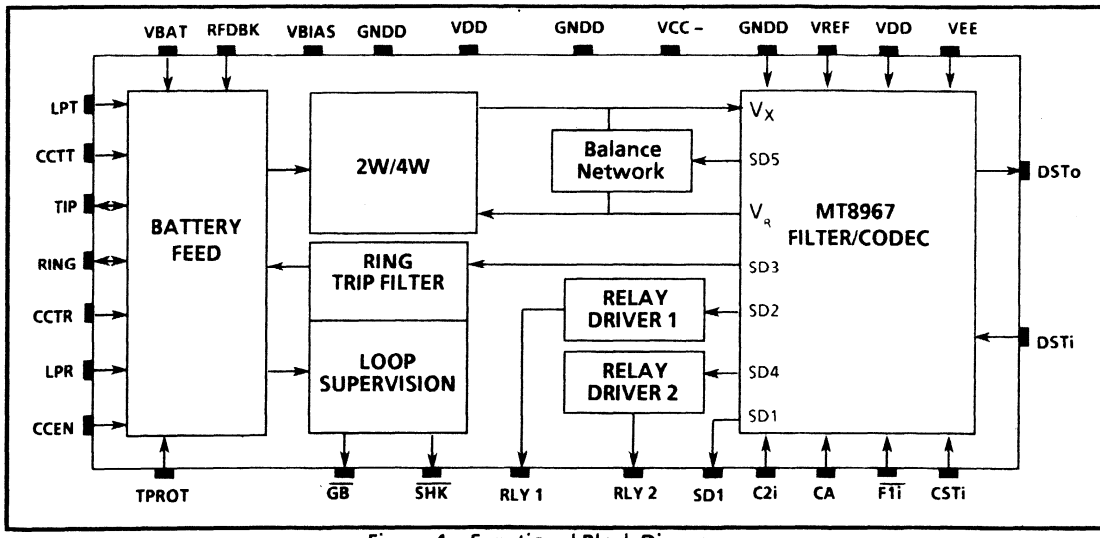


Figure 1 - Functional Block Diagram

Refer to the MH89620 Data Sheet for the functional description. Contact your Mitel representative for more information.

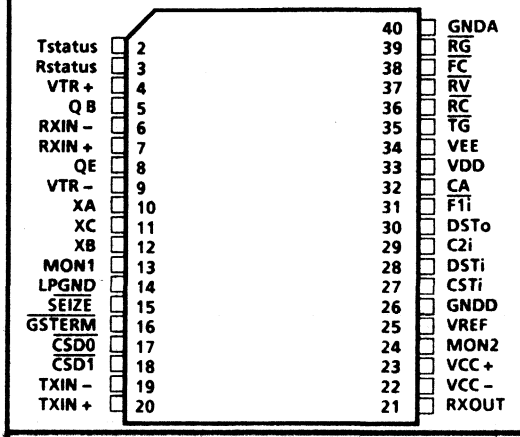
ST-BUS™ FAMILY MH89630
μ-Law Central Office Interface
Preliminary Information

9161-002-061-NA ISSUE 1 APRIL 1986

Features

- MITEL ST-BUS™ compatible
- Transformerless 2W to 4W conversion
- A/D and D/A conversion
- Conforms with μ-law PCM
- Line state detection outputs:
  - -forward current -reverse current
  - -ring ground -tip ground
  - -ringing voltage
- Line state control outputs:
  - -loop seize signalling
  - -two uncommitted control outputs
- Software selectable control:
  - -ground or loop start termination
  - -audio transmit and receive gain control
  - -600 Ω or AT&T compromise balance network
- Analog and digital loopback

Pin Connections



Ordering Information

MH89630AT 40 pin DIL Lead Frame Hybrid Package with Plastic Lid
MH89630AS 40 pin DIL C-Clip Lead with a Socket Assembly
0° C TO 70° C

Applications

- Digital PBX Interface to Central Office
- Subscriber line concentrators

Description

The Mitel MH89630 central office trunk interface circuit provides a complete audio and signalling link between digital switching equipment and a central office. The loop seize circuitry is controlled via software to provide either loop start or ground start termination to the C.O. The device is fabricated using thick film hybrid technology to achieve optimized circuit design and high circuit density.

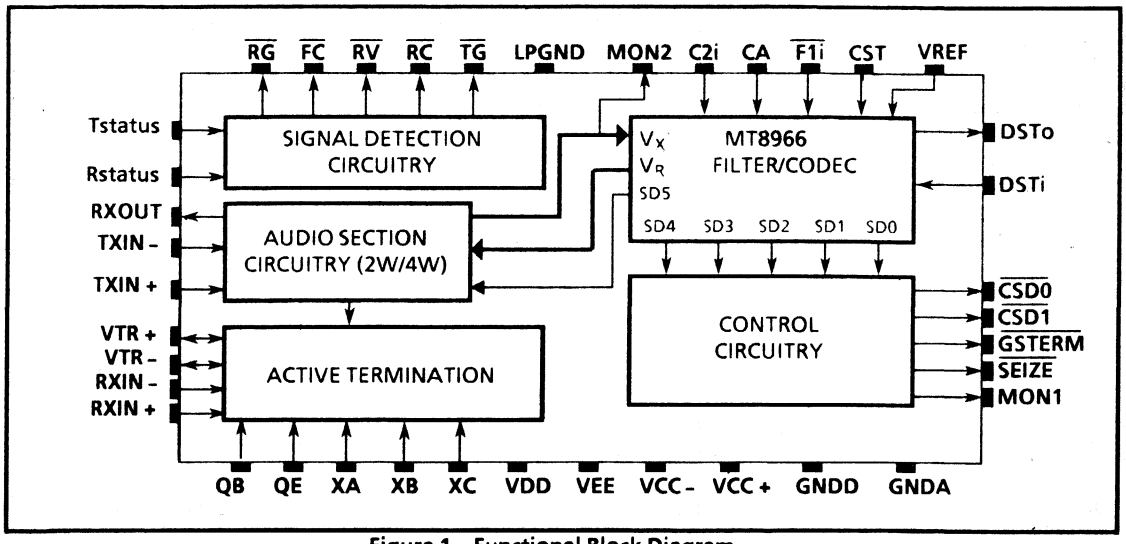


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to GNDD unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD}	-0.3	+6.0	V
		V_{EE}	-6.0	+0.3	V
		V_{CC}^+		+18.0	V
		V_{CC}^-	-18.0		V
2	Reference Voltage	V_{Ref}	GNDA	V_{DD}	V
3	Storage Temperature	T_{STG}	-20	+85	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to GNDD unless otherwise stated.

		Characteristics		Sym	Min	Typ*	Max	Units	Comments
1		Operating Supply Voltage		V_{DD}	4.75	5.0	5.25	V	
				V_{EE}	-5.25	-5.0	-4.75	V	
				V_{Ref}	2.4875	2.50	2.5125	V	See Note 1
				V_{cc+}	11.4	12.0	12.6	V	
				V_{cc-}	-12.6	-12.0	-11.4	V	
2		Operating Current	V_{DD}	I_{DD}	3.0	5.0	10.0	mA	
			V_{EE}	I_{EE}	-10.0	-5.0	-3.0	mA	
			V_{Ref}	I_{Ref}		2.0		µA	
			V_{cc+}	I_{cc+}	2.0	4.0	10.0	mA	
			V_{cc-}	I_{cc-}	-10.0	3.0	-1.2	mA	
3		Power Consumption		P_C			270	mW	Stand-by
							340	mW	Active
							325	mW	Active (Power from C.O.)
4		Operating Temperature		T_O	0		70	°C	

Note 1: Temperature coefficient of V_{Ref} should be better than 100 ppm/°C.

DC Electrical Characteristics for Digital Interface - Voltages are with respect to GNDD unless otherwise stated.

T_O = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = −5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz.
Outputs unloaded unless otherwise specified

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1		Input Current	Except CA	I_I			10.0	µA	V_{IN} = GNDD to V_{DD}
			CA	I_{IC}			10.0	µA	V_{IN} = V_{EE} to V_{DD}
2		Input Low Voltage	Except CA	V_{IL}	0.0		0.8	V	
			CA	V_{ILC}	V_{EE}		V_{EE} + 1.2	V	
3	D	Input High Voltage	All Inputs	V_{IH}	2.4		5.0	V	
4	I	Input Intermediate Voltage	CA	V_{IIC}	0.0		0.8	V	
5	G	Output Leakage Current	DSTo	I_{OZ}	-1.0	±0.1	1.0	µA	Output High Impedance
6	I	Output Low Voltage	DSTo	V_{OL}			0.4	V	I_{OUT} = 1.6mA
7	T	Output High Voltage	DSTo	V_{OH}	4.0			V	I_{OUT} = -100µA
8	A	Output Capacitance	DSTo	C_{OUT}		4.0		pF	Output High Impedance
	L								

* Typical figures are at 25°C with nominal ±5V supplies and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - TIP/RING Line State Outputs

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Output High Voltage ($\overline{TG}$, $\overline{RC}$, $\overline{RV}$, $\overline{FC}$, $\overline{RG}$)		3.0	4.75	5.0	V	12kΩ pull up to $5V_{DC}$ No Load on output
2	Output High Source Current $\overline{TG}$, $\overline{RG}$ $\overline{RC}$, $\overline{RV}$, $\overline{FC}$		0.17 0.20	0.50 0.37		mA mA	12kΩ pull up to $5V_{DC}$ V_{OH} = $2.4V_{DC}$
3	Output Low Voltage ($\overline{TG}$, $\overline{RC}$, $\overline{RV}$, $\overline{FC}$, $\overline{RG}$)		-2.40	-0.50	0.10	V	12kΩ pull up to $5V_{DC}$ No Load on output
4	Output Low Sink Current $\overline{TG}$, $\overline{RG}$ $\overline{RC}$, $\overline{RV}$, $\overline{FC}$		0.40 0.40	0.50 0.41		mA mA	12kΩ pull up to $5V_{DC}$ V_{OL} = $0.4V_{DC}$

* Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Audio Transmission

	Characteristics	Sym	Min	Typ*	Max	Units	Test
1	Ringing Voltage	V_R	45	90		V_{RMS}	@20Hz
2	**Operating Loop Current**	I_{LOOP}	18		70	mA	
3	Off-Hook DC Resistance	R_T			260 247	Ω Ω	@ 18mA @ 60mA
4	Operating Loop Resistance	R_{LOOP}			2300	Ω	@ 18mA
5	On-Hook Leakage Current			30		μA	
6	Ring Ground Sink Current	I_{RG}			100	mA	-$48V_{DC}$ on Ring
7	Tip and Ring AC Impedance			600		Ω	with 10kΩ + 1.0μF in parallel with Tip and Ring
8	Longitudinal Balance			70 60		dB dB	0.2 - 1.0 kHz 1.0 - 3.0 kHz
9	Single Frequency Return Loss Trunk to Line		15 18 26 28	21 28 36 40		dB dB dB dB	220Hz 540Hz 1020Hz 3220Hz
10	Transhybrid Loss (single frequency) into 600Ω + 2.16μF		-16 -21 -21	-18.5 -34 -30		dB dB dB	0.2kHz 1.0kHz 3.0kHz
11	Transhybrid Loss (Single Frequency) into AT & T Compromise		-17 -21 -18	-17.5 -31 -31		dB dB dB	0.2kHz 1.0kHz 3.0kHz

* Typical figures at 25°C are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics for Digital Interface - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{Ref} = 2.5V ± 0.5%, GNDA = GNDD = 0V,
Clock Frequency = 2.048 MHz, Outputs unloaded unless otherwise specified.

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	DIGITAL	Clock Frequency	C2i	f_C	2.046	2.048	2.05	MHz	See Note 2
2		Clock Rise Time	C2i	t_{CR}			50	ns	
3		Clock Fall Time	C2i	t_{CF}			50	ns	
4		Clock Duty Cycle	C2i		40	50	60	%	
5		Chip Enable Rise Time	$\overline{F1i}$	t_{ER}			100	ns	
6		Chip Enable Fall Time	$\overline{F1i}$	t_{EF}			100	ns	
7		Chip Enable Setup Time	$\overline{F1i}$	t_{ES}	50			ns	See Note 3
8		Chip Enable Hold Time	$\overline{F1i}$	t_{EH}	25			ns	See Note 3
9		Output Rise Time	DSTo	t_{OR}			100	ns	
10		Output Fall Time	DSTo	t_{OF}			100	ns	
11		Propagation Delay Clock to Output Enable	DSTo	t_{PZL}			122	ns	
				t_{PZH}			122	ns	R_L = 10kΩ to V_{CC}
12		Propagation Delay Clock to Output	DSTo	t_{PLH}			100	ns	C_L = 100 pF
				t_{PHL}			100	ns	
13		Input Rise Time	CSTi	t_{IR}			100	ns	
			DSTi				100	ns	
14		Input Fall Time	CSTi	t_{IF}			100	ns	
			DSTi				100	ns	
15		Input Set Up Time	CSTi	t_{ISH}	25			ns	
			DSTi	t_{ISL}	0			ns	
16		Input Hold Time	CSTi	t_{IH}	60			ns	
			DSTi		60				
17		Digital Loopback Time DSTi to DSTo		t_{DL}			122	ns	

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.
(See Figures 2a, 2b, 2c)

Note 2: The filter characteristics are totally dependent upon the accuracy of the clock frequency but, providing $\overline{F1i}$ is synchronized to C2i, the codec function is unaffected by changes in the clock frequency.

Note 3: This gives a 75 ns period, 50 ns before and 25 ns after the 50% point of C2i rising edge, when any change in $\overline{F1i}$ will give an undetermined state to the internally synchronized enable signal.

AC Electrical Characteristics - Transmit (A/D) Path - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{REF} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Absolute Gain	G_{AX}	-4.30	-4.0	-3.70	dB	0dB gain in Codec (Gain is selectable from -4 to +3dB, in 1dB step via Codec). See Note 4
2	Max. Analog Input Level at Tip/Ring before clipping at Codec	V_{IN}		7.17 0.17		dBm dBm	0dB gain in Codec 7dB gain in Codec
3	Gain Tracking AT &T CCITT G.712 (Method 2)	GT_X	 -0.25 -0.50 -1.50		 +0.25 +0.50 +1.50	 dB dB dB	Sinusoidal input level @ 1020Hz +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Quantization Distortion AT & T CCITT G.712 (Method 2)	D_{QX}	 35.3 29.3	 37.0 29.1 23.4		 dB dB dB	Sinusoidal input level @ 1020Hz 0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Idle Channel Noise	N_{CX}			 18	 dBrnC0	C-Message 7dB gain in Codec
6	Frequency Response w.r.t. 1020Hz, +4dBm Sinusoidal level on Tip/Ring	G_{RX}	 -0.25 -1.0	-63 -2.8 -0.8 -4.0	-30 +0.25 -0.1	dB dB dB dB dB	60Hz (See Fig. 4) 140Hz 300-3000Hz 3400Hz 3600Hz

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 4: 0dBm on Tip/Ring will appear as -4dBm0 on DSTo of the hybrid. This implies -4dB gain.

AC Electrical Characteristics - Receive (D/A) Path - Voltages are with respect to GNDD unless otherwise stated.

T_o = 0 to 70°C, V_{DD} = 5V ± 5%, V_{EE} = -5V ± 5%, V_{REF} = 2.5V ± 0.5%, GNDA = GNDD = 0V, Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Absolute Gain	G_{AR}	2.70	+3.0	+3.30	dB	0dB gain in Codec (Gain is selectable from -4 to +3dB, in 1dB steps via Codec). See Note 5
2	Maximum Analog Output Level at Tip/Ring	V_{OUT}		6.17		dBm	0dB gain in Codec
3	Gain Tracking AT &T CCITT G.712 (Method 2)	GT_R	 -0.25 -0.50 -1.50		 +0.25 +0.50 +1.50	 dB dB dB	Sinusoidal input level @ 1020Hz : +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Quantization Distortion AT & T CCITT G.712 (Method 2)	D_{QR}	 36.4 30.4 25.4			 dB dB dB	Sinusoidal input level @ 1020Hz: 0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Idle Channel Noise	N_{CR}		13.4	15	dBrnC0	C-Message 0dB gain in Codec
6	Frequency Response w.r.t. 1020Hz, +0dBm0 Sinusoidal level on Tip/Ring	G_{RR}	-0.25 -1.0	 -0.85 -3.7	+0.25 -0.1	dB dB dB	300Hz to3000Hz (See Fig.5) 3400Hz 3600Hz

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 5 : 0dBm0 into DSTi of the hybrid will appear +3dBm at Tip/Ring. This implies a +3dB gain.

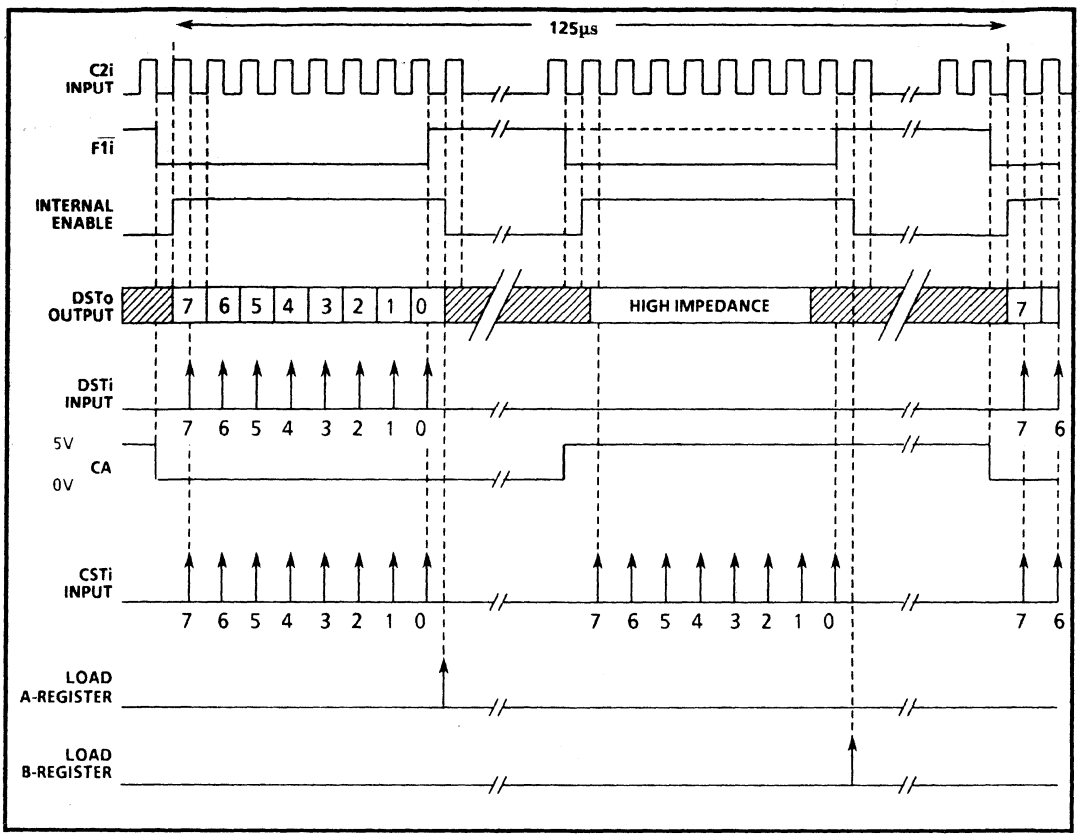


Figure 2a - Timing Diagram - 125µS Frame Period

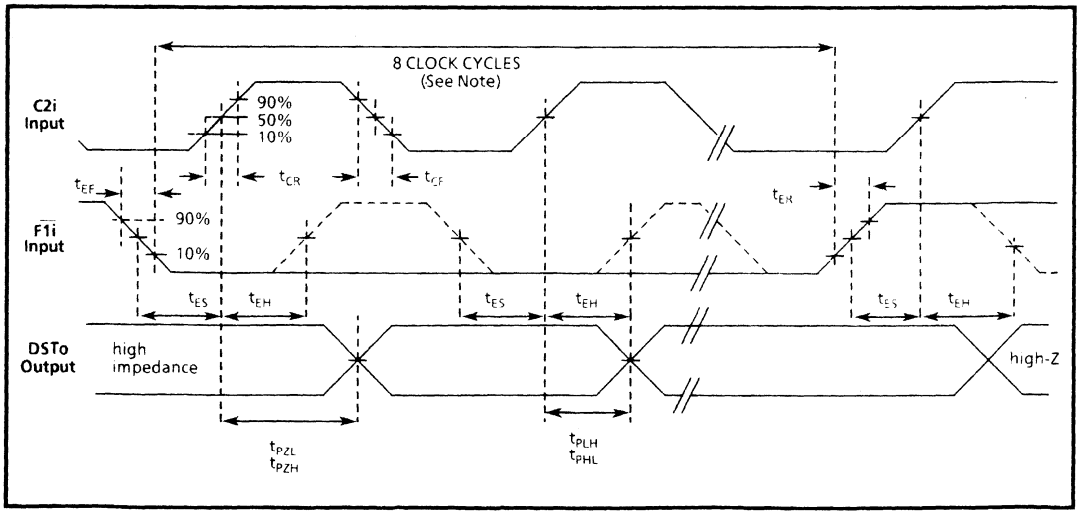


Figure 2b -Timing Diagram - Output Enable

Note: In typical applications, $\overline{F1i}$ will remain low for 8 cycles of C2i. However, the device will function normally as long as t_{ES} and t_{EH} are met at each positive edge of C2i.

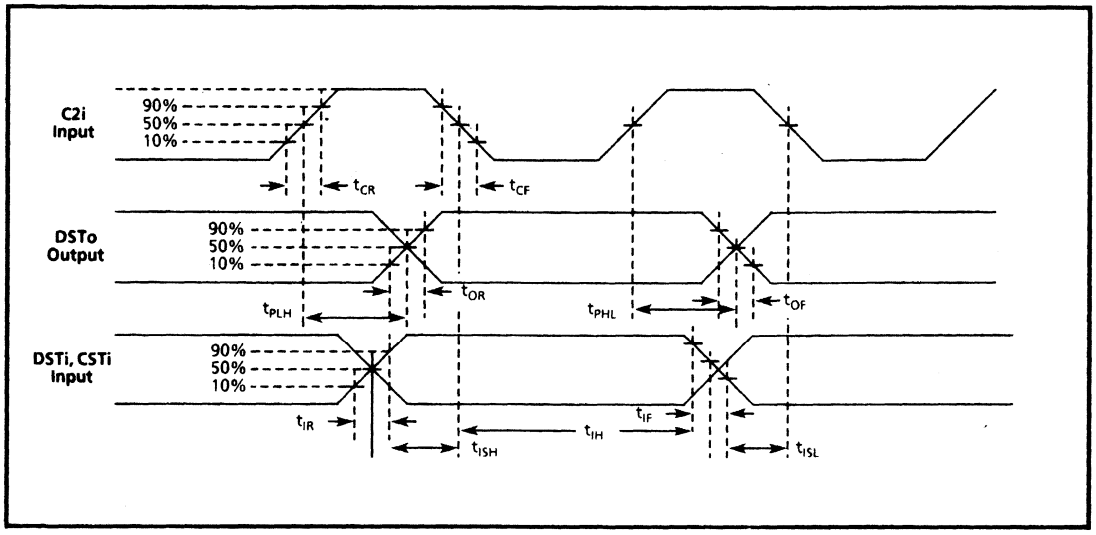


Figure 2c - Timing Diagram - Input/Output

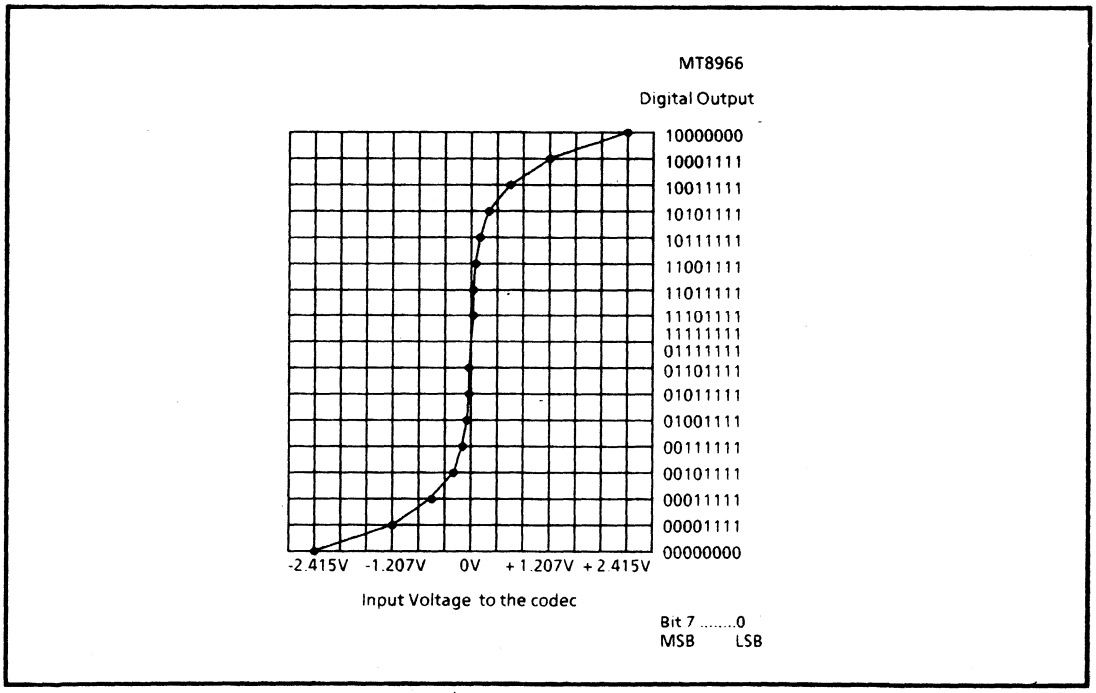


Figure 3 - μ-Law Encoder Transfer Characteristic

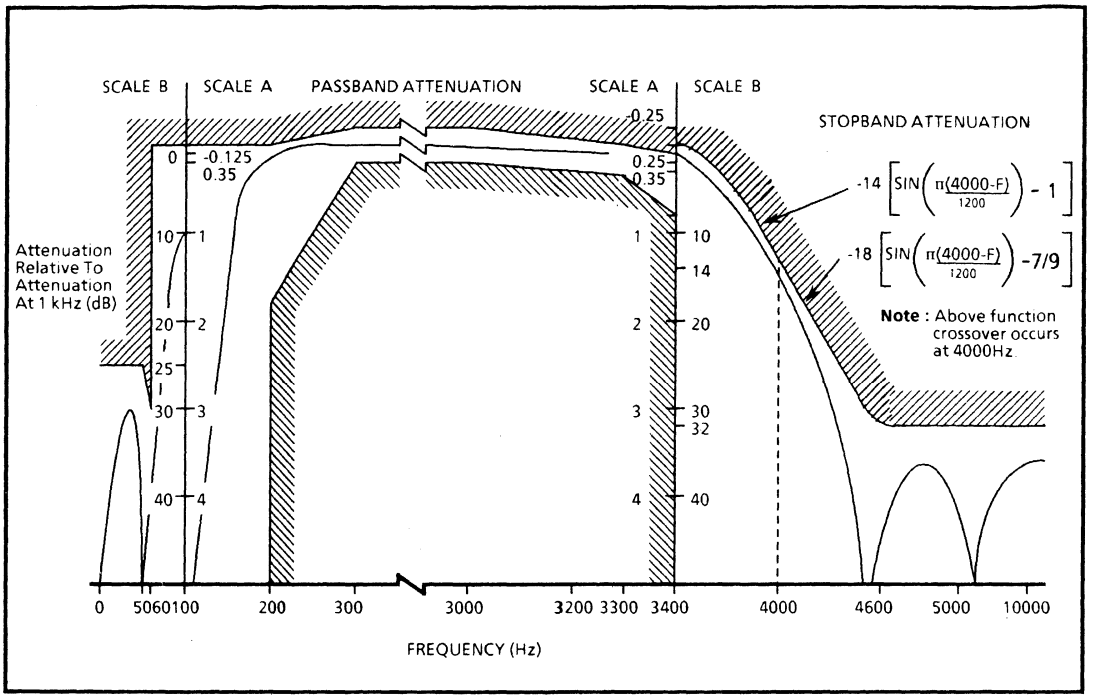


Figure 4 - Attenuation vs. Frequency for Transmit (A/D) Filter

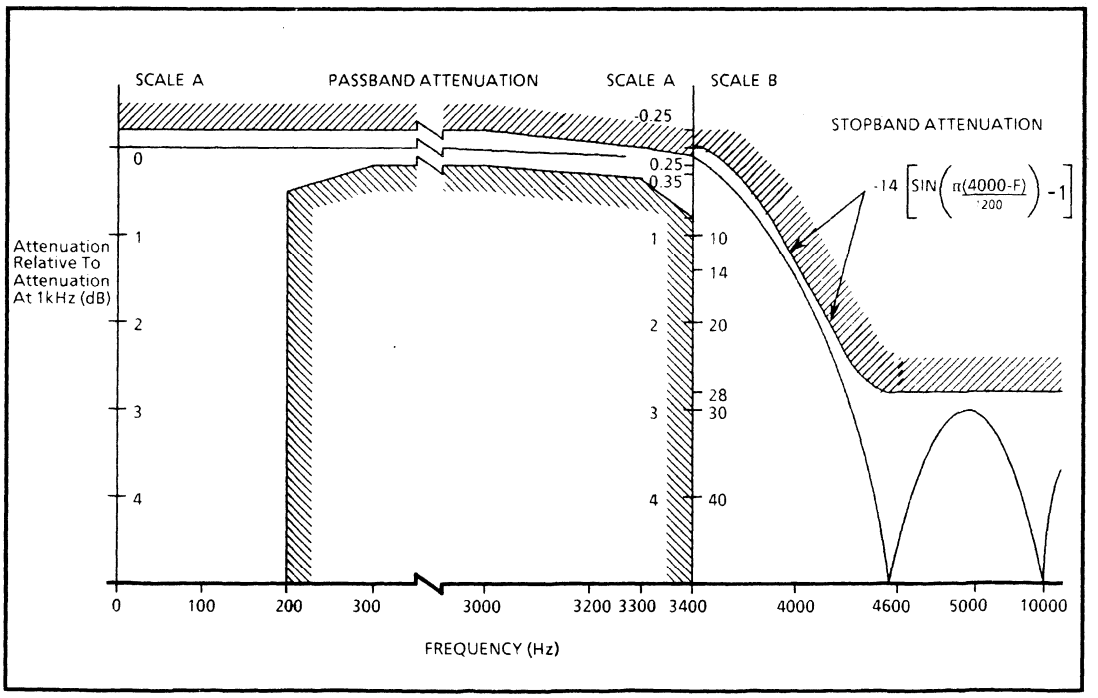


Figure 5 - Attenuation vs. Frequency for Receive (D/A) Filter

Pin Description†

Pin #	Name	Description
2	T_{status}	**Tip Status (Input).** Monitors the tip voltage. Normally connects to the "TIP".
3	R_{status}	**Ring Status (Input).** Monitors the ring voltage. Normally connects to the "RING".
4	$V_{TR}+$	Connects to the positive terminal of the external diode bridge (BR).
5	Q_B	Connects to the base of external current drive transistor (Q1).
6	$R_{XIN}-$	**Receive** differential audio input from R_{XOUT} (pin 21), via a decoupling capacitor (C3).
7	$R_{XIN}+$	**Receive** differential audio input,connects to analog ground via a decoupling capacitor (C4).
8	Q_E	Connects to the emitter of external current drive transistor (Q1).
9	$V_{TR}-$	Connects to the negative terminal of the external diode bridge (BR).
10	X_A	External relay contact (K1) connection from $V_{TR}+$ (pin 4), activated by loop seize control output.
11	X_C	External relay contact (K1) connection from X_B (pin 12), activated by loop seize control output.
12	X_B	External relay contact (K1) connection from X_C (pin 11), activated by loop seize control output.
13	MON1	**Ring Start Monitor.** Normally no connection.
14	LPGND	**Loop Ground** is the system ground reference with respect to -48 volts.
15	$\overline{SEIZE}$	**Loop Seize Control (Output).** Active low, will drive a relay (K1) to connect active trunk termination across the tip and ring.
16	$\overline{GSTERM}$	**Ground Start Termination (Output).** Active low, will drive a relay (K2) to provide proper biasing to the tip and ring. This output drive is used for ground start trunk only.
17	$\overline{CSD0}$	**Control System Drive 0 (Output).** Active low, open collector, controlled by codec register B, bit 0.
18	$\overline{CSD1}$	**Control System Drive 1 (Output).** Active low, open collector, controlled by codec register B, bit 1.
19	$T_{XIN}-$	**Transmit (input)** differential audio signal from $V_{TR}+$ (pin 4),via a decoupling capacitor (C2).
20	$T_{XIN}+$	**Transmit (input)** differential audio signal from $V_{TR}-$ (pin 9), via a decoupling capacitor (C1).
21	R_{XOUT}	Audio signal **(output)** from the filter/codec after the D/A conversion. Normally connects to the $R_{xin}-$ (pin 6),via a decoupling capacitor (C3).
22	$V_{cc}+$	**Positive Analog Power Supply Voltage** (+ 12V).
23	$V_{cc}-$	**Negative Analog Power Supply Voltage** (– 12V).
24	MON2	**Monitor** of the audio input signal to the codec transmit filter.
25	V_{ref}	**Voltage Reference (Input)** to the codec (2.5 V ± 0.5%).
26	GNDD	**Digital Ground.**
27	CSTi	**Control ST-Bus (Input).** TTL-Compatible digital input is used to control the function of the filter/codec. Three modes of operation may be selected by applying to this input a logic high (V_{DD}), logic low (GNDD) or an 8- bit serial word, depending on the logic states of CA and $\overline{F1i}$.
28	DSTi	**Data ST-Bus (Input).** Accepts the incoming 8-bit PCM word. Input TTL-compatible.
29	C2i	**Clock (Input)**. TTL-Compatible 2.048MHz clock.
30	DSTo	**Data ST-Bus (Output).** A tri-state digital output drives the PCM bus with the outgoing 8-bit PCM word.

† Components designation refers to Figure 8 unless otherwise stated

Pin Description†

Pin #	Name	Description
31	$\overline{F1i}$	**Framing Signal Type 1 (Input).** Active low digital input enabling (in conjunction with CA) the PCM input, PCM output and digital control input. It is internally sampled on every positive edge of the clock, C2i, and provides frame and channel synchronization.
32	CA	**Control Address (Input).** A three level digital input which enables PCM input and output and determines into which control register (A or B) the serial data, presented to CSTi, is stored.
33	V_{DD}	**Positive Power Supply** (+ 5V).
34	V_{EE}	**Negative Power Supply** (– 5V).
35	$\overline{TG}$	**Tip Lead Ground Detect (Output).** Active low. Digital output of an internal op-amp (LM324, ± 5V) connects in series with a 5 kΩ resistor. Refer to Figure 6.
36	$\overline{RC}$	**Reverse Loop Current Detect (Output).** Active low. Digital output of a comparator (LM339, ± 5V) with a 5 kΩ resistor in series, and internal pull-up with a 17 kΩ resistor to 5V. Refer to Figure 7.
37	$\overline{RV}$	**Ringing Voltage Detect (Output).** Active low. Digital output of a comparator (LM339, ± 5V) with a 5 kΩ resistor in series, and internal pull-up with a 17 kΩ resistor to 5V. Refer to Figure 7.
38	$\overline{FC}$	**Forward Loop Current Detect (Output).** Active low. Digital output of a comparator (LM339, ± 5V) with a 5 kΩ resistor in series, and internal pull-up with a 17 kΩ resistor to 5V. Refer to Figure 7.
39	$\overline{RG}$	**Ring Lead Ground Detect (Output).** Active Low. Digital output of an internal op-amp (LM324, ± 5V) connects in series with a 5 kΩ resistor. Refer to Figure 6.
40	GNDA	**Analog Ground.**

† Components designation refers to Figure 8 unless otherwise stated.

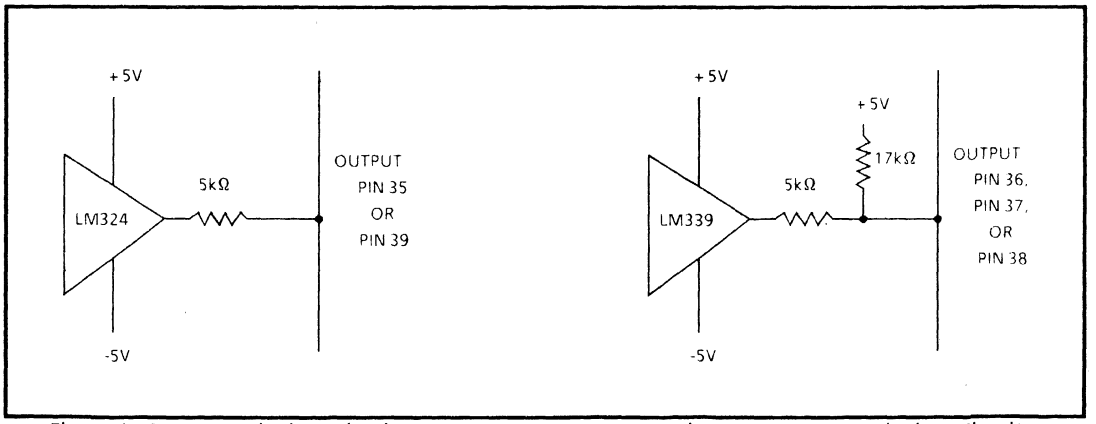


Figure 6 - Output Equivalent Circuit Pin 35 or Pin 39

Figure 7 - Output Equivalent Circuit Pin 36, Pin 37 or Pin 38

Functional Description

The MH89630 is an analog trunk interface between a digital switching equipment (PABX) and the central office. It provides the conversion interface between the voiceband analog signal of a telephone loop and the digital signal required in a digital PCM (Pulse Code Modulation) switching system. In addition, it also provides alerting detection (ringing) for signalling from the far end.

The trunk circuit performs transformerless 2-wire to 4-wire conversion, between the 2-wire trunk and the 4-wire internal transmit and receive pairs which are connected to the filter/codec. The transmit filter of the filter/codec bandlimits the incoming analog frequency range 300 to 3400Hz, while the receive filter ensures that any modulation signal outside the 50 to 3400Hz frequency range from the analog output of the codec, are not passed to the trunk.

Incoming analog (voiceband) signals from the C.O. applied differentially across the tip and ring,are passed through an external full wave bridge rectifier (see Figure 8) to the trunk circuit at the input of T_{XIN-} and T_{XIN+} where a good longitudinal balance at low frequency is provided. The analog signal entering the filter/codec, is sampled at 8kHz, μ-law companded and assigned an 8-bit digital word. This 8-bit digital word is then serially output at DSTo pin at a nominal rate of 2.048MHz, via the output buffer as the 8 bits of the 125μs sampling frame. Figure 3 shows the digital output code of the codec on the module.

The 8-bit PCM encoded digital word from the digital network side is serially transmitted to DSTi input of the trunk circuit where it is decoded and reconstructed into staircase analog signals by the filter/codec. After bandpass filtering, the audio signals are transmitted from the output of R_{XOUT}, through an external decoupling capacitor (C3) to the input of R_{XIN-}. A suitable gain is applied at the active termination before the balanced audio signals output at V_{TR+} and V_{TR-}. These outputs are then differentially applied to the tip and ring through the external full wave bridge rectifier (BR).

A maximum transhybrid loss is provided to ensure that the incoming receive signal is not coupled to the transmit pairs. There are two software selectable options to balance the line impedance. One is a 600 ohms balancing network that is used when feeding channel banks or when performing external tests on the trunk circuit. The second balance network is used to balance against an AT&T compromise network consisting of 350 ohms + 1k ohms shunted by 0.21μF. The latter option is intended for considerable loop lengths as in a real C.O. connection.

All functions of the the trunk interface are controlled by the System Drive (SD) of the codec on the module (see Digital Control Functions for details). The SD control is provided over a dedicated 32 channels ST-BUS serial data link (CSTi). Each trunk interface requires two channels of data to load the Internal Register A and B of the codec. In total, up to 16 trunk circuits can be concatenated into one serial bit stream of 32 channels.

The codec Register A provides the transmit and receive gain setting, the digital and analog loopback, and the power-down function. Depending on the equipment design of VIA NET LOSS plan (VNL), the transmit filter gain of the codec can be adjusted from 0 dB to 7dB in 1dB steps by means of three binary (bit 0,1 & 2) controlled gain pads. By the same token, the receive filter gain can be adjusted from 0dB to -7dB in 1 dB steps by means of three binary (Bit 3, 4 and 5) controlled gain pads. The trunk circuit is so designed that with 0dB gain or loss set in the filter/codec incoming audio will have 4dB of loss, and outgoing audio will have 3dB of gain. Data from the CSTi link is strobed into Register A whenever $\overline{F1i}$ is low and CA is at V_{EE} or GNDD (see Table 1).

The codec Register B provides various circuit functions. Data from the CSTi link is strobed into Register B whenever $\overline{F1i}$ is low and CA is at V_{DD}. The control bits control two uncommitted outputs, ground start termination, loop seize, ring start, balance network and codec testing (see Digital Control Functions for details). Bits 8 and 7 of the Register B are used during manufacturing and testing of the codec. During normal call processing these two bits should be set at '0'.

Signal Detection Circuitry

The signal detection circuitry in MH89630 provides loop state detection outputs for peripheral processor monitoring.

When the central office applies ringing voltage to the Ring lead, the trunk circuit will provide a debounced ringing detector, and output low at $\overline{RV}$ during the ringing burst period. It holds for approximately 100ms after the ringing voltage is removed. Ringing voltage above 45 V_{RMS} at 20Hz will be detected.

The Tip Ground ($\overline{TG}$) and Ring Ground ($\overline{RG}$) outputs provide a means of determining call origination or disconnect handshaking functions. The trunk circuit has very high impedance detection circuitry to

detect both Tip Ground and Ring Ground voltages within about 15 volts of true ground.

Both Forward Current ($\overline{FC}$) and Reverse Current ($\overline{RC}$) outputs are used to determine the polarity of the Tip and Ring pair for signalling purposes in the active (off-hook) state. When the active termination is applied across the Tip and Ring, the forward current is detected and output low at $\overline{FC}$ to indicate the trunk in normal or unreversed state. Some central offices may reverse the polarity of the Tip and Ring as to indicate the talking state. This reverse current will be detected and output low at $\overline{RC}$.

Filter/Codec Timing:

The codec operates in a synchronous manner (see Figure 2a). It is activated on the first positive edge of C2i after $\overline{F1i}$ has gone low. The digital output at DSTo (which is a three state output driver) will then change from a high impedance state to the sign bit of the encoded PCM word to be output. This will remain valid until the next positive edge, when the next most significant bit will be output.

On the first negative clock edge (after $\overline{F1i}$ signal has been internally synchronized and CA is at GNDD or V_{EE}) the logic signal present at DSTi will be clocked into the input shift register as the sign bit of incoming PCM word.

The 8-bit word is thus input at DSTi on negative edges of C2i and output at DSTo on positive edges of C2i.

$\overline{F1i}$ must return to a high level after the 8th clock pulse causing DSTo to enter high impedance and preventing further input data to DSTi. $\overline{F1i}$ will continue to be sampled on every positive edge of C2i. (Note: $\overline{F1i}$ may subsequently be taken low during the same sampling frame to enable entry of serial data into CSTi. This occurs usually mid-frame, in conjunction with CA = V_{DD}, in order to enter an 8-bit control word into Register B. In this case, PCM input and output are inhibited by CA at V_{DD}).

Internally the codec will then perform a decode cycle on the newly input PCM word. The sampled and held analog signal, thus decoded, will be updated 25µs from the start of the cycle. After this, the analog input from the filter is sampled for 18µs, after which digital conversion takes place during the remaining 82µs of the sampling cycle.

Since a single clock frequency of 2.048MHz is required, all digital data is input and output at this rate. DSTo, therefore, assumes a high impedance state for all but 3.9µs of the 125µs frame. Similarly, DSTi input data is valid for only 3.9µs.

Digital Control Functions:

CSTi is a digital input (levels GNDD to V_{DD}) which is used to control the function of the filter/codec. It operates in three different modes depending on thelogic levels applied to Control Address input(CA) and codec enable input ($\overline{F1i}$) (see Table 1).

MODE	CA	CSTi	FUNCTION
1	V_{EE}	GNDD	Normal operation.
		V_{DD}	Power down.
2	V_{EE}	Serial Data	8-bit control word into Register A. Register B is reset.
3	GNDD	Serial Data	8-bit control word into Register A. Register B unaffected.
	V_{DD}	Serial Data	8-bit control word into Register B. Register A unaffected.

Table 1 - Digital Control Modes

Note 1: $\overline{F1i}$ at GNDD for each mode of operation.
Note 2: PCM input and output inhibited by CA = V_{DD} when in Mode 3.

Mode 1

CA = -5V (V_{EE}); CSTi = 0V (GNDD)
The filter/codec is in normal operation with nominal transmit and receive gain of 0dB. The SD outputs are in their active states and the test modes cannot be entered.

CA = -5V (V_{EE}); CSTi = + 5V (V_{DD})
A state of power-down is forced upon the codec whereby DSTo becomes high impedance,transmit filter (V_R) is connected to GNDA and all analog sections have power removed.

Mode 2

CA = -5V (V_{EE}); CSTi receives an 8-bit control word. CSTi accepts a serial data stream synchronously with DSTi (i.e., it accepts an 8-bit serial word in a 3.9µs timeslot, updated every 125µs, and is specified identically to DSTi for timing considerations). This 8 -bit control word is entered into Control Register A and enables programming of the following functions: transmit and receive gain, power-down, loopback. Register B is reset to zero and the SD outputs assume their inactive state. Test modes cannot be entered.

Mode 3

CA = 0V (GNDD); CSTi receives an 8-bit control word. As in Mode 2, the control word enters Register A and the aforementioned functions are controlled. In this mode, however, register B is not reset, thus not affecting the states of the SD outputs.

CA = +5V (V_{DD}); CSTi receives an 8-bit control word. In this case the control word is transferred into Register B. Register A is unaffected. The input and output of PCM data is inhibited.

The contents of Register B control six outputs, SD5-SD0, which in turn control the output function of the trunk circuit (see Table 3) and also provide entry into one of the three test modes of the codec.

Note: for Modes 1 and 2, $\overline{F1i}$ must be at logic low for one period of 3.9µs, in each 125µs cycle, when PCM data is being input and output, and the control word at CSTi enters Register A. For Mode 3, $\overline{F1i}$ must be at a logic low for two periods of 3.9µs, in each 125µs cycle. In the first period, CA must be at GNDD or V_{EE}, and in the second period CA must be high (V_{DD}).

Control Registers A & B:

The contents of these registers control the filter/codec functions as described in Tables 2 and 3.

Bit 7 of the registers is the MSB and is defined as the first bit of the serial data stream input (corresponding to the sign bit of the PCM word).

On initial power-up these registers are set to the power-down condition for a maximum of 25 clock cycles, during which time it is impossible to change the data in these registers.

Loopback:

Loopback of the filter/codec is controlled by the control word entered into Register A. Bits 6 and 7 (most significant bits) provide either a digital or analog loopback condition.

Digital loopback is defined as follows:

1) PCM input data at DSTi is loaded into the PCM input register and the output of this register is connected to the input of the 3-state PCM output buffer.

2) The digital input to the codec is forced to (-0).

7	6	5	4	3	2	1	0
Functional Control		Receive (D/A) Filter Gain			Transmit (A/D) Filter Gain		

BIT 2	BIT 1	BIT 0	TRANSMIT (A/D) FILTER GAIN (dB)
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	+4
1	0	1	+5
1	1	0	+6
1	1	1	+7
BIT 5	**BIT 4**	**BIT 3**	**RECEIVE (D/A) FILTER GAIN (dB)**
0	0	0	0
0	0	1	-1
0	1	0	-2
0	1	1	-3
1	0	0	-4
1	0	1	-5
1	1	0	-6
1	1	1	-7
BIT 7	**BIT 6**	**FUNCTIONAL CONTROL**	
0	0	Normal Operation	
0	1	Digital Loopback	
1	0	Analog Loopback	
1	1	Power Down	

Table 2 - Control States - Register A

3) The output of the PCM encoder is disabled and thus the encoded data is lost. The PCM output at DSTo is determined by the PCM input data.

Analog loopback is defined as follows:

1) PCM input data is decoded and filtered as normal but not output at V_R of the codec.

2) Analog output buffer at V_R has its input shorted to GNDA and disconnected from the receive filter output.

3) Analog input to the codec at V_X is disconnected from the transmit filter input.

4) The receive filter output is connected to the transmit filter input. Thus the decode signal is fed back through the receive path and encoded in the normal way. The analog output buffer at V_R is not tested by this configuration.

In both cases of loopback, DSTi is the input and DSTo is the output.

7	6	5	4	3	2	1	0
CODEC TESTING		BALANCE NETWORK	RING START	LOOP SEIZE	GSTERM	CSD1	CSD0

BIT	NAME	DESCRIPTION
0	CSD0	When this bit is logic '0', the control output is open collector and the emitter is internally tied to GNDD. If this bit is logic '1', the control output will sink to zero. This is uncommitted control output which can be used for a relay drive or status lamp control.
1	CSD1	
2	GSTERM	This control output is primarily used for Ground Start Trunk only. A logic'1', the output will drive a relay (K2) to provide proper biasing to the Tip and Ring. For Loop Start Trunk,this bit is always set at '0'.
3	Loop Seize	A logic '1', the control output of loop seize will activate a relay (K1) to connect the trunk active termination across the Tip and Ring. Toggling this bit with appropriate timing will transmit dial pulse information to the central office.
4	Ring Start	For Ground Start Trunk only, a logic '1' enables the trunk circuit to ground the Ring conductor through a low impedance (390Ω). This is a signal to the central office that the interface is seizing the line. For Loop Start Trunk, it should be permanently set at logic '0'.
5	Balance Network	A logic'0'will select 600Ω transhybrid balance network.For a long haul trunk,the AT&T compromise network should be selected to improve transhybrid loss,which is set at '1'.
6,7	Codec Testing	These two bits are used during manufacturing process in testing the codec and must be set to 0 for normal operation..

Table 3 - Control States - Register B

Power-Down

Power-down of the codec is achieved in several ways:

Internal Control

1) Initial Power-Up. Initial application of V_{DD} and V_{EE} causes power-down for a period of 25 clock cycles and during this period the codec will accept input only from C2i. The register B is reset to zero forcing SD0-5 to be inactive. Bits 0-5 of Register A (gain adjust bits) are forced to zero and bits 6 and 7 of Register A become logic high, thus reinforcing the power-down.

2) Loss of C2i. Power-Down is entered 10 to 40µsec after C2i has assumed a continuous logic low (GNDD), the digital data and status is indeterminate.

External Control

1) Register A. Power-down is controlled by bits 6 and 7 (when both at logic high) of Register A which in turn receives its control word input via CSTi, when $\overline{F1i}$ is low and CA input is either at V_{EE} or GNDD. Power is removed from the filters and analog sections of the codec. The analog output buffer at V_R will be connected to GNDA. DSTo becomes high impedance and the clocks to the majority of the logic are stopped. SD outputs are unaffected and may be updated as normal.

2) CSTi Input. With CA at V_{EE} and CSTi held at continuous logic high, the codec assumes the same state as described in External Control (1) above.

Application

A typical application circuit shown in Figure 8 illustrates the use of trunk circuit to interface to the central office. As can be seen there are a few external components that are required to complete the circuit. The Dummy Ringer (R6, C6), part of the 600 ohm termination impedance, is required for the Loop Start and Ground Start Trunk. The external full wave bridge rectifier (BR) is used to provide the positive and negative terminals for DC active termination.

When the loop seize control output is active, it will activate the external relay K1 to apply termination across the Tip and Ring lead. The relay contact (K1) closed at X_A, will supply power to active termination, while the other relay contact (K1) closed between X_B and X_C, will provide supply voltage for the internal circuit. The power transistor (Q1) supplies current gain for the active

Components List

R1,R2	= 30.9kΩ, ± 1%, ¼w
R3,R4	= 30kΩ, ± 5%, ¼w
R5	= 510Ω, ± 5%, ¼w
R6	= 10kΩ, ± 5%, ¼w
R7	= 100kΩ, ± 5%, ¼w
R8,R9,R10,R11,R12	= 12kΩ, ± 5%, ¼w
C1,C2,C3,C4	= 0.22µF, ± 10%, 100V
C5	= 0.1µF, ± 5%, 250V
C6	= 1.0µF, ± 5%, 250V
Q1	= MJE340, NPN 300V, 0.5A, 20w
Q2 ,Q3	= 2N3645, PNP 60V, 0.5A, 20w
D1,D2	= 1N4148, 75V, 0.2A, 0.5w
K1,K2	= 2A Reed Relay, E/M 12V 2FormC Dip
BR	= A Diode Bridge Rectifier 400V 1A Dip VM48
RV1,RV2, RV3	= Varistor Metal Oxide 395V,45 Joules V150LA10A

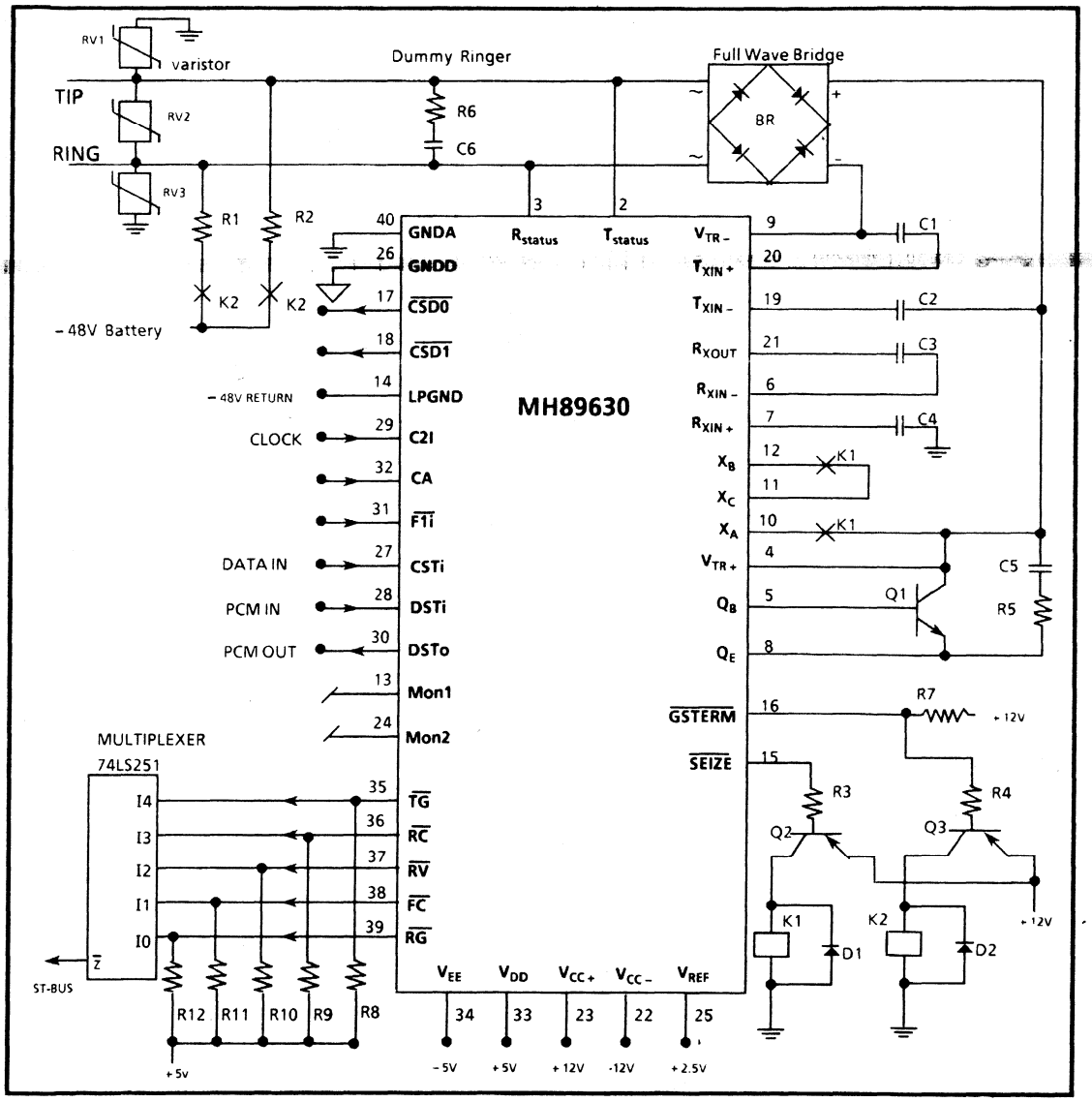


Figure 8 - Application Circuit

termination. Resistor (R5) and capacitor (C5) is used for high frequency filtering.

For Ground Start Trunk, output low at $\overline{\text{GSTERM}}$ will activate the relay K2 to connect -48 volts through a resistor R1 to the Ring lead and R2 to the Tip lead.

If the central office is Loop Start , the bit 2 of the Register B in the filter /codec should be set at '0'.

Figure 9 shows a simple digital switching system using the trunk circuit to interface with the central office.

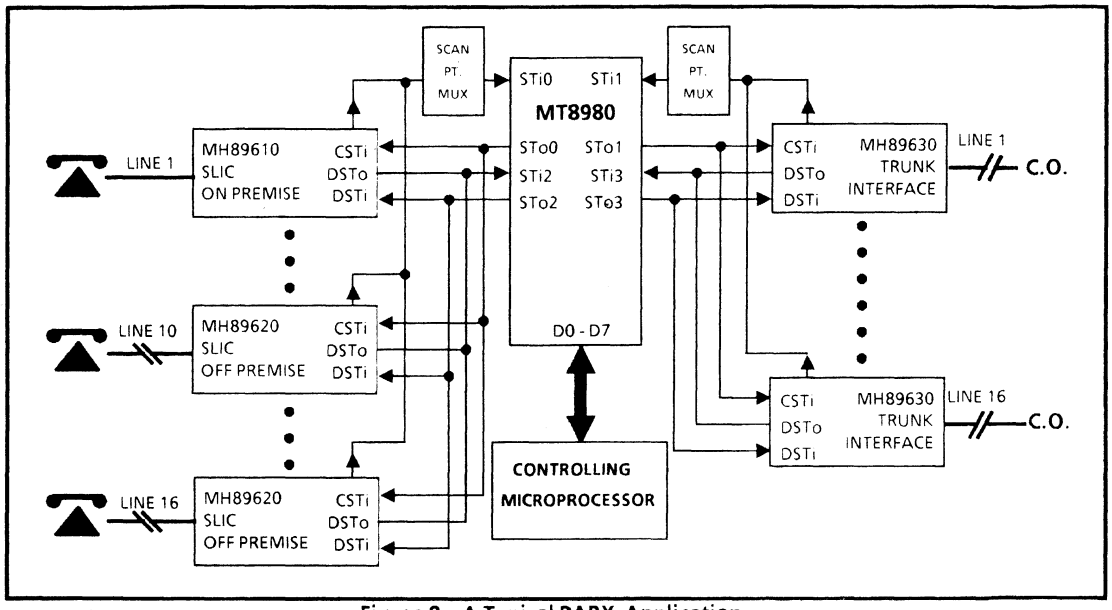


Figure 9 - A Typical PABX Application

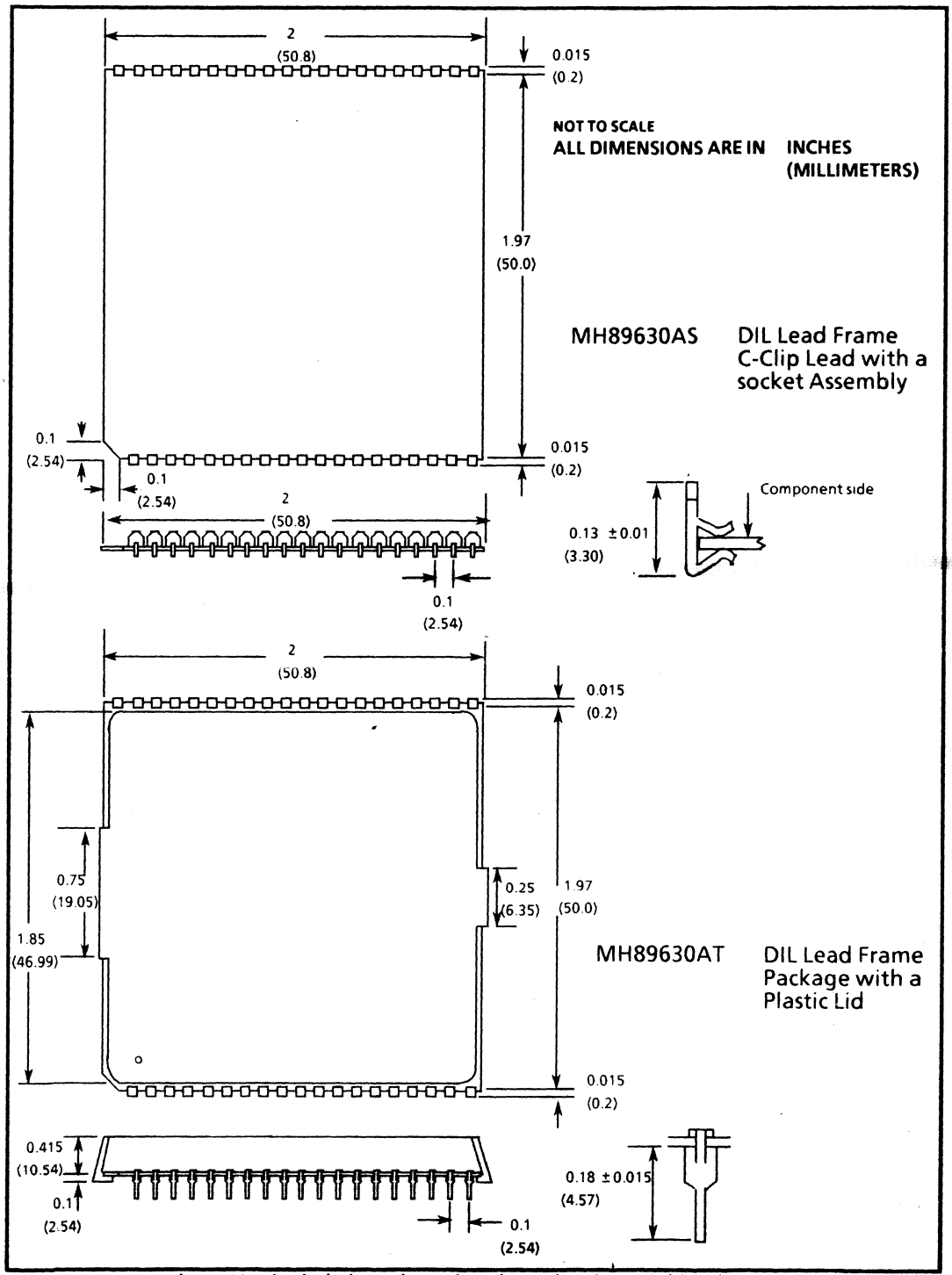


Figure 10 - Physical Dimensions of 40 Pin Dual In Line Hybrid Package

ST-BUS™ FAMILY MH89635
A-Law Central Office Interface

Preliminary Information

9161-002-078-NA ISSUE 1 AUGUST 1986

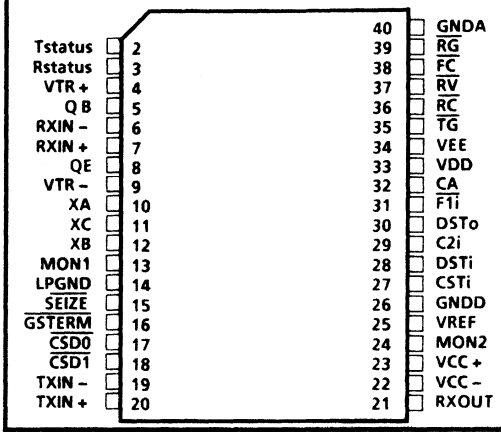
Features

- MITEL ST-BUS™ compatible
- Transformerless 2W to 4W conversion
- A/D and D/A conversion
- Conforms with CCITT G.711 and G.712 A-Law PCM
- Line state detection outputs:
  - -forward current -reverse current
  - -ring ground -tip ground
  - -ringing voltage
- Line state control outputs:
  - - loop seize signalling
  - -two uncommitted control outputs
- Software selectable control:
  - -ground or loop start termination
  - -audio transmit and receive gain control
  - -600 Ω or an alternative complex impedance balance network
- **Analog and digital loopback**

Applications

- Digital PBX Interface to Central Office
- Subscriber line concentrators

Pin Connections



Ordering Information

MH89635AT	40 pin DIL Lead Frame Hybrid Package with Plastic Lid
MH89635AS	40 pin DIL C-Clip Lead with a Socket Assembly

0° C TO 70° C

Description

The Mitel MH89635 central office trunk interface circuit provides a complete audio and signalling link between digital switching equipment and a central office. The loop seize circuitry is controlled via software to provide either loop start or ground start termination to the C.O. The device is fabricated using thick film hybrid technology to achieve optimized circuit design and high circuit density.

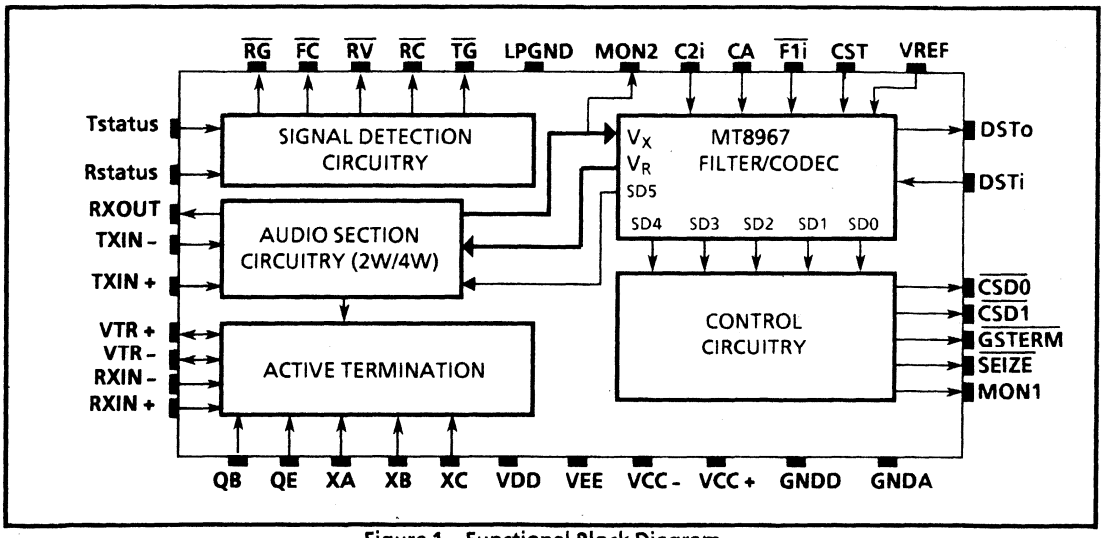


Figure 1 - Functional Block Diagram

Refer to the MH89630 Data Sheet for the functional description. Contact your Mitel representative for more information.

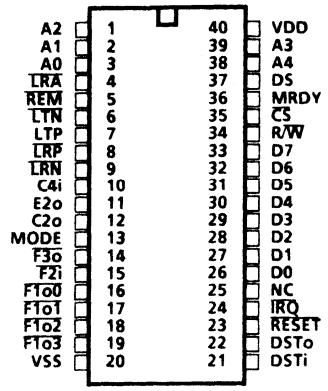
ISO-CMOS ST-BUS™ FAMILY MT8970
Digital Line Interface Circuit
Preliminary Information

9161-002-026-NA ISSUE 3 AUGUST 1986

Features
- MITEL ST-BUS™ Compatible
- Full Duplex Transmission over 2 Telephone Pairs
- Selectable 256 or 128 kbit/s Line Rate
- Interface for Both Ends of Line
- 3 Port Device:
  - 2 or 4 x 64 kbit/s Channel Line Port
  - 4 x 64 kbit/s Channel ST-BUS™ Port
  - 3 Channel Asynchronous Microprocessor Port
- Frame Synchronisation and Clock Extraction
- Modified AMI Coded Line Transmission
- 6800/68000 Bus Compatible
- Single 4.096 MHz Clock Input

Applications
The MT8970 can be used as the digital line interface within telephone sets, PBXs, computers, computer peripherals etc.

Pin Connections



Ordering Information

MT8970AC 40 Pin Ceramic DIL
0°C to 70°C

Description
The MT8970 is a digital line interface which is capable of transmitting and receiving data on a twisted pair line at speeds up to 256 kbit/s formatted in 4 x 64 kbit/s channels. Data may be switched between any channels on its 3 ports. It is a general interface between an ST-BUS™ port, a microprocessor port and a 128 or 256 kbit/s line. The MT8970 is fabricated in Mitel's ISO-CMOS technology.

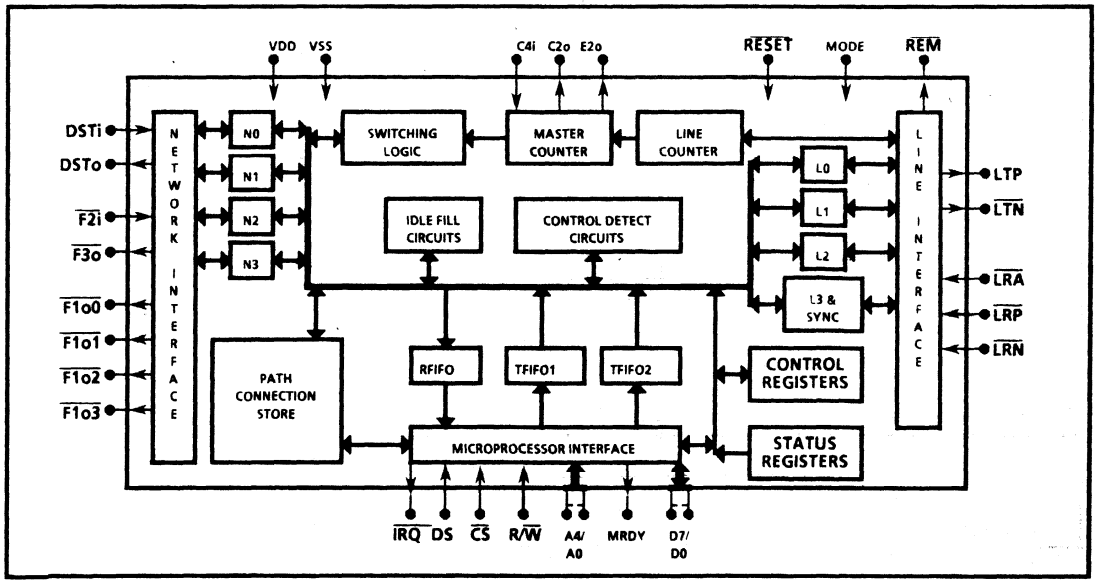


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7	V
2	Voltage at Digital Inputs	V_I	-0.3	V_{DD} + 0.3	V
3	Current at Digital Inputs	I_I		20	mA
4	Voltage at Digital Outputs	V_O	-0.3	V_{DD} + 0.3	V
5	Current at Digital Outputs	I_O		20	mA
6	Storage Temperature	T_{ST}	-65	150	°C
7	Power Dissipation	P		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	0		70	°C	
2	Supply Voltage	V_{DD}	4.75	5	5.25	V	
3	Input Voltage	V_I	0		V_{DD}	V	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Power Dissipation	P		10	26.2	mW	Outputs unloaded
2	Supply Current	I_{DD}		2	5	mA	Outputs unloaded
3	Input High at $\overline{\text{RESET}}$ Pin	V_{IHR}	4.0		V_{DD}	V	At least 0.5 V Hysteresis
4	Input Low at $\overline{\text{RESET}}$ Pin	V_{ILR}	0		1	V	At least 0.5 V Hysteresis
5	Input High at Other Inputs	V_{IH}	2.7		V_{DD}	V	
6	Input Low at Other Inputs	V_{IL}	0		0.4	V	
7	Input Leakage	I_{IL}		0.1	1	uA	
8	Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = 1.6 mA
9	Output High Current	I_{OH}	1.6	15		mA	Source. V_{OH} = 2.4 V
10	Output High Current	I_{OH}	1.3			mA	Source. V_{OH} = 3.0 V
11	Output Low Voltage	V_{OL}	V_{SS}		0.4	V	I_{OL} = 6.4 mA
13	Output Low Current	I_{OL}	6.4	15		mA	Sink. V_{OL} = 0.4 V
14	Output Low Current	I_{OL}	15			mA	Sink. V_{OL} = 2.0 V
15	High Impedance Leakage	I_{OZ}			10	uA	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Capacitances

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Input Pin Capacitance	C_I		10		pF	
2	Output Pin Capacitance	C_O		10		pF	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figures 2 & 3)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Clock Period*	t_{CLK}		244		ns	
2	Clock Width High or Low	t_{CHL}		102		ns	
3	Clock Transition Time	t_{CTT}		20		ns	
4	C2o Delay	t_{C2D}		40	80	ns	30 pF load
5	E2o Delay	t_{E2D}		50	100	ns	30 pF load

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* To ensure system synchronisation a tolerance of 0.05% on the C4i inputs of the devices at either end of the line is required.

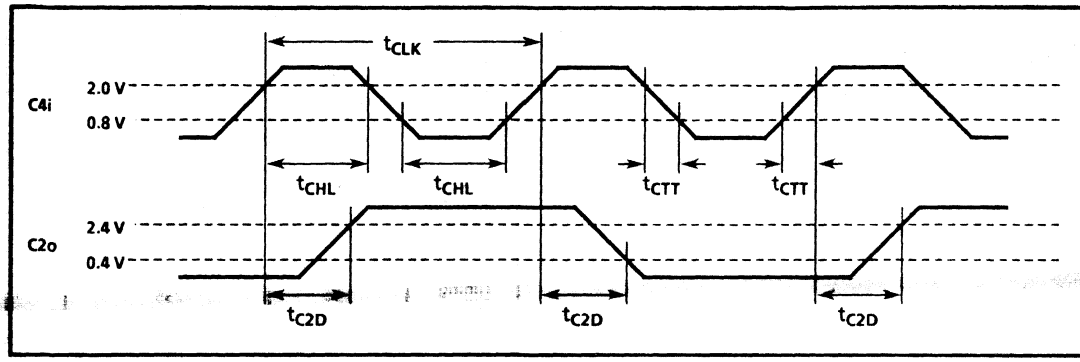


Figure 2 - C2o Timing

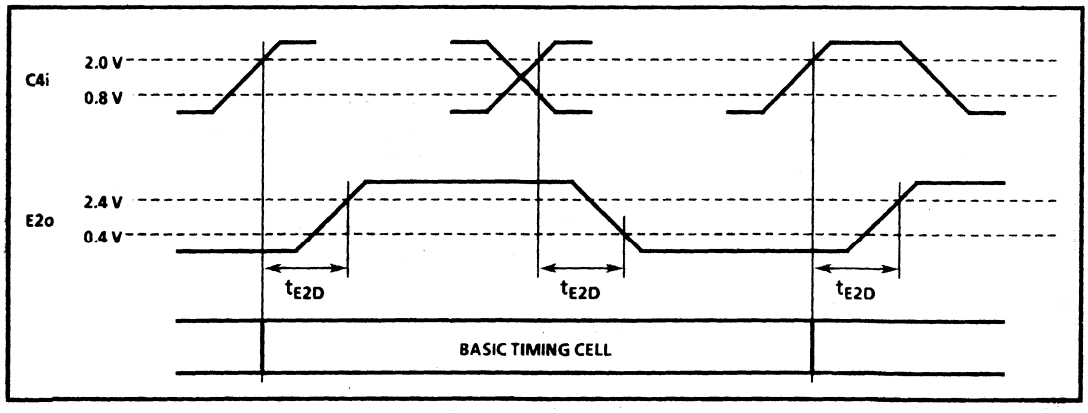


Figure 3 - E2o Timing and Definition of Basic Timing Cells

NB: The AC Characteristics for the ST-BUS™ and Line Ports are specified in terms of the Basic Timing Cells. This allows the same specification to be used in both the Master and the Slave Mode.

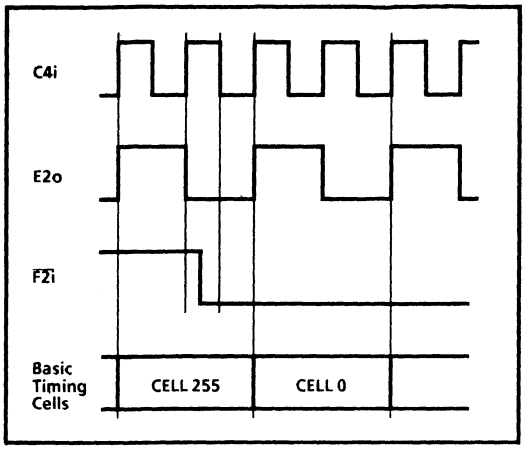


Figure 4 - Alignment of Basic Timing Cells in Master Mode

NB: In Master Mode E2o is not corrected and Basic Timing Cell 255 does not change.

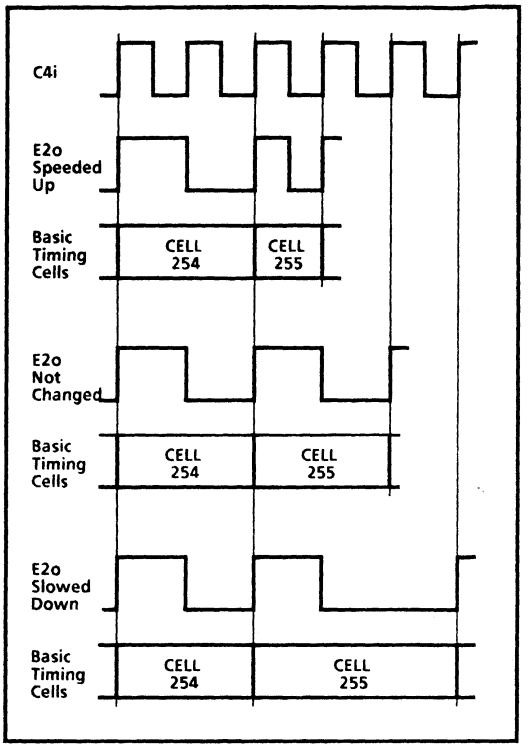


Figure 5 - Correction of E2o and Basic Timing Cell 255 in Slave Mode

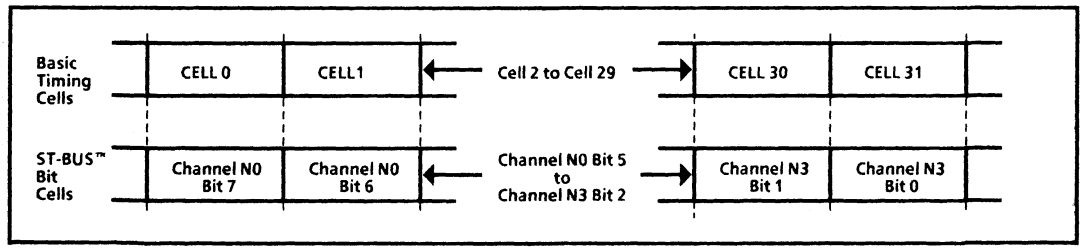


Figure 6 - Network Channel Alignment

NB: In Master Mode the frame synchronization is controlled by the $\overline{F2i}$ input (Figure 4)

In Slave Mode the frame synchronization is determined by the arrival of the SYNC bytes on the L3 channel (see Users' Guide) and is indicated on the $\overline{F3o}$ and $\overline{F1o0}$ to $\overline{F1o3}$ outputs (Figures 13 and 14). In Slave Mode Basic Timing Cell 255 is corrected by the internal phase-locked loop.

AC Electrical Characteristics† - ST-BUS™ Streams (Figures 4, 5, 6 & 7)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	DSTo Delay	t_{STD}	0	20	100	ns	50 pF load
2	DSTi Set Up Time	t_{STS}	50			ns	
3	DSTi Hold Time	t_{STH}	50			ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

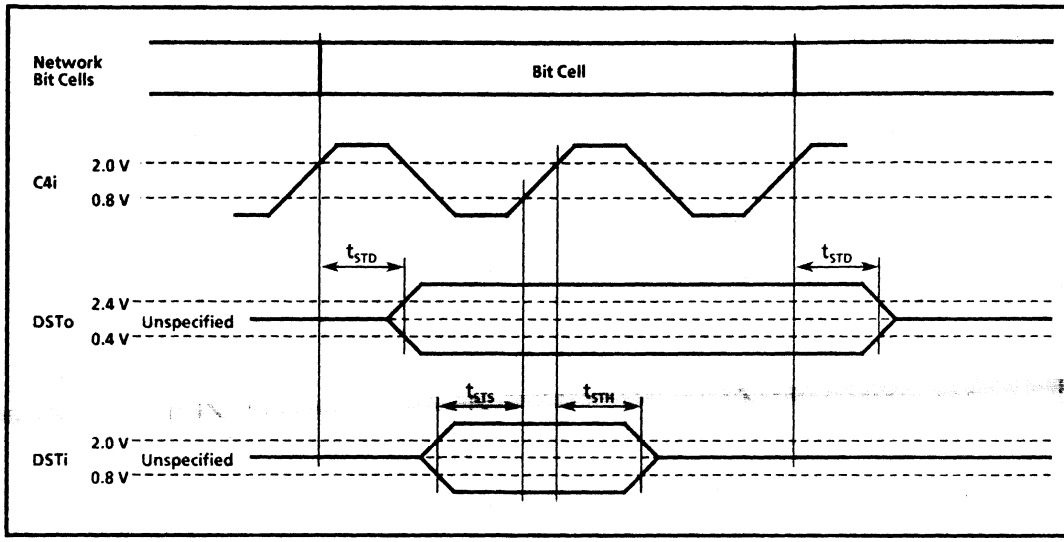


Figure 7 - ST-BUS™ Streams

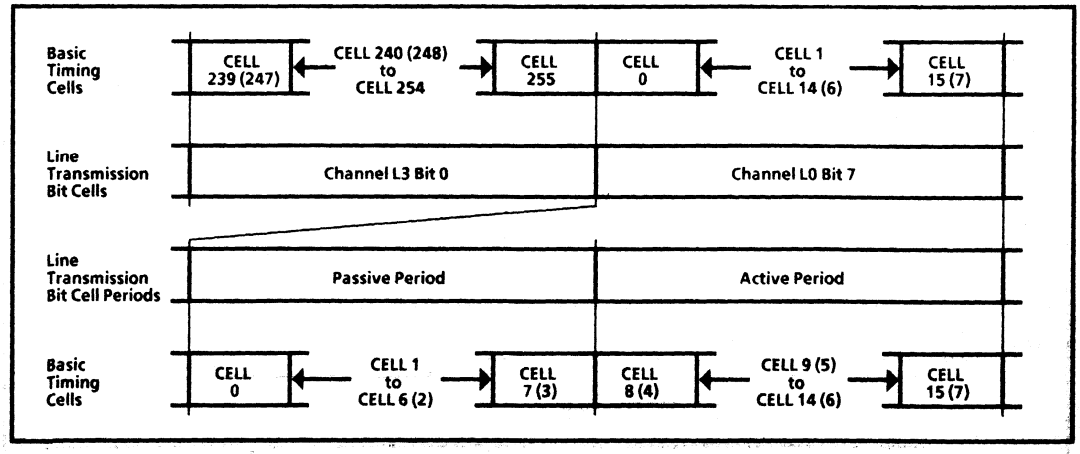


Figure 8 - Line Channel Alignment for Transmission at 128 (256) kbit/s

AC Electrical Characteristics† - Line Data (Figures 4, 5, 8, 9 & 10)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Line Transmit Delay	t_{LTD}	0		150	ns	50 pF load
2	Line Receive Period	t_{LRP}	3.2			µs	
3	Line Receive Active Delay	t_{RAD}	1.6			µs	
4	Line Receive Data Delay	t_{RDD}	1.6			µs	
5	Line Receive Data Set Up Time	t_{RDS}			400	ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
NB: Data transmitted on the line should be at the same rate as data received from the line to within 0.1% averaged over 125 µs. This may be ensured by having a tolerance of 0.05% or better on the C4i inputs of the devices at either end of the line.

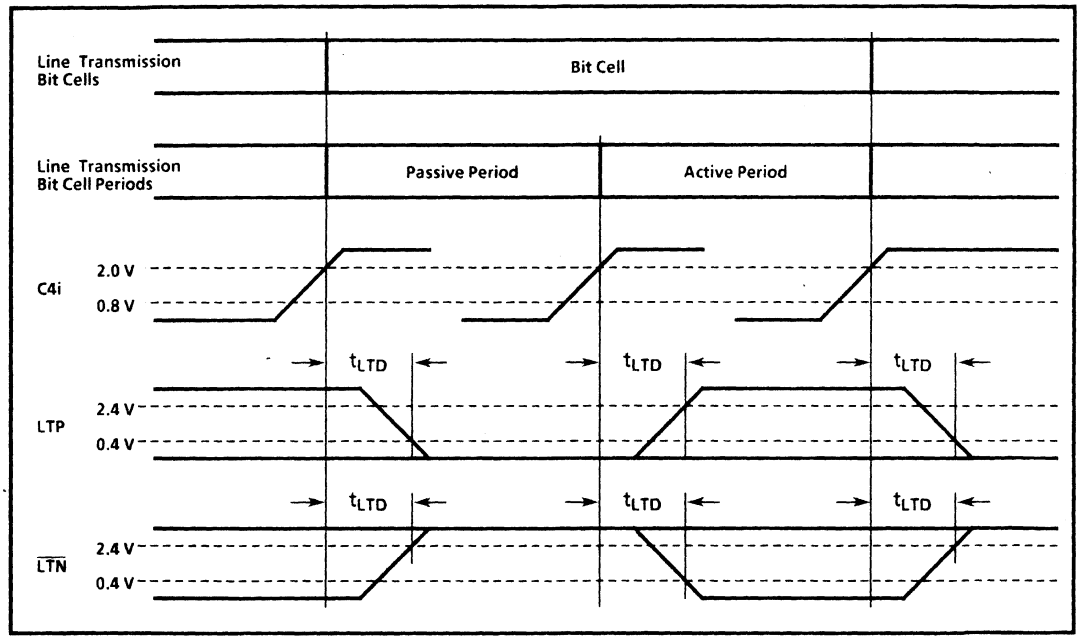


Figure 9 - Line Transmission Data

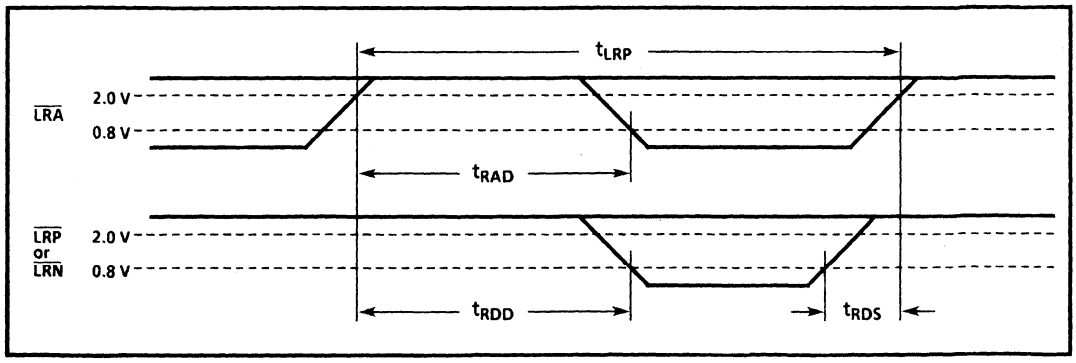


Figure 10 - Line Receive Data

AC Electrical Characteristics† - ST-BUS™ Synchronisation (Figures 4, 5, 6, 11, 12, 13 & 14)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	F2i Set Up Time	t_{F2S}	10		200	ns	
2	F3o Delay	t_{F3D}	0	110	150	ns	50 pF load
3	F1o0 / F1o3 Delay	t_{F1D}	0	110	150	ns	50 pF load

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

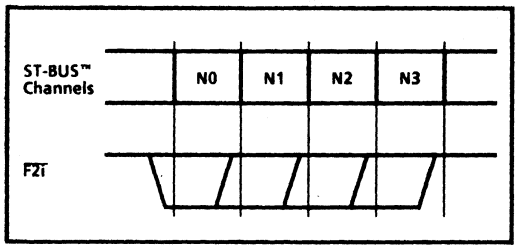


Figure 11 - $\overline{F2i}$ Alignment

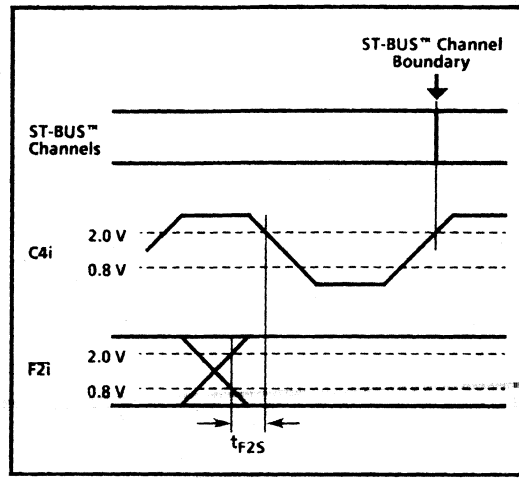


Figure 11 - $\overline{F2i}$ Timing

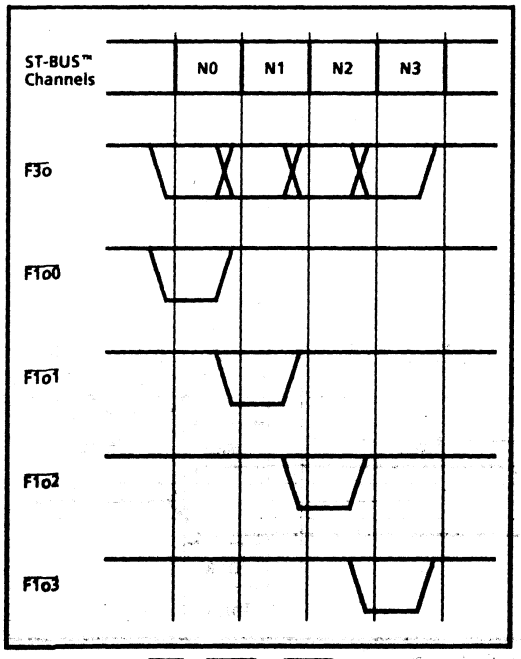


Figure 13 - $\overline{F3o}$ & $\overline{F1o0}$ to $\overline{F1o3}$ Alignment

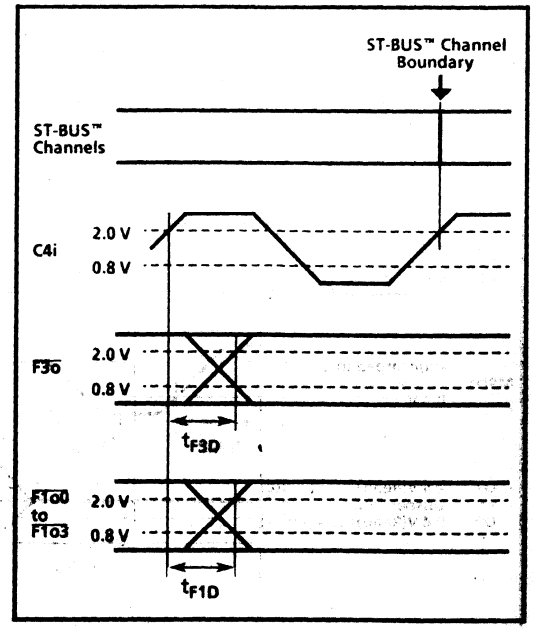


Figure 14 - $\overline{F3o}$ & $\overline{F1o0}$ to $\overline{F1o3}$ Timing

AC Electrical Characteristics† - Bus Interface Timing (Figure 15)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Chip Select Set Up Time - Read	t_{CSR}	-25			ns	
2	Chip Select Set Up Time - Write	t_{CSW}	40			ns	
3	Read/Write Set Up Time	t_{RWS}	80			ns	
4	Address Set Up Time	t_{ADS}	30			ns	
5	Data Strobe Width	t_{DSW}	150			ns	
6	Memory Ready Delay	t_{MRD}	0	25	90	ns	50 pF load
7	Read Data Delay*	t_{RDD}		70	125	ns	50 pF load
8	Write Data Set Up Time	t_{WDS}	145			ns	
9	Data Hold Time - Read	t_{DHR}	20	25		ns	50 pF load
10	Data Hold Time - Write	t_{DHW}	18			ns	
11	Chip Select Hold Time	t_{CSH}	20			ns	
12	Read/Write Hold Time	t_{RWH}	0			ns	
13	Address Hold Time	t_{ADH}	0			ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Taken from the later of DS high and $\overline{CS}$ low

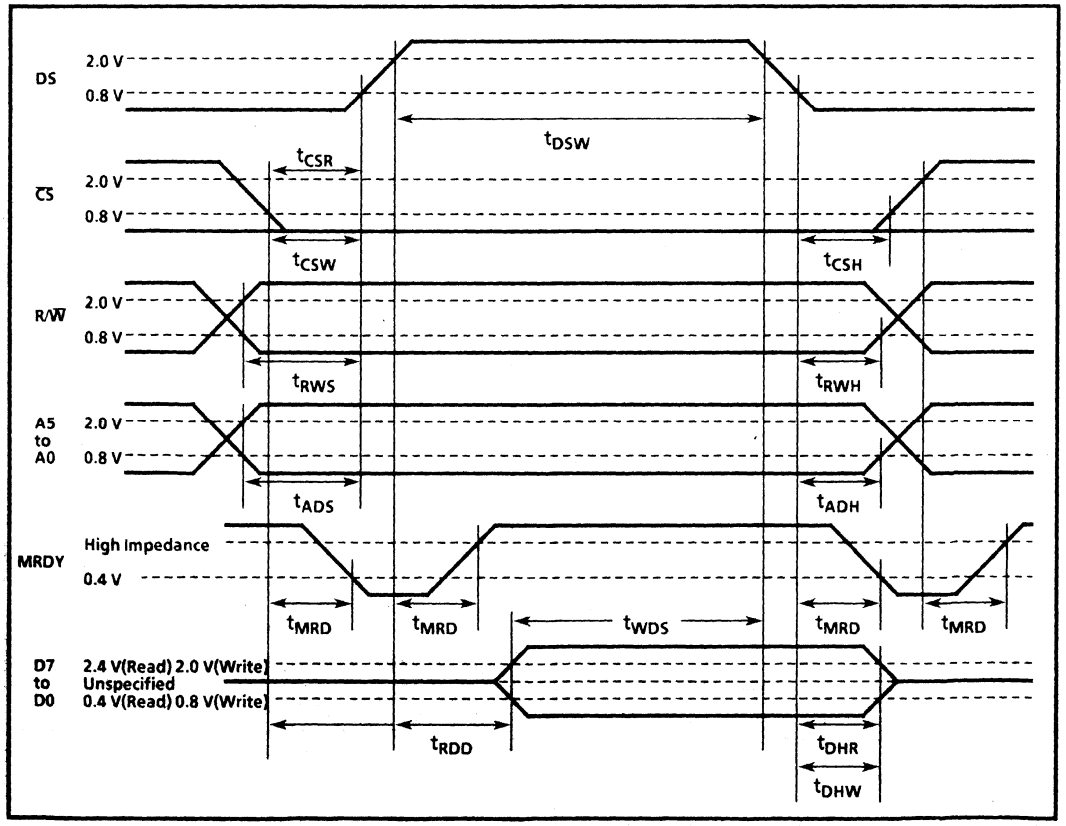


Figure 15 - Processor Interface Timing

Pin Description

Pin	Name	Description
1 / 3	A2 / A0	**Address 2 to 0 (Inputs).** These are inputs for the address lines on the microprocessor interface.
4	$\overline{\text{LRA}}$	**Line Receive Active (Input).** A low on this input is the signal that the level detector has sensed that the AMI coded line is non-zero. This signal may be triggered at line voltages different from those for $\overline{\text{LRP}}$ and $\overline{\text{LRN}}$. It is used to synchronize the phase locked loop.
5	$\overline{\text{REM}}$	**Remote Reset (Open Drain Pulldown Output).** This pin is high-impedance during normal operation. It is pulled low if an all 1s signal is received on the line for more than 2 superframes (4mS). The pin goes to its high impedance state during a device reset. This feature can be used for simple signalling or to generate a reset.
6	$\overline{\text{LTN}}$	**Line Transmit Negative (Complementary Output).** A low on this pin indicates that the line driver should pull the line low for AMI coded transmission.
7	LTP	**Line Transmit Positive (Complementary Output).** A high on this pin indicates that the line driver should pull the line high for AMI coded transmission.
8	$\overline{\text{LRP}}$	**Line Receive Positive (Input).** A low on this pin is the signal to the device that the line detector has sensed that the AMI coded line is high.
9	$\overline{\text{LRN}}$	**Line Receive Negative (Input).** A low on this pin is the signal to the device that the line detector has sensed that the AMI coded line is low.
10	C4i	**Clock - 4.096 MHz (Input).** This is the input for the 4.096 MHz clock.
11	E2o	**Extracted Clock - 2.048 MHz (Complementary Output).** This pin provides a 2.048MHz clock which is corrected by the line data rate when the MODE pin is high (Slave Mode). The clock is corrected once every 256 cycles. If the MODE pin is low (Master Mode) then this output is equivalent to C2o.
12	C2o	**Clock - 2.048 MHz (Complementary Output).** This pin provides a 2.048MHz clock which is obtained by dividing the 4.098MHz input clock on C4i by two.
13	MODE	**Mode (Input).** A high on this pin puts the chip in set mode and a low puts it in system mode. In Master Mode the C4i clock and the $\overline{\text{F2i}}$ pulse control the timing and synchronisation. In Slave Mode the device is synchronized to the incoming line data rate and the E2o output may be corrected. In either mode the E2o output clock is synchronized to the ST-BUS™ and to the transmitted line bit streams.
14	$\overline{\text{F3o}}$	**Framing Signal Type 3 (Complementary Output).** A low on this output signals that some ST-BUS™ channel is active.
15	$\overline{\text{F2i}}$	**Framing Signal Type 2 (Input).** This pin should be pulled low once every frame to select channels on the ST-BUS™ port when the chip is in Master Mode (MODE pin low) In Slave Mode frame synchronization is obtained from the line and is indicated on the $\overline{\text{F3o}}$ and $\overline{\text{F1o0}}$ to $\overline{\text{F1o3}}$ pins. Any logical signal may be applied to this pin when the chip is in Slave Mode but the pin should not be allowed to float.
16 / 19	$\overline{\text{F1o0}}$ / $\overline{\text{F1o3}}$	**Framing Signal Type 1 for N0 / 3 (Complementary Outputs).** A low on one of these outputs indcates that the corresponding N0 to N3 ST-BUS™ channel is active.
20	VSS	**Ground (Power Input).**
21	DSTi	**Data ST-BUS™ (Input).** This is the input pin for channels on the ST-BUS™ port.
22	DSTo	**Data ST-BUS™ (Three-State Output).** This is the output pin for channels on the ST-BUS™ port.

Pin Description (continued)

Pin	Name	Description
23	$\overline{\text{RESET}}$	**Reset (Input).** A low on this input causes the device to reset the three ports and sets the RESET bit in Control Register 1. The device will not come out of reset until this bit is cleared through the microprocessor interface. During reset frame synchronisation is lost, RFIFO, TFIFO1 and TFIFO2 are cleared, LTP is pulled low, $\overline{\text{LTN}}$ is pulled high, and DSTo, $\overline{\text{REM}}$ and $\overline{\text{IRQ}}$ are put into their high impedance state. If the MODE pin is high (Slave Mode) E2o is pulled low.
24	$\overline{\text{IRQ}}$	**Interrupt Request (Open Drain Pulldown Output).** This output is pulled low to signal an interrupt request on the microprocessor interface.
25	NC	**No Connect.** Leave this pin unconnected.
26 / 33	D0 / D7	**Data 0 to 7 (Three-state I/O Pins).** These are the bidirectional data pins on the microprocessor interface.
34	R/$\overline{\text{W}}$	**Read / Write (Input).** This is the input for he read/write signal on the microprocessor interface - high for read, low for write.
35	$\overline{\text{CS}}$	**Chip Select (Input).** This is the input for the active low chip select signal on the microprocessor interface.
36	MRDY	**Memory Ready (Open Drain Pulldown Output).** This is the memory ready output on the microprocessor interface. It is held low until the chip has completed a read or write.
37	DS	**Data Strobe (Input).** This is the input for the data strobe on the microprocessor interface.
38 / 39	A4 / A3	**Address 4 to 3 (Inputs).** These are inputs for the address lines on the microprocessor interface.
40	VDD	**+ 5V (Power Input).**

Functional Description

The MT8970 switches data between channels on 3 ports which operate at different speeds. The data is in the form of 8 bit bytes which may be PCM coded speech. At the line and ST-BUS™ ports the bytes are part of serial data streams, while at the microprocessor port the bytes arrive and depart on the parallel data bus. The microprocessor port also allows access to the Path Connection Store which defines the paths between the channels and to the Control and Status Registers through which the MT8970 is monitored and controlled.

Data arrives at the ST-BUS™ port as a 2048 kbit/s serial ST-BUS™ stream on the DSTi pin. This stream contains 32 channels, each having the bandwidth of digitized speech (64 kbit/s). The MT8970 may use up to four consecutive channels which are referred to as the N0 to N3 channels.

On the microprocessor port data for transmission should be written to hex addresses 19 (TFIFO1) or 1A (TFIFO2).

Data arriving at the line port is AMI (Alternate Mark Inversion) coded with zero bytes replaced with a special zero code. The AMI coding is supplied to the chip on the $\overline{\text{LRA}}$, $\overline{\text{LRP}}$ and $\overline{\text{LRN}}$ pins. This data should arrive at 128 kbit/s or 256 kbit/s (2 or 4 channels). The line channels are L0, L1, L2 and L3 at 256 kbit/s or L0 and L3 at 128 kbit/s Two bytes out of every 16 on the L3 channel are used for synchronization.

The data is routed to destinations according to the contents of the Path Connection Store. There are two types of Service Circuit, Idle-fill or Control-detect, which may be used on connections. Idle-fill Service Circuits allow asynchronous data written to the TFIFOs to be matched to the 64 kbit/s ST-BUS™ and line channels by injecting additional bytes. Control Detect Service Circuits allow the additional bytes to be stripped.

Data routed to the ST-BUS™ channels is output as a ST-BUS™ stream on the DSTo pin.

Data routed to the microprocessor port is placed in the RFIFO buffer (hex address 18).

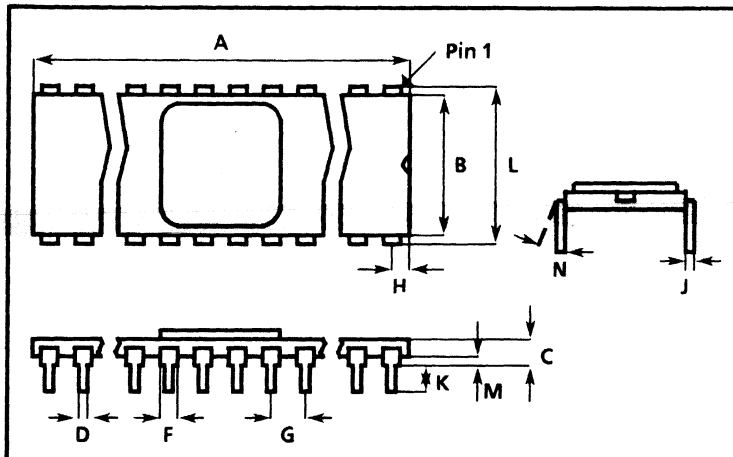
Data routed to the line port is AMI coded with zero bytes replaced by zero code and the coding is output on the LTP and $\overline{\text{LTN}}$ pins at either 128 kbit/s or 256 kbit/s. Synchronization on the line is achieved by transmitting 2 "SYNC" bytes once every 16 bytes on the L3 channel.

The microprocessor interface also gives access to the 3 Control Registers and the 3 Status Registers allowing the microprocessor to control and monitor the MT8970.

The MT8970 has the capability to concatenate connections between the microprocessor channels and the ST-BUS™ and line channels, creating an effective data channel of up to 256 kbit/s.

The MT8970 also allows a special control channel with limited capacity from TFIFO2 to be submultiplexed onto the L3 line channel.

The MT8970 has been designed as a general interface between a PCM voice or data network, a digital line and a microprocessor. It is an extremely flexible device. A more complete description is contained in the Users' Guide.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.73	15.24	0.580	0.600
C	2.92	3.94	0.115	0.155
D	0.41	0.51	0.016	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.14	1.40	0.045	0.055
J	0.23	0.30	0.009	0.012
K	2.54	3.81	0.100	0.150
L	15.24 BSC		0.600 BSC	
M	1.02	1.52	0.040	0.060
N	-	10°	-	10°

Figure 16 - Physical Dimensions of 40-Pin Dual-In-Line Ceramic Package

Notes

Notes

MITEL®

ST-BUS™ FAMILY **MH89700**

Digital Line Interface Module

Preliminary Information

9161-002-010-NA ISSUE 3 AUGUST 1986

Features

- MITEL ST-BUS™ Compatible
- Full Duplex Transmission over 2 Telephone Pairs
- Selectable 256 or 128 kbit/s Line Rate
- Interface for Both Ends of Line
- 3 Port Device:
  - 2 or 4 x 64 kbit/s Channel Line Port
  - 4 x 64 kbit/s Channel ST-BUS™ Port
  - 3 Channel Asynchronous Microprocessor Port
- Frame Synchronisation and Clock Extraction
- Modified AMI Coded Line Transmission
- 6800/68000 Bus Compatible
- Single 4.096 MHz Clock Input

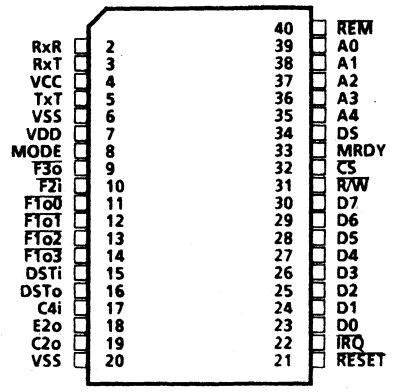
Applications

The MH89700 can be used as the digital line interface within telephone sets, PBXs, computers, computer peripherals etc.

Description

The MH89700 is a digital line interface which is capable of transmitting and receiving data on a line at speeds up to 256 kbit/s formatted in 4 x 64 kbit/s channels. Data may be switched between any channels on its 3 ports. All line driving, sensing and synchronisation functions are performed. Transmission over one mile of telephone cable can be readily achieved.

Pin Connections



Ordering Information

MH89700 40 Pin DIL Hybrid Module

0°C to + 70°C

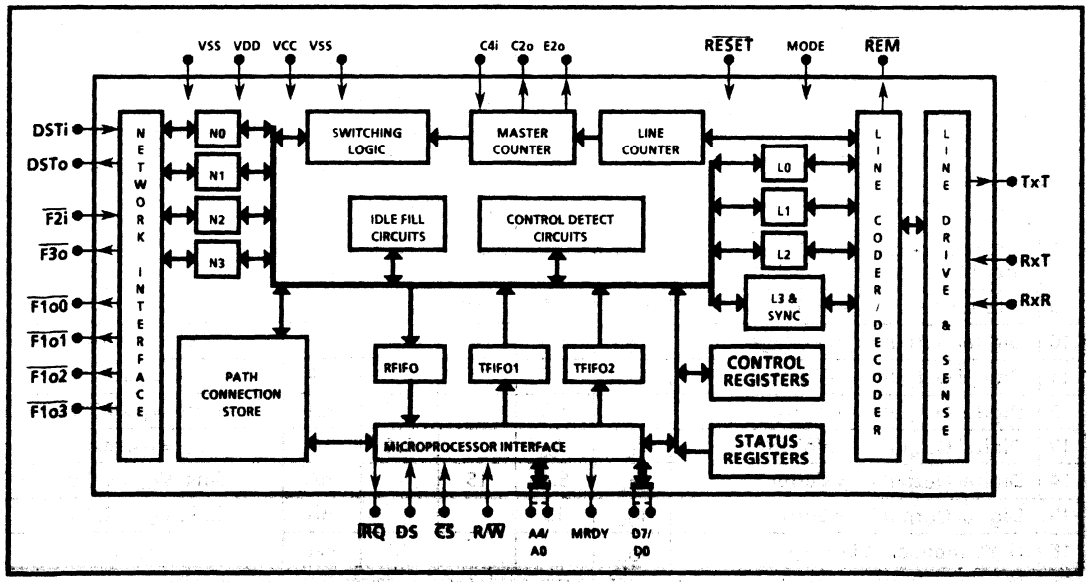


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	12 Volt Supply	V_{CC}	-0.3	14	V
2	5 Volt Supply	V_{DD}	-0.3	7	V
3	Voltage at RxR Line Pin	V_{RxR}	$V_{CC}/2$ - 0.5	$V_{CC}/2$ + 0.5	V
4	Voltage at RxT Line Pin	V_{RxT}	0	V_{CC}	V
5	Voltage at TxT Line Pin	V_{TxT}	-2	V_{DD}	V
6	Current at Line Pins	I_{LIN}		15	mA
7	Voltage at Digital Pins	V_D	-0.3	V_{DD} + 0.3	V
8	Current at Digital Pins	I_D		20	mA
9	Storage Temperature	T_{ST}	-65	150	°C
10	Power Dissipation	P		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	0		70	°C	
2	12 Volt Supply	V_{CC}	11.5	12	12.5	V	
3	5 Volt Supply	V_{DD}	4.75	5	5.25	V	
4	Voltage at RxR Line Pin	V_{RxR}	5.75	6	6.25	V	
5	Voltage at RxT Line Pin	V_{RxT}	4.0		8.0	V	
6	Voltage at TxT Line Pin	V_{TxT}	-1.5		1.5	V	
7	Voltage at Digital Pins	V_D	0		V_{DD}	V	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	12 Volt Supply Current	I_{CC}			30	mA	Outputs unloaded
2	5 Volt Supply Current	I_{DD}		2	5	mA	Outputs unloaded
3	Input Impedance (RxT to RxR)	Z_I	360	375	390	Ω	
4	Input High at $\overline{\text{RESET}}$ Pin	V_{IHR}	4.0		V_{DD}	V	At least 0.5 V Hysteresis
5	Input Low at $\overline{\text{RESET}}$ Pin	V_{ILR}	0		1	V	At least 0.5 V Hysteresis
6	Input High at Other Digital Pins	V_{IH}	2.7		V_{DD}	V	
7	Input Low at Other Digital Pins	V_{IL}	0		0.4	V	
8	Input Leakage at Digital Pins	I_{IL}		0.1	1	uA	
9	Internal Resistance (TxT)*	R_{TxT}	100	150	200	V	
10	Digital Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = 1.6 mA
11	Digital Output High Current	I_{OH}	1.6	15		mA	Source. V_{OH} = 2.4 V
12	Digital Output High Current	I_{OH}	1.3			mA	Source. V_{OH} = 3.0 V
13	Digital Output Low Voltage	V_{OL}	V_{SS}		0.4	V	I_{OL} = 6.4 mA
14	Digital Output Low Current	I_{OL}	6.4	15		mA	Sink. V_{OL} = 0.4 V
15	Digital Output Low Current	I_{OL}	15			mA	Sink. V_{OL} = 2.0 V
16	High Impedance Leakage	I_{OZ}			10	uA	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

*TxT behaves as a Voltage Source with an internal impedance in series with a capacitor.

AC Electrical Characteristics - Capacitances

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Output Capacitance (TxT)*	C_{TxT}		1		uF	
2	Input Pin Capacitance	C_I		10		pF	
3	Output Pin Capacitance	C_O		10		pF	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
*TxT behaves as a Voltage Source with an internal impedance in series with a capacitor.

AC Electrical Characteristics† - Clock Timing (Figures 2 & 3)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Clock Period*	t_{CLK}		244		ns	
2	Clock Width High or Low	t_{CHL}		102		ns	
3	Clock Transition Time	t_{CTT}		20		ns	
4	C2o Delay	t_{C2D}		40	80	ns	30 pF load
5	E2o Delay	t_{E2D}		50	100	ns	30 pF load

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* To ensure system synchronisation a tolerance of 0.05% on the C4i inputs of the devices at either end of the line is required.

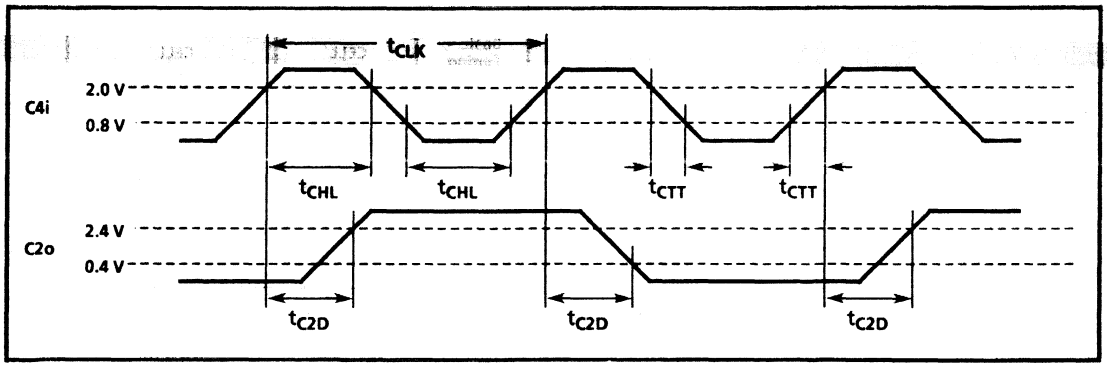


Figure 2 - C2o Timing

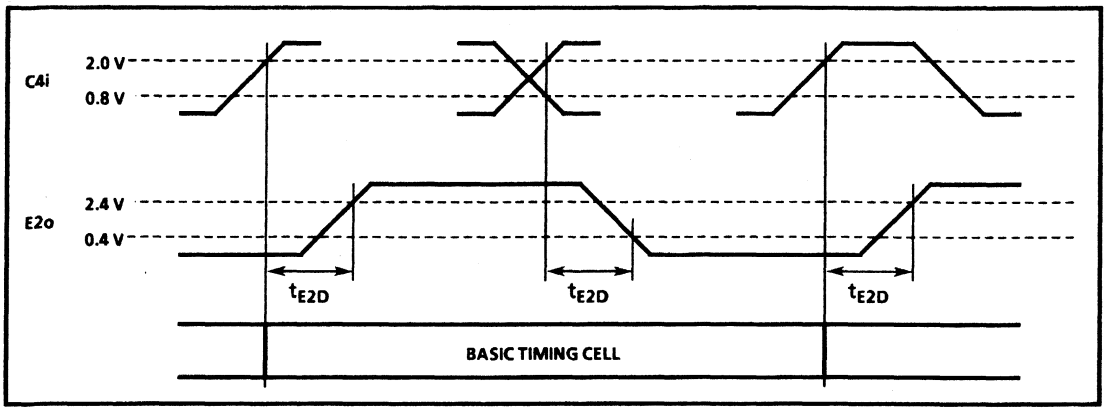


Figure 3 - E2o Timing and Definition of Basic Timing Cells

NB: The AC Characteristics for the ST-BUS™ and Line Ports are specified in terms of the Basic Timing Cells. This allows the same specification to be used in both the Master and the Slave Mode.

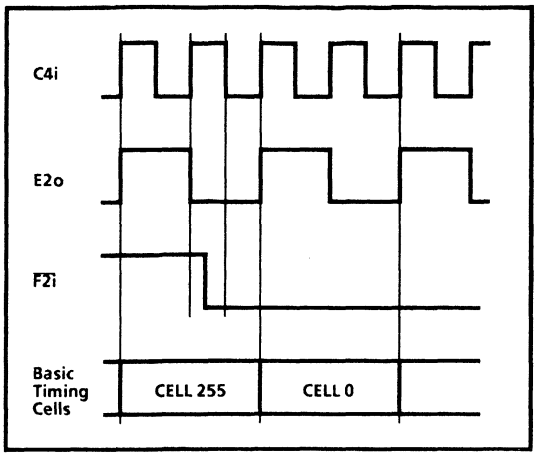


Figure 4 - Alignment of Basic Timing Cells in Master Mode

NB: In Master Mode E2o is not corrected and Basic Timing Cell 255 does not change.

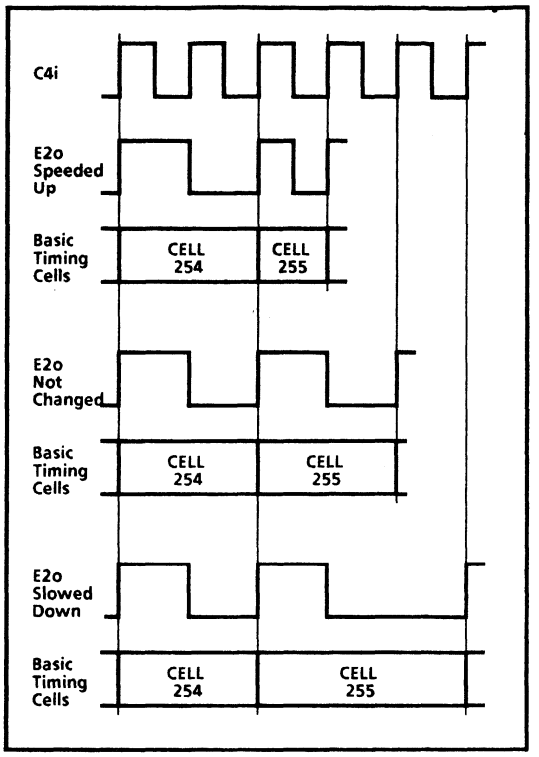


Figure 5 - Correction of E2o and Basic Timing Cell 255 in Slave Mode

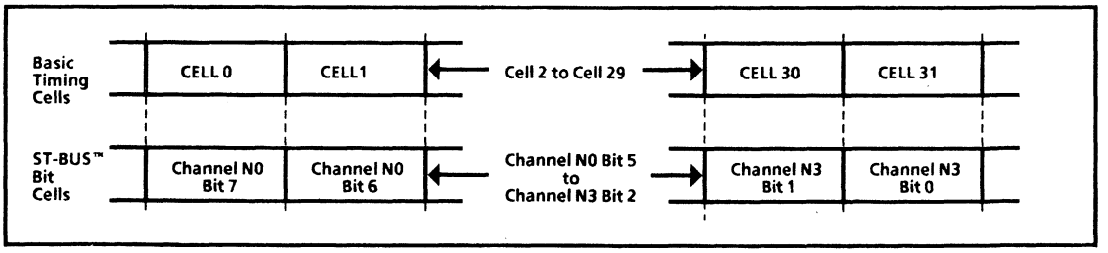


Figure 6 - Network Channel Alignment

NB: In Master Mode the frame synchronization is controlled by the $\overline{F2i}$ input (Figure 4)

In Slave Mode the frame synchronization is determined by the arrival of the SYNC bytes on the L3 channel (see Users' Guide) and is indicated on the $\overline{F3o}$ and $\overline{F1o0}$ to $\overline{F1o3}$ outputs (Figures 13 and 14). In Slave Mode Basic Timing Cell 255 is corrected by the internal phase-locked loop.

AC Electrical Characteristics† - ST-BUS™ Streams (Figures 4, 5, 6 & 7)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	DSTo Delay	t_{STD}	0	20	100	ns	50 pF load
2	DSTi Set Up Time	t_{STS}	50			ns	
3	DSTi Hold Time	t_{STH}	50			ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

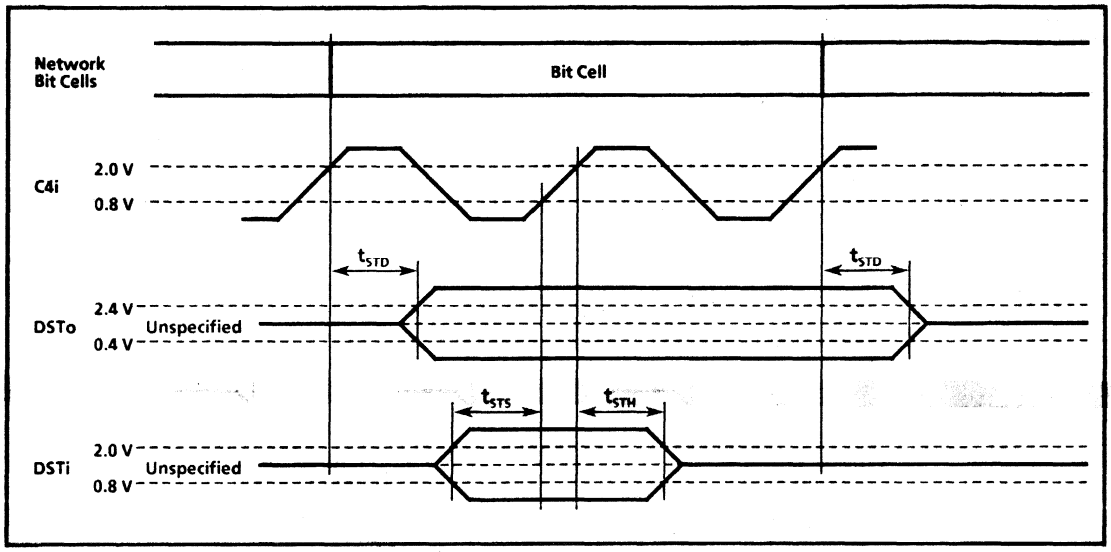


Figure 7 - ST-BUS™ Streams

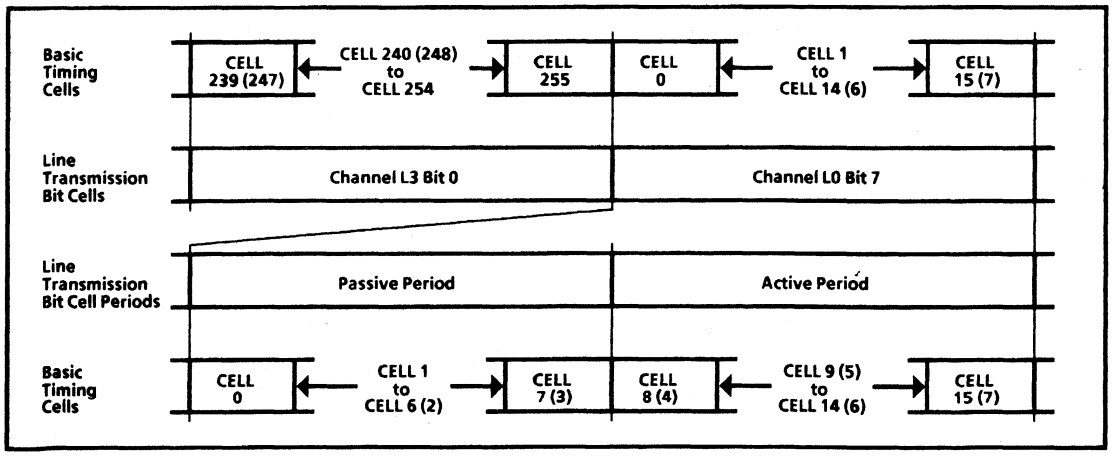


Figure 8 - Line Channel Alignment for Transmission at 128 (256) kbit/s

AC Electrical Characteristics† - Line Data (Figures 4, 5, 8, 9 & 10)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Transmit Peak Voltage	V_{TPK}		1.4		V	Open Circuit
2	Transmit Peak Voltage	V_{TPK}		1.0		V	400Ω load
3	Transmit Half Peak Delay	$t_{TP/2}$		290		ns	400Ω load
4	Receive Peak Voltage	V_{RPK}	0.3		1.0	V	
5	Receive Eye Opening	P_{REO}	80		100	%	Relative to V_{RPK}

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
NB: Data transmitted on the line should be at the same rate as data received from the line to within 0.1% averaged over 125 µs. This may be ensured by having a tolerance of 0.05% or better on the C4i inputs of the devices at either end of the line.

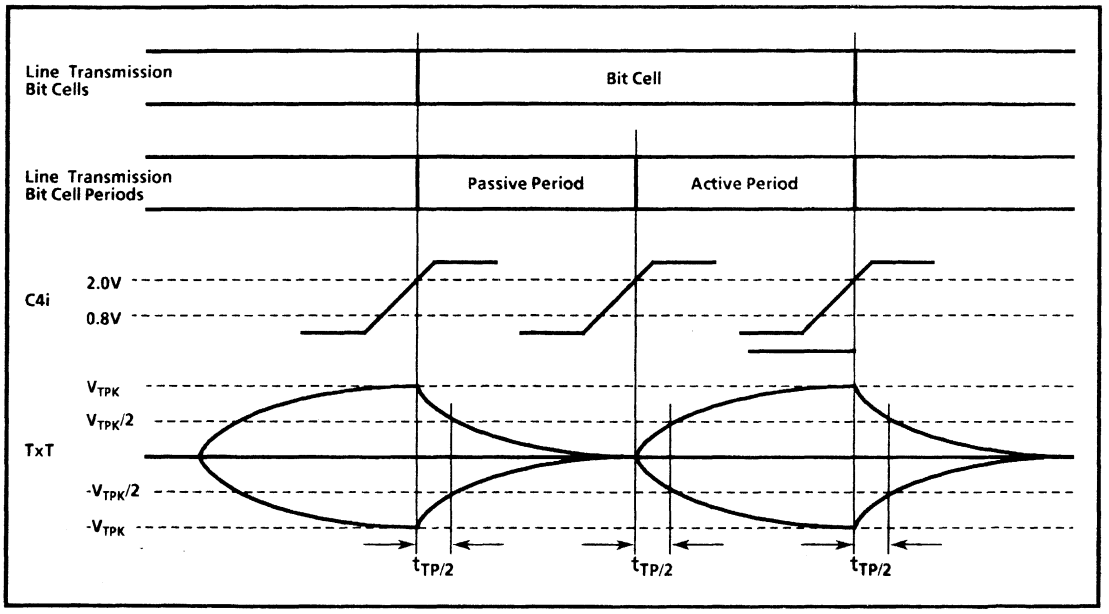


Figure 9 - Line Transmission Data

NB: TxT is a capacitatively coupled output with a negligible DC component.

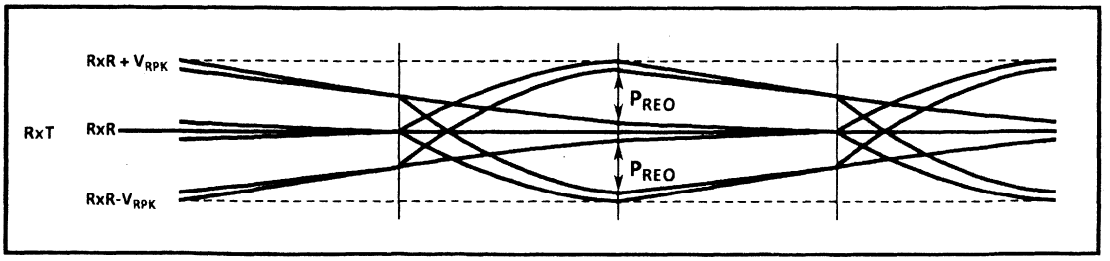


Figure 10 - Line Receive Data

NB: RxR is held at 6V by the module.
NB: The received pulse form and amplitude is assumed to be distorted by transmission down a telephone pair.

AC Electrical Characteristics† - ST-BUS™ Synchronisation (Figures 4, 5, 6, 11, 12, 13 & 14)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	F2i Set Up Time	t_{F2S}	10		200	ns	
2	F3o Delay	t_{F3D}	0	110	150	ns	50 pF load
3	F1o0 / F1o3 Delay	t_{F1D}	0	110	150	ns	50 pF load

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

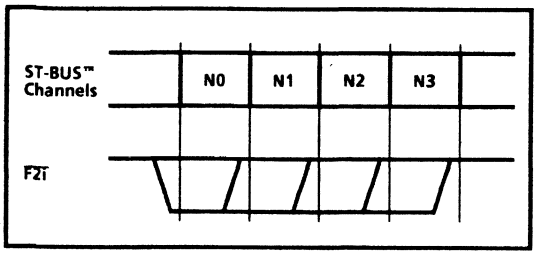


Figure 11 - $\overline{F2i}$ Alignment

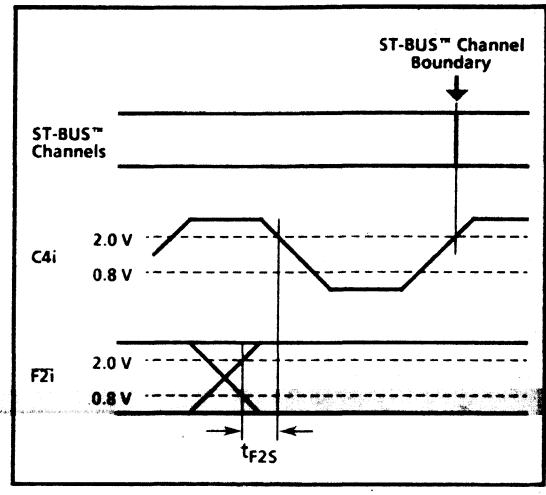


Figure 11 - $\overline{F2i}$ Timing

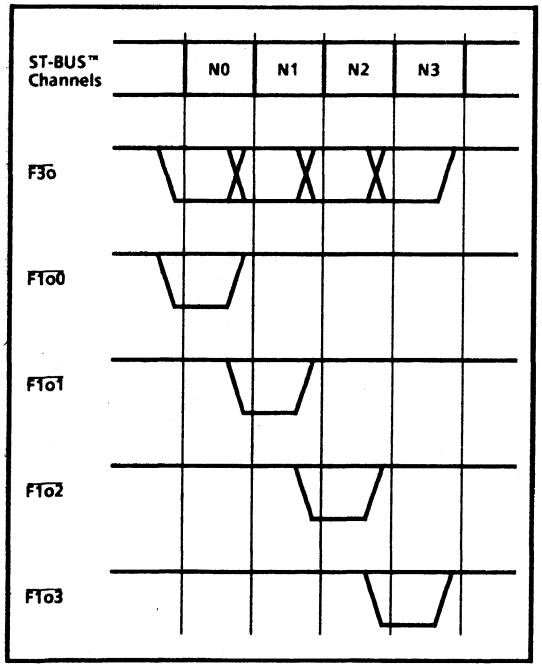


Figure 13 - $\overline{F3o}$ & $\overline{F1o0}$ to $\overline{F1o3}$ Alignment

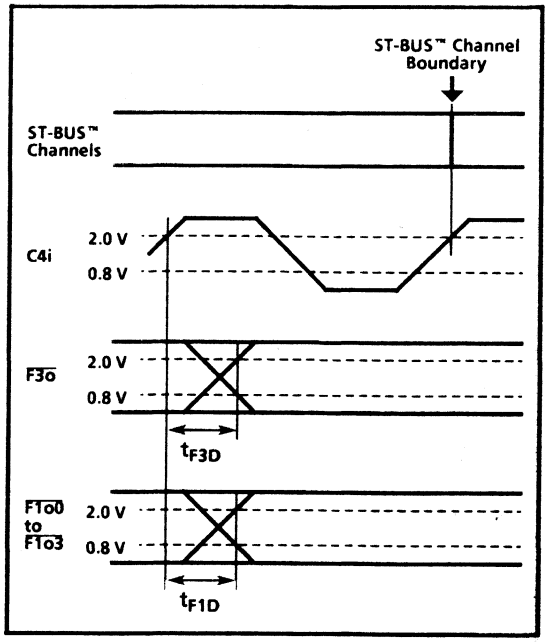


Figure 14 - $\overline{F3o}$ & $\overline{F1o0}$ to $\overline{F1o3}$ Timing

AC Electrical Characteristics† - Bus Interface Timing (Figure 15)

	Characteristics	Sym	Min	Typ#	Max	Units	Test Conditions
1	Chip Select Set Up Time - Read	t_{CSR}	-25			ns	
2	Chip Select Set Up Time - Write	t_{CSW}	40			ns	
3	Read/Write Set Up Time	t_{RWS}	80			ns	
4	Address Set Up Time	t_{ADS}	30			ns	
5	Data Strobe Width	t_{DSW}	150			ns	
6	Memory Ready Delay	t_{MRD}	0	25	90	ns	50 pF load
7	Read Data Delay*	t_{RDD}		70	125	ns	50 pF load
8	Write Data Set Up Time	t_{WDS}	145			ns	
9	Data Hold Time - Read	t_{DHR}	20	25		ns	50 pF load
10	Data Hold Time - Write	t_{DHW}	18			ns	
11	Chip Select Hold Time	t_{CSH}	20			ns	
12	Read/Write Hold Time	t_{RWH}	0			ns	
13	Address Hold Time	t_{ADH}	0			ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
# Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Taken from the later of DS high and $\overline{CS}$ low

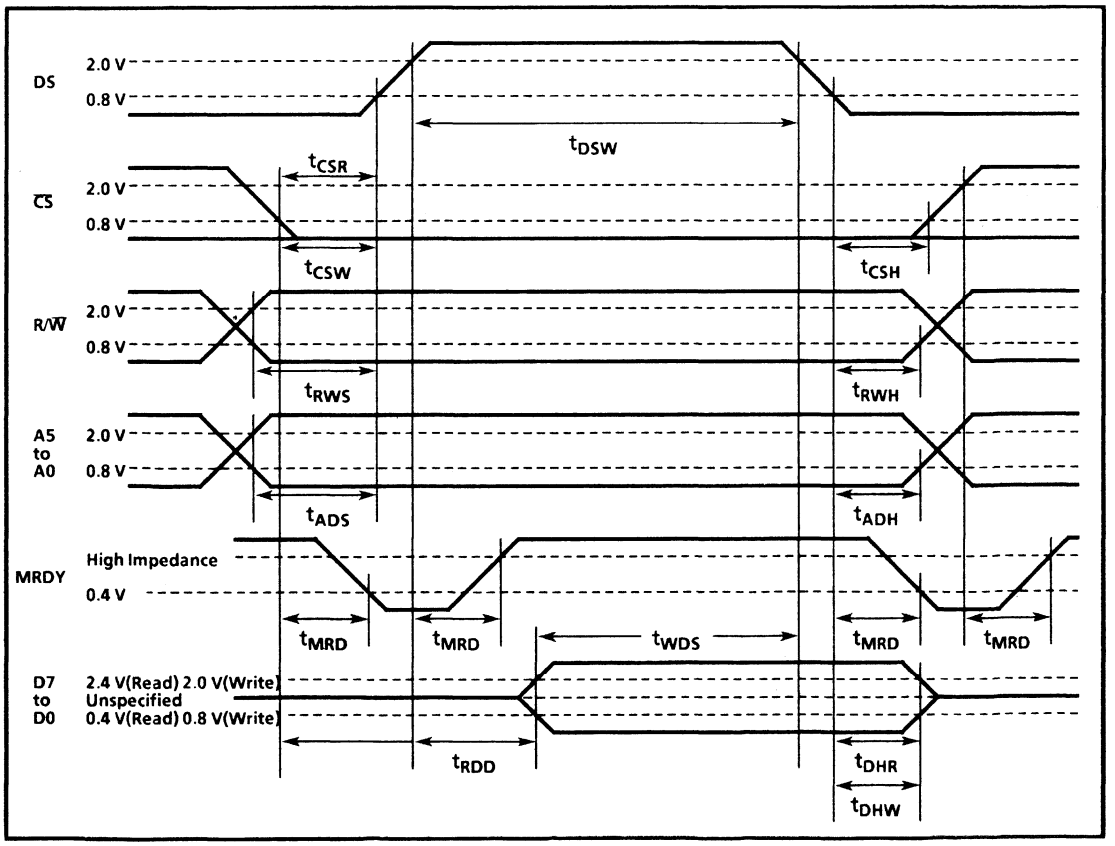


Figure 15 - Processor Interface Timing

Pin Description

Pin	Name	Description
2	RxR	**Receive Ring (Analog Input).** This pin is connected to one of the wires at the receive end of the line through a transformer or some other balancing network. It is held at 6 Volts by the module.
3	RxT	**Receive Tip (Analog Input).** This pin is connected to the second wire at the receive end of the line through the transformer or other balancing network. Data is received at either 128 kbit/s or 256 kbit/s. If this pin is high the chip is in Slave Mode
4	VCC	**+ 12 Volts (Power Input).If this pin is**
5	TxT	**Transmit Tip (Analog Output).** This pin is used to drive the transmit end of the line through a transformer or some other balancing network. If a transformer is used then the other side should be connected to ground. Data is transmitted at either 128 kbit/s or 256 kbit/s.
6	VSS	**Ground (Power Input).** This pin is connected to Pin 20 internally.
7	VDD	**+ 5 Volts (Power Input).**
8	MODE	**Mode (Input).** A high on this pin puts the chip in Slave Mode and a low puts it in Master Mode. In Master Mode the C4i clock and the $\overline{F2i}$ pulse control the timing and synchronisation. In Slave Mode the device is synchronized to the incoming line data rate and the E2o output may be corrected. In either mode the E2o output clock is sychonized to the ST-BUS™ and to the transmitted line bit streams.
9	$\overline{F3o}$	**Framing Signal Type 3 (Complementary Output).** A low on this output signals that some ST-BUS™ channel is active.
10	$\overline{F2i}$	**Framing Signal Type 2 (Input).** This pin should be pulled low once every frame to select channels on the ST-BUS™ port when the chip is in Master Mode (MODE pin low) In Slave Mode frame synchronization is obtained from the line and is indicated on the $\overline{F3o}$ and $\overline{F1o0}$ to $\overline{F1o3}$ pins. Any logical signal may be applied to this pin when the chip is in Slave Mode but the pin should not be allowed to float.
11 / 14	$\overline{F1o0}$ / $\overline{F1o3}$	**Framing Signal Type 1 for N0 / 3 (Complementary Outputs).** A low on one of these outputs indicates that the corresponding N0 to N3 ST-BUS™ channel is active.
15	DSTi	**Data ST-BUS™ (Input).** This is the input pin for channels on the ST-BUS™ port.
16	DSTo	**Data ST-BUS™ (Three-State Output).** This is the output pin for channels on the ST-BUS™ port.
17	C4i	**Clock - 4.096 MHz (Input).** This is the input for the 4.096 MHz. clock.
18	E2o	**Extracted Clock - 2.048 MHz (Complementary Output).** This pin provides a 2.048MHz. clock which is corrected by the line data rate when the MODE pin is high (Slave Mode). The clock is corrected once every 256 cycles. If the MODE pin is low (Master Mode) then this output is equivalent to C2o.
19	C2o	**Clock - 2.048 MHz (Complementary Output).** This pin provides a 2.048MHz. clock which is obtained by dividing the 4.098MHz. input clock on C4i by two.
20	VSS	**Ground (Power Input).** This pin is connected to Pin 6 internally.

Pin Description (continued)

Pin	Name	Description
21	$\overline{\text{RESET}}$	**Reset (Input).** A low on this input causes the device to reset the three ports and sets the RESET bit in Control Register 1. The device will not come out of reset until this bit is cleared through the microprocessor interface. During reset, frame synchronisation is lost, RFIFO, TFIFO1 and TFIFO2 are cleared, TxT goes to its zero level, DSTo, $\overline{\text{REM}}$ and $\overline{\text{IRQ}}$ go to their high impedance state, and if the MODE pin is high (Slave Mode) E2o is pulled low.
22	$\overline{\text{IRQ}}$	**Interrupt Reqest (Open Drain Pulldown Output).** This output is pulled low to signal an interrupt request on the microprocessor interface.
23 / 30	D0 / D7	**Data 0 to 7 (Three-state I/O Pins).** These are the bidirectional data pins on the microprocessor interface.
31	R/$\overline{\text{W}}$	**Read / Write (Input).** This is the input for he read/write signal on the microprocessor interface - high for read, low for write.
32	$\overline{\text{CS}}$	**Chip Select (Input).** This is the input for the active low chip select signal on the microprocessor interface.
33	MRDY	**Memory Ready (Open Drain Pulldown Output).** This is the memory ready output on the microprocessor interface. It is held low until the chip has completed a read or write.
34	DS	**Data Strobe (Input).** This is the input for the data strobe on the microprocessor interface.
35 / 39	A4 / A0	**Address 4 to 0 (Inputs).** These are inputs for the address lines on the microprocessor interface.
40	$\overline{\text{REM}}$	**Remote Reset (Open Drain Pulldown Output).** This pin is high-impedance during normal operation. It is pulled low if an all 1s signal is received on the line for more than 2 superframes (4mS). The pin goes to its high impedance state during a device reset. This feature can be used for simple signalling or to generate a reset.

Functional Description

The device switches data between channels on 3 ports which operate at different speeds. The data is in the form of 8 bit bytes which may be PCM coded speech. At the line and ST-BUS™ ports the bytes are part of serial data streams, while at the microprocessor port the bytes arrive and depart on the parallel data bus. The microprocessor port also allows access to the Path Connection Store which defines the paths between the channels and to the Control and Status Registers through which the device is monitored and controlled.

Data arrives at the ST-BUS™ port as a 2048 kbit/s serial ST-BUS™ stream on the DSTi pin. This stream contains 32 channels, each having the bandwidth of digitized speech (64 kbit/s). The device may use up to four consecutive channels which are referred to as the N0 to N3 channels.

On the microprocessor port data for transmission should be written to hex addresses 19 (TFIFO1) or 1A (TFIFO2).

Data arriving at the line port is AMI (Alternate Mark Inversion) coded with zero bytes replaced with a special zero code. The AMI coding is supplied to the module on the RxT and RxR pins. This data should arrive at 128 kbit/s or 256 kbit/s (2 or 4 channels). The line channels are L0, L1, L2 and L3 at 256 kbit/s or L0 and L3 at 128 kbit/s Two bytes out of every 16 on the L3 channel are used for synchronization.

The data is routed to destinations according to the contents of the Path Connection Store. There are two types of Service Circuit, Idle-fill or Control-detect, which may be used on connections. Idle-fill Service Circuits allow asynchronous data written to the TFIFOs to be matched to the 64 kbit/s ST-BUS™ and line channels by injecting additional bytes.

Control detect circuits allow the additional bytes to be stripped.

Data routed to the ST-BUS™ channels is output as a ST-BUS™ stream on the DSTo pin.

Data routed to the microprocessor port is placed in the RFIFO buffer (hex address 18).

Data routed to the line port is AMI coded with zero bytes replaced by zero code and tranmitted on the TxT pin at either 128 kbit/s or 256 kbit/s. Synchronization on the line is acheived by transmitting 2 "SYNC" bytes once every 16 bytes on the L3 channel.

The microprocessor interface also gives access to the 3 Control Registers and the 3 Status Registers allowing the microprocessor to control and monitor the device.

The device has the capability to concatenate connections between the microprocessor channels and the ST-BUS™ and line channels, creating an effective data channel of up to 256 kbit/s.

The device also allows a special control channel, with limited capacity, from TFIFO2 to be submultiplexed onto the L3 line channel.

The device has been designed as a general interface between a PCM voice or data network, a digital line and a microprocessor. It is extremely flexible. A more complete description is contained in the Users' Guide.

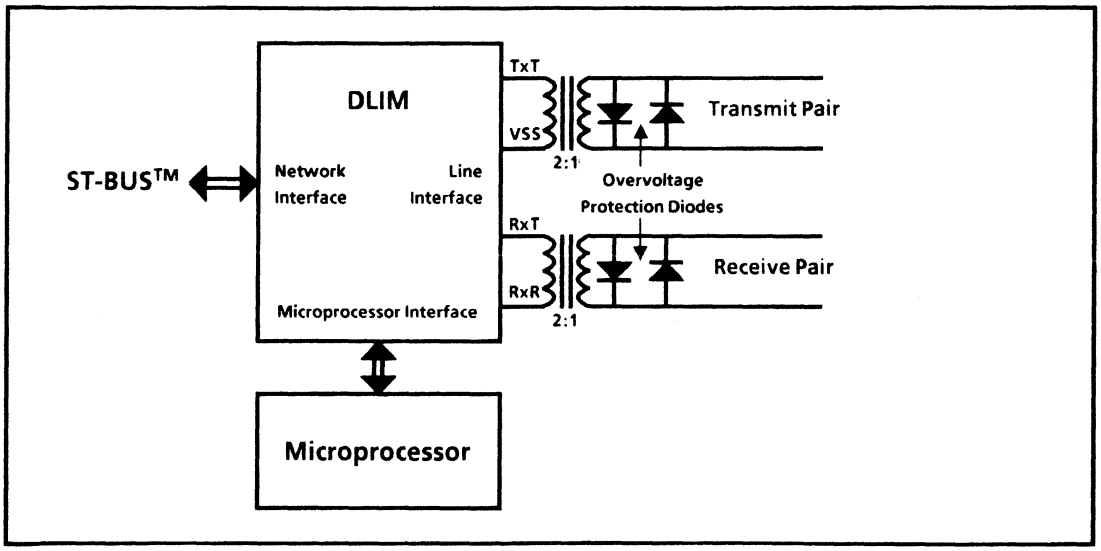


Figure 16 - Typical Connection to Telephone Pairs

Notes

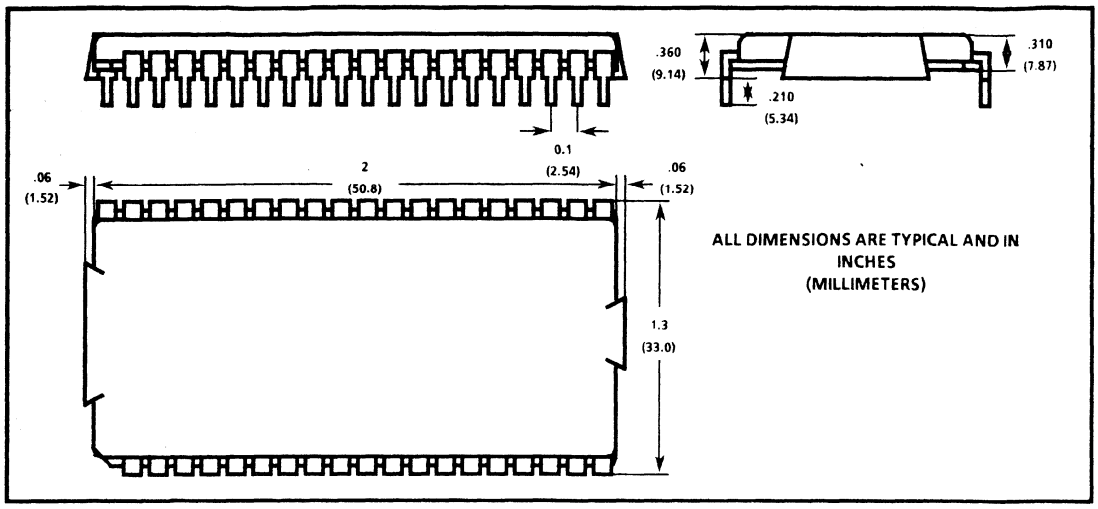


Figure 17 - Physical Dimensions of 40 Pin Dual in Line Hybrid Package

ST-BUS™ FAMILY MT8972
Digital Network Interface Circuit
Preliminary Information

9161 - 002 - 030 - NA ISSUE 4 JULY 1986

Features

- ISDN Recommendations compatible (2B + D)
- MITEL ST-BUS™ compatible
- Full duplex transmission over a single twisted pair
- Selectable 80 or 160 kbit/s Line Rate
- Adaptive Echo Cancellation
- Frame synchronization and clock extraction
- Transparent modem capability
- Up to 5 km at 80 kbit/s and 4 km at 160 kbit/s
- Low power consumption. (Typically 50 mW)
- Single 5V power supply

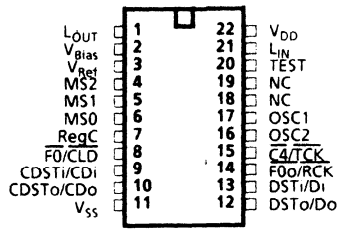
Applications

- Digital Subscriber Lines
- ISDN U-Interface
- Digital PABX line cards and telephone sets.
- 80 or 160 kbit/s single chip modem.

Description

The MT8972 is a multifunction device providing a high speed full duplex digital transmission link over a single pair of twisted wires by the use of echo-cancelling techniques as recommended by T1D1.3.

Pin Connections



Ordering Information

MT8972AC 22 Pin Cerdip
0°C to + 70°C

The DNIC may be used for interfacing to digital telephone networks (DN mode) or as a high speed modem (MOD mode). It corresponds to the ISDN recommendations for the U-Interface. Data on the line is in the CCITT recommended 2B + D format. It can also operate as a high speed, limited distance modem with data rates up to 160 kbit/s.

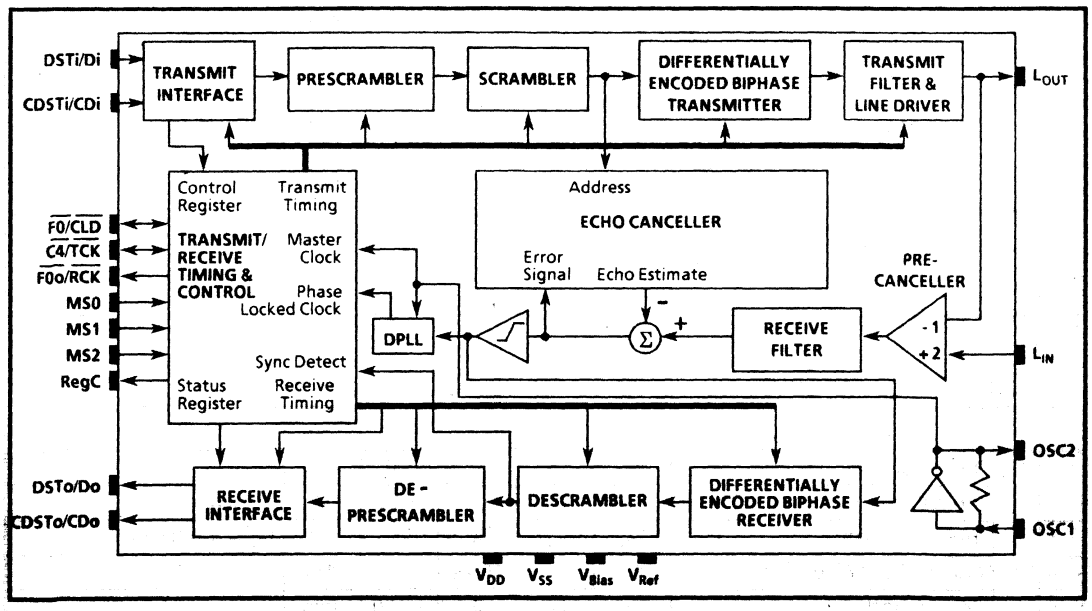


Figure 1. Functional Block Diagram

Absolute Maximum Ratings** - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7	V
2	Voltage On Any Pin (other than supply)	V_{Max}	-0.3	V_{DD} + 0.3	V
3	Current On Any Pin (other than supply)	I_{Max}		40	mA
4	Storage Temperature	T_{ST}	-65	+ 150	°C
5	Package Power Dissipation‡	P_{Diss}		750	mW

**Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
‡Derate 16mW/°C above 75°C

Recommended Operating Conditions† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Operating Supply Voltage	V_{DD}	4.75	5.00	5.25	V	
2	Operating Temperature	T_{OP}	0		70	°C	
3	Input High Voltage (except OSC1)	V_{IH}	2.4		V_{DD}	V	for 400 mV noise margin
4	Input Low Voltage (except OSC1)	V_{IL}	0		0.4	V	for 400 mV noise margin

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
†Parameters over recommended temperature & power supply voltage ranges.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	OUTPUTS	Operating Supply Current	I_{DD}		10	15	mA	
2		Output High Voltage (ex OSC2)	V_{OH}	2.4			V	I_{OH} = 10mA
3		Output High Current (except OSC2)	I_{OH}	10	15		mA	Source current. V_{OH} = 2.4V
4				8	12		mA	Source current. V_{OH} = 3.0V
5		Output High Current - OSC2	I_{OH}	10			µA	Source current V_{OH} = 3.5V
6		Output Low Voltage (ex OSC2)	V_{OL}			0.4	V	I_{OL} = 5mA
7		Output Low Current (except OSC2)	I_{OL}	5	7.5		mA	Sink current. V_{OL} = 0.4V
8				20	30		mA	Sink current. V_{OL} = 2.0V
9		Output Low Current - OSC2	I_{OL}	10			µA	Sink current. V_{OL} = 1.5V
10		High Imped. Output Leakage	I_{OZ}			10	µA	V_{IN} = V_{SS} to V_{DD}
11		Output Voltage (V_{Ref})	V_O		V_{Bias}-1.8		V	
12		(V_{Bias})			$V_{DD}/2$		V	
13	INPUTS	Input High Voltage (ex OSC1)	V_{IH}	2.0			V	
14		Input Low Voltage (ex OSC1)	V_{IL}			0.8	V	
15		Input Leakage Current	I_{IL}			10	µA	V_{IN} = V_{SS} to V_{DD}

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
†Parameters over recommended temperature & power supply voltage ranges.

AC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	INPUTS	Input Voltage (L_{IN})	V_{IN}			5.0	V_{pp}	
2		Input Current (L_{IN})	I_{IN}	-10		+ 10	µA	f_{Baud} = 160 kHz
3		Input Impedance (L_{IN})	Z_{IN}		50		kΩ	f_{Baud} = 160 kHz
4		Crystal/Clock Frequency	f_C		10.24		MHz	
5		Crystal/Clock Tolerance	T_C	-100	0	+ 100	ppm	

AC Electrical Characteristics Cont'd† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
6		Crystal/Clock Duty Cycle	DC_C	40	50	60	%	
7		Crystal/Clock Loading	C_L		33	50	pF	From OSC1 & OSC2 to V_{SS}.
8	O	Output Capacitance (L_{OUT})	C_o		8		pF	
9	U	Load Resistance (L_{OUT})	$R_{L_{out}}$		500		Ω	
	T	(V_{Bias}, V_{Ref})			100		kΩ	
10	P	Load Capacitance (L_{OUT})	$C_{L_{out}}$			20	pF	Capacitance to V_{Bias}.
	U	(V_{Bias}, V_{Ref})		0.1			µF	
11	T S	Output Voltage (L_{OUT})	V_o	4.2	4.5	4.8	V_{pp}	$R_{L_{out}}$ = 500Ω, $C_{L_{out}}$ = 20pF

AC Electrical Characteristics† - Clock Timing - DN Mode (Figures 3 & 4)

	Characteristics	Sym	Min	Typ*	Max	Units	TEST CONDITIONS
1	$\overline{C4}$ Clock Period	t_{C4P}		244		ns	
2	$\overline{C4}$ Clock Width High or Low	t_{C4W}	90	122	150	ns	In Master Mode - Note 1
3	Frame Pulse Set Up Time	t_{F0S}	50			ns	
4	Frame Pulse Hold Time	t_{F0H}	50			ns	
5	Frame Pulse Width	t_{F0W}	172	244		ns	
6	10.24 MHz Clock Jitter (wrt $\overline{C4}$)	J_C	-15		+ 15	ns	Note 2

†Timing is over recommended temperature & power supply voltage ranges.
*Typical figures are at 25°C, for design aid only; not guaranteed and not subject to production testing.

Notes: 1) When operating as a SLAVE the $\overline{C4}$ clock has a 40% duty cycle.

2) If operating in MAS/ DN mode, the $\overline{C4}$ and Oscillator clocks must be externally frequency locked (i.e. $f_C = 2.5 \times f_{C4}$). The relative phase between these two clocks (ϕ in Fig. 4) is not critical and may vary from 0 ns. to t_{C4P}. However, the relative jitter must be less than J_C.(See Fig. 4).

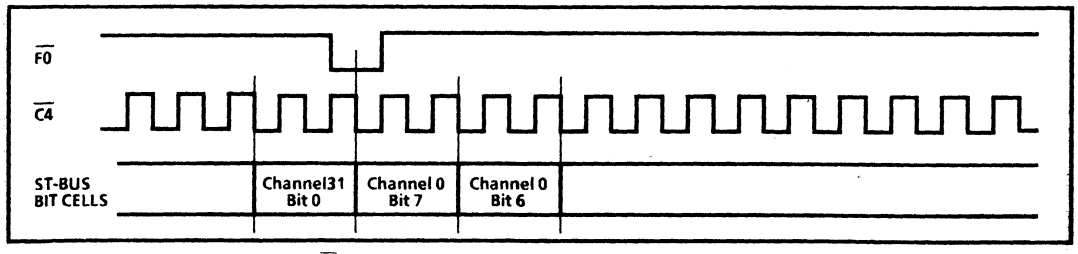


Figure 2. $\overline{C4}$ Clock & Frame Pulse Alignment for ST-BUS Streams

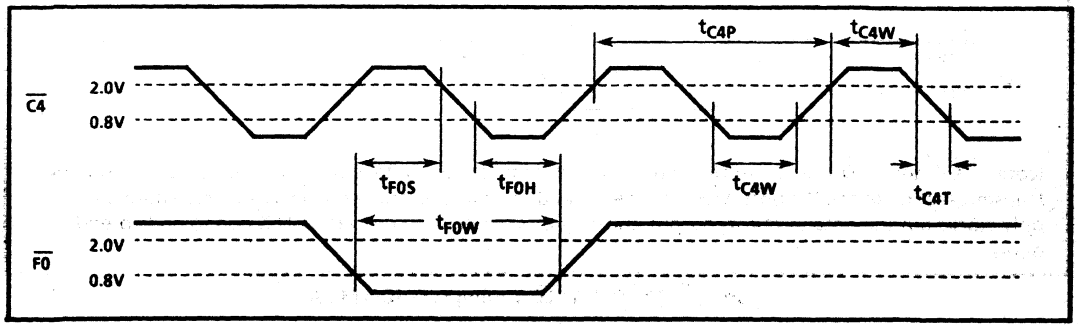


Figure 3. C4 $\overline{C}$lock & Frame Pulse Timing for ST-BUS Streams in DN Mode

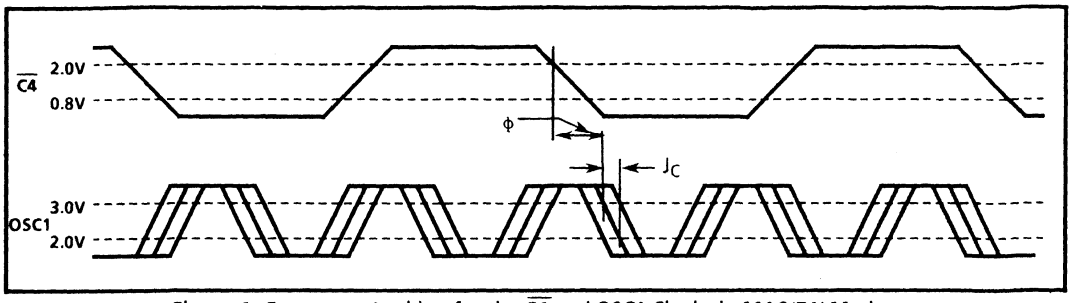
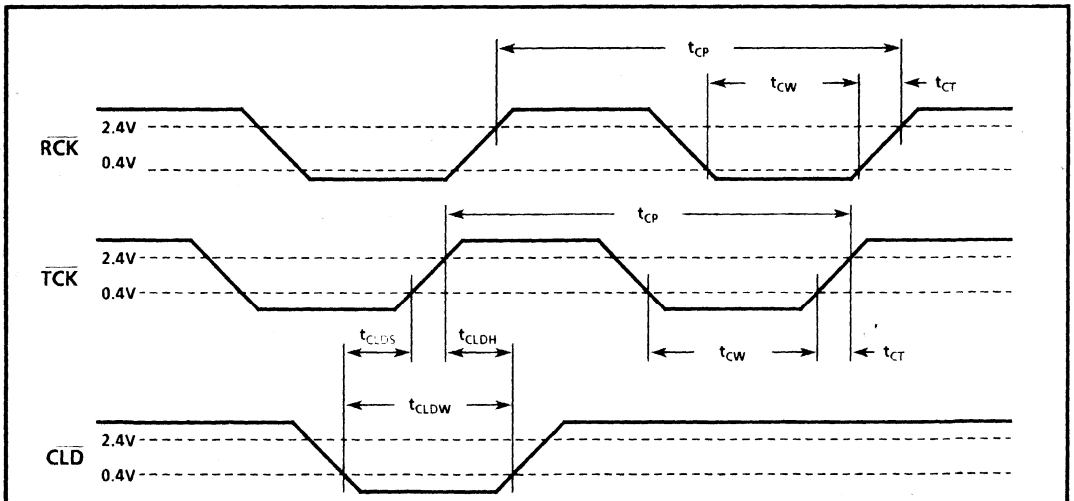


Figure 4. Frequency Locking for the C4 and OSC1 Clocks in MAS/DN Mode

AC Electrical Characteristics† - Clock Timing - MOD Mode (Figure 5)

	Characteristics	Sym	80 kbit/s			160 kbit/s			Units	Test Conditions
			Min	Typ*	Max	Min	Typ*	Max		
1	TCK/RCK Clock Period	t_{CP}		12.5			6.25		µs	
2	TCK/RCK Clock Width	t_{CW}		6.25			3.125		µs	
3	TCK/RCK Clock Transition Time	t_{CT}		20			20		ns	C_L = 40pF
4	CLD to TCK Setup Time	t_{CLDS}		3.125			1.56		µs	
5	CLD to TCK Hold Time	t_{CLDH}		3.125			1.56		µs	
6	CLD Width Low	t_{CLDW}		6.05			2.925		µs	
7	CLD Period	t_{CLDP}		8xt_{CP}			8xt_{CP}		µs	

†Timing is over recommended temperature & power supply voltage ranges.
* Typical figures are at 25°C, for design aid only: not guaranteed and not subject to production testing.



Note: TCK and CLD are generated on chip and provide the data clocks for the CD port and the transmit section of the DV port. RCK, also generated on chip, is extracted from the receive data and only clocks out the data at the D_O output and may be skewed with respect to TCK due to end-to-end delay.

Figure 5. RCK, TCK & CLD Timing For MOD Mode

AC Electrical Characteristics† - Data Timing - DN Mode (Figure 6)

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	DSTi/CDSTi Data Setup Time	t_{RS}	30		250	ns	
2	DSTi/CDSTi Data Hold Time	t_{RH}	50		122	ns	
3	DSTo/CDSTo Data Delay	t_{TD}	20		120	ns	C_L = 40pF

†Timing is over recommended temperature & power supply voltage ranges.
* Typical figures are at 25°C, for design aid only: not guaranteed and not subject to production testing.

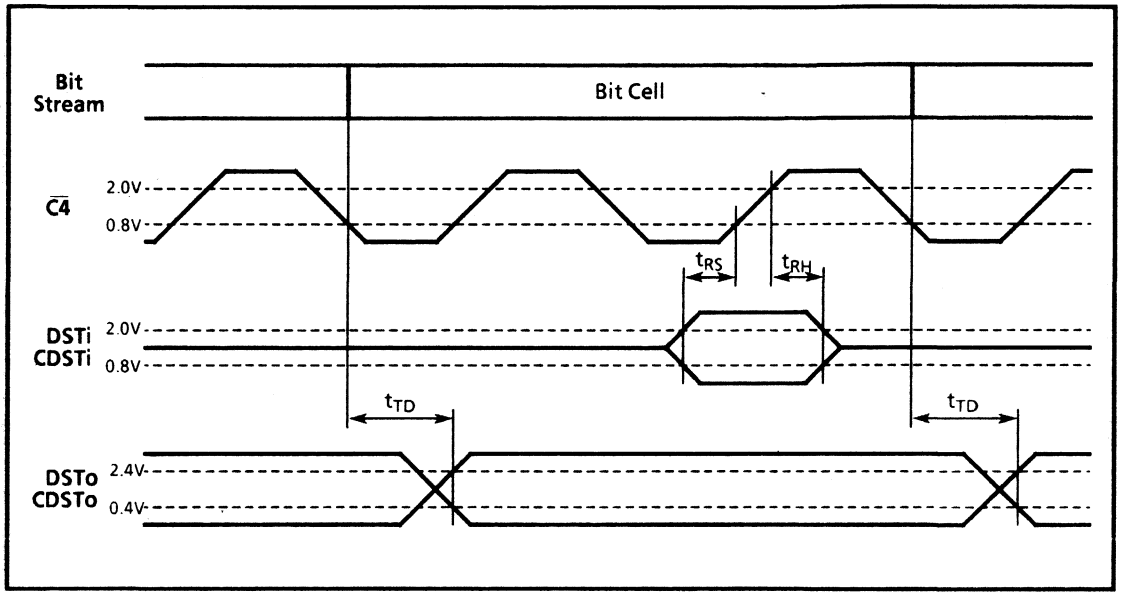


Figure 6. Data Timing For DN Mode

AC Electrical Characteristics† - Data Timing - MOD Mode (Figure 7)

	Characteristics	Sym	80 kbit/s			160 kbit/s			Units	Test Conditions
			Min	Typ*	Max	Min	Typ*	Max		
1	Di/CDi Data Setup Time	t_{RS}		-3.125			-1.56		µs	
2	Di/CDi Data Hold Time	t_{RH}		-3.125			-1.56		µs	
3	Do Data Delay Time	t_{RD}			100			100	ns	C_L = 40pF
4	CDo Data Delay Time	t_{TD}			100			100	ns	C_L = 40pF

†Timing is over recommended temperature & power supply voltage ranges.
* Typical figures are at 25°C, for design aid only: not guaranteed and not subject to production testing.

Performance Characteristics

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Allowable Attenuation	A_{fb}		40		dB	f_b component, Note 1
2	Line Length at 80 kbit/s - 24 AWG - 26 AWG	L_{80}		5.0 3.4		km	attenuation - 6.9 dB/km attenuation - 10.0 dB/km
3	Line Length at 160 kbit/s - 24 AWG - 26 AWG	L_{160}		4.0 3.0		km	attenuation - 8.0 dB/km attenuation - 11.5 dB/km

Note 1: Attenuation from L_{OUT} at master to L_{IN} at slave.
* Typical figures are at 25°C, for design aid only: not guaranteed and not subject to production testing.

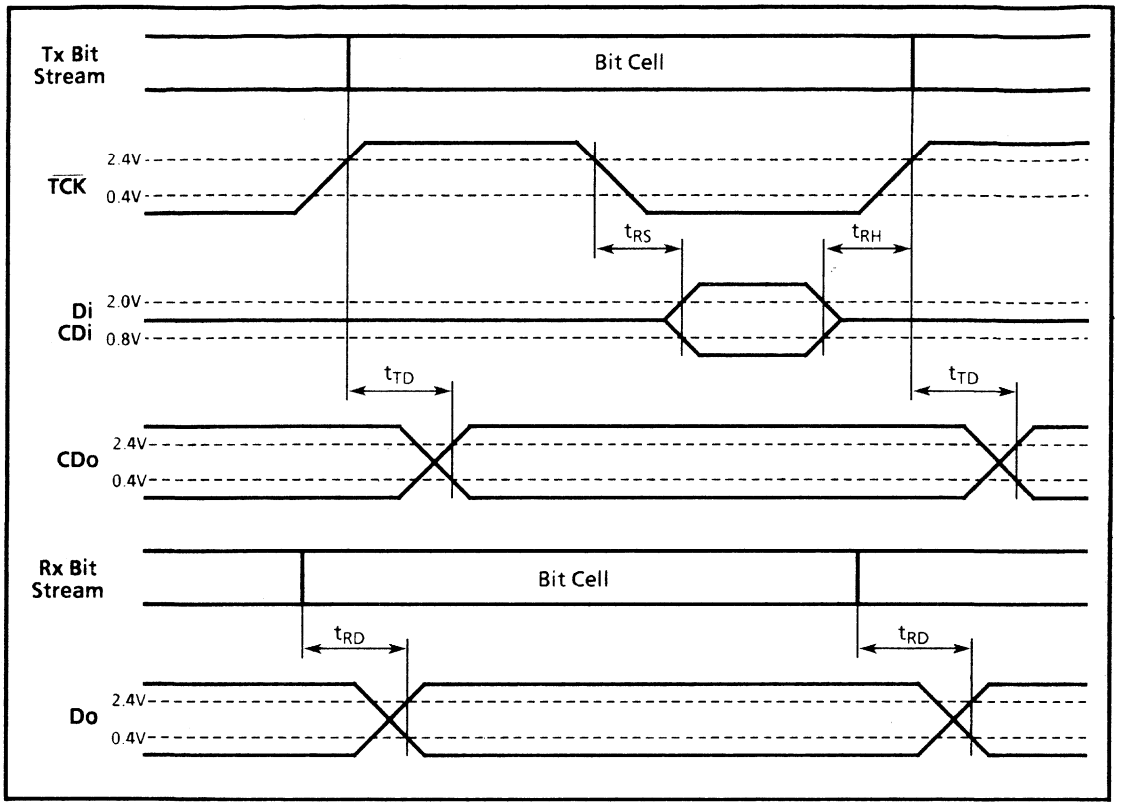


Figure 7. Data Timing For MOD Mode

Pin Description

Pin	Name	Description
1	L_{OUT}	**Line Out.** Transmit Signal output (Analog). Referenced to V_{Bias}.
2	V_{Bias}	**Internal Bias Voltage** output. Connect via 0.33 µF decoupling capacitor to V_{SS}
3	V_{Ref}	**Internal Reference Voltage** output. Connect via 0.33 µF decoupling capacitor to V_{SS}.
4-6	MS2-MS0	**Mode Select** inputs (Digital). The logic levels present on these pins select the various operating modes for a particular application. See Table 1 for the operating modes.
7	RegC	**Regulator Control** output (Digital). A 512 kHz clock used for switch mode power supplies. Unused in MAS/MOD mode and should be left open circuit.
8	F0/CLD	**Frame Pulse/C Channel Load** (Digital). In DN mode a 244 ns wide negative pulse input for the MASTER indicating the start of the active channel times of the device. Output for the SLAVE indicating the start of the active channel times of the device. Output in MOD mode providing a pulse indicating the start of the C channel.
9	CDSTi/ CDi	**Control/Data ST-BUS In/Control/Data In** (Digital). A 2.048 Mbit/s serial control & signalling input in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.

Pin Description Cont'd

Pin	Name	Description
10	CDSTo/ CDo	**Control/Data ST-BUS Out/Control/Data Out** (Digital). A 2.048 Mbit/s serial control& signalling output in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.
11	V_{SS}	**Negative Power Supply** input.
12	DSTo/Do	**Data ST-BUS Out/Data Out** (Digital). A 2.048 Mbit/s serial PCM/data output in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.
13	DSTi/Di	**Data ST-BUS In/Data In** (Digital). A 2.048 Mbit/s serial PCM/data input in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.
14	$\overline{F0o}$/RCK	**Frame Pulse Out/Receive Bit Rate Clock** output (Digital). In DN mode a 244 ns wide negative pulse indicating the end of the active channel times of the device to allow daisy chaining. In MOD mode provides the receive bit rate clock to the system.
15	C4/TCK	**Data Clock/Transmit Baud Rate Clock** (Digital). A 4.096 MHz TTL compatible clock input for the MASTER and output for the SLAVE in DN mode. For MOD mode this pin provides the transmit bit rate clock to the system.
16	OSC2	**Oscillator Output**. CMOS Output.
17	OSC1	**Oscillator Input**. CMOS Input.
18	NC	**No Connection**. Reserved for future functionality. Leave open circuit
19	NC	**No Connection**. Reserved for future functionality. Leave open circuit
20	TEST	**Test Pin**. Connect to V_{SS}.
21	L_{IN}	**Receive Signal** input (Analog). Referenced to V_{Bias}.
22	V_{DD}	**Positive Power Supply** input.

Functional Description

The MT8972 (DNIC) is a device which has been designed primarily as an interface for the Integrated Services Digital Network (ISDN). However, it may be used in practically any application that requires high speed data transmission over two wires, including smart telephone sets, work stations, data terminals and computers.

In the ISDN, the DNIC is ideal for providing the interface at the U reference point. The device supports the 2B + D channel format (two 64 kbit/s B-channels and one 16 kbit/s D-channel) over 2 wires as recommended by the CCITT. The line data is converted to and from the ST-BUS format on the system side of the network to allow for easy interfacing with other components such as the S-Interface device in an NT1 arrangement, or to digital PABX components.

Smart telephone sets with data and voice capability can be easily implemented using the MT8972 as a line interface. The device's high bandwidth and long loop length capability allows its use in a wide variety of sets. This can be extended to provide full data and voice capability to the private subscriber by the installation of equipment in both the home and central office or remote concentration equipment. Within the subscriber equipment the MT8972 would terminate the line and encode/decode the data and voice for transmission while additional electronics could provide interfaces for a standard telephone set and any number of data ports supporting standard data rates for such things as computer communications and telemetry for remote meter reading. Digital workstations with a high degree of networking capability can be designed using the DNIC for the line interface, offering up to 160 kbit/s data transmission over existing telephone lines. The MT8972 could also be valuable within existing computer networks for connecting a large number of terminals to a computer or for intercomputer links. The highest data rates existing for terminal to computer links is

19.2 kbit/s over conventional analog modems. With the DNIC this can be increased up to 160 kbit/s at a very low cost per line for terminal to computer links and in many cases this bandwidth would be sufficient for computer to computer links.

Figure 1 shows the block diagram of the MT8972. The DNIC provides a bidirectional interface between the DV (data/voice) port and a full duplex line operating at 80 or 160 kbit/s over a single pair of twisted wires. The DNIC has 3 serial ports. The DV port (DSTi/Di, DSTo/Do), the CD (control/data) port (CDSTi/CDi, CDSTo/CDo) and a line port (L_{IN}, L_{OUT}). The data on the line is made up of information from the DV and CD ports. The DNIC must combine information received from both the DV and CD ports and put it onto the line. At the same time, the data received from the line must be split into the various channels and directed to the proper ports. The usable data rates are 72 and 144 kbit/s as recommended by the CCITT for the ISDN U-reference point. Full duplex transmission is made possible through on board adaptive echo cancellation.

The DNIC has various modes of operation which are selected through the mode select pins MS0-2. The two major modes of operation are the MODEM (MOD) and DIGITAL NETWORK (DN) modes. MOD mode is a transparent 80 or 160 kbit/s modem. In DN mode the line carries the B and D channels formatted for the ISDN at either 80 or 160 kbit/s. In the DN mode the DV and CD ports are standard ST-BUS and in MOD mode they are transparent serial data streams at 80 or 160 kbit/s. Other modes include: MASTER (MAS) or SLAVE (SLV) mode, where the timebase and frame synchronization are provided externally or are extracted from the line and DUAL or SINGLE (SINGL) port modes, where both the DV and CD ports are active or where the CD port is inactive and all information is passed through the DV port. For a detailed description of the modes see Operating Modes section.

In DIGITAL NETWORK (DN) mode there are three channels transferred by the DV and CD ports. They are the B, C and D channels. The B1 and B2 channels each have a bandwidth of 64 kbit/s and are used for carrying PCM encoded voice or data. These channels are always transmitted and received through the DV port (Figures 9, 10, 11, 12). The C-channel, having a bandwidth of 64 kbit/s, provides a means for the system to control the DNIC and for the DNIC to pass status information back to the system. The C-channel has a Housekeeping (HK) bit which is the only bit of the C-Channel transmitted and received on the line. The D-channel can be transmitted or received on the line with either a 8, 16 or 64 kbit/s bandwidth depending on the DNIC's mode of operation. Both the HK bit and the D-channel can be used for end-to-end signalling or low speed data transfer. In DUAL port mode the C and D channels are accessed via the CD port (Figure 13) while in SINGL port mode they are transferred through the DV port (Figures 11, 12) along with the B1 and B2 channels.

In DIGITAL NETWORK (DN) mode, upon entering the DNIC from the DV and CD ports, the B-channel data, D-channel D_0 (and D_1 for 160 kbit/s), the HK bit of the C-channel (160kbit/s only) and a SYNC bit are combined in a serial format to be sent out on the line by the Transmit Interface (Figures 16, 17). The SYNC bit produces an alternating 1-0 pattern each frame in order for the remote end to extract the frame alignment from the line. It is possible for the remote end to lock onto a data bit pattern which simulates this alternating 1-0 pattern that is not the true SYNC. To decrease the probability of this happening the DNIC may be programmed to put the data through a prescrambler that scrambles the data according to a predetermined polynomial with respect to the SYNC bit. This greatly decreases the probability that the SYNC pattern can be reproduced by any data on the line. In order for the echo canceller to function correctly, a dedicated scrambler is used with a scambling algorithm which is different for the SLV and MAS modes. These algorithms are calculated in such a way as to provide orthogonality between the near and far end data streams such that the correlation between the two signals is very low.

For any two DNICs on a link, one must be in SLV mode with the other in MAS mode. The scrambled data is differentially encoded which serves to make the data on the line polarity-independent. It is then biphase encoded as shown in Figure 15. See Line Interface section for more details on the encoding. Before leaving the DNIC the differentially encoded biphase data is passed through a pulse-shaping bandpass transmit filter that filters out the high and low frequency components and conditions the signal for transmission on the line.

The composite transmit and receive signal is received at L_{IN}. On entering the DNIC this signal passes through a Pre-Canceller which is a summing amplifier and low pass filter that partially cancels the near-end signal and provides first order antialiasing for the received signal. The resultant signal passes through a receive filter to bandlimit

and equalize it. At this point, the echo estimate from the echo canceller is subtracted from the precancelled received signal. This difference signal is then input to the echo canceller as an error signal and also squared up by a comparator and passed to the biphase receiver. Within the echo canceller, the sign of this error signal is determined. Depending on the sign, the echo estimate is either incremented or decremented and this new estimate is stored back in RAM.

The timebase in both SLV and MAS modes (generated internally in SLV mode and externally in MAS mode) is phase locked to the received data stream. This phase locked clock operates the Biphase Decoder, Descrambler and Deprescrambler in MAS mode and the entire chip in SLV mode. The Biphase Decoder decodes the received encoded bit stream resulting in the original NRZ data which is passed onto the Descrambler and Deprescrambler where the data is restored to its original content by performing the reverse polynomials. The SYNC bits are extracted and the Receive Interface separates the channels and outputs them to the proper ports in the proper channel times. The destination of the various channels is the same as that received on the input DV and CD ports.

The Transmit/Receive Timing and Control block generates all the clocks for the transmit and receive functions and controls the entire chip according to the control register. In order that more than one DNIC may be connected to the same DV and CD ports an $\overline{F0o}$ signal is generated which signals the next device in a daisy chain that its channel times are now active. In this arrangement only the first DNIC in the chain receives the system $\overline{F0}$ with the following devices receiving its predecessor's $\overline{F0o}$.

In MOD mode, all the ports have a different format. The line port again operates at 80 or 160 kbit/s, however there is no synchronization overhead, only transparent data. The DV and CD ports carry serial data at 80 or 160 kbit/s with the DV port transferring all the data for the line and the CD port carrying the C-channel only. In this mode the transfer of data at both ports is synchronized to the $\overline{TCK}$ and $\overline{RCK}$ clocks for transmit and receive data respectively.

The $\overline{CLD}$ signal goes low to indicate the start of the C-channel data on the CD port. It is used to load and latch the input and output C-channel but has no relationship to the data on the DV port.

Operating Modes (MS0-2)

The logic levels present on the mode select pins MS0, MS1 and MS2 program the DNIC for different operating modes and configure the DV and CD ports accordingly. Table 1 shows the modes corresponding to the state of MS0-2. These pins select the DNIC to operate as a MASTER or SLAVE, in DUAL or SINGLE port operation, in MODEM or DIGITAL NETWORK mode and the order of the C and D channels on the CD port. Table 2 provides a description of each mode and Table 3 gives a pin configuration according to the mode selected for all pins that have variable functions. These functions vary depending on whether it is in MAS or SLV, and whether DN or MOD mode is used.

The overall mode of operation of the DNIC can be programmed to be either a baseband modem (MOD mode) or a digital network transceiver (DN mode). As a baseband modem, transmit/receive data is passed transparently through the device at 80 or 160 kbit/s by the DV port. The CD port transfers the C-channel and D-Channel also at 80 or 160 kbit/s.

Mode Select Pins			Mode	Operating Mode								
MS2	MS1	MS0		SLV	MAS	DUAL	SINGL	MOD	DN	D-C	C-D	ODE
0	0	0	0		E		E		E	E		E
0	0	1	1		E	E		E		X	X	E
0	1	0	2		E	E			E		E	E
0	1	1	3		E	E			E	E		E
1	0	0	4	E			E		E	E		E
1	0	1	5	E		E		E		X	X	E
1	1	0	6	E		E			E		E	E
1	1	1	7		E	E			E	E		

E = Enabled X = Not Applicable
Blanks are disabled

Table 1. Mode Select Pins

In DN mode, both the DV and CD ports operate as ST-BUS streams at 2.048 Mbit/s and the DNIC performs all the necessary functions to comply with the ISDN U-Interface requirements. The DV port transfers data over pins DSTi and DSTo while on the CD port, the CDSTi and CDSTo pins are used. The SINGL port option only exists in DN mode.

In MOD mode, DUAL port operation must be used and the D, B1 and B2 channel designations no longer exist. The selection of SLV or MAS will determine which of the DNICs is using the externally supplied clock and which is phase locking to the data on the line. Due to jitter and end to end delay, one end must be the master to generate

Mode	Function
SLV	**SLAVE** - The chip timebase is extracted from the received line data and the external 10.24 MHz crystal is phase locked to it to provide clocks for the entire device and are output for the external system to synchronize to.
MAS	**MASTER** - The timebase is derived from the externally supplied data clocks and 10.24 MHz clock which must be frequency locked. The transmit data is synchronized to the system timing with the receive data recovered by a clock extracted from the receive data and resynchronized to the system timing.
DUAL	**DUAL PORT** - Both the CD and DV ports are active with the CD port transferring the C&D channels and the DV port transferring the B1& B2 channels.
SINGL	**SINGLE PORT** - The B1& B2, C and D channels are all transferred through the DV port. The CD port is disabled and CDSTi should be pulled high.
MOD	**MODEM** - Baseband operation at 80 or 160 kbits/s. The line data is received and transmitted through the DV port at the baud rate selected. The C-channel is transferred through the CD port also at the baud rate and is synchronized to the $\overline{CLD}$ output.
DN	**DIGITAL NETWORK** - Intended for use in the digital network with the DV and CD ports operating at 2.048 Mbits/s and the line at 80 or 160 kbits/s configured according to the applicable ISDN recommendation.
D-C	**D BEFORE C-CHANNEL** - The D-channel is transferred before the C channel following $\overline{F0}$.
C-D	**C BEFORE D-CHANNEL** - The C-channel is transferred before the D channel following $\overline{F0}$.
ODE	**OUTPUT DATA ENABLE** - When high the DV and CD ports are enabled during the appropriate channel times. When low, both busses are three state. Intended for power-up reset to avoid bus contention and possible damage to the device during the initial random state in a daisy-chain configuration of DNICs.

Table 2. Mode Definitions

Mode #	Pin 8		Pin 14		Pin 15	
	Name	Input/Output	Name	Input/Output	Name	Input/Output
0	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input
1	$\overline{CLD}$	Output	$\overline{RCK}$	Output	$\overline{TCK}$	Output
2	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input
3	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input
4	$\overline{F0}$	Output	$\overline{F0o}$	Output	$\overline{C4}$	Output
5	$\overline{CLD}$	Output	$\overline{RCK}$	Output	$\overline{TCK}$	Output
6	$\overline{F0}$	Output	$\overline{F0o}$	Output	$\overline{C4}$	Output
7	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input

Table 3. Pin Configurations

all the timing for the link and the other must extract the timing from the receive data and synchronize itself to this timing in order to recover the synchronous data. DUAL port mode allows the user to use two separate serial buses: the DV port for PCM/data (B channels) and the CD port for control and signalling information (C and D channels). In the SINGL port mode, all four channels are concatenated into one serial stream and input to the DNIC via the DV port. The order of the C and D channels may be changed only in DN/DUAL mode. The DNIC may be configured to transfer the D-channel in channel 0 and the C-channel in channel 16 or vice versa. One other feature exists; ODE, where both the DV and CD ports are tristated in order that no devices are damaged due to excessive loading while all DNICs are in a random state on power up in a daisy chain arrangement.

DV Port (DSTi/Di, DSTo/Do)

The DV port transfers data or PCM encoded voice to and from the line according to the particular mode selected by the mode select pins. The modes affecting the configuration of the DV port are MOD or DN and DUAL or SINGL. In DN mode the DV port operates as an ST-BUS at 2.048 Mbit/s with 32, 8 bit channels per frame as shown in Figure 8. In this mode the DV port channel configuration depends upon whether DUAL or SINGL port is selected. When DUAL port mode is used, the C and D channels are passed through the CD port and the B1 and B2 channels are passed through the DV port. At 80 kbit/s only one channel of the available 32 at the DV port is utilized, this being channel 0 which carries the B1-channel. This is shown in Figure 9. At 160 kbit/s, two channels are used, these being 0 and 16 carrying the B1 and B2 channels respectively. This is shown in Figure 10. When SINGL port mode is used, channels B1, B2, C and D are all passed via the DV port and the CD port is disabled. See CD port description for an explanation of the C and D channels.

The D-channel is always passed during channel time 0 followed by the C and B1 channels in channel times 1 and 2 respectively for 80 kbit/s. See Figure 11. For 160 kbit/s the B2 channel is added and occupies channel time 3 of the DV port. See Figure 12. For all of the various configurations the bit orders are shown by the respective diagram. In MOD mode the DV and CD ports no longer operate at 2.048 Mbits/s but are continuous serial bit streams operating at the bit rate selected of 80 or 160 kbit/s. While in the MOD mode only DUAL port operation can be used.

In order for more than one DNIC to be connected to any one DV and CD port, making more efficient use of the busses, the DSTo and CDSTo outputs are put into high impedance during the inactive channel times of the DNIC. This allows additional DNICs to be cascaded onto the same DV and CD ports. When used in this way a signal called $\overline{F0o}$ is used as an indication to the next DNIC in a daisy chain that its channel time is now active. Only the first DNIC in the chain receives the system frame pulse and all others receive the $\overline{F0o}$ from its predecessor in the chain. This allows up to 16 DNICs to be cascaded.

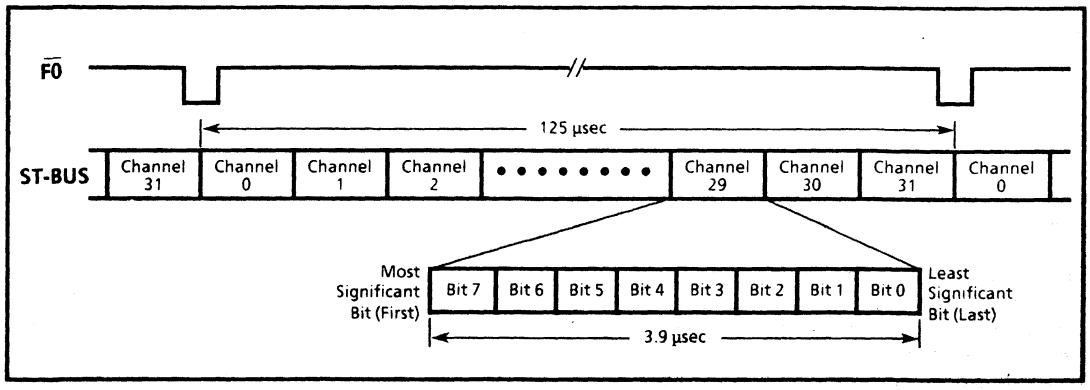


Figure 8. ST-BUS Format

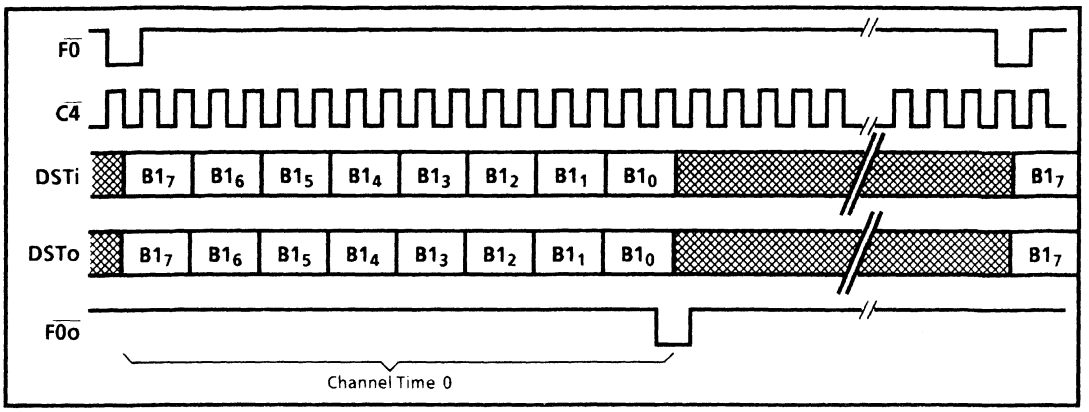


Figure 9. DV Port - 80 kbit/s (Modes 2, 3, 6)

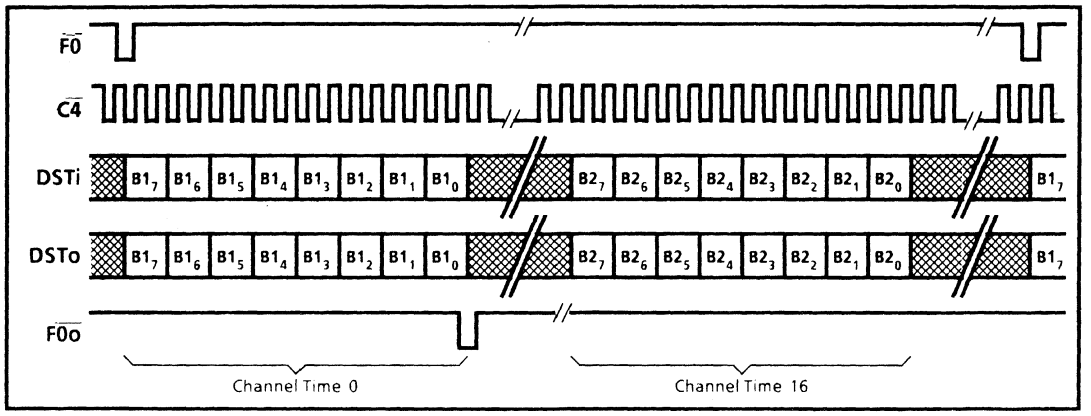


Figure 10. DV Port - 160 kbit/s (Modes 2, 3, 6)

CD Port (CDSTi/CDi, CDSTo/CDo)

The CD port is a serial bidirectional port used only in DUAL port mode. It is a means by which the DNIC receives its control information for things such as setting the bit rate, enabling internal loopback tests, sending status information back to the system and transferring low speed signalling data to and from the line.

The CD port is composed of the C and D-Channels. The C-channel is used for transferring control and status information between the DNIC and the system. The D-channel is used for sending and receiving signalling information and lower speed data between the line and the system. In DN/DUAL mode the DNIC receives a C-channel on CDSTi while transmitting a C-channel on CDSTo. Fifteen channel times later (halfway through the frame) a D-channel is received on CDSTi while a D- channel is transmitted on CDSTo. This is shown in Figure 13. The order of the C and D bytes in DUAL port mode can be reversed by the mode select pins. See Table 1 for a listing of the byte orientations.

The D-channel exists only in (DN) mode and may be used for transferring low speed data or signalling information over the line at 8, 16 or 64 kbit/s (by using the DINB feature). The information passes transparently through the DNIC and is transmitted to or received from the line at the bit rate selected in the Control Register.

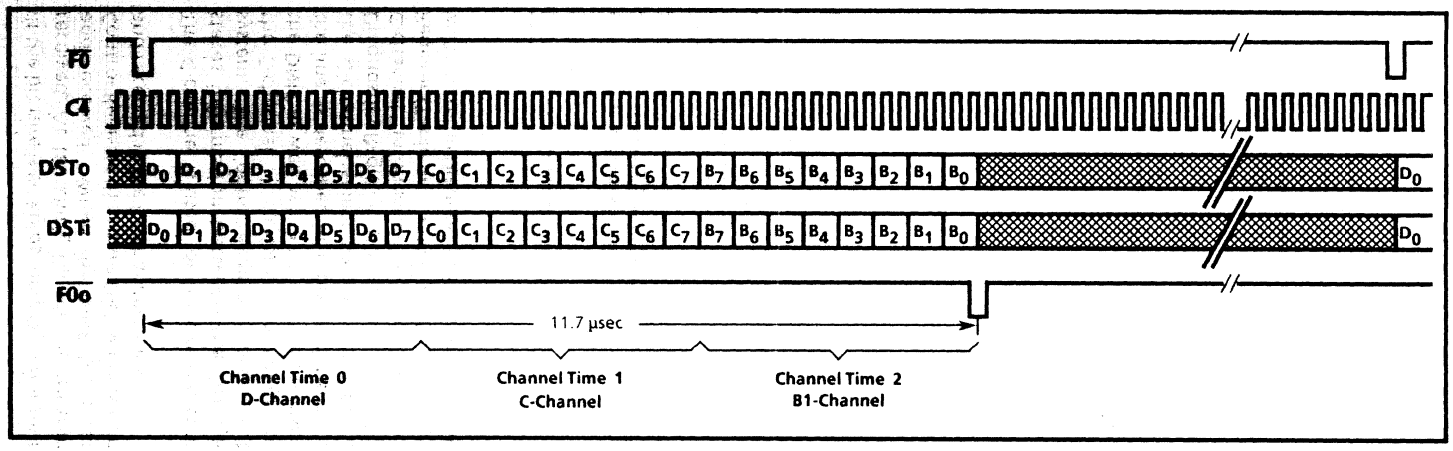


Figure 11. DV Port - 80 kbit/s (Modes 0,4)

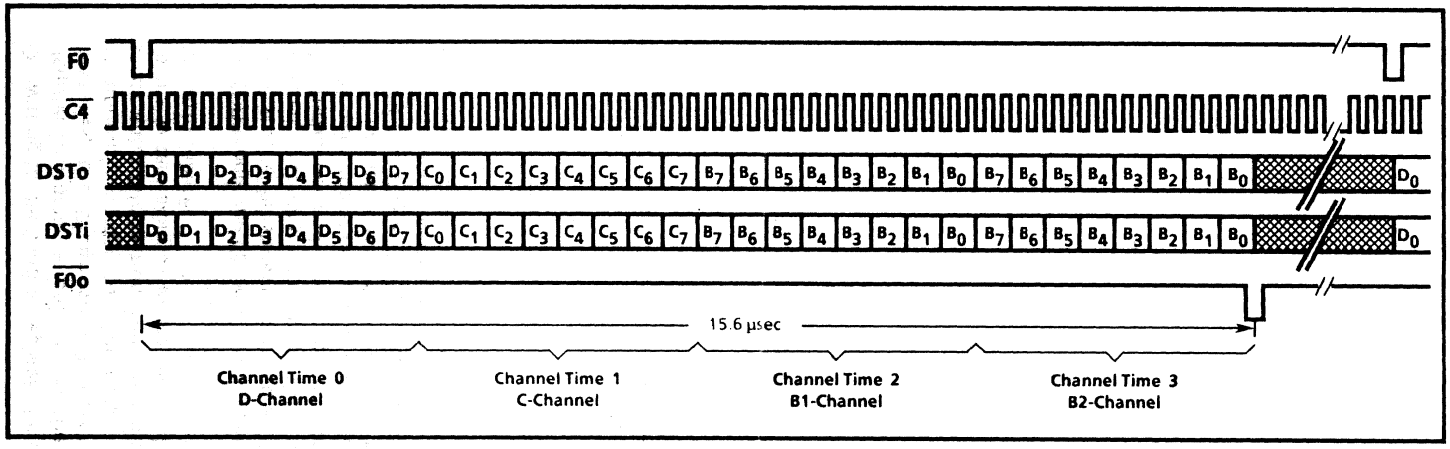


Figure 12. DV Port - 160 kbit/s (Modes 0,4)

If the bit rate is 80 kbit/s, only D_0 is transmitted and received. At 160 kbit/s, D_0 and D_1 are transmitted and received. When the DINB bit is set in the Control Register the entire D-channel is transmitted and received in the B1-channel timeslot.

The C-channel is used for transferring control and status information between the DNIC and the system. The Control Register is accessed through the C-channel. It contains information to control the DNIC as well as the HK bit to be transmitted on the line as described in Tables 4, 5. Bits 0 and 1 of the C-channel select between the Control and Diagnostics Register. If these bits are 0, 0 then the C-channel information is written to the Control Register (Table 4). If they are 0, 1 the C-channel is written to the Diagnostics Register (Table 5).

On writing to the Control Register, the Diagnostics Register is cleared. In order to use the diagnostic features, the Diagnostics Register must be continuously written to The output C-channel sends status information from the Status Register to the system along with the received HK bit as shown in Table 6.

In MOD mode, the CD port is no longer an ST-BUS but is a serial bit stream operating at the bit rate selected. It continues to transfer the C-channel but the D-channel and the HK bit no longer exist. DUAL port operation must be used in MOD mode. The C-channel is clocked in and out of the CD port by TCK and CLD with TCK defining the bits and CLD the channel boundaries of the data stream as shown in Figure 14.

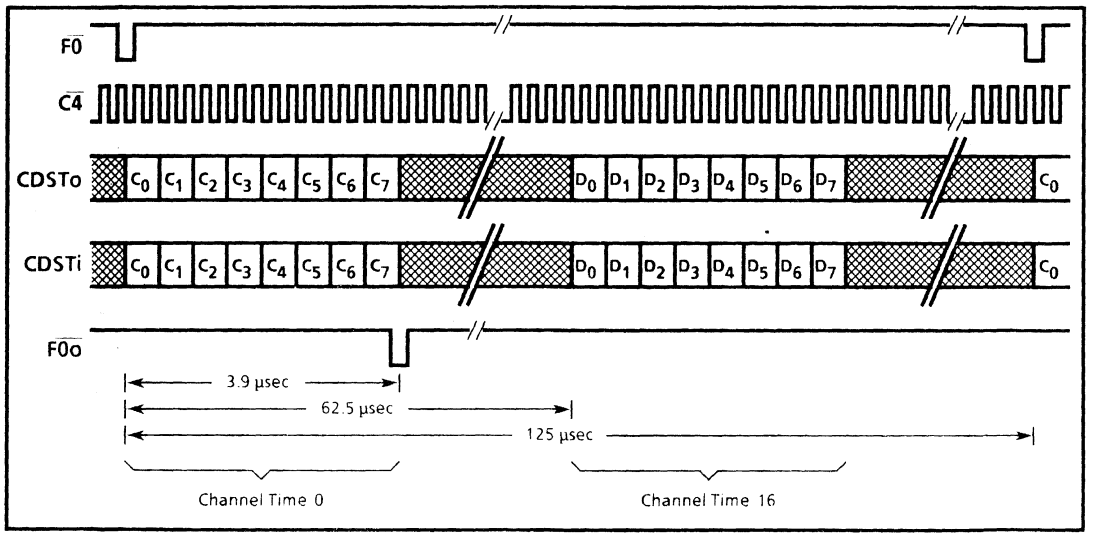


Figure 13. CD Port (Modes 2, 6)

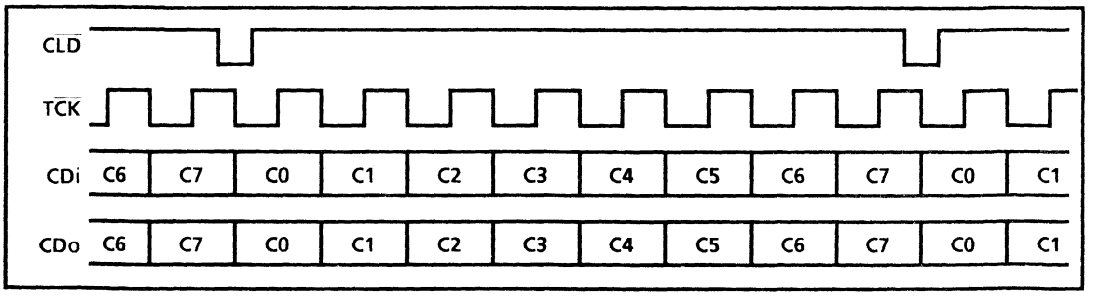
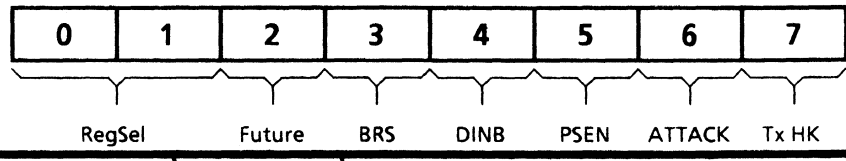


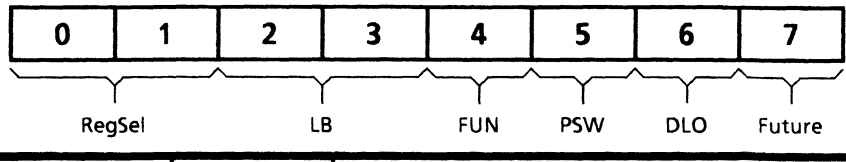
Figure 14. CD Port (Modes 1, 5)



Control Register								Control Function	Resulting Function
0	1	2	3	4	5	6	7		
0	0	0	X	X	X	X	X	Future	Reserved for Future Functionality. Connect to V_{SS}
0	0	X	0	X	X	X	X	Bit Rate Select (BRS)	80 kbit/s
0	0	X	1	X	X	X	X		160 kbit/s
0	0	X	X	0	X	X	X	D Channel In B Timeslot (DINB)	Only the D-channel bits corresponding to the bit rate are transmitted during the normal D-channel bit times.
0	0	X	X	1	X	X	X		The entire D-channel is transmitted during the B1-channel time slot on the line providing a 64 kbit/s D-channel link.
0	0	X	X	X	0	X	X	Prescrambler/ Deprescrambler Enable (PSEN)	The data prescrambler & deprescrambler are disabled.
0	0	X	X	X	1	X	X		The data prescrambler & deprescrambler are enabled.
0	0	X	X	X	X	0	X	Convergence Speedup (ATTACK)	The echo canceller will require the normal amount of time to converge to a reflection coefficient.
0	0	X	X	X	X	1	X		The echo canceller will converge to the reflection coefficient much faster. Used on power up for fast convergence. Note 1
0	0	X	X	X	X	X	0/1	Tx HK	Housekeeping bit to be transmitted over the line.
X	X	X	1	1	1	1	1	Default Modes	By tying CDSTi/CDi high a default mode operation is selected where the bit rate is 160 kbit/s and ATTACK, PSEN and DINB are all disabled and Tx HK = 0.
X	X	X	0	0	0	0	0		By tying CDSTi/CDi low a default mode operation is selected where the bit rate is 80 kbit/s and ATTACK, PSEN and DINB are all disabled and Tx HK = 0.

Table 4. Control Register

Notes : 1) Suggested use of ATTACK: At 160 kbit/s full convergence requires 850 msec with ATTACK held high for the first 240 frames or 30 ms.
At 80 kbit/s full convergence requires 1.75 sec with ATTACK held high for the first 480 frames or 60 ms.



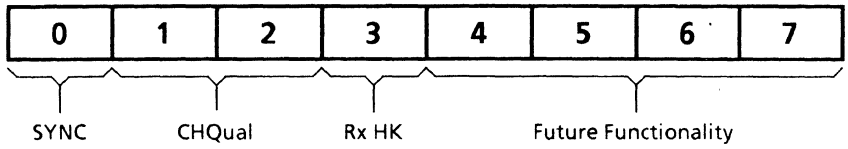
Diagnostics Register								Diagnostic Function	Resulting Function
0	1	2	3	4	5	6	7		
0	1	0	0	X	X	X	X	Internal Loopback Tests (LB)	All loopback testing functions disabled. Normal operation.
0	1	1	0	X	X	X	X		L_{OUT} is internally looped back into L_{IN} for system diagnostics.[1]
0	1	0	1	X	X	X	X		DSTi is internally looped back into DSTo for system diagnostics.
0	1	1	1	X	X	X	X		DSTo is internally looped back into DSTi for end to end testing.[2]

1 Do not use L_{OUT} to L_{IN} loopback in DN/SLV mode
2 Do Not use DSTo to DSTi loopback in MOD/MAS mode

Table 5. Diagnostics Register

Diagnostics Register								Diagnostic Function	Resulting Function
0	1	2	3	4	5	6	7		
0	1	X	X	0	X	X	X	Force UnSync (FUN)	Operation continues in synchronization.
0	1	X	X	1	X	X	X		DNIC is forced out of SYNC to test the SYNC recovery circuitry.
0	1	X	X	X	0	X	X	Polynomial Swap (PSW)	Polynomials retain their normal designations
0	1	X	X	X	1	X	X		Scrambling and descrambling polynomials are interchanged. Use for MAS mode only.
0	1	X	X	X	X	0	X	Disable Line Out (DLO)	L_{out} pin functions normally
0	1	X	X	X	X	1	X		The signal on L_{out} is set to V_{Bias}
0	1	X	X	X	X	X	0	Future	Future Functionality. Should be held at 0 for normal operation

Table 5. Diagnostics Register Cont'd



Status Register	Name	Function
0	**SYNC**	**Synchronization** - When set this bit indicates that synchronization to the received line data sync pattern has been acquired. For DN mode only.
1-2	**CHQual**	**Channel Quality** - These bits provide an estimate of the receiver's margin against noise. The farther this 2 bit value is from 0 the better the SNR.
3	**Rx HK**	**House Keeping** - This bit is the received housekeeping (HK) bit from the far end.
4-7	**Future**	**Future Functionality**

Table 6. Status Register

Line Port (L_{IN}, L_{OUT})

The line interface is made up of L_{OUT} and L_{IN} with L_{OUT} driving the transmit signal onto the line and L_{IN} receiving the composite transmit and receive signal from the line. The line code used in the DNIC is Biphase and is shown in Figure 15. The scrambled NRZ data is differentially encoded meaning the previous differential encoded output is XOR'd with the current data bit which produces the current output. This is then biphase encoded where transitions occur midway through the bit cell with a negative going transition indicating a logic "0" and a positive going transition indicating a logic "1".

There are some major reasons for using a biphase line code. The power density is concentrated in a spectral region that minimizes dispersion and differential attenuation. This can shorten the line response and reduce the intersymbol interference which are critical for adaptive echo cancellation. There are regular zero crossings halfway through every bit cell or baud which allows simple clock extraction at the receiving end. There is no D.C. content in the code so that phantom power feed may be applied to the line and simple transformer coupling may be used with no effect on the data. It is bipolar, making data reception simple and providing a high signal to noise ratio. The signal is then passed through a bandpass filter which conditions the signal for the line by limiting the spectral content from $0.2f_{Baud}$ to $1.6f_{Baud}$ and on to a line driver where it is made available to be put onto the line biased at V_{Bias}. The resulting transmit signal will have a distributed spectrum with a peak at $\frac{3}{4}f_{Baud}$. The receive signal is the above transmit signal superimposed on the signal from the remote end and any reflections or delayed symbols of the near end signal.

The frame format of the transmit data on the line is shown in Figures 16 and 17 for the DN mode at 80 and 160 kbit/s. At 80 kbit/s a SYNC bit for frame recovery, one bit of the D-channel and the B1-channel are transmitted. At 160 kbit/s a SYNC bit, the HK bit, two bits of the D-channel and both B1 and B2 channels are transmitted.

If the DINB bit of the Control Register is set, the entire D-channel is transmitted during the B1-channel time slot. In MOD mode the SYNC, HK and D-channel bits are not transmitted or received but rather a continuous data stream at 80 or 160 kbit/s is present. No frame recovery information is present on the line in MOD mode.

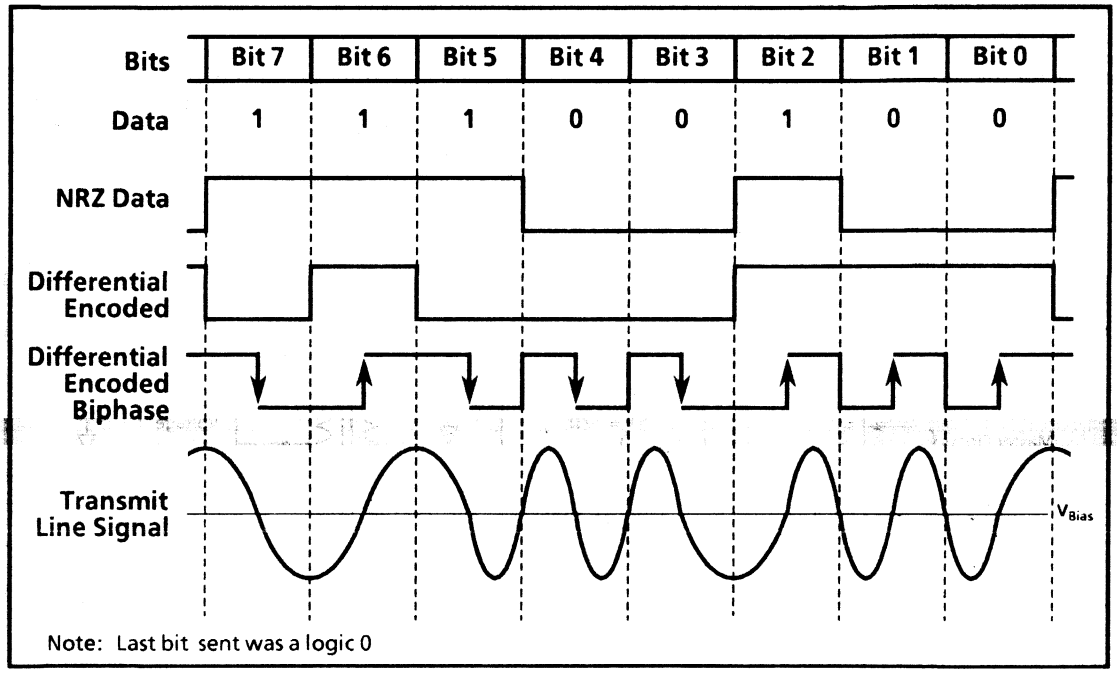


Figure 15. Data & Line Encoding

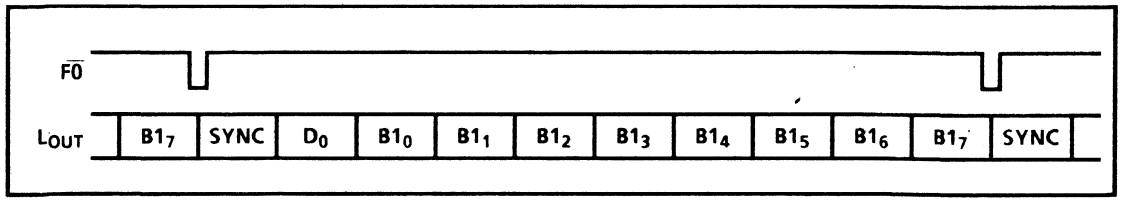


Figure 16. Frame Format - 80 kbit/s (Modes 0, 2, 3, 4, 6)

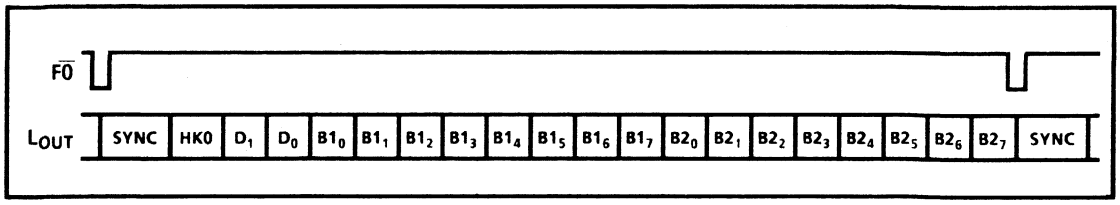


Figure 17. Frame Format - 160 kbit/s (Modes 0, 2, 3, 4, 6)

Applications

Typical connection diagrams are shown in Figures 18 and 19 for the DN mode as a MASTER and SLAVE respectively. L_{OUT} is connected to the coupling transformer through a resistor R2 and capacitors C2 and C2' to match the line characteristic impedance. Suggested values of R2, C2 and C2' for 80 and 160 kbit/s operation are provided in Figures 18 and 19. Overvoltage protection is provided by R1, D1 and D2. C1 is present to properly bias the received line signal for the L_{IN} input. A 2:1 coupling transformer is used to couple to the line with a secondary center tap for optional phantom power feed. Varistors have been shown for surge protection against such things as lightning strikes.

If the scramblers power up with all zeroes in them, they are not capable of randomizing this all-zeroes data sequence. This increases the correlation between the transmit and receive data which may cause loss of convergence in the echo canceller and high bit error rates.

In DN mode the insertion of the SYNC pattern will provide enough pseudo-random activity to maintain convergence. In MOD mode the SYNC pattern is not inserted. For this reason, at least one "1" must be fed into the DNIC on power up to ensure that the scramblers will randomize any subsequent all-zeroes sequence.

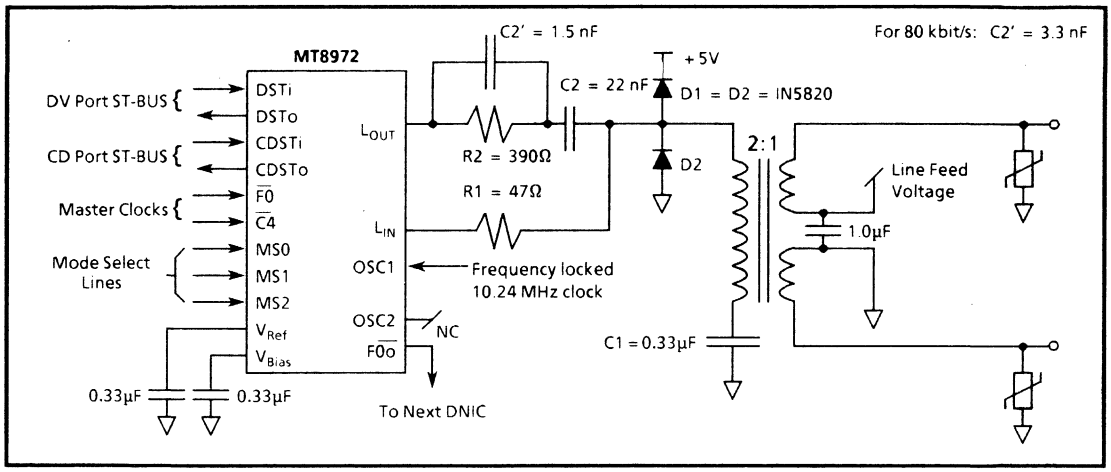


Figure 18. Typical Connection Diagram - MAS/DN Mode, 160 kbit/s

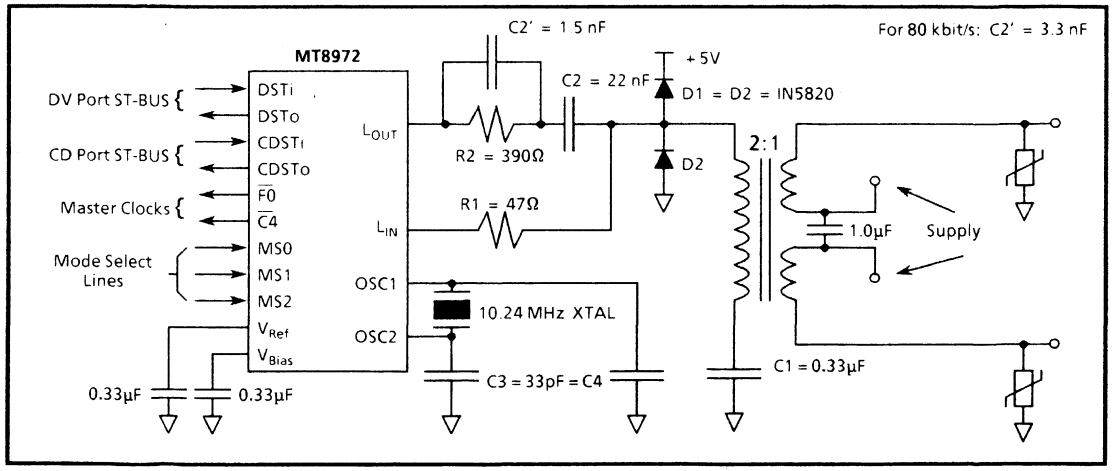


Figure 19. Typical Connection Diagram - SLV/DN Mode, 160 kbit/s

MT8972-EVAL-PKG
DNIC EVALUATION BOARD SET

JAN 1985

Features

- Tested DNIC evaluation board set
- Two boards for end-to-end testing
- Comprehensive user's manual
- Parallel microprocessor or ST-BUS access
- Serial interface to bit error rate testers

Ordering Information	
MT8972-EVAL-PKG	•Two boards plus documentation

Description

To assist designers in the breadboard and analysis of the Mitel ISO-CMOS Digital Network Interface Chip (MT8972), Mitel has developed a low-cost fully tested board set. With the board set, the designer can quickly connect a cable pair between the two evaluation boards, supply a serial or parallel source of data, and power supplies and in a matter of minutes have full duplex data running over 2 wires at up to 160 kb/s. It is then a simple matter to evaluate the performance of the MT8972 in respect to bit error rates, and apply additional impairments such as bridged taps, gauge changes, and crosstalk.

The documentation details both the microprocessor and serial interfaces to the boards, and includes a schematic of the line interface circuit, and why the components were selected. The boards can be switched to either master or slave to emulate respectively the exchange and subscriber sides of the network.

Purchasers of the board set are added to the DNIC mailing list so that all information relating to the DNIC performance, characterization, and results of standardization efforts can be forwarded to the user.

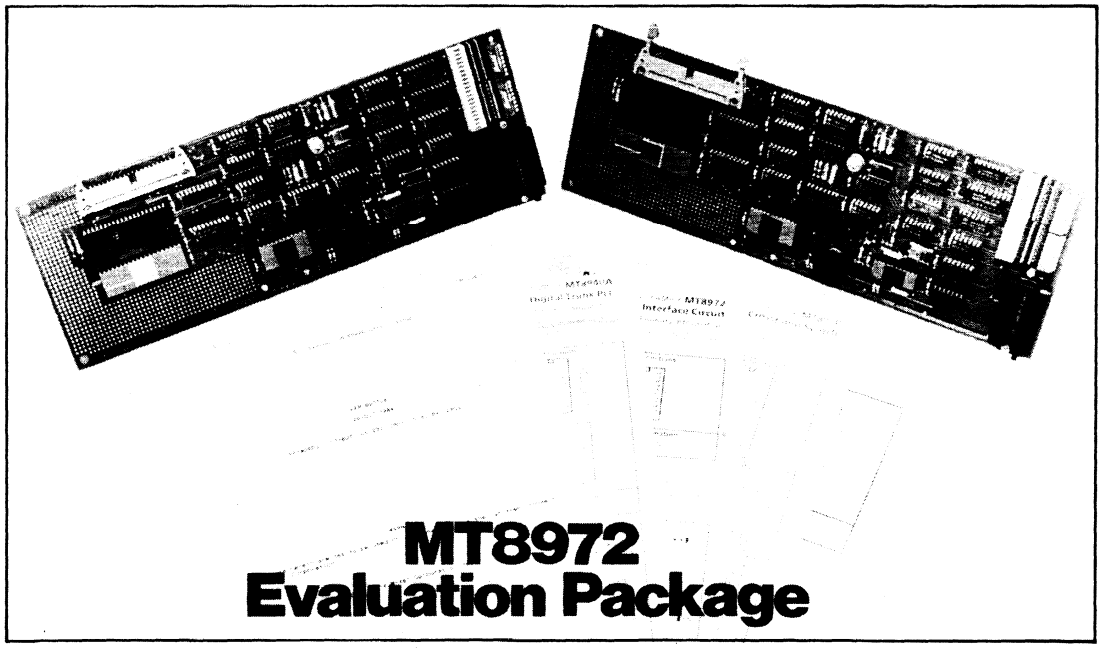


Figure 1 MT8972 Evaluation Package

MH89728 and MH89726
MT8972 Loop Extender Circuits

Advance Information

9161-002-075NA ISSUE 1 July 1986

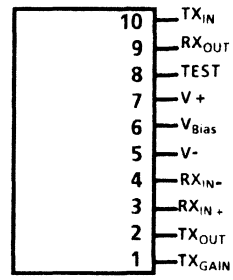
Features

- Operates from single or dual power supply.
- MH89728 extends transmission performance for the MT8972 (DNIC) at 80kbit/s line rate.
- MH89726 extends transmission performance for the MT8972 (DNIC) at 160kbit/s line rate.
- MH89728 and MH89726 are pin for pin compatible with each other.
- Compact SIL package
- Over 6km loop range on 24 AWG

Applications

- Digital subscriber lines
- Digital PABX line cards and telephone sets
- **High speed, limited distance modem**
- ISDN U - Interface

Pin Connections



Ordering Information

MH89728
MH89726 10 pin SIL Hybrid
0°C to 70°C

Description

The MH89728 and MH89726 are thick film hybrid devices which may be used to extend the operating range of the MT8972 (DNIC). The hybrids combine signal equalization and amplification for the receive and transmit paths on each device.

The small size of these hybrids makes them suitable for line card or terminal use with the MT8972. The gain of the transmit signal may be adjusted through the use of an external resistor.

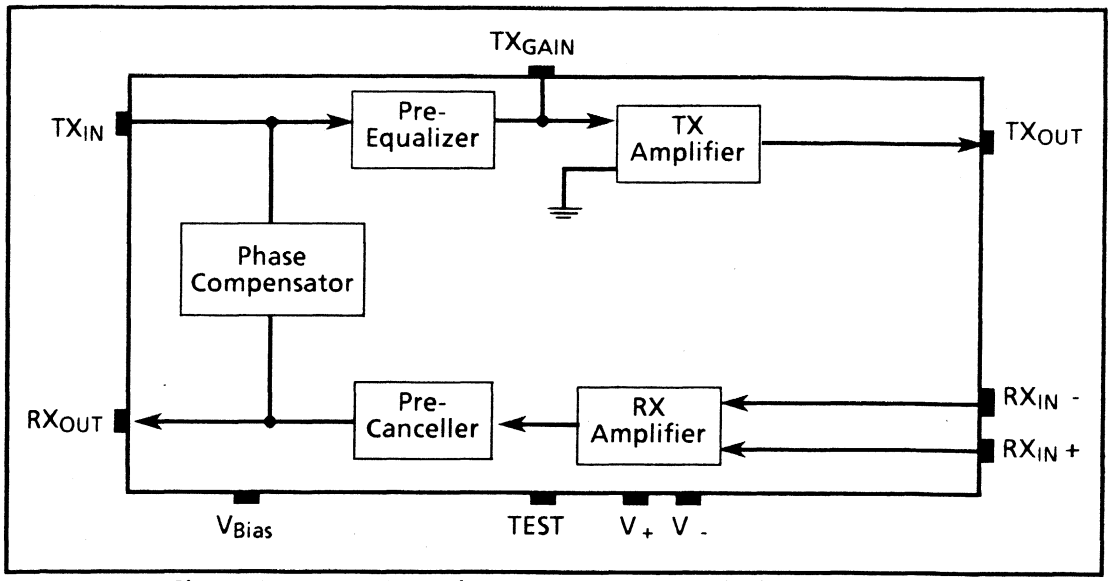


Figure 1 - MH89728 and MH89726 Functional Block Diagram

Recomended Operating Conditions

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	+ 15 V Supply	V_{DD}	13.5	15.0	16.5	V	Note 1
2	- 15 V Supply	V_{SS}	-16.5	-15.0	-13.5	V	Note 2
3	Standby Current	I_S		3.0		mA	

Note 1: A single voltage supply of + 30V ± 10% can be used on V_{DD} with V_{Bias} grounded through a 0.33µF capacitor and V_{SS} grounded.
Note 2: A single voltage supply of -30V ± 10% can be used on V_{SS} with V_{Bias} grounded through a 0.33µF capacitor and V_{DD} grounded.

A.C. Electrical Characteristics

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Active Current	I_A		7.0		mA	@ 60 kHz for 80kbit/s @120 kHz for 160kbit/s
2	TX Gain	A_{TX}		9.0		dB	"
3	TX Phase Angle	Φ_{TX}		-170.0		°	"
4	RX Gain	A_{RX}		0.0		dB	"
5	RX Phase Angle	Φ_{RX}		12.0		°	"
6	Line Power			10.0		dBm	With 2:1 transformer

Pin Descriptions

Pin #	Pin Name	Description
1	TX_{GAIN}	**Transmit Gain:** To be connected to Pin 2. An increase in gain can be achieved by connecting an external resistor R_{EXT} between Pin 1 and Pin 2. The resultant gain is calculated using; **A = (R/24) + 2.8,** where A = Gain and R = R_{EXT} (kΩ).
2	TX_{OUT}	**Transmit Output:** Connect to the termination network.
3	RX_{IN-}	**Negative Receive Signal:** Connect to TX_{OUT}, Pin 2.
4	RX_{IN+}	**Positive Receive Signal:** Connected to line transformer.
5	V -	**Negative power supply.**
6	V_{Bias}	**Internal Bias Voltage:** Connect to GND through 0.33µF for single power supplies. Connect to GND directly for split power supplies.
7	V +	**Positive power supply.**
8	TEST	**Test:** Used for production testing. Leave unconnected.
9	RX_{OUT}	**Receive Output:** Connect to L_{IN} (Pin 21) of MT8972.
10	TX_{IN}	**Transmit Input:** Connect to L_{OUT} (Pin 1) of MT8972.

Functional Description

The MH89728 is a 10 pin SIL thick film hybrid circuit that may be used to extend the loop range capability of the MT8972 (DNIC). For a detailed description of the DNIC, refer to the MT8972 data sheet.

Figure 1 shows a block diagram of the Loop Extender Circuit (LEC). The LEC takes the line signal which is transmitted by the DNIC on L_{OUT}, pre-equalizes, and amplifies it before sending it to the termination network. The gain of the TX amplifier is adjustable by using an external resistor between pins 1 and 2. If no external resistor is added, TX_{GAIN} and TX_{OUT} must be shorted together, and the default gain condition exists. This gain results in a transmit signal power level of + 10 dBm.

On the receive side, the LEC receives the differential line signal from the transformer, and performs first-order pre-cancellation as well as gain and phase adjustment of the receive signal. The signal is then output on RX_{OUT} which is connected to L_{IN} of the MT8972.

Tables 1 and 2 show typical results obtained by using the LEC with the MT8972. Actual distance achieved may vary depending on the characteristics of the transmission cable being used. Most important factors include cable attenuation (dB/km), bridged taps, and crosstalk interference.

The LEC is powered typically from +/ - 15 Volts if dual power supplies are available. Alternately 0 to + 30 Volts, or - 30 to 0 Volts can be used if only a single power supply is available.

Applications

Figure 2 shows a typical connection diagram of the MT8972 and MH89728. RX_{OUT} and TX_{IN} of the LEC are connected to L_{OUT} and L_{IN} of the DNIC respectively. Pins 5, 6 and 7 are the power supply pins, with the voltages being supplied as indicated in the table. An external resistor, R_{EXT}, may be used to increase the gain of the transmitter. Without R_{EXT}, TX_{GAIN} and TX_{OUT} are shorted together resulting in a transmit power level of + 10 dBm.

R_{LL}, R_L, and C_L comprise the termination network and are used to match the characteristic impedance of the transmission line. This provides the 4 wire to 2 wire hybrid conversion necessary for twisted pair transmission.

Figure 3 shows a typical application of the LEC. On short loops, jumpers (or switches) could be used to remove the LEC from the circuit. For longer loops, the jumpers could be changed to include the LEC in the signal path.

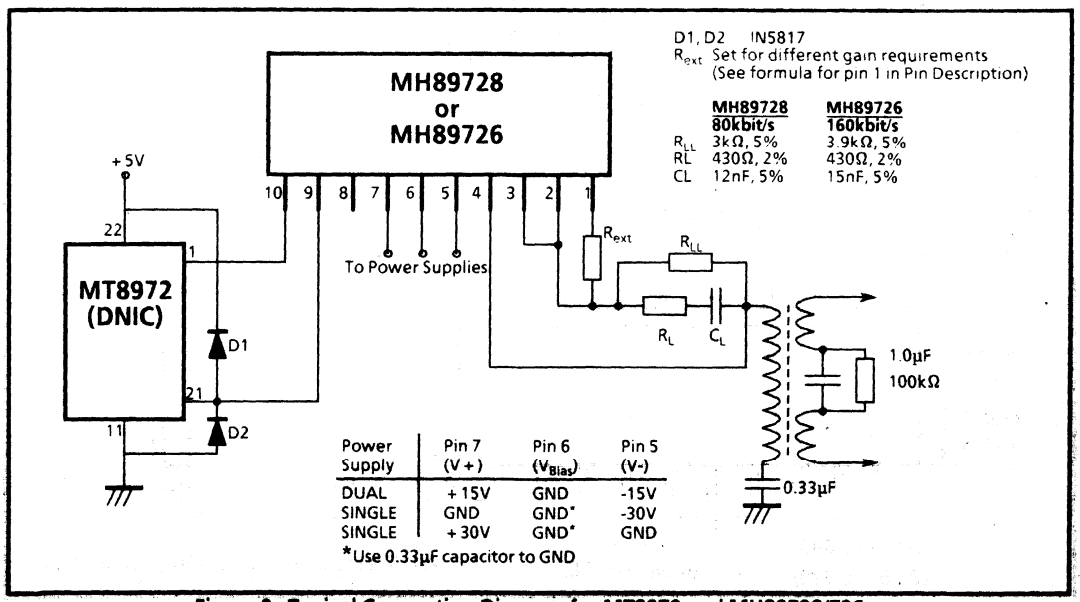


Figure 2. Typical Connection Diagram for MT8972 and MH89728/726

MH89728 (80 kbit/s)		
CABLE / CONFIGURATION	24 AWG (6.9 dB/km at 60kHz)(Note 1)	26 AWG (10.0 dB/km at 60kHz)
DNIC to DNIC	0.0 to 5.2 km	0.0 to 3.4 km
DNIC with LEC to DNIC and LEC	0.9 to 6.5 km	0.65 to 4.1 km

Table 1 - Typical Transmission Performance at 80kbit/s

Note 1: The attenuation of the cable as specified by Bell System Technical Reference PUB 62411.

MH89726 (160 kbit/s)		
CABLE / CONFIGURATION	24 AWG (8.0 dB/km at 120kHz)	26 AWG (11.5 dB/km at 120kHz)
DNIC to DNIC	0.0 to 4.1 km	0.0 to 3.0 km
DNIC with LEC to DNIC with LEC	0.65 to 5.1 km	0.5 to 3.6 km

Table 2 - Typical Transmission Performance at 160kbit/s

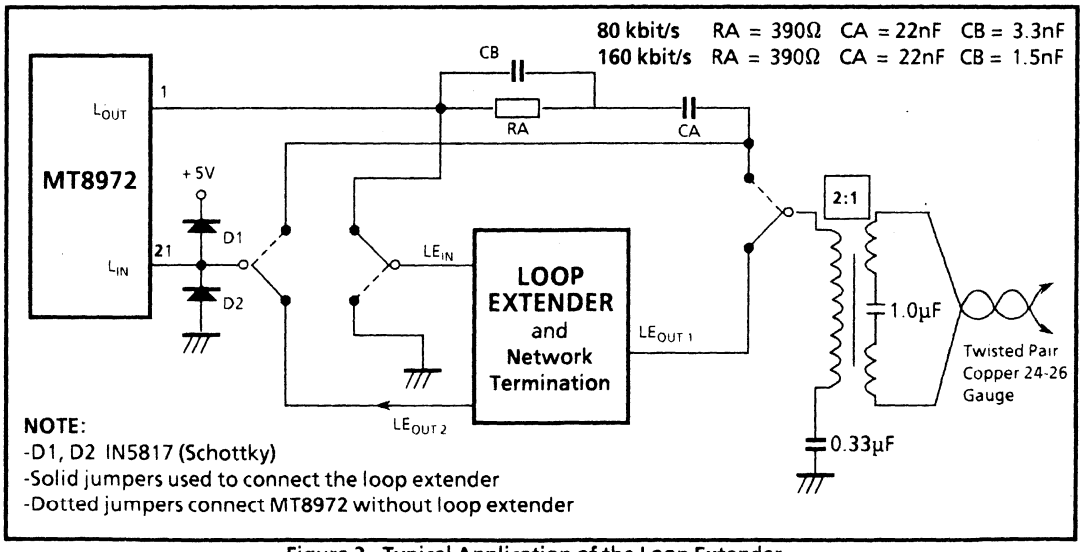


Figure 3 - Typical Application of the Loop Extender

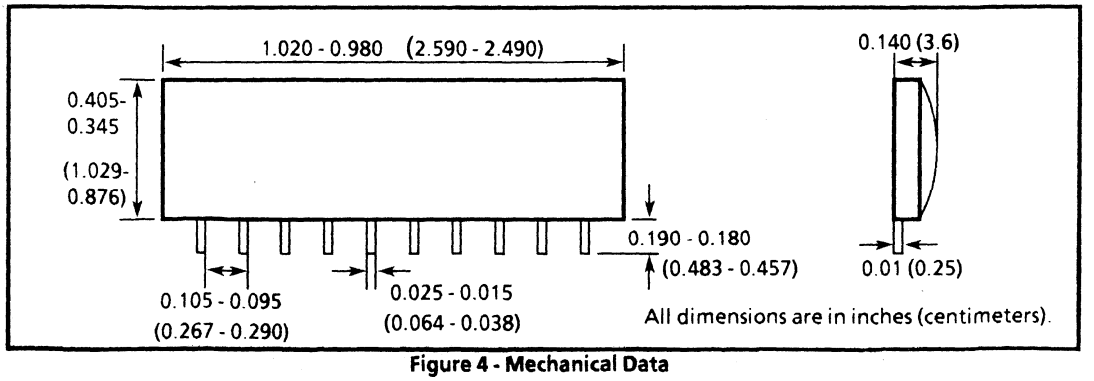


Figure 4 - Mechanical Data

ST-BUS™ FAMILY ISO-CMOS **MT8975**
DS1/T1 Digital Trunk Interface Circuit

9161-002-015-NA ISSUE 4 JUNE 1986

Features

- MITEL ST-BUS™ Compatible
- Interface to bidirectional DS1 link
- 2 Frame Elastic Buffer
- Insertion of A,B and S signalling and alignment bits
- Selectable zero code replacement
- Per channel control
- Programmable digital attenuation of PCM signals
- AMI encoding and decoding
- Bipolar steering outputs
- Debounce of received A & B bits
- External control and status pins
- Low power ISO-CMOS construction
- Single 5V power supply
- TTL compatible inputs and outputs

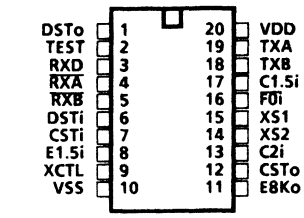
Applications

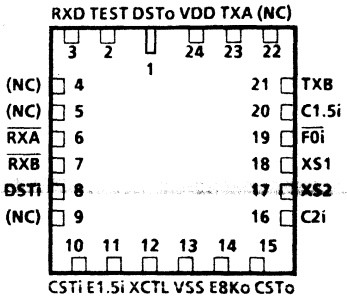
- High speed data links using DS1 transmission link
- PBX or computer to DS1 carrier interface
- Channel banks

Description

The MT8975 is an interface circuit for use between serial 2048 kbit/s ST-BUS™ time division multiplexed streams and a bidirectional 1544 kbit/s DS1 link. All functions except clock extraction, line driving and line sensing are provided. The MT8975 is fabricated in Mitel's ISO-CMOS technology.

Pin Connections





Ordering Information

MT8975AC	20 Pin Ceramic
MT8975AY	24 Pin LCC

-40°C to +85°C

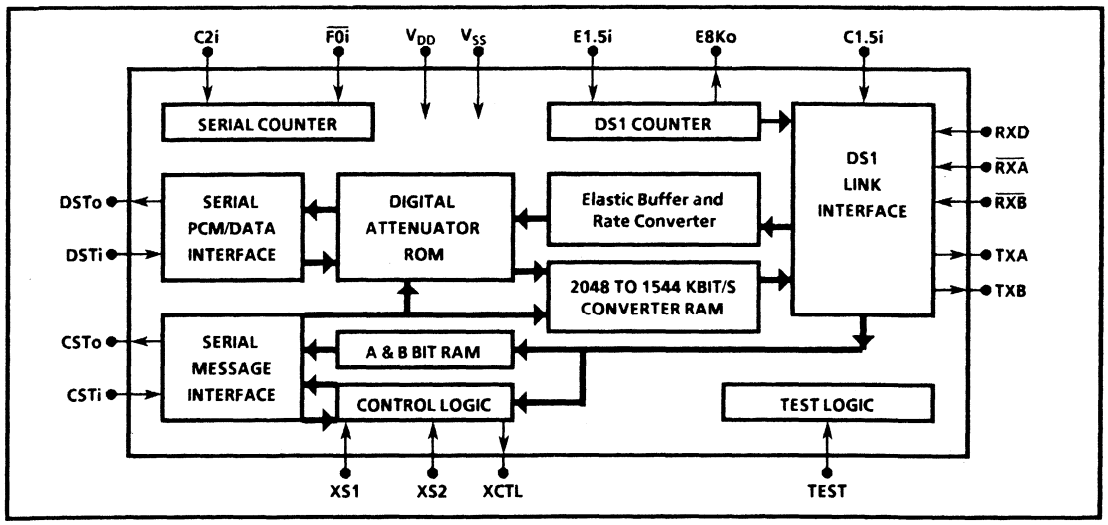


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7	V
2	Voltage at Digital Inputs	V_I	-0.3	V_{DD} + 0.3	V
3	Current at Digital Inputs	I_I		20	mA
4	Voltage at Digital Outputs	V_O	-0.3	V_{DD} + 0.3	V
5	Current at Digital Outputs	I_O		20	mA
6	Storage Temperature	T_{ST}	-65	150	°C
7	Power Dissipation	P		800	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		85	°C	
2	Supply Voltage	V_{DD}	4.5	5	5.5	V	
3	Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Power Dissipation	P		31.5	82.5	mW	Outputs unloaded
2	Supply Current	I_{DD}		6.3	15	mA	Outputs unloaded
3	Input High Voltage	V_{IH}	2.0		V_{DD}	V	
4	Input Low Voltage	V_{IL}	0		0.8	V	
5	Input Leakage	I_{IL}		1	10	µA	
6	Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = 10 mA @ V_{OH} = 2.4V
7	Output High Current	I_{OH}	8	16		mA	Source. V_{OH} = 3.0 V
8	Output Low Voltage	V_{OL}	V_{SS}		0.4	V	I_{OL} = 2 mA @ V_{OH} = 0.4V
9	Output Low Current	I_{OL}	2	10		mA	Sink. V_{OL} = 2.0 V
10	High Impedance Leakage	I_{OZ}		1	10	uA	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Capacitances

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Pin Capacitance	C_I		8		pF	
2	Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figures 2 & 3)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C2i Period	t_{P20}	400	488	600	ns	
2	C2i Width High or Low	t_{W20}	200	244	300	ns	
3	C2i Transition Time	t_{T20}		20		ns	
4	Frame Pulse Set Up Time*	t_{FPS}	50	10		ns	
5	Frame Pulse Hold Time*	t_{FPH}	50	10		ns	
6	Frame Pulse Width*	t_{FPW}	100	244		ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Frame pulse is repeated every 125 µs in synchronisation with the clock.

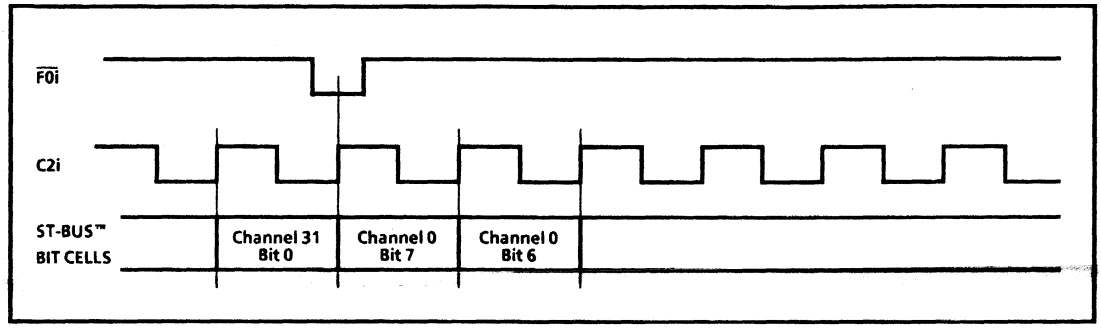


Figure 2 - Clock & Frame Alignment for 2048 kbit/s ST-BUS™ Streams

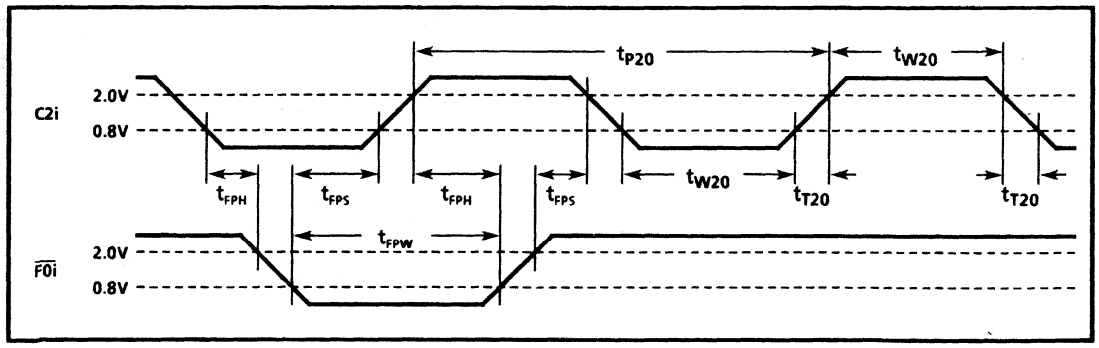


Figure 3 - Clock & Frame Timing for 2048 kbit/s ST-BUS™ Streams

AC Electrical Characteristics† - Clock Timing (Figures 2 & 3)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C1.5i Period	t_{P15}	500	648	800	ns	
2	C1.5i Width High or Low	t_{W15}	200	324	400	ns	
3	C1.5i Transition Time	t_{T15}		20		ns	
4	C1.5i Set Up Time	t_{S15}	50	-20		ns	
5	C1.5i Hold Time	t_{H15}	100	25		ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
NB: C1.5i must be locked to C2i so that 193 periods of C1.5i correspond to 256 periods of C2i.

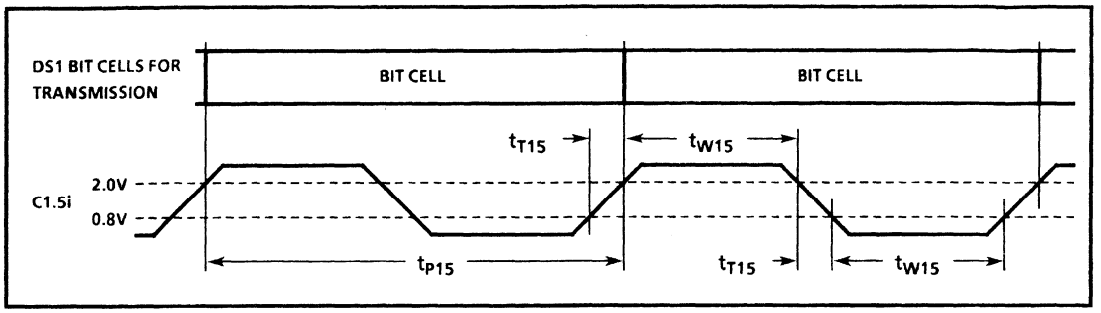


Figure 4 - Timing of DS1 Transmit Clock

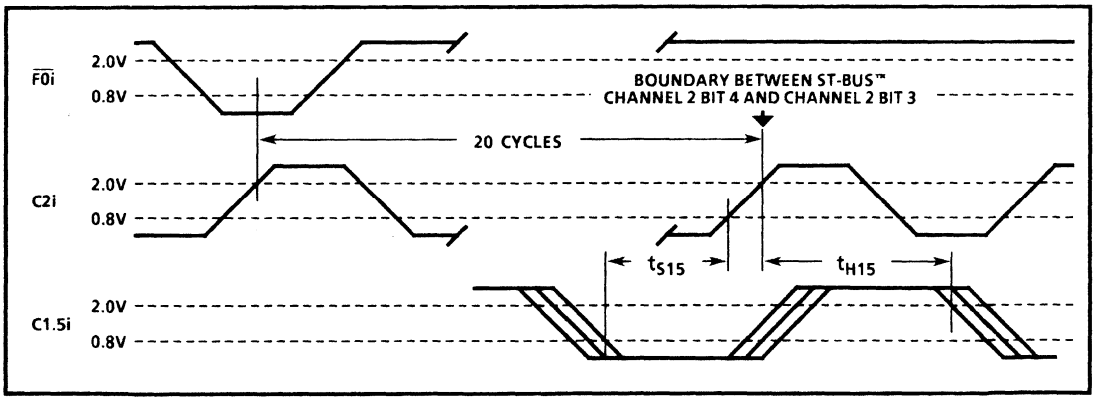


Figure 5 - Synchronisation of DS1 Transmit Clock to C2i

AC Electrical Characteristics† - Timing for Receive DS1 Clock (Figure 6)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	E1.5i Period	t_{PEC}	500	648	800	ns	
2	E1.5i Width High or Low	t_{WEC}	200	324	400	ns	
3	E1.5i Transition Time	t_{TEC}		20		ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

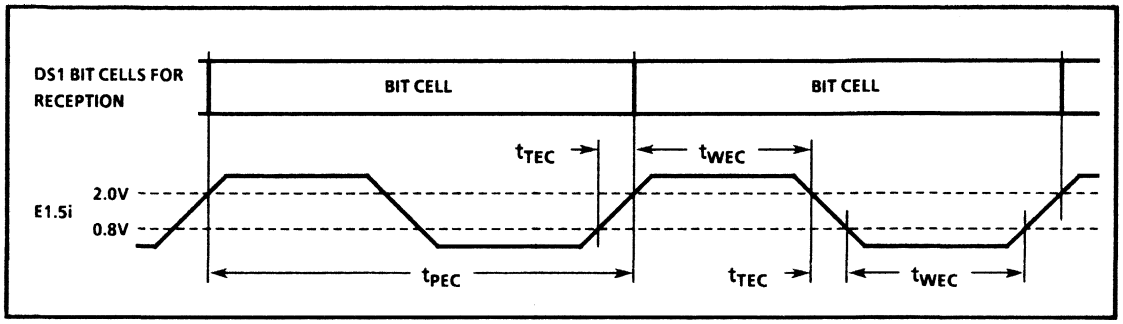


Figure 6 - Timing of DS1 Receive Clock

AC Electrical Characteristics† - 2048 kbit/s ST-BUS™ Streams (Figure 7)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Serial Output Delay	t_{SOD}		35	125	ns	150 pF load
2	Serial Input Set-Up Time	t_{SIS}	30	0		ns	
3	Serial Input Hold Time	t_{SIH}	90	10		ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

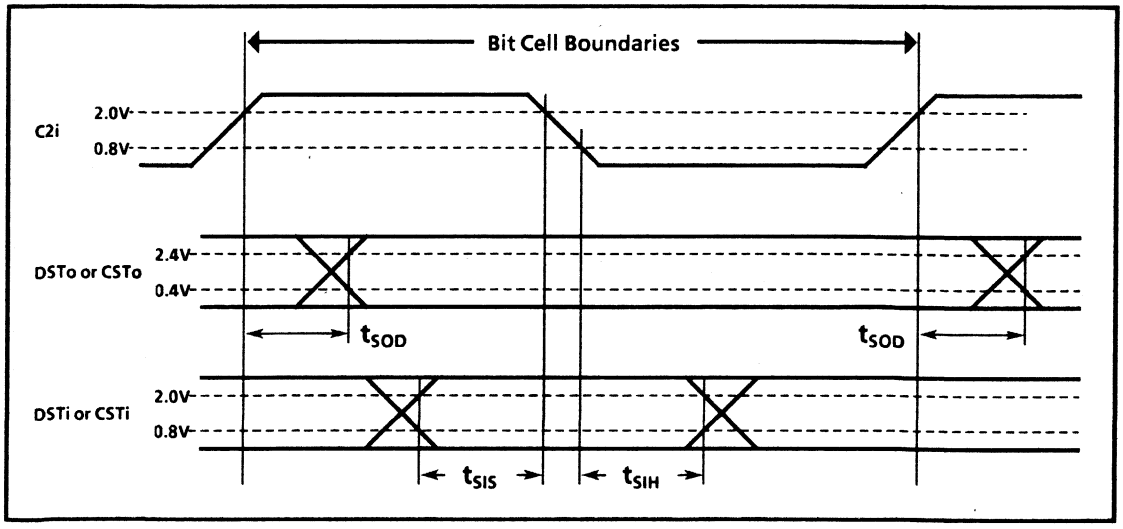


Figure 7 - 2048 kbit/s ST-BUS™ Streams

AC Electrical Characteristics† - Clock Timing (Figures 8, 9 & 10)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	External Control Delay	t_{XCD}		50	100	ns	50 pF load
2	External Status Set-Up Time	t_{XSS}	100	50		ns	
3	External Status Hold Time	t_{XSH}	100	10		ns	
4	E8Ko Output Delay	t_{8OD}		50	100	ns	50 pF load
5	E8Ko Output Low Width	t_{8OL}		77.7		µs	50 pF load
6	E8Ko Output High Width	t_{8OH}		47.3		µs	50 pF load
7	E8Ko Output Transition Time	t_{8OT}		5	20	ns	50 pF load

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

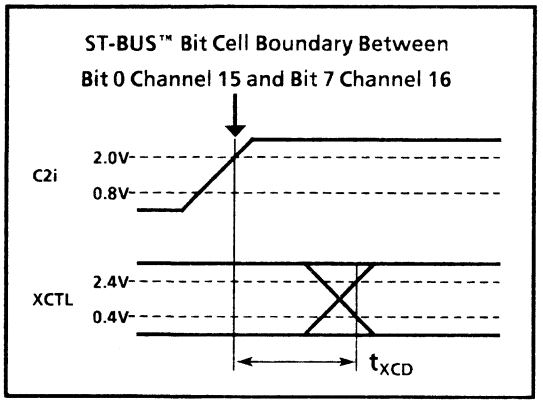


Figure 8 - XCTL Timing

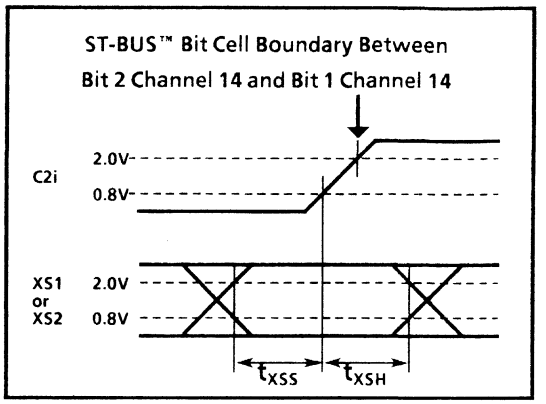


Figure 9 - XS1 & XS2 Timing

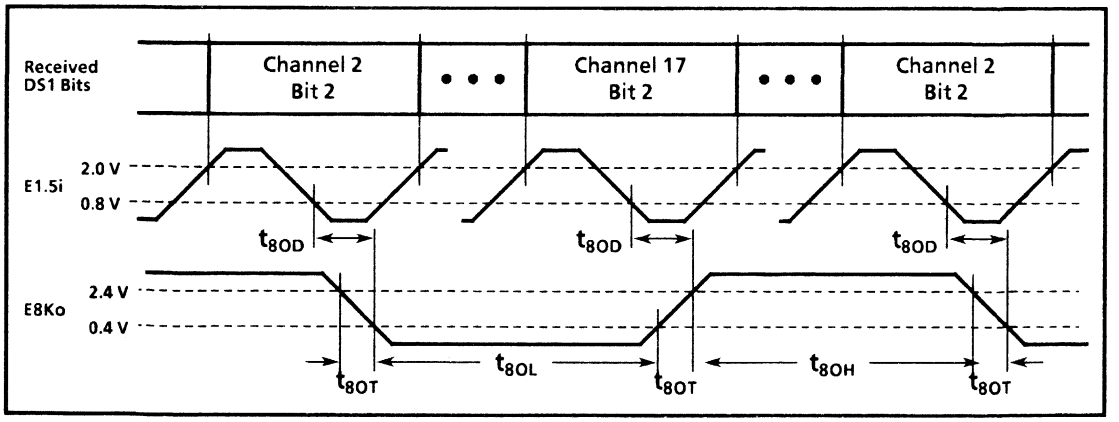


Figure 10 - E8Ko Timing

AC Electrical Characteristics† - Clock Timing (Figures 11 & 12)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit Steering Delay*	t_{TSD}		30	150	ns	200 pF load.
2	Receive Data Set-Up Time	t_{RDS}	30			ns	
3	Receive Data Hold Time	t_{RDH}	40			ns	
4	Receive Steering Set-Up Time	t_{RSS}	30			ns	
5	Receive Steering Hold Time	t_{RSH}	40			ns	
6	Transmit Steering Transition Time	t_{TST}		5	20	ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* The difference between t_{TSD} for TXA and TXB is typically 20 ns.

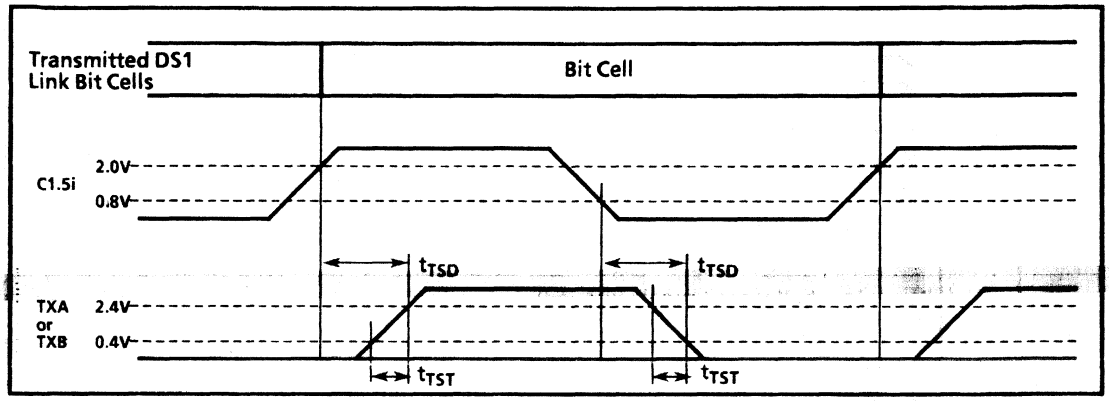


Figure 11 - Transmit Timing for DS1 Link

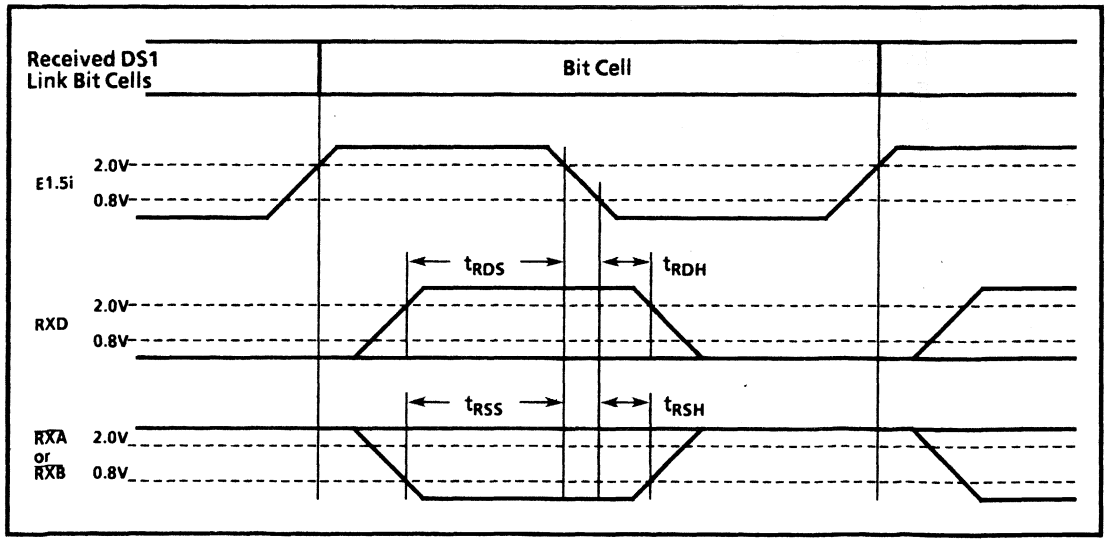


Figure 12 - Receive Timing for DS1 Link

Pin Description

Pin #	Name	Description
1	DSTo	**Data ST-BUS™ Out (Output).** This pin outputs a 2048 kbit/s ST-BUS™ stream. The data received on the DS1 link is stripped of S alignment bits and is presented on 24 of the 32 channels output on this pin.
2	IC	Internal connection, tie to VSS for normal operation.
3	RXD	**Receive Data (Input).** This is the input for the data received on the DS1 link. It should be high if the received link signal is sensed to be non-zero.
4 /5	$\overline{\text{RXA}}$ / $\overline{\text{RXB}}$	**Receive A & B (Inputs).** Split phase unipolar inputs used to sense bipolar violation and zero code on the AMI-coded DS1 link. These signals are NANDed externally to produce RXD.
6	DSTi	**Data ST-BUS™ In (Input).** This is the input for the 2048 kbit/s ST-BUS™ stream which contains the 24 acive PCM or data channels for transmission on the DS1 link.
7	CSTi	**Control ST-BUS™ In (Input).** This is the input for the 2048 kbit/s ST-BUS™ stream which controls the chip and contains the per channel control information.
8	E1.5i	**Extracted 1.544 MHz (Input).** A 1.544 MHz extracted clock input used to sample the received data. This clock should be derived from the receive data and must be phase aligned in order to sample RXD in the center of the bit pulse.
9	XCTL	**External Control (Output).** An uncommited external contol output which reflects the data found on bit 3 of channel 15 of the CSTi control stream.
10	VSS	**Power Input.** Negative supply (ground).
11	E8Ko	**Extracted 8 kHz (Three-state Output).** This output optionally provides an 8kHz clock derived by dividing the E1.5i extracted clock by 193. Bit 4 channel 15 of the ST-BUS™ input control stream (CSTi) determines whether this output is active or in a high impedance state.
12	CSTo	**Control ST-BUS™ Out (Output).** This pin outputs a 2048 kbit/s ST-BUS™ stream which contains the signalling and status information.
13	C2i	**2.048 MHz Clock (Input).** This is the input to the counter for the 2048 kbit/s ST-BUS™ streams.
14 /15	XS2 / XS1	**External Status 2 / 1 (Inputs).** Data presented on these inputs is transmitted as bits on channel 15 on CSTo.
16	$\overline{\text{F0i}}$	**Frame Pulse (Input).** This is the input for the frame synchronization pulse for the 2048 kbit/s ST-BUS™ streams. A low on this input indicates the start of a frame.
17	C1.5i	**1.544 MHz Clock (Input).** 1.544 MHz clock input phase locked to C2i. This clock controls the transmission rate at the DS1 link interface.
18 /19	TXB / TXA	**Transmit A & B (Output).** Split phase unipolar outputs which are used to steer the bipolar line driver.
20	VDD	**Power Input.** Positive supply.

Functional Description

The MT8975 provides an interface between a bidirectional DS1 link and 2048 kbit/s ST-BUS™ streams used for PCM/Data and control.

The serial PCM voice or data arriving at the DSTi input is converted to 8 bit bytes at the Serial PCM/Data Interface. Each channel can be digitally attenuated before signalling and synchronisation bits are inserted according to the DS1 format. The data is AMI [Alternate Mark Inversion] coded with selectable replacement of sequences of 8 zero bits with an zero suppression code.The bipolar steering for the line driver is output on TXA and TXB at 1544 kbit/s.

Data arriving on the DS1 link is examined for bipolar violations and zero suppression code. The A & B signalling bits are tapped off and the data is passed through a two frame elastic buffer. This buffer will also perform the 1544 kbit/s to 2048 kbit/s conversion. The output of this RAM may be digitally attenuated before it emerges on the 24 active channels on the DSTo pin.

The tapped A & B signalling bits are buffered and debounced before they are merged with status information. The combined signalling and status data emerges on the CSTo ST-BUS™ output. The status part of this bus contains bits representing the state of the XS1 and XS2 pins.

The CSTi ST-BUS™ input is used to provide the A & B bits for transmission on the DS1 link. It also controls independent PCM/Data channels and the XCTL pin.

The E8Ko pin provides a clock with a period corresponding to 193 cycles of the extracted E1.5i clock. This period is equivalent to the time taken for a frame of 24 channels plus the S-bit to arrive on the DS1 link. The pin can be used to synchronise the DS1 and ST-BUS™ systems.

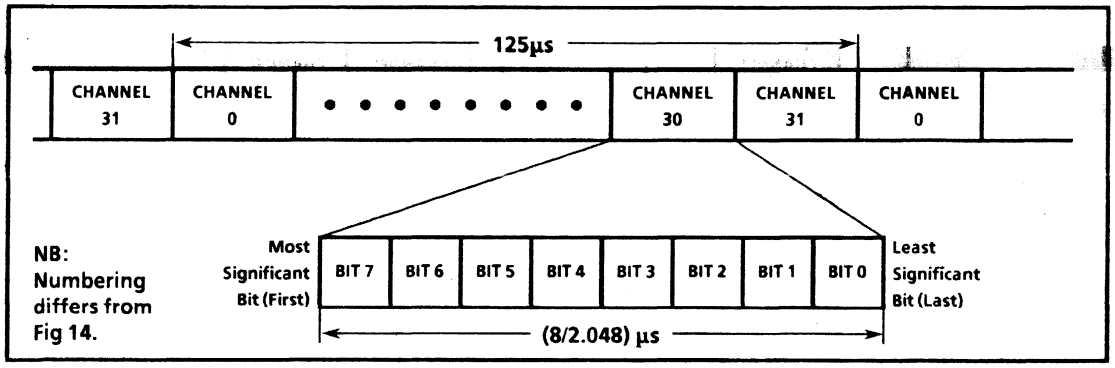


Figure 13 - Format of 2048 kbit/s ST-BUS™ Streams

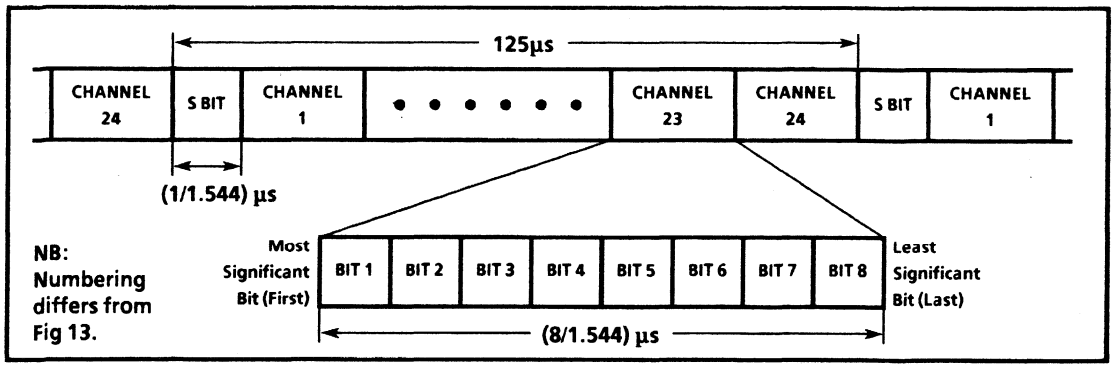


Figure 14 - DS1 Link Frame Format

Frame Formats

The ST-BUS™ streams consist of frames of 32 channels, numbered from 0 to 31, each containing 8 bits numbered from 7 to 0. The first bit in each frame is bit 7 of channel 0 and frames are 125 µs long (see Figure 13).

Frames on the DS1 link are also 125 µs long but are formatted differently (see Figure 14) and sequences of 12 frames are grouped together to form multiframes (see Figure 15). The first bit in each frame is the S-bit which carries a signal defining the position of the frame in the multiframe. Following the S-bit there are 24 channels, numbered 1 to 24, which contain 8 bits, numbered 1 to 8. The second bit in each frame is bit 1 of channel 1.

Bit 8 of every channel on frame 6 and 12 of each multiframe, contains the per-channel signalling information (see Figure 16). In frame 6 these bits are the A-bits and in frame 12 these are the B-bits. Each channel has an A-bit and B-bit which are each transmitted once every 1.5 ms.

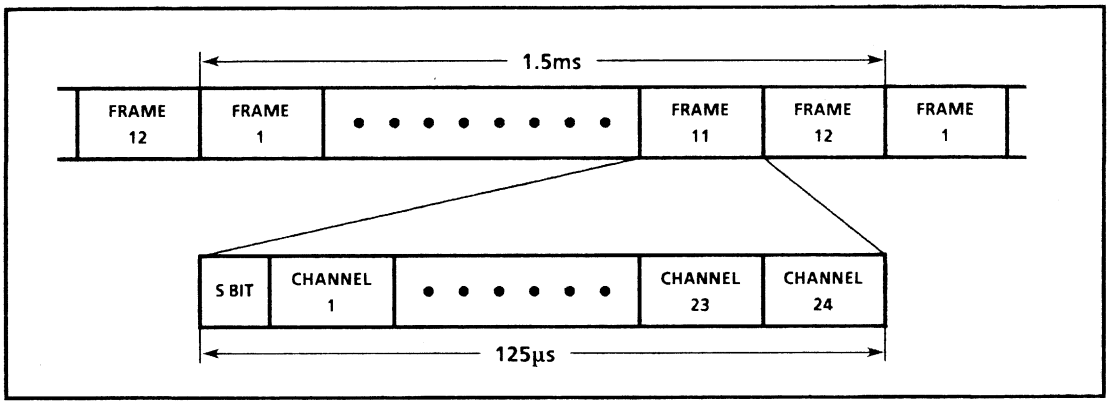


Figure 15 - DS1 Link Multiframe Format

FRAME NUMBER	S BIT		BIT NUMBERS IN CHANNELS		SIGNALLING CHANNEL
	Frame Alignment Signal	Multiframe Alignment Signal	Character Bits	Signalling Bits	
1	1		1-8		
2		0	1-8		
3	0		1-8		
4		0	1-8		
5	1		1-8		
6		1	1-7	8	A
7	0		1-8		
8		1	1-8		
9	1		1-8		
10		1	1-8		
11	0		1-8		
12		0	1-7	8	B

Figure 16 - Assignment of Alignment and Signalling Bits on DS1 Link Multiframe

DSTi	X				X				X				X				X				X				X				X			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

Figure 17 - Relationship Between Input DSTi Channels and Transmitted DS1 Channels
- X Denotes Unused DSTi Channels

DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24
DSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	X				X				X				X				X				X				X				X			

Figure 18 - Relationship Between Received DS1 Channels and Output DSTo Channels
- X Denotes Unused DSTo Channels

CSTi				N				N				N				C				N				N				N				N
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

Figure 19 - Relationship Between Input CSTi Channels and Controlled DS1 Channels
- N Denotes Null CSTi Channels (Must Contain Hex 00)
- C Denotes Master Control Channel

DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	
CSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
				X				X				X				S				X				X				X				X

Figure 20 - Relationship Between Received DS1 Channels and Output CSTo Channels
- X Denotes Unused CSTo Channels
- S Denotes Master Status Channel

BIT	NAME	DESCRIPTION
7	(unused)	
6	B8ZS	If 0 then Bit 7 of the DS1 carrier (the second last bit transmitted, corresponding to Bit 1 in the DSTi ST-BUS™) is jammed to 1 if all other bits of the channel on the DS1 carrier are 0. If 1 then all sequences of 8 zeros on data routed to the DS1 carrier are replaced by B8ZS code irrespective of channel boundaries or the presence of the S-bit in the 8 zeros. B8ZS code received from the DS1 carrier is always replaced by 8 zeros.
5	(unused)	
4	8KHZSEL	If 1 then the E8Ko pin is low for received DS1 channels 2 bit 2 to channel 17 bit 2 and high for channel 17 bit 2 to channel 2 bit 2. If 0 then the E8Ko pin is high impedance.
3	XCTL	The information at this location is output directly onto the XCTL pin once per frame.
2	NA	Keep at 0 for normal operation.
1	CCS	If 1 then bit stealing by A & B signalling bits is prevented. Valid PCM or data is transmitted on every channel of the DS1 carrier for all frames. If 0 then the A & B signalling bits which are input on PCM bits 1 & 0 of the appropriate CSTi channels are sampled during frames 6 and 12 replace PCM bit 0 of the DSTi channels for these frames.
0	ALARM	If 1 then bit 2 of every channel transmitted on the DS1 carrier is jammed to zero If 0 then bit 2 of the DS1 carrier behaves normally.

Figure 21 - Data Format on CSTi Channel 15 - Master Control

BIT	NAME	DESCRIPTION
7,6	RXPAD2,1	Per channel receive attenuation control bits RXPAD2 RXPAD1 Gain(dB) 0 0 0 0 1 -5 1 0 -3 1 1 -6
5,4,3	TXPAD4,2,1	Per channel transmit attenuation control bits TXPAD4 TXPAD2 TXPAD1 Gain(dB) 0 0 0 0 0 0 1 -4 0 1 0 -5 0 1 1 -1 1 0 0 -3 1 0 1 -2 1 1 0 -6 1 1 1 1
2	LOOP	When this bit is 1 the transmitted DS1 channel is looped internally to replace the corresponding received DS1 channel. Only a single DS1 channel may be looped at any one time.
1	TX A-BIT	This bit is sampled and output instead of bit 0 of the corresponding DSTI channel during frame 6 unless the CCS bit (bit 1 on CSTi channel 15) is 1.
0	TX B-BIT	This bit is sampled and output instead of bit 0 of the corresponding DSTI channel during frame 12 unless the CCS bit (bit 1 on CSTi channel 15) is 1.

Figure 22 - Data Format on CSTi Channels used for Controlling Channels on the DS1 Link

Monitoring and Control

Only 24 of the 32 channels on the 2048 kbit/s ST-BUS™ stream which is input on the DSTi pin are transmitted on the DS1 link. Figure 17 shows the correspondence between the channels on DSTi and on the DS1 link.

The 24 channels received on the DS1 link are output on 24 of the 32 channels of the 2048 kbit/s ST-BUS™ stream at DSTo. The correspondence between these channels is shown in Figure 18.

The 2048 kbit/s ST-BUS™ stream which is input on the CSTi pin controls both the general features of the chip and the specific features for individual channels. Status information for both the chip and for individual channels is output on the 2048 kbit/s ST-BUS™ stream at CSTo.

Figure 19 shows the way channels on CSTi are assigned. Channel 15 on CSTi is used to control the general features of the chip. The way in which the individual bits on this channel are used is shown in Figure 21. The remaining channels on CSTi are used to control the specific features for individual channels as shown in Figure 22. This control information is always input to the chip one channel before the corresponding channel on DSTi or DSTo.

Channels on CSTo are assigned in a similar way to channels on CSTi (see Figure 20). Channel 15 of CSTo gives the general status of the chip. The information presented on individual bits in this channel is given in Figure 23 . The A-bit and the B-bit signalling information is output on 24 of the remaining channels as shown in Figure 24. Like the control information, the status information is one channel ahead of the corresponding channel on DSTo.

BIT	NAME	DESCRIPTION
7-6	(unused)	
5	XS2	This bit contains the data sampled at the XS2 pin once per frame.
4	XS1	This bit contains the data sampled at the XS1 pin once per frame.
3	RX0	This bit goes to 1 when the alarm condition is detected for 576 ms on the received DS1 link (i.e. bit 2 of every received channel is zero) and returns to 0 after the alarm condition is removed for 192 ms.
2	BPV	This bit changes state after 256 bipolar violations (other than B8ZS code) have been detected on the received DS1 link in a sample period of 96 ms.
1	SLIP	This bit changes state after a slip between the received DS1 link and the DSTo ST-BUS™ stream has been detected.
0	$\overline{\text{SYN}}$	This bit goes to 1 when synchronisation to the received DS1 link is lost and returns to 0 once synchronisation is regained.

Figure 23 - Data Format on CSTo Channel 15 - Master Status

BIT	NAME	DESCRIPTION
7-2	(unused)	
1	RX A-BIT	This bit is the A signalling bit from the DS1 carrier after it has been debounced for 7.5 ms to 9 ms.
0	RX B-BIT	This bit is the B signalling bit from the DS1 carrier after it has been debounced for 7.5 ms to 9 ms.

Figure 24 - Data Format on CSTo Channels used for Monitoring Channels on the DS1 Link

Notes

ST-BUS™ FAMILY MH89750

DS-1/T1 Digital Trunk Interface

Preliminary Information

9161-002-020 NA ISSUE 3 AUGUST 1986

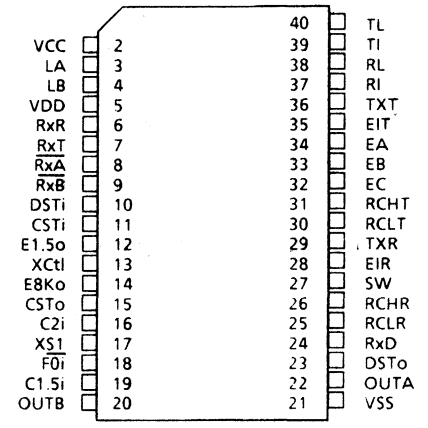
Features

- MITEL ST-BUS compatible
- Interface between a 2048 kb/s,(ST-BUS), serial data stream and a bidirectional DS1 link
- Robbed bit signalling or clear channel capabilities
- Insertion and detection of S bit
- Selectable B8ZS/Jammed bit Zero code replacement
- AMI encoding and decoding
- Per channel control
- Programmable digital attenuation
- 1.544 Mhz clock extraction from received line
- Three line equalization circuits for direct drive of 0-150 ft, 150-450 ft, 450-750 ft, plus a 6dB pad
- 2 Frame elastic buffering
- One uncommitted scan point and drive point
- Compatible with AT&T T.A. #34

Applications

- High speed data link using DS1 transmission link
- PBX or computer to DS1 interface

Pin Connections



Ordering Information

MH89750 40 pin DIL Hybrid Module
0°C to 70°C

Description

The MH89750 provides a complete interface between 2048 kb/s (ST-BUS) serial data and a 1544 kb/s bidirectional DS1 link. In a 2048 kb/s TDM system this thick film hybrid module converts the 24 active channels to a 24 channel 1544 kb/s DS1 format.

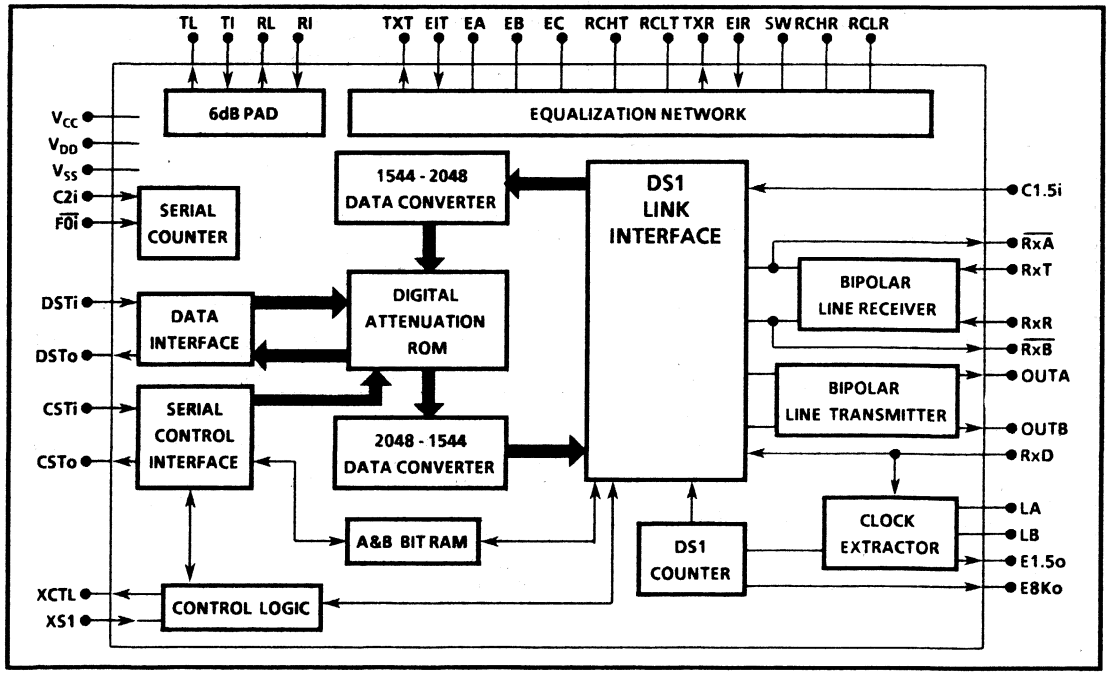


Figure 1. Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power Supplies With respect to V_{SS}	V_{CC}	-.3	15	V
		V_{DD}	-.3	7	V
2	Voltage on any pin other than supplies and OUTA or OUTB		V_{SS}-0.3	V_{DD} + 0.3	V
3	Voltage on OUTA or OUTB			15	V
4	Current at any pin other than OUTA OUTB and supplies			20	mA
5	Current at OUTA and OUTB			200	mA
6	Storage Temperature	T_{ST}	-20	85	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Inputs	Operating Temperature	T_{OP}	0		70	°C	
2		Power Supplies	V_{CC}	11.4	12	12.6	V	
			V_{DD}	4.5	5.0	5.5	V	
3		Input High Voltage	V_{IH}	2.4		V_{DD}	V	Digital Inputs
			V_{IH}		3.0		V	Line Inputs
4		Input Low Voltage	V_{IL}	V_{SS}		0.4	V	Digital Inputs
			V_{IL}		0.3		V	Line Inputs

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Clocked operation over recommended temperature ranges

		Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Inputs	Supply Current	I_{CC}		10	20	mA	Outputs Unloaded
			I_{DD}		15	30	mA	Outputs Unloaded
2		Input High Voltage	V_{IH}	2.0			V	Digital Inputs
3		Input Low Voltage	V_{IL}			0.8	V	Digital Inputs
4		Input Leakage Current	I_{IL}		± 1	± 10	µA	Digital Inputs V_{IN} = 0to V_{DD}
5	Outputs	Output High Voltage Digital	V_{OH}	2.4			V	I_{OL} = 10mA
6		Output High Leakage	I_{OL}			500	nA	
7		Output High Current Digital Except E1544	I_{OH}	10	20		mA	Source Current V_{OH} = 2.4V
			I_{OH}	8	16		mA	Source Current V_{OH} = 3.0V
8		Output Low Voltage Digital	V_{OL}			0.4	V	I_{OL} = 2mA
		OUTA or OUTB	V_{OL}			.25	V	I_{OL} = 10mA
9		Output Low Current Digital	I_{OL}	2	10		mA	Sink Current V_{OL} = 0.4V
		Except E1544	I_{OL}	6	30		mA	Sink Current V_{OL} = 2.0V
10		Input Impedance RxT to RxR	Z_{IN}		400		Ω	
		RxT or RxR to Gnd			1K		Ω	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Functional Timing Diagrams

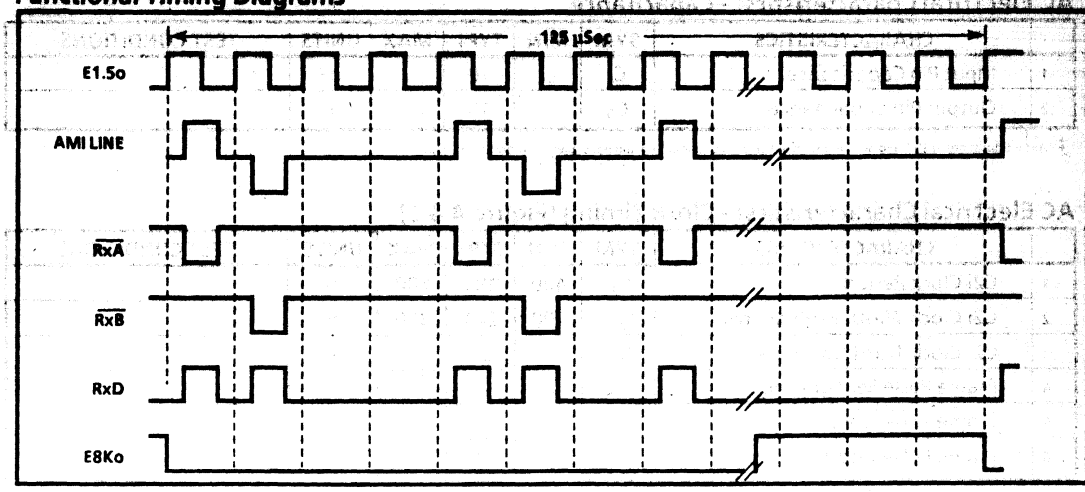


Figure 2. DS1 Receive

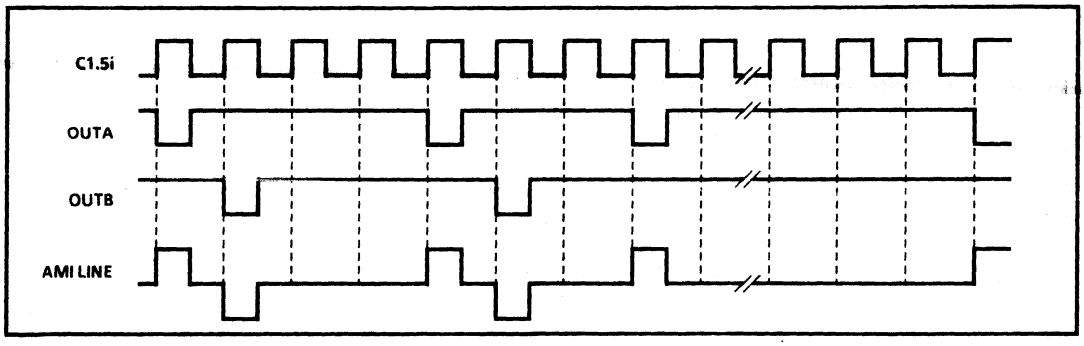


Figure 2a. DS1Transmit

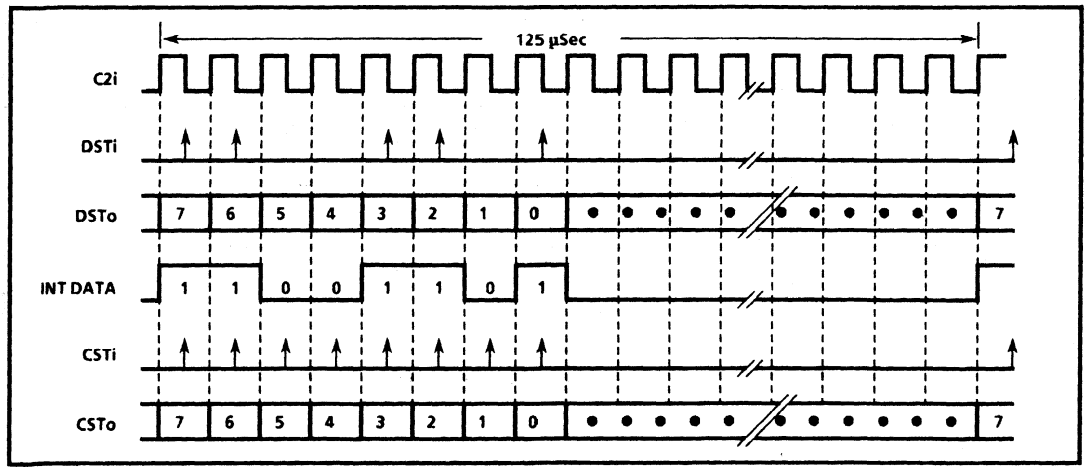


Figure 3. ST-BUS

AC Electrical Characteristics† - Capacitance

	CHARACTERISTICS	SYM	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS
1	Input Pin Capacitance	C_I		10		pF	
2	Output Pin Capacitance	C_O		10		pF	

‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figure 4 & 5)

	CHARACTERISTICS	SYM	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS
1	C2i Clock Period	t_{P20}	400	488	600	ns	
2	C2i Clock Width High or Low	t_{W20}	200	244	300	ns	
3	C2i Clock Transition Time	t_{T20}		20		ns	
4	Frame Pulse Set Up Time	t_{FPS}	50			ns	
5	Frame Pulse Hold Time	t_{FPH}	50			ns	
6	Frame Pulse Width	t_{FPW}		244		ns	

NB: Frame pulse is repeated every 125 in synchronization with the clock.
†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

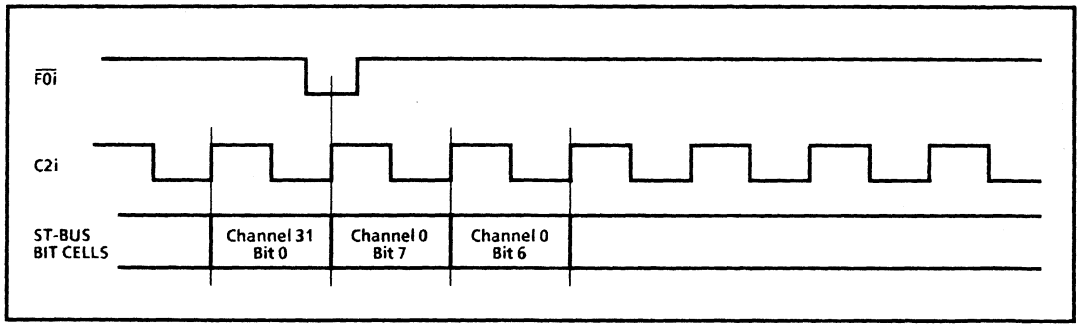


Figure 4. Clock & Frame Alignment for ST-BUS Streams

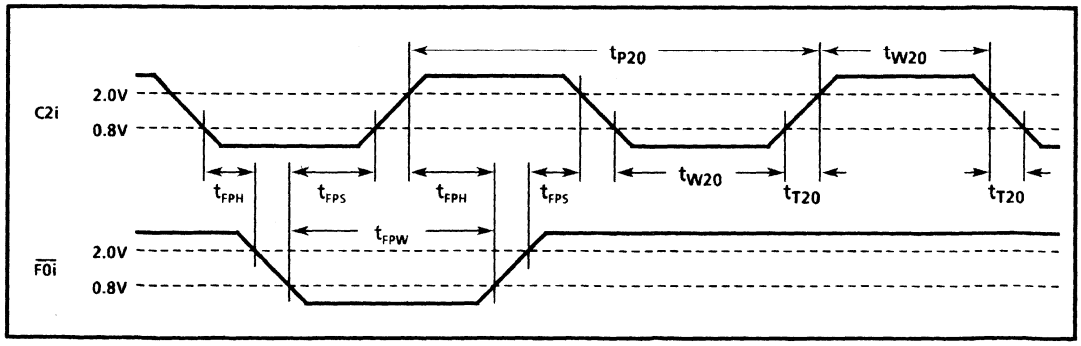


Figure 5. Clock & Frame Pulse Timing for ST-BUS Streams

AC Electrical Characteristics† - DS1 Transmit Clock (Figure 6 & 7)

	CHARACTERISTICS	SYM	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS
1	C1.5i Clock Period	t_{P15}		648		ns	
2	C1.5i Clock Width High or Low	t_{W15}		324		ns	
3	C1.5i Clock Transition Time	t_{T15}		20		ns	
4	C1.5i Clock Set Up Time	t_{S15}	20			ns	
5	C1.5i Clock Hold Time	t_{H15}	100			ns	

NB: C1544 must be locked to C2048 so that 193 periods of C1544 correspond to 256 periods of C2048.
†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

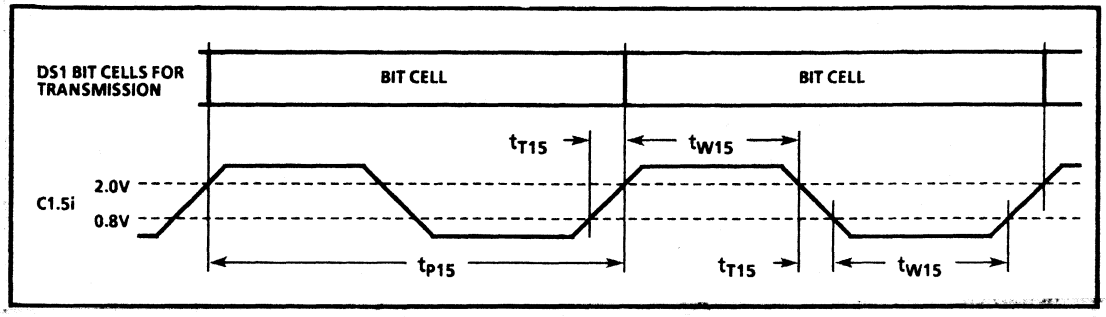


Figure 6. Timing of DS1 Transmit Clock

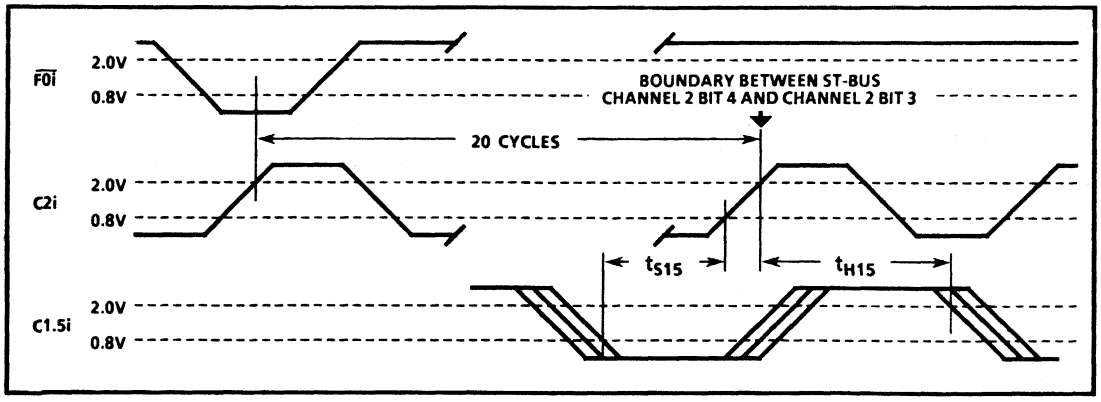


Figure 7. Synchronization of DS1 Transmit Clock C1.5i to C2i

AC Electrical Characteristicst - ST-BUS Streams (Figure 8)

	CHARACTERISTIC	SYM	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS
1	Serial Output Delay	t_{SOD}			125	ns	150pF load
2	Serial Input Set-Up Time	t_{SIS}	30			ns	
3	Serial Input Hold Time	t_{SIH}	90			ns	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

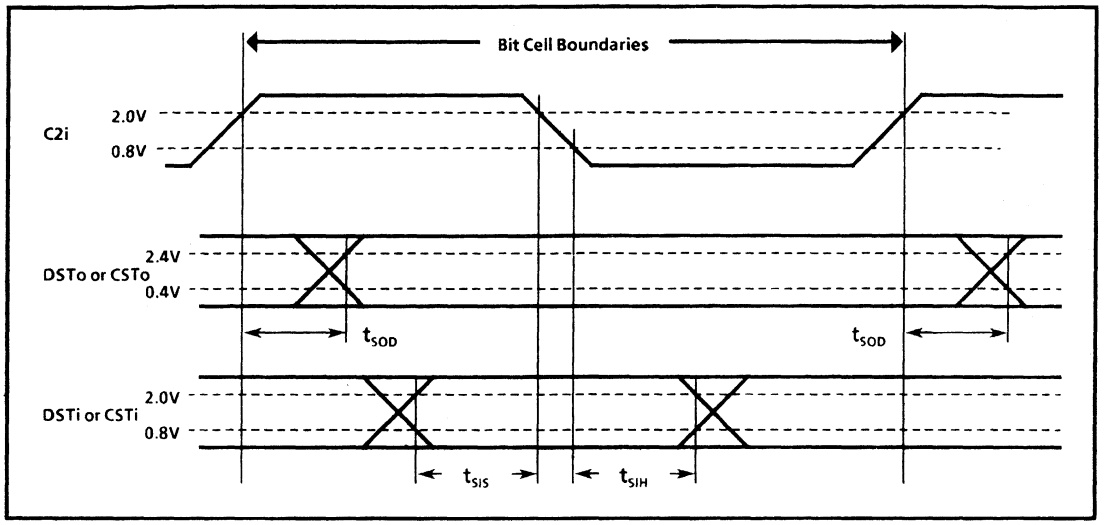


Figure 8. ST-BUS Streams

AC Electrical Characteristicst - Timing for Receive DS1 Clock (Figure 9)

	CHARACTERISTICS	SYM	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS
1	E1.5o Clock Period	t_{PEC}		648		ns	
2	E1.5o Clock Width High or Low	t_{WEC}		324		ns	
3	E1.5o Clock Transition Time	t_{TEC}		20		ns	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

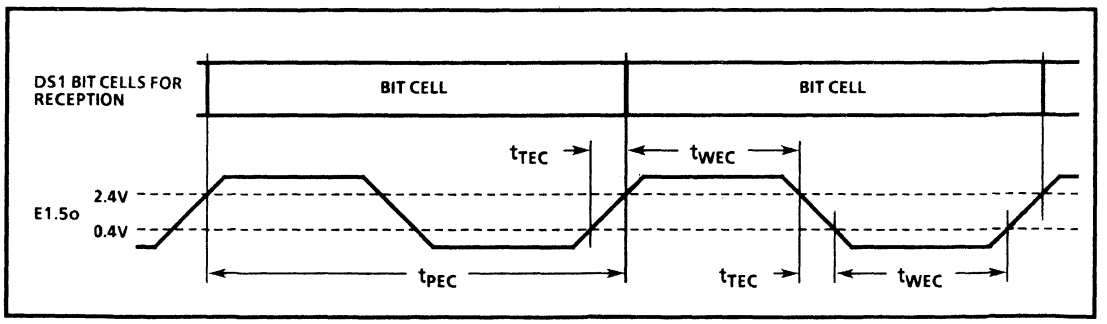


Figure 9. Timing of DS1 Receive Clock

AC Electrical Characteristics† - XCTL, XS1, & E8Ko(Figures 10, 11 & 12)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	External Control Delay	t_{XCD}	0	100		ns	50 pF load
2	External Status Set-Up Time	t_{XSS}		100		ns	
3	External Status Hold Time	t_{XSH}		100		ns	
4	E8Ko Output Delay	t_{8OD}	0	100		ns	50 pF load
5	E8Ko Output Low Width	t_{8OL}		77.7		µs	50 pF load
6	E8Ko Output High Width	t_{8OH}		47.3		µs	50 pF load
7	E8Ko Output Rise Time	t_{8OR}		20		ns	50 pF load
8	E8Ko Output Fall Time	t_{8OF}		20		ns	50 pF load

† Timing is over recommended temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

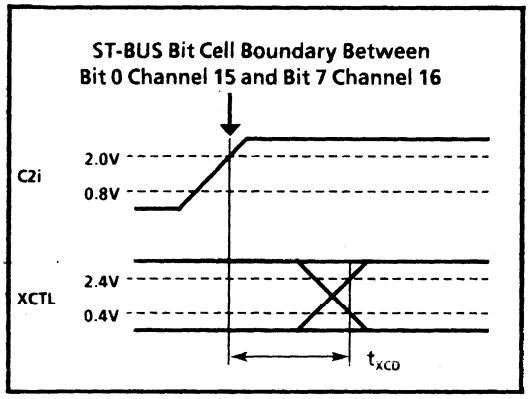


Figure 10. XCTL Timing

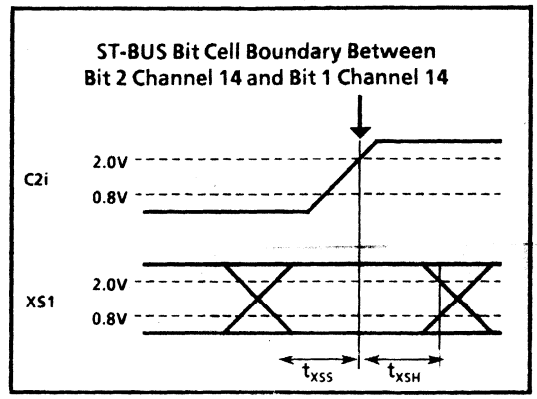


Figure 11. XS1 Timing

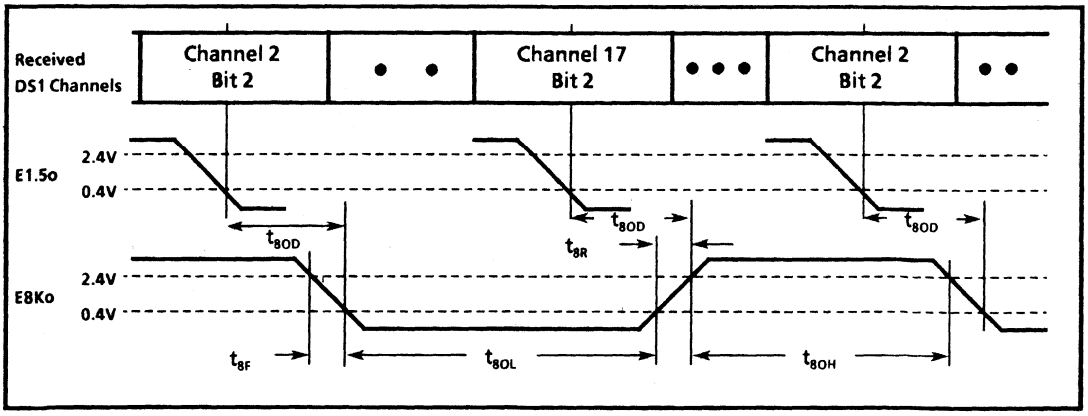


Figure 12. 8KHZ Timing

AC Electrical Characteristics† - DS1 Link Timing (Figure 13 & 14)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit Steering Delay	t_{TSD}	0	150		ns	See Figure 15
2	Received Data Delay	t_{RDD}			100	ns	
3	Received Data Rise Time	t_{RDR}		20		ns	See Figure 16
4	Received Data Fall Time	t_{RDF}		20		ns	See Figure 16
5	Received Steering Rise Time	t_{RSR}		20		ns	
6	Received Steering Fall Time	t_{RSF}		20		ns	
7	Received Data Set-Up Time	t_{RDS}	100			ns	
8	Received Data Hold Time	t_{RDH}	100			ns	
9	Received Steering Pulse Width	t_{RSW}		324		ns	

Note: The difference between t_{TSD} for OUTA and OUTB is typically 20 ns.

†Timing is over recommended temperature & power supply voltage ranges.

‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

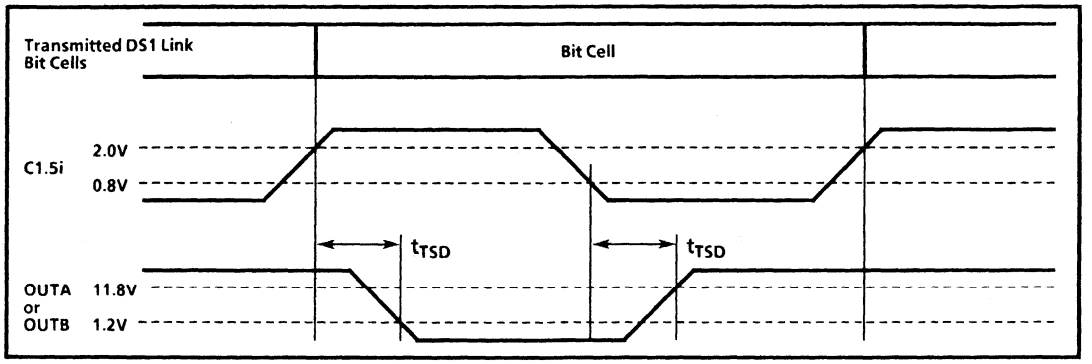


Figure 13. Transmit Timing for DS1 Link

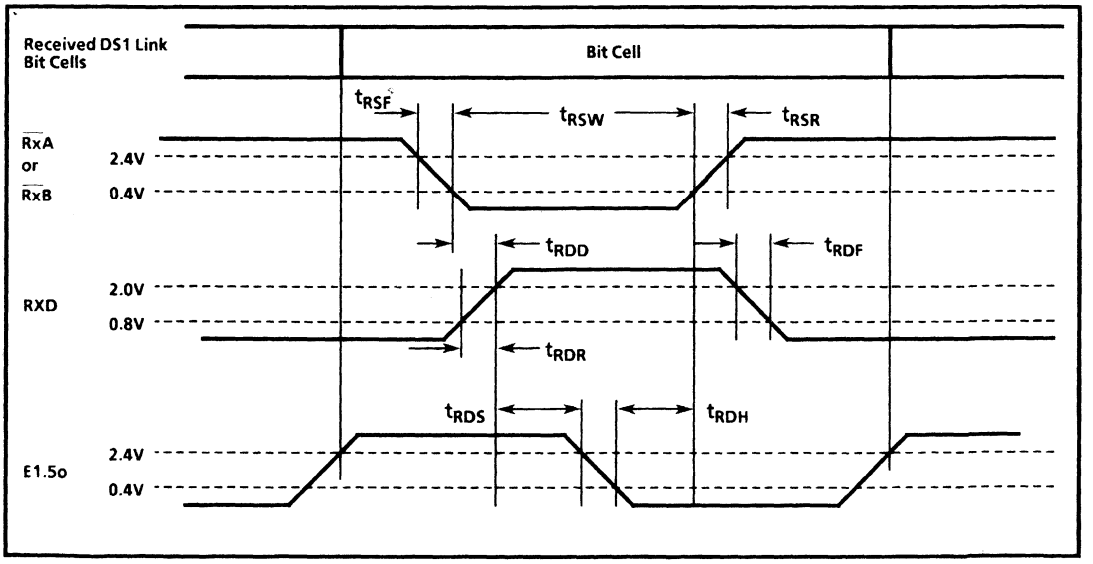


Figure 14. Receive Timing for DS1 Link*

***Note:** $\overline{RxA}$ and $\overline{RxB}$ are derived from RxT and RxR which must meet AT&T technical specification #34. The parameters t_{RDS} and t_{RDH} are related to device functionality. Network constraints may require tighter tolerances than the device specifications. The frequency of E1544 must be adjusted with the external inductor to meet the device and/or the network tolerances.

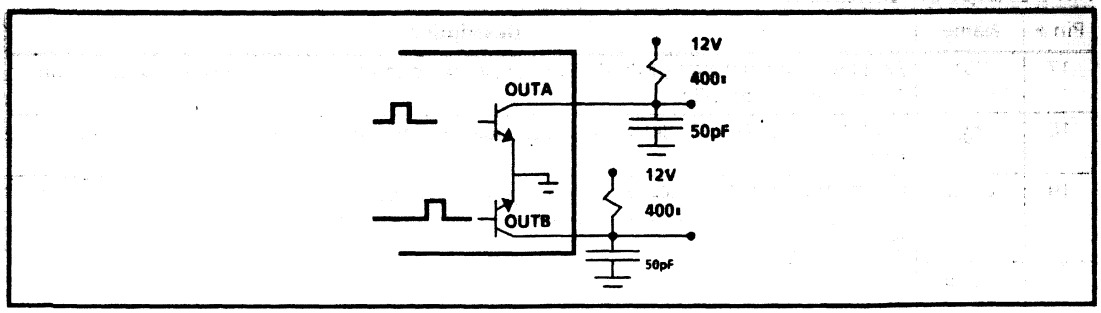


Figure 15. OUTA and OUTB Test Circuit

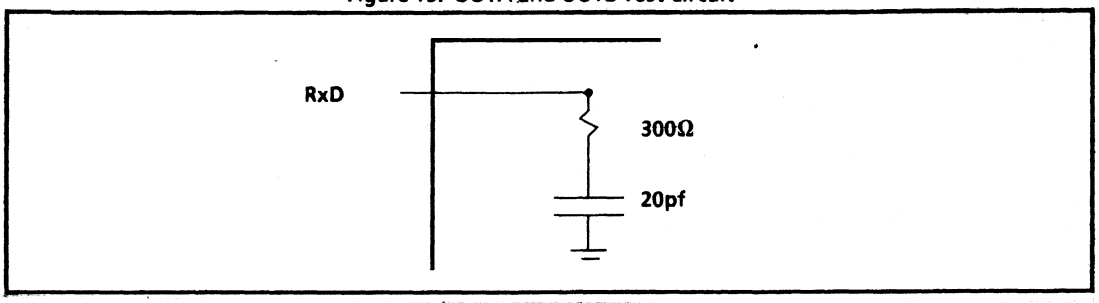


Figure 16. RxD Typical Equivalent Input Circuit

Pin Description

Pin #	Name	Description
2	V_{CC}	Analog power supply voltage.
3 4	LA LB	The external, manually controlled inductor is connected between these two pins to adjust the frequency of the extracted clock.
5	V_{DD}	Digital supply voltage.
6 7	RxR RxT	RECEIVE RING&TIP (INPUTS). Bipolar split phase inputs from the tip and ring leads of the input transformer. Impedance to Gnd = 1KΩ. Impedance between pins = 400Ω.
8 9	$\overline{RxA}$ $\overline{RxB}$	RECEIVE A& B (OUTPUTS). Decoded receive side unipolar split phase return to zero signals. These two signals are also inputs for the external NAND gate used to generate RxD.
10	DSTi	DATA ST-BUS (INPUT). A 32 channel (24 active) ST-BUS input data stream which contains the ingormation to be transmitted on the T1 line.
11	CSTi	CONTROL ST-BUS (INPUT). A 32 channel control ST-BUS input which contains the per channel control information as well as the DS1 line control.
12	E1.5o	EXTRACTED 1.544 MHz CLOCK (OUTPUT). A 1.544 MHz extracted clock output which is derived from the received data on the T1 line.
13	XCtl	EXTERNAL CONTROL (OUTPUT). An uncommittedexternal control output which reflects the dat found on bit 1 of channel 31 of the CSTi control stream.
14	E8Ko	8kHz (THREE-STATE OUTPUT). An output that can be used for office synchronization. It is enabled by bit 2 on channel 15 of CSTi, it is updated once per frame.
15	CSTo	CONTROL ST-BUS (OUTPUT). A 32 channel control output (24 active) that carries received signalling information and the DS1 interface status information (ST-BUS format).
16	C2i	MASTER CLOCK (INPUT). A 2.048 MHz system clock synchronized to the input frame pulse and is used to drive all the counters for the ST-BUS stream.

Pin Description Continued

Pin #	Name	Description
17	XS1	EXTERNAL SCAN POINT (INPUT). Data presented on this pin is sampled and output on bit 4 of channel 15 of CSTo.
18	$\overline{F0i}$	FRAME PULSE (INPUT). 8kHz 244 nsec. wide, used to indicate the start of a 32 channel frame.
19	C1.5i	DS1 CLOCK (INPUT). 1.544 Mhz clock input that is phase locked to C2i, ie: 193 cycles of C1.5i must correspond to 256 cycles of C2i. This is the transmission clock for the DS1 interface.
20	OUTB	OUTPUT A (OPEN COLLECTOR OUTPUT). The output of the transmit bipolar steering network.
21	V_{SS}	POWER INPUT. System ground.
22	OUTA	OUTPUT A (OUTPUT OPEN COLLECTOR). The output from the transmit bipolar steering network.
23	DSTo	DATA ST-BUS (OUTPUT). A 32 channel (24 active) ST-BUS data output stream which contains the information received on the T1/DS1 link.
24	RxD	RECEIVED DATA (INPUT) in a unipolar return to zero format. It is generated by gating $\overline{RxA}$ and $\overline{RxB}$ in an external NAND gate (see input circuit in Figure 16).
25 26	RCLR RCHR	EQUALIZER. These 2 pins are equalizer options on the ring leg of the equalizer.
27	SW	EQUALIZER SWITCH. The common switch point of the center leg of the equalizer.
28	EIR	EQUALIZER INPUT RING. The ring lead input to the equalizer. Input impedance between EIR and EIT is 100Ω.
29	TXR	EQUALIZER TRANSMIT RING. The ring lead output of the equalizer. Output impedance between TXR and TXT is 100Ω.
30 31	RCLT RCHT	EQUALIZER. These 2 pins are equalizer options on the tip leg of the equalizer.
32 33 34	EC EB EA	EQUALIZER. These 3 pins are three settings for the center leg of the equalizer, corresponding to the 0-150', 150-450', and the 450-750' equalizers.
35	EIT	EQUALIZER INPUT TIP. Input to the equalizer.
36	TXT	EQUALIZER TRANSMIT TIP. The tip lead output of the equalizer.
37	RI	RING IN (INPUT). The ring lead input to the 6 dB pad. The input impedance between RI and TI is 100Ω.
38	RL	RING LINE (OUTPUT). The ring lead output on the line side of the 6 dB pad. The output impedance between RL and TL is 100Ω.
39	TI	TIPIN (INPUT). The tip lead input to the 6 dB pad.
40	TL	TIP LINE (OUTPUT). The tip lead output on the line side of the 6 dB pad.

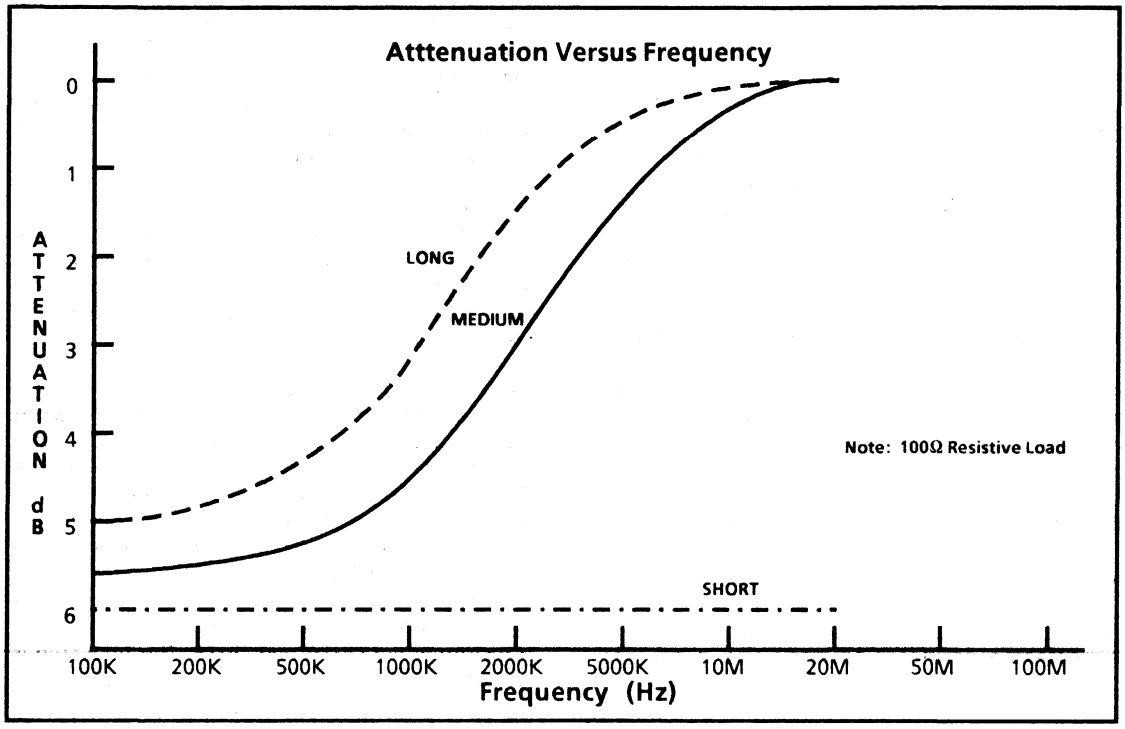


Figure 17a. Typical Frequency Response of the Equalizers

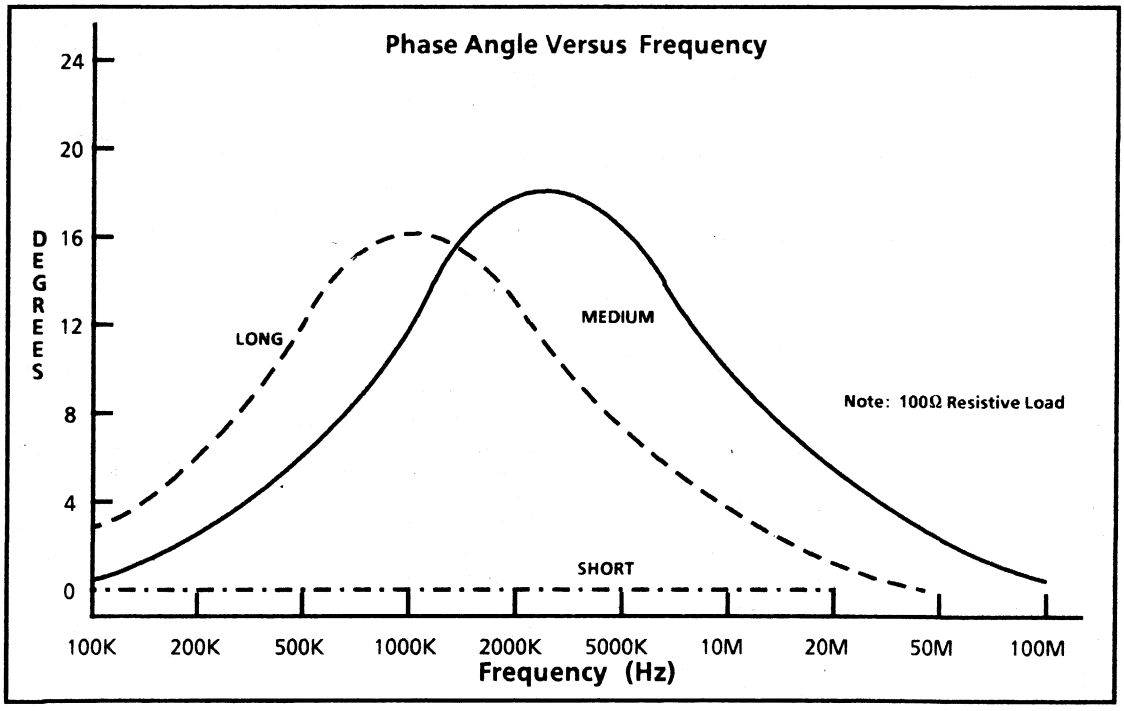


Figure 17b. Typical Phase Response of the Equalizers

FUNCTIONAL DESCRIPTION

The MH89750 is a T1 to 2048 kbit/s serial stream, (ST-BUS), interface. It does the conversion from the DS1 format on the T1 line to the ST-BUS format of the Data Interface, (DSTi, DSTo). The classical application for a device such as this is the transmission of Time Multiplexed Voice, but it is also applicable for data communication, such as a high speed serial data link between a PBX and a host computer, or a serial data link between two host computers.

Functions included on the MH89750 are software control over the operation of the interface, bipolar line receivers and transmitters, 2 frame of elastic store, controled slip, clock extraction from the received data, one uncommitted scan point and drive point for custom applications, and line equalization for driving up to 750 feet of twisted pair to the Line Terminating Equipment (LTE). The interface complies with AT&T Technical Advisory #34 at a distance of 650 feet, over 22 AWG cable.

The MH89750 inserts and deletes the S bit for the superframe format and does the data rate conversion between the 1544 kbit/s DS1 carrier and the 2048 kbit/s ST-BUS. It does the coding and decoding of the Alternate Mark Inversion (AMI) DS1 line and replaces or inserts information as specified by the Serial Control Interface (CSTi). The control interface has two functions. There is a master control word that initializes the DS1 interface and a control word for each of the DS1 channels. The master control word programs the DS1 link interface for B8ZS/Jammed bit zero code replacement, uncommitted external control output (XCTL), an 8kHz synchronized output (E8Ko), selects clear channel or A/B bit signalling and enables the transmission of the alarm state. Each individual channel has a control word that supplies digital attenuation information of + 1 to - 6 dB in 8 steps for transmit and 0 to -7 dB in 4 steps for receive on the DS1 interface, the A/B bits for insertion into the serial stream, if bit stealing has been selected by the master control word, and a loop around bit for each individual channel.

Status information from the MH89750 is provided via the Serial Control Interface (CSTo). This status information has two components. There is a master status word that supplies information on the operating condition of the interface, and the per channel status words. The master status word supplies the status of the uncommitted external scan point (XS1), of a bit to indicate that an alarm state has been received on the DS1 carrier, of the number of bipolar violations, of whether the DS1 carrier is synchronized, and of whether there has been a slip in the data received on the DS1 carrier. The per channel status word returns the value of the A&B bits received from the DS1 line after they have been debounced.

The data for transmission on the DS1 line interfaces with the device at DSTi and DSTo. The information is in ST-BUS format of 32 8-bit channels. This is the same format used by the serial control interface. Synchronization is done by an external 8 kHz frame pulse, ($\overline{F0i}$).

Data is input in ST-BUS format to the data interface. After the information is input at DSTi it is attenuated by the Digital Attenuation Rom. Next the data rate is converted to 1544 kbits/s by the 2048-1544 data converter. In the DS1 Interface each channel has the appropriate bits added, as specified by the serial control stream. It is now in DS1 format and ready to be AMI encoded by the bipolar line transmitter. The DS1 formatted signal is then output to an external line coupling transformer via OUTA and OUTB. The final step is to pass the signal through the line equalization best suited to the distance to the line terminating equipment.

Information arriving on the DS1 line is a 1544 kbit/s serial stream. It is divided into 24 8-bit channels plus an S bit. The S bit is patterned in such a way as to allow the identification of single frame and superframe sequences. The data arriving on the DS1 line at RxT and RxR passes through a two frame elastic buffer to the DS1 link interface. Data input on the DS1 side of the interface is output on DSTo in ST-BUS format.

ST-BUS Format

The ST-BUS is a 2048 kbit/s serial stream that is divided into 32 8-bit channels. Frame boundaries are determined by an external frame pulse with an 8 kHz period. The frame pulse must go low for approximately 1/2 a clock cycle once every 125 µsec. The next rising clock edge after frame pulse goes low marks the beginning of the ST-BUS frame. Figures 4 and 5 illustrate the relationship between Frame Pulse and the ST-BUS. The ST-BUS format is shown in Figure 18.

All of the network inputs and outputs are in the ST-BUS format, CSTi, CSTo, DSTi, and DSTo.

DS1 Format

Information on the DS1 line is a 1544 kbit/s serial stream. The DS1 format is 24 8-bit words plus an S bit. It should be noted from Figure 19 that the DS1 format numbers the channels starting with 1, instead of 0 as on the ST-BUS, and the bits are numbered 1 to 8 (MSB to LSB) instead of 7 to 0. Synchronization of the DS1 serial stream is done with the S bit that is embedded in the data stream.

By inserting a predefined pattern in the S bit position, (the first bit of the frame), two frame patterns can be defined. In this way the S bit defines the beginning of each frame and that frames position within a group of 12 frames called a superframe. Figure 20 shows the superframe format and Figure 21 shows the frame alignment signal and the superframe alignment signal and how they are inserted into the S bit position.

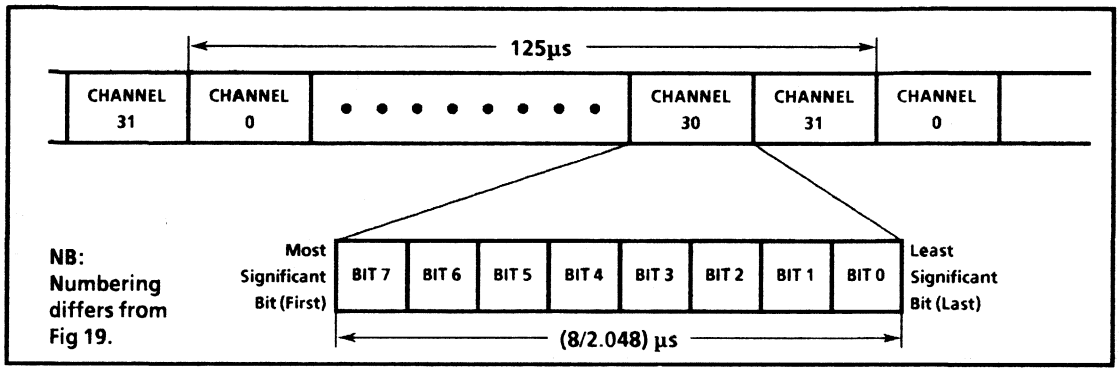


Figure 18. ST-BUS Format

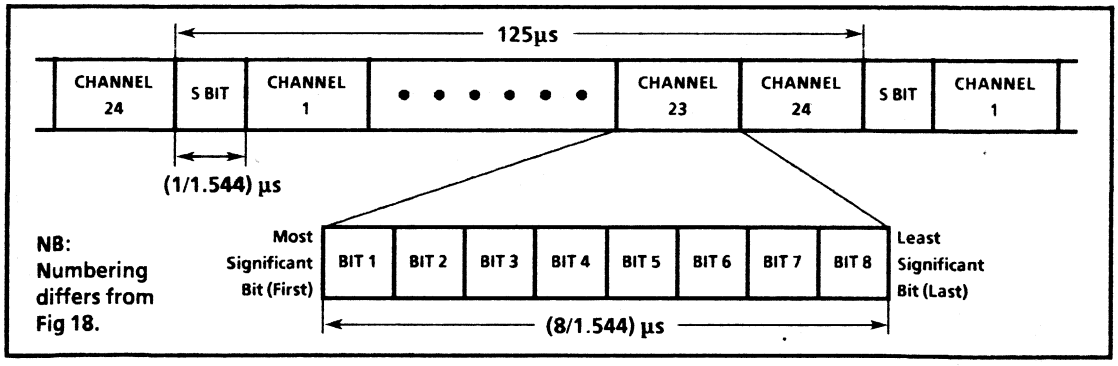


Figure 19. DS1 Frame Format

I/O Channel Configuration

The ST-BUS has 8 more channels than the T1 link, therefore only 24 ST-BUS channels can be transferred to the DS1 link. One out of every 4 DSTi channels is left empty. Figure 22 shows how the input of DSTi is configured and how the input channels relate to the transmitted DS1 channels. There are also only 24 valid channels in DSTo. The empty channels and how they relate to the received DS1 channels are illustrated in Figure 23.

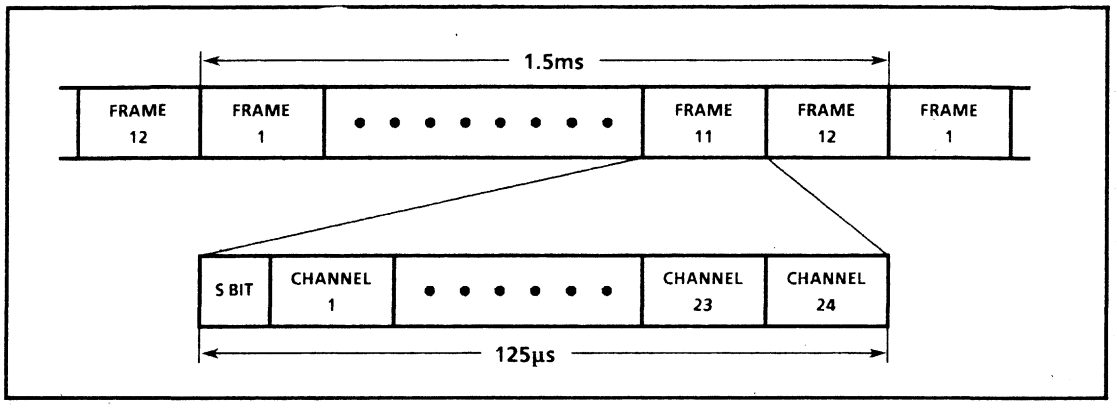


Figure 20. DS1 Link Superframe Format

FRAME NUMBER	S BIT		BIT NUMBERS IN CHANNELS		SIGNALLING CHANNEL
	Frame Alignment Signal	Multiframe Alignment Signal	Character Bits	Signalling Bit	
1	1		1-8		
2		0	1-8		
3	0		1-8		
4		0	1-8		
5	1		1-8		
6		1	1-7	8	A
7	0		1-8		
8		1	1-8		
9	1		1-8		
10		1	1-8		
11	0		1-8		
12		0	1-7	8	B

Figure 21. Assignment of Alignment and Signalling Bits on DS1 Superframe

DSTi	X				X				X				X				X				X				X				X			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

Figure 22. Relationship Between Input DSTi Channels and Transmitted DS1 Channels
- X Denotes Unused DSTi Channels
Note: Functional representation only

DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24
DSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	X				X				X				X				X				X				X				X			

Figure 23. Relationship Between Received DS1 Channels and Output DSTo Channels
- X Denotes Unused DSTo Channels
Note: Functional representation only

CSTi				X				X				X				C				X				X				X				X
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DSTi	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	0

Figure 24. Relationship Between Input CSTi Channels and Controlled DSTi Channels
- X Denotes Unused CSTi & DSTi Channels. Unused CSTi input channels must be set to $00
- C Denotes Master Control Channel
Note: Functional representation only

DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	
CSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
				X				X				X				S				X				X				X				X

Figure 25. Relationship Between Received DS1 Channels and Output CSTo Channels
- X Denotes Unused CSTo Channels
- S Denotes Master Status Channel
Note: Functional representation only

Serial Control

CSTi and CSTo are also ST-BUS format, but they have a different channel assignment from DSTi and DSTo. The control information for a DSTi channel must be input one channel before on the CSTi serial stream, ie: channel 0 of CSTi controls channel 1 of DSTi (see Figure 24). Control information for a channel of DSTo is also output one channel early on CSTo.

The CSTi input stream contains the individual channel control words and the master control word for the DS1 interface. The bit assignment for the master control word is shown in Figure 26 and the per channel control word is in Figure 27.

The signalling method used is selected by the Common Channel Signalling bit (CCS), bit 1. When bit stealing is active the A and B bits for each channel are inserted into the DS1 serial stream in bit position 8 of the 6th and 12th frames in the multiframe format shown in Figure 21. When the CCS pin is not active then common channel signalling can be implemented by the user.

It should be noted that only one channel per frame can be looped back by bit 2 of the per channel control words.

Control Output (CSTo) contains the master status word and the status words for each of the channels output on DSTo. Figure 25 shows how the information output on CSTo corresponds to the received DS1 channels. Master status information is output in channel 15 and the bit allocation is shown in Figure 28. Bits decoded as A and B signalling bits from frames 6 and 12 are output on the individual status channels after they have been debounced for 7.5msec to 9msec. The bit positions of the A and B signalling information in the per channel status word of CSTo is shown in Figure 29.

Bipolar Receiver

The receiver inputs of the Hybrid are intended to be coupled to the line through a center tapped pulse transformer. The bipolar receiver decodes the AMI input signal into split phase bipolar return to zero format, output at $\overline{RxA}$ and $\overline{RxB}$. These two signal are gated by and external NAND gate to form Received Data, (RxD), which is the input to the clock extractor and the DS1 interface. The pulse shape and height at the inputs (RxT to RxR) must conform to the AT&T Technical Advisory #34 specifications.

Bipolar Transmitter

The bipolar transmitter converts the outgoing data to the AMI code used on the digital transmission line. The output stage at OUTA and OUTB is open collector designed to be coupled to the line with a center tapped pulse transformer.

Equalization

Two equalization networks are provided on the hybrid. The first is a 6 dB pad used for external loop around, and the second compensates for directly driving three lengths of line. The second equalizer has pre-emphasis with three settings to drive 0-150, 150-450, and 450-750 foot lengths of transmission line to the line terminating equipment. Figures 17a and 17b shows the frequency and phase response of the short medium and long settings. Both equalizers have input and output impedances of 100Ω. The pre-emphasized equalizers have been optimized for 22 AWG quad cable.

Clock Extraction

The clock extraction circuitry creates a 1.544 MHz clock that is synchronized to the data rate on the DS1 line. This clock is used to write data to the DS1 interface. The frequency of this extracted clock is controlled by a 43µH to 48.5µH externally tuneable inductor. Tuning of the clock extractor should be done at set up time with no data on RxD. The frequency of the clock extractor must be adjusted to meet the set-up and hold times for $\overline{RxA}$, $\overline{RxB}$ and RxD. The particular network conditions that the MH89750 is operating under may impose tighter restrictions on the set-up and hold times of RxD than the device specifications.

Applications

A typical application circuit is shown in Figure 30. As can be seen there are very few external components that must be added to build a working DS1 interface. The 4PDT relay contacts show how the 6 dB pad is used for external loop around, the 7 switches illustrate the connection pattern for the second equalization circuit.

The L2 and C1 combination on the center tap of the transmit transformer filters out switching noise from the 12V power supply. To meet the AT&T specification the output pulse is shaped by the R2, C2, L3 network on the secondary of the output transformer.

BIT	NAME	DESCRIPTION
7	(unused)	
6	B8ZS	If 0 then Bit 7 of the DS1 carrier (the second last bit transmitted, corresponding to Bit 1 in the DSTI ST-BUS™) is jammed to 1 if all other bits of the channel on the DS1 carrier are 0. If 1 then all sequences of 8 zeros on data routed to the DS1 carrier are replaced by B8ZS code irrespective of channel boundaries or the presence of the S-bit in the 8 zeros. B8ZS code received from the DS1 carrier is always replaced by 8 zeros.
5	(unused)	
4	8kHzSEL	If 1 then the 8kHz pin is low for received DS1 channels 1 to 15 and high for channel 16 to the S-bit. If 0 then the 8kHz pin is high impedance.
3	XCTL	The information at this location is output directly onto the XCTL pin once per frame.
2	(unused)	Test bit. Keep at 0 for normal operation
1	CCS	If 1 then bit stealing by A & B signalling bits is prevented. Valid PCM or data is transmitted on every channel of the DS1 carrier for all frames.This option is used when common channel signalling is used. If 0 then the A & B signalling bits which are input on PCM bits 1 & 0 of the appropriate CSTi channels are sampled during frames 6 and 12 replace PCM bit 0 of the DSTi channels for these frames.
0	ALARM	If 1 then bit 2 of every channel transmitted on the DS1 carrier is jammed to zero. If 0 then bit 2 of the DS1 carrier behaves normally.

Figure 26. Data Format on CSTi Channel 15 - Master Control

BIT	NAME	DESCRIPTION
7,6	RXPAD2,1	Per channel receive attenuation control bits RXPAD2 RXPAD1 Gain(dB) 0 0 0 0 1 -5 1 0 -3 1 1 -6
5,4,3	TXPAD4,2,1	Per channel transmit attenuation control bits TXPAD4 TXPAD2 TXPAD1 Gain (dB) 0 0 0 0 0 0 1 -4 0 1 0 -5 0 1 1 -1 1 0 0 -3 1 0 1 -2 1 1 0 -6 1 1 1 1
2	LOOP	When this bit is 1 the transmitted DS1 channel is looped internally to replace the corresponding received DS1 channel. Only a single DS1 channel may be looped at any one time.
1	TX A-BIT	This bit is sampled and output instead of bit 0 of the corresponding DSTi channel during frame 6 unless the CCS bit (bit 1 on CSTi channel 15) is 1.
0	TX B-BIT	This bit is sampled and output instead of bit 0 of the corresponding DSTi channel during frame 12 unless the CCS bit (bit 1 on CSTi channel 15) is 1.

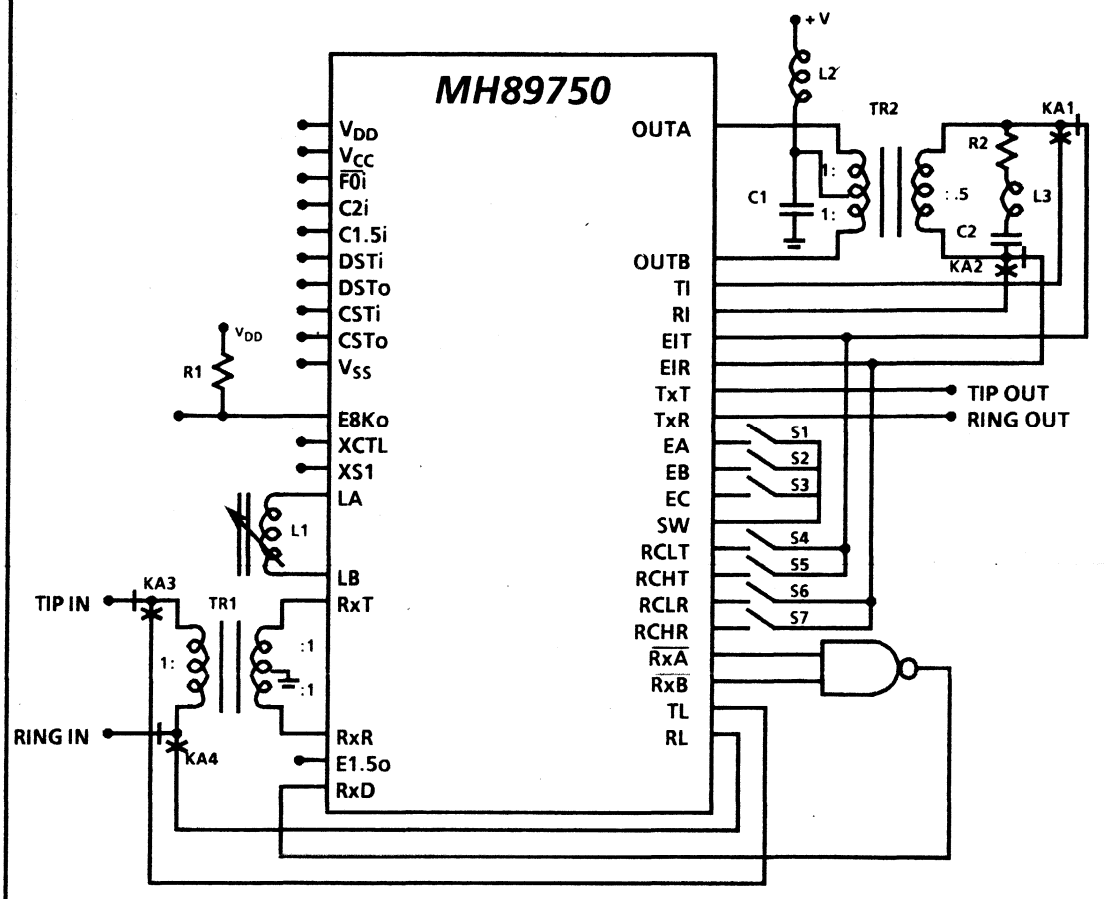
Figure 27. Data Format on CSTi Channels used for Controlling Channels on the DS1 Link

BIT	NAME	DESCRIPTION
7-5	(unused)	
4	XS1	This bit contains the data sampled at the XS1 pin once per frame.
3	RX0	This bit goes to 1 when the yellow alarm condition is detected for 500 ms on the received DS1 link (i.e. bit 2 of every received channel is zero) and returns to 0 after the alarm condition is removed for 200 ms.
2	BPV	This bit changes state after 256 bipolar violations other than B8ZS code has been detected on the received DS1 link within a sample period of 96 ms.
1	SLIP	This bit changes state once a slip condition occures between the recieved DS1 data and the output ST-BUS data. (Slips occur on the frame boundary)
0	$\overline{SYN}$	This bit goes to 1 when synchronization to the received DS1 link is lost and returns to 0 once synchronization is regained.

Figure 28. Data Format on CSTo Channel 15 - Master Status

BIT	NAME	DESCRIPTION
7-2	(unused)	
1	RX A-BIT	This bit is the A signalling bit from the DS1 carrier after it has been debounced for 7.5 ms to 9 ms.
0	RX B-BIT	This bit is the B signalling bit from the DS1 carrier after it has been debounced for 7.5 ms to 9 ms.

Figure 29. Data format on CSTo channels used for Monitoring Channels on the DS1 link



	0-150'	150-450'	450-750'
S1	CLOSE	OPEN	OPEN
S2	OPEN	CLOSE	OPEN
S4	OPEN	OPEN	CLOSE
S4	OPEN	CLOSE	OPEN
S5	OPEN	OPEN	CLOSE
S6	OPEN	CLOSE	OPEN
S7	OPEN	OPEN	CLOSE

Equalizer settings

Note: The equalizer has been optimized for 22 gauge cable

Figure 30. Typical Application Circuit

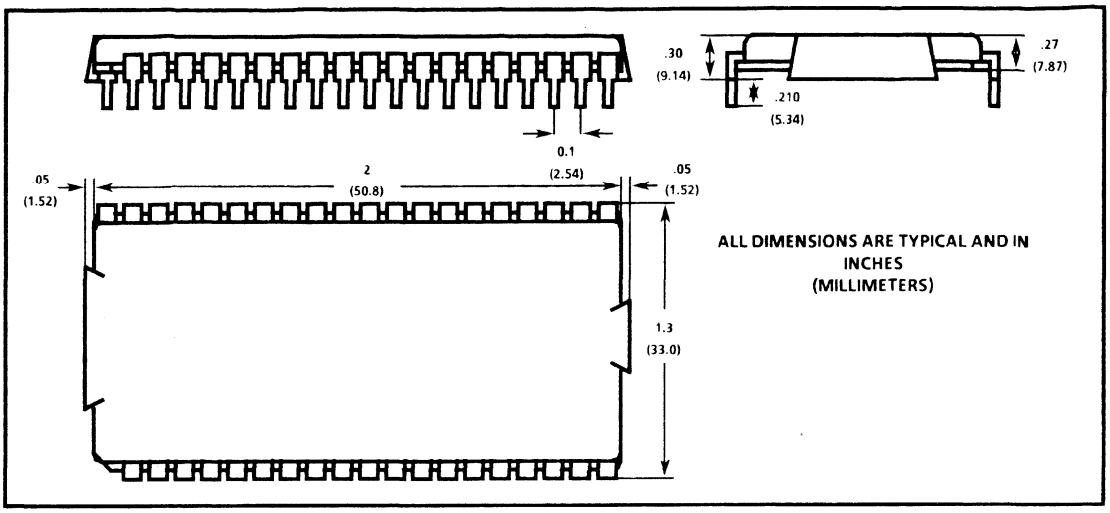


Figure 31. - Physical Dimensions of 40 Pin Dual in Line Hybrid Package

Printed in Canada

ST-BUS™ FAMILY MT8976
T1/ESF Digital Trunk Interface
Advanced Information

9161-002-060 NA ISSUE 2 JUNE 1986

Features

- D3/D4 or ESF Framing
- 2 frame elastic buffer
- 16 State signalling
- Signalling freeze with optional debounce
- Selectable B8ZS/jammed bit (ZCS) or transparent Zero Code Suppression
- Yellow alarm and Blue alarm capabilities
- Link/per channel robbed bit signalling disable
- Frame and Super frame sync signals, Tx and Rx
- Bipolar violation count, F_T error count, signal loss, CRC error count
- SLC*-96 Compatible
- Insertion of signalling, framing, CRC and FDL bits
- Per channel, local or remote loop around
- External control and status pins
- Interface between ST-BUS™ and DS1 link

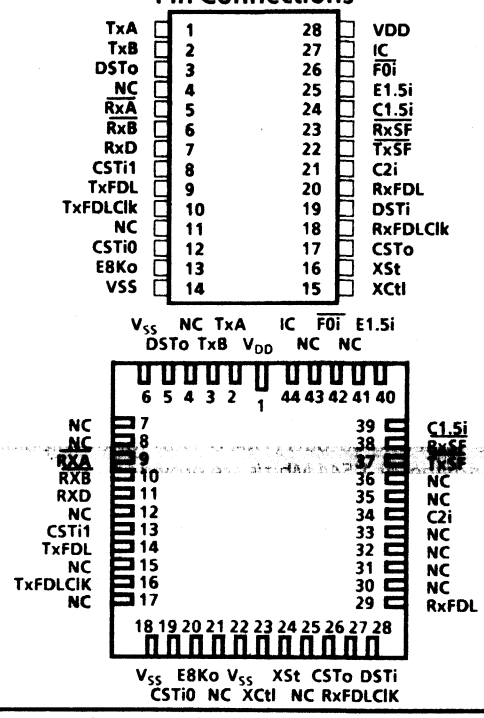
Applications

- PBX or computer to DS1 carrier interface
- Channel Bank and other digital switches

Description

The MT8976 is a digital line interface for use between a bidirectional 1.544 Mbit/s DS1 link and a serial 2.048 Mbits/s ST-BUS™ TDM stream. All functions for the link level interface are provided except clock extraction, line driving and sensing. The MT8976 is fabricated in Mitel's ISO-CMOS technology.

Pin Connections



Ordering Information -40 to 85°C

MT8976AC	28 Pin CERDIP
MT8976AY	44 Pin LCC

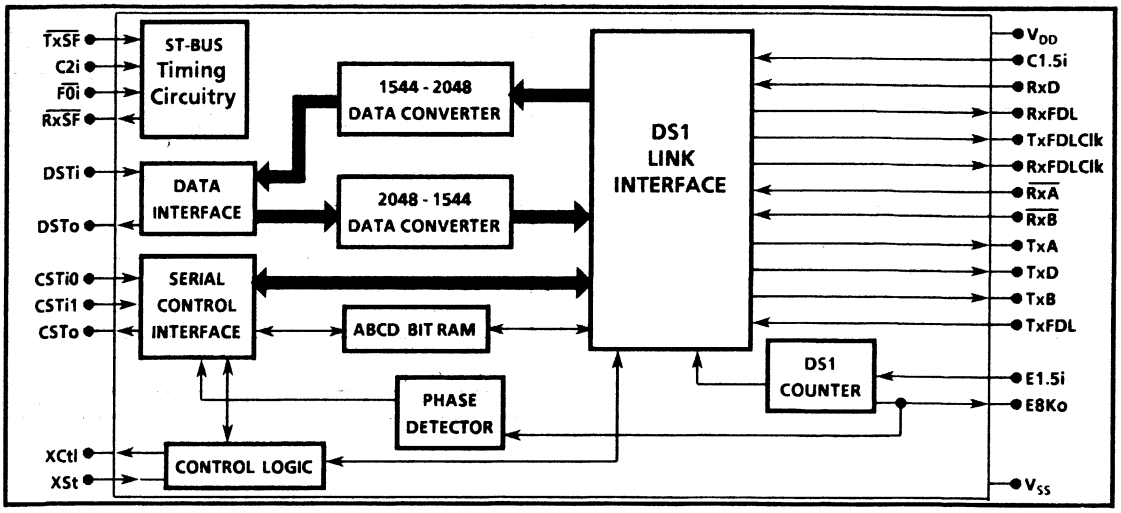


Figure 1. Functional Block Diagram

Functional Description

Data, which is to be transmitted onto the DS1/ESF TDM link, is input to the MT8976 on the ST-BUS™ data pin (DSTi). This serial data is passed through a 2.048 to 1.544 Mbit/s data rate converter before signalling and synchronization bits are inserted. The insertion of the sync bit follows one of three modes which consist of the D3/D4 mode, SLC*-96 mode and the ESF mode. While in D3/D4 or ESF mode, the synchronization bits are inserted according to the pattern shown in Fig. 2 & 3 respectively. In SLC*-96 mode, the F_T bit sequence is generated from within while the F_S bit pattern is sourced externally at a 4KHz rate. These synchronization bits are inserted into the PCM stream at the start of each frame.

The chip will optionally perform a logical inversion between the 24 active channels input on the ST-BUS™ and data output on the T1 line without inverting the signalling information. The data is AMI encoded with optional replacement of an 8 zero sequence with a selected zero suppression code. Steering outputs (TXA & TXB) for the bipolar line driving at 1.544 Mbit/s are provided.

Data arriving on the T1 line is examined for bipolar violations and zero code suppression (optional).

FRAME #	F_T	F_S	SIGNALLING †
1	1		
2		0	
3	0		
4		0	
5	1		
6		1	A
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	B

Figure 2. D3/D4 Framer

† These signalling bits are only valid if the robbed bit signalling is active.

The incoming data is demultiplexed into data and control streams and buffered in a 1.544 Mbit/s to 2.048 Mbit/s converter RAM before emerging on the DSTo output.

The 4 or 16 state signalling bits are buffered and debounced before being merged with the master status information. The combined signalling and status data emerges on the CSTo ST-BUS™ output. If the ESF framer is selected, the facility data link (FDL) received on the T1 line will be output as a 4 Kbit/s signal on the RxFDL pin. Conversely if D3/D4 framing is selected with the SLC*-96 option, the F_S sync pattern is output on the RxFDL pin.

This chip uses two distinct framing algorithms which are used on the T1/DS1 link. The D3/D4 framer is based on the 12 frame superframe having an F_T & F_S sync pattern. (Refer to Fig. 2). The ESF was developed to provide greater immunity to false framing. This algorithm is based on a 24 frame superframe carrying 16 state signalling, a cyclical rebundancy check and a facility data link (Refer to Fig 3). The framer will operate in an off line mode, that is, it will search for new frame position as a background task and will reposition the frame once the new frame position has been found.

FRAME #	FPS	FDL	CRC	SIGNALLING †
1		X		
2			CB1	
3		X		
4	0			
5		X		
6			CB2	A
7		X		
8	0			
9		X		
10			CB3	
11		X		
12	1			B
13		X		
14			CB4	
15		X		
16	0			
17		X		
18			CB5	C
19		X		
20	1			
21		X		
22			CB6	
23		X		
24	1			D

Figure 3. ESF Frame Pattern

Pin Description

Pin #	Name	Description
1	TxA	**Transmit B Output:** A split phase unipolar signal suitable for use with TxB and an external line driver and transformer to construct the bipolar line signal.
2	TxB	**Transmit A Output:** A split phase unipolar signal suitable for use with TxA and an external line driver and transformer to construct the bipolar line signal.
3	DSTo	**Data ST-BUS™ Output:** Received data is decoded, buffered, and output on 24 of the 32 ST-BUS™ output channels. Bit 2 of per channel control word 1 determines if there is a net inversion between the data received at RxD and the data output on DSTo.
4	NC	Unused
5	$\overline{RxA}$	**Receive A Complementary Input:** Received split phase unipolar signal decoded from the bipolar line receiver.
6	$\overline{RxB}$	**Receive B Complementary Input:** Received split phase unipolar signal decoded from the bipolar line receiver.
7	RxD	**Received Data Input:** Input of the unipolar RZ data generated by gating $\overline{RxA}$ and $\overline{RxB}$ in an external NAND gate.
8	CSTi1	**Control ST-BUS™ Input 1:** A 32 channel 2.048 Mb/s control stream (24 active) supplies the per channel signalling information.
9	TxFDL	**Transmit Facility Data Link Input:** A 4 KHz serial input stream that is muxed into the FDL position in the ESF mode, or the F_s pattern when SLC*-96 mode is active.
10	TxFDLClk	**Facility Data Link Output Clock: A 4 KHz clock input used to input FDL information.**
11	NC	Unused
12	CSTi0	**Control ST-BUS™ Input 0:** A 32 channel, 2.048 MHz serial control stream containing the 24 per-channel control words and 2 master control words.
13	E8Ko	**Extracted 8 KHz Output:** The 1.544 MHz received clock is internally divided by 193 to produce an 8 KHz signal which is synchronized to the incoming data rate.
14	V_{SS}	**Negative Power Supply Input** (Ground)
15	XCtl	**External Control Output:** This is an uncommitted external control output which reflects the data found on the bit in the control stream.
16	XSt	**External Status Input:** This level sensitive pin is an uncommitted input which can be used to monitor an external event. The status of this test point is provided in a bit of the output control stream.
17	CSTo	**Control ST-BUS™ Output:** A 32 channel control ST-BUS™ output which carries the received signalling bits as well as the T1/ESF trunk status information.
18	RxFDLClk	**Facility Data Link Output Clock:** A 4KHz clock input used to output the received FDL information.
19	DSTi	**Data ST-BUS™ Input:** A 32 channel (24 active) ST-BUS input data stream which contains the information to be transmitted on the T1 line.
20	RxFDL	**Received Facility Data Link Output:** A 4 KHz serial output stream that is demultiplexed from the FDL in ESF mode or the received F_s bit pattern when in SLC*-96 mode.
21	C2i	**2.048 MHz System Clock Input:** This master system clock is used to control all ST-BUS™ transactions. All data on the ST-BUS™ is clocked in on the falling edge and output on the rising edge.
22	$\overline{TxSF}$	**Transmit Superframe Boundary Complementary Input:** An input pulse once every superframe will set the transmitted superframe boundary (clear the frame counter). The period is 12 frames long in D3/D4 mode and 24 frames long in ESF mode. The chip will generate a continuous sync pattern if this pin is held high.

Pin Description (cont.)

Pin #	Name	Description
23	$\overline{RxSF}$	**Received Superframe Boundary Complementary Output**: An output pulse , which similar to a frame pulse, delimiting the received frame boundary. The period is 12 frames long in a D3/D4 mode and 24 frames long in ESF mode.
24	C1.5i	**Transmit 1.544 MHz Clock Input**: The rising edge of this 1.544 MHz clock is used to transmit the data on TxA and TxB. This clock must be phase locked to the 2.048 MHz system clock.
25	E1.5i	**Extracted 1.544 MHz Clock Input**: The falling edge of this 1.544 MHz clock is used to latch the received data into the device. This clock input must be derived from the T1/ESF received data and must have its falling edge aligned with the center of the received bit (RxD).
26	$\overline{F0i}$	**Frame Pulse Complementary Input**: A 244 ns wide, 8KHz frame pulse input which is used to indicate the start of a 32 channel ST-BUS™ frame.
27	IC	**Internal Connection**: Tie to V_{SS} (Ground) for normal operation
28	V_{DD}	**Digital Power Supply Input** (+ 5 Volts)

* SLC is a Trademark of AT&T Technologies Inc.

Notes:

MITEL

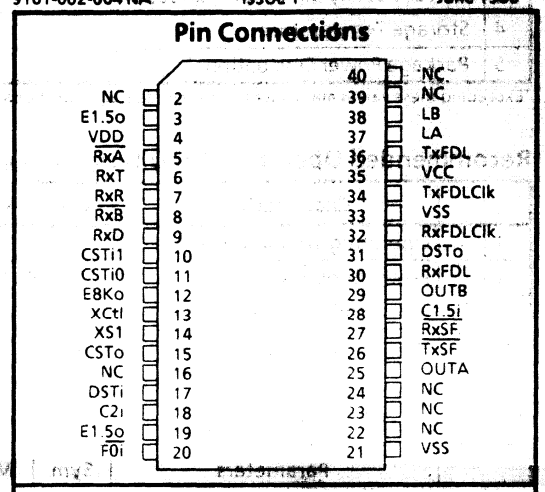
ST-BUS™ FAMILY MH89760
ESF Digital Trunk Interface
Preliminary Information

9161-002-064 NA ISSUE 1 June 1986

Features

- Complete interface to a bidirectional T1 link
- ST-BUS compatible
- D3/D4 or ESF framing and SLC96 compatible
- 2 frame elastic buffer with 32 μsec jitter buffer
- Insertion and detection of A, B,C,D bits. Signalling freeze, optional debounce
- Selectable B8ZS/jammed bit (ZCS) or transparent Zero code replacement
- Yellow alarm and blue signal capabilities
- Bipolar violation count, F_T error count, CRC error count
- Robbed bit signalling, overall or per channel
- Frame and superframe sync. signals, Tx and Rx
- AMI encoding and decoding
- Per channel, overall, and remote loop around
- 8KHz synchronization output
- Digital phase detector between T1 line and ST-BUS
- One uncommitted scan point and drive point

Pin Connections



Ordering Information

MH89760 40 pin DIL Hybrid
-40°C to 85°C

Applications

- DS1/ESF digital trunk interfaces
- Computer to PBX interfaces (DMI and CPI)
- High speed computer to computer data links

Description

The MH89760 is Mitel's second generation T1 interface solution. The MH89760 is designed to meet the new Extended Super Frame format (ESF), the current D3/D4 format and to be compatible with SLC-96 systems. The MH89760 provides the interface between the asynchronous 1.544 Mbit/sec digital trunk and Mitel's synchronous Serial Telecom Bus, the ST-BUS.

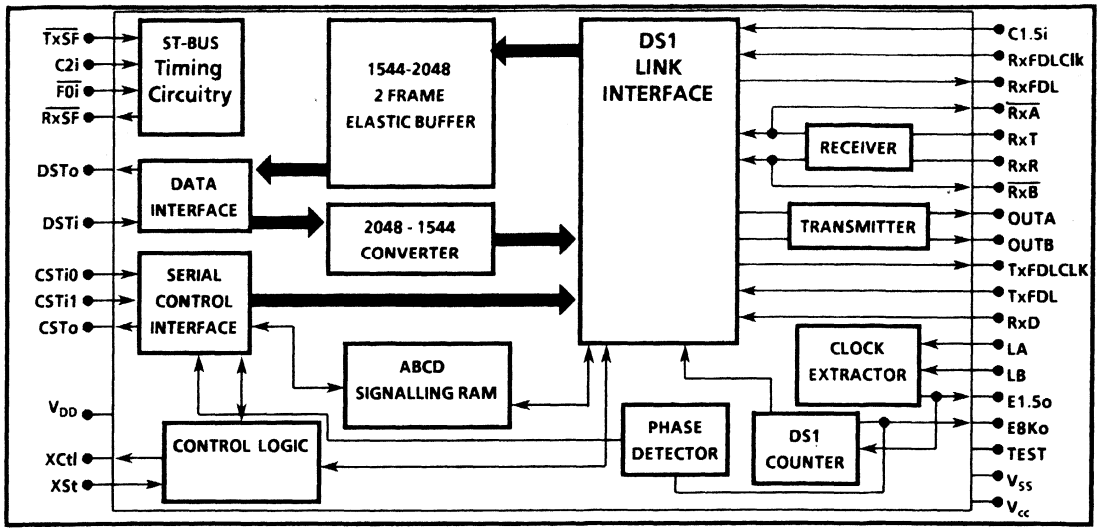


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power Supplies with respect to V_{SS}	V_{DD}	-0.3	7	V
2	Voltage on any pin other than supplies		V_{SS}-0.3	V_{DD} + 0.3	V
3	Current at any pin other than supplies			40	mA
4	Storage Temperature	T_{ST}	-55	125	°C
5	Package Power Dissipation	P		800	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Inputs	Operating Temperature	T_{OP}	-40		85	°C	
2		Power Supplies	V_{DD}	4.5	5.0	5.5	V	
3		Input High Voltage	V_{IH}	2.4		V_{DD}	V	For 400 mV noise margin
4		Input Low Voltage	V_{IL}	V_{SS}		0.4	V	For 400 mV noise margin

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Clocked operation over recommended temperature ranges and power supply voltages

		Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Inputs	Supply Current	I_{DD}			15	mA	Outputs Unloaded
2		Input High Voltage	V_{IH}	2.0			V	Digital Inputs
3		Input Low Voltage	V_{IL}			0.8	V	Digital Inputs
4		Input Leakage Current	I_{IL}		± 1	± 10	µA	Digital Inputs V_{IN} = 0 to V_{DD}
5	Outputs	Output High Voltage	V_{OH}	2.4			V	I_{OL} = 10mA
6		Output High Current	I_{OH}	10	20		mA	Source Current V_{OH} = 2.4V
			I_{OH}		16		mA	Source Current V_{OH} = 3.0V
7		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2mA
8		Output Low Current	I_{OL}	2	10		mA	Sink Current V_{OL} = 0.4V
			I_{OL}		30		mA	Sink Current V_{OL} = 2.0V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Capacitance

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Input Pin Capacitance	C_I		10		pF	
2		Output Pin Capacitance	C_O		10		pF	

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figure 2 & 3)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C2i Clock Period	t_{P20}	400	488	600	ns	
2	C2i Clock Width High or Low	t_{W20}	200	244	300	ns	
3	Frame Pulse Set Up Time	t_{FPS}	50			ns	
4	Frame Pulse Hold Time	t_{FPH}	50			ns	
5	Frame Pulse Width	t_{FPW}		244		ns	
6	$\overline{RxSF}$ Output Delay	t_{FPOD}			100	ns	
7	$\overline{TxSF}$ Hold Time	t_{TxSFH}	.1		124.5	µs	
8	$\overline{TxSF}$ Setup Time	t_{TxSFS}	.1		124.5	µs	

NB: Frame Pulse is repeated every 125µs in synchronization with the clock

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

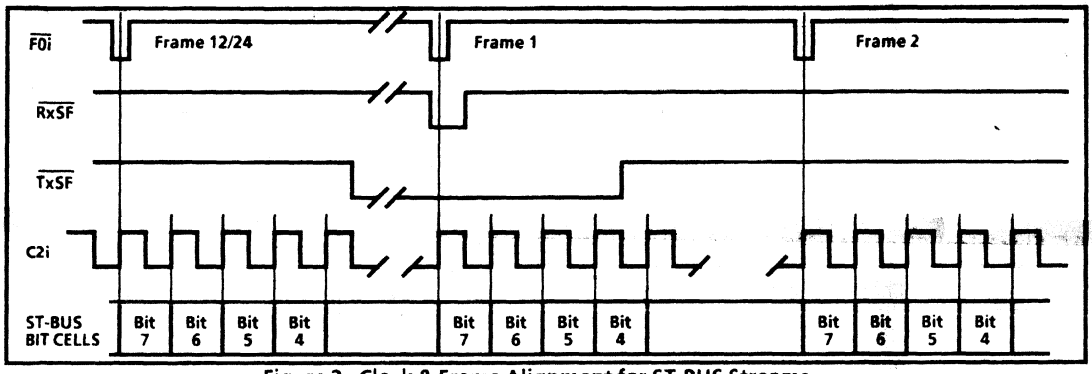


Figure 2 - Clock & Frame Alignment for ST-BUS Streams

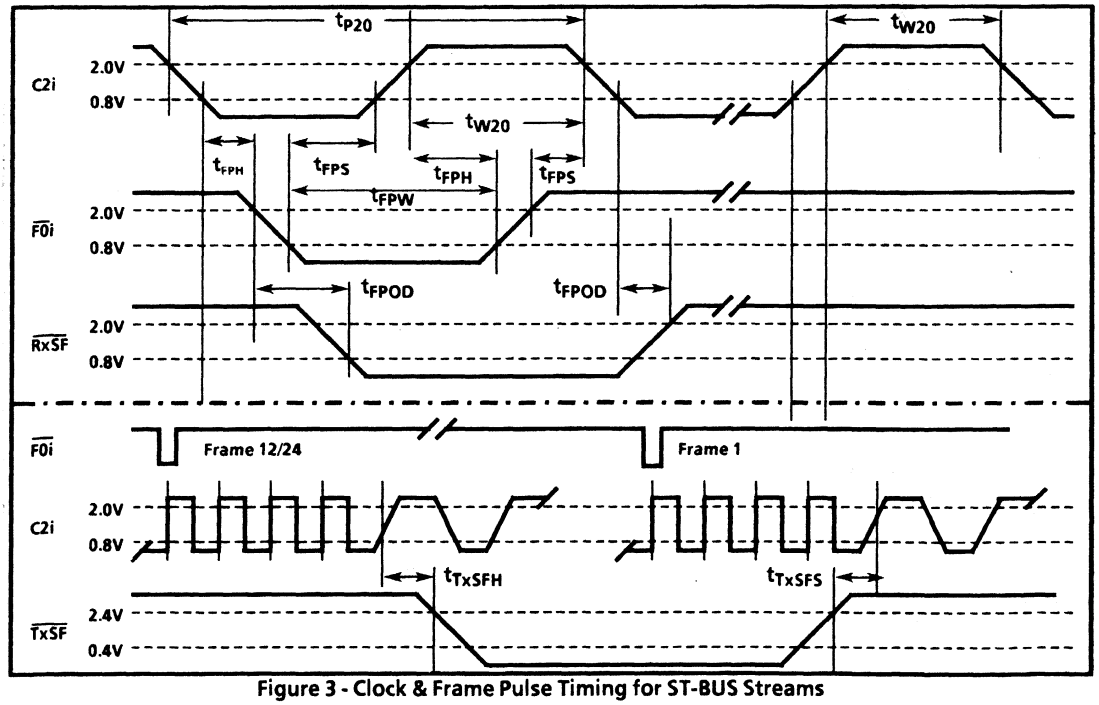


Figure 3 - Clock & Frame Pulse Timing for ST-BUS Streams

AC Electrical Characteristics† - Timing For DS1 Link Bit Cells (Figure 4)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	E1.5o Clock Period	t_{PEC}		648		ns	
2	E1.5o Clock Width High or Low	t_{WEC}		324		ns	
3	E1.5o Clock Rise Time	t_{REC}		60		ns	
4	E1.5o Clock Fall Time	t_{FEC}		20		ns	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

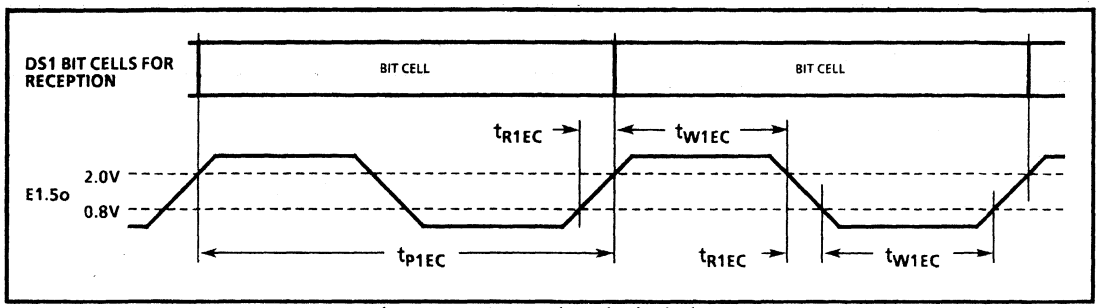


Figure 4 - DS1 Receive Clock Timing

AC Electrical Characteristics† - 2048 Kbit/s ST-BUS Streams (Figure 5)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Serial Output Delay	t_{SOD}			125	ns	150pF load
2	Serial Input Set-Up Time	t_{SIS}	30			ns	
3	Serial Input Hold Time	t_{SIH}	90			ns	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

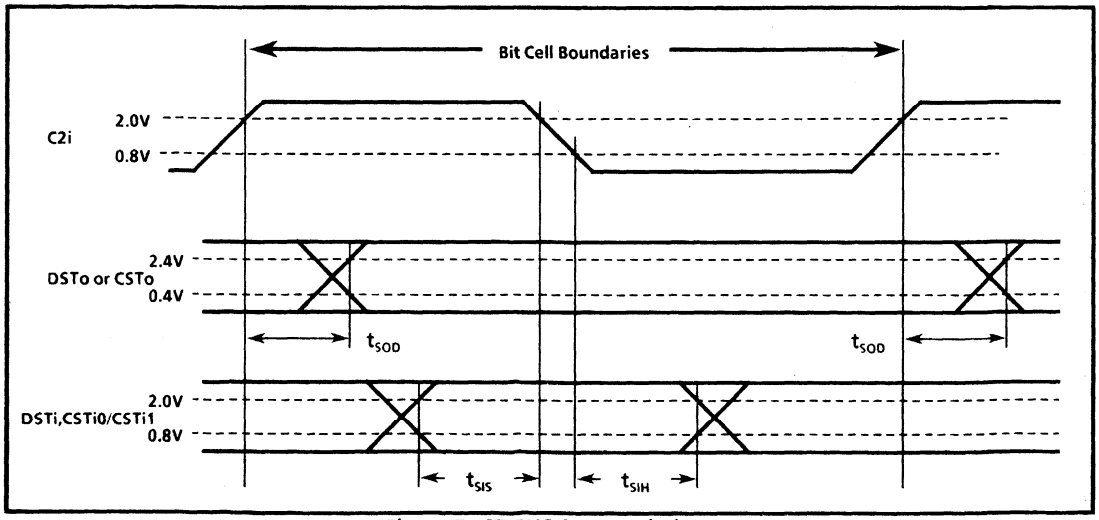


Figure 5 - ST-BUS Stream Timing

AC Electrical Characteristics† - XCTL, XSt, & E8Ko (Figure 6, 7, & 8)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	External Control Delay	t_{XCD}			150	ns	
2	External Status Set-Up Time	t_{XSS}			100	ns	
3	External Status Hold Time	t_{XSH}			100	ns	
4	8KHz Output Delay	t_{8OD}			150	ns	
5	8KHz Output Low Width	t_{8OL}		66		%	
6	8KHz Output High Width	t_{8OH}		44		%	
7	8KHz Rise Time	t_{8R}			40	ns	
8	8KHz Fall Time	t_{8F}			40	ns	
9	8KHz Disable Delay	t_{8DD}			100	ns	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

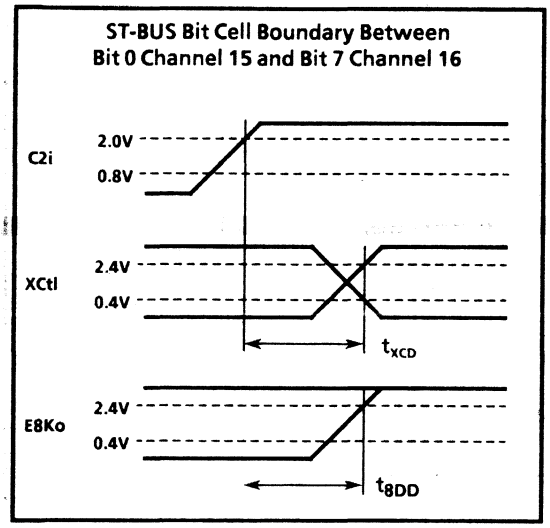


Figure 6 - XCTL Timing

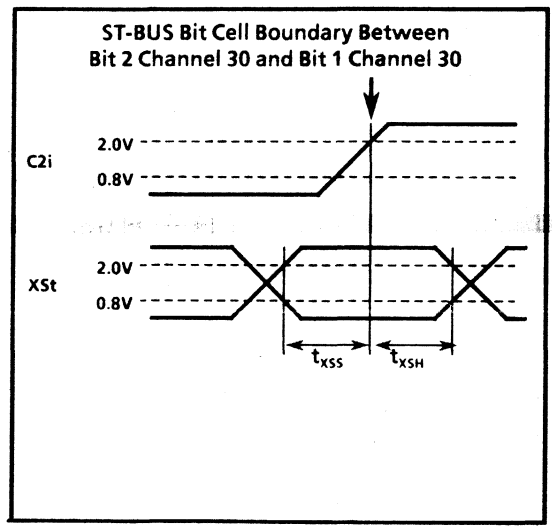


Figure 7 - XST Timing

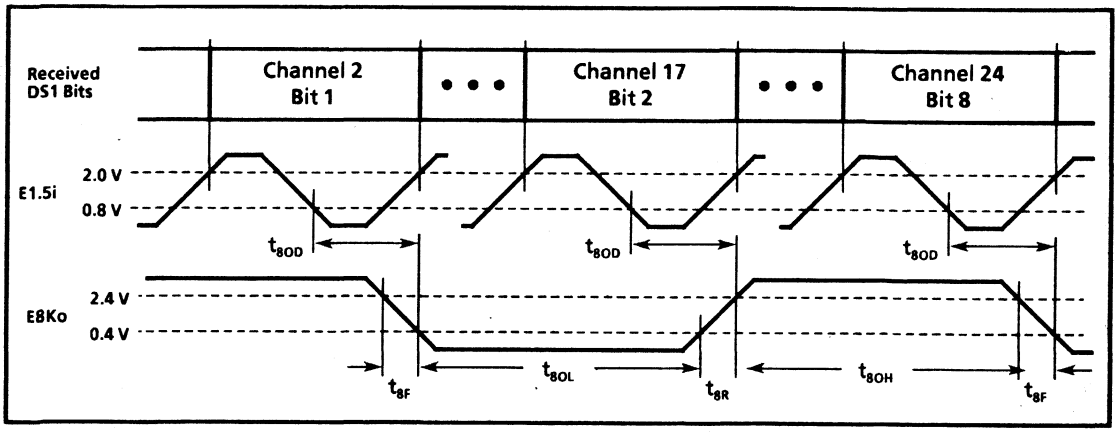


Figure 8 - E8Ko Timing

AC Electrical Characteristics† - DS1 Link Timing (Figure 9 & 10)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit Steering Delay	t_{TSD}	0		150	ns	See Note 1
2	Received Steering Rise Time	t_{RSR}		20		ns	
3	Received Steering Fall Time	t_{RSF}		20		ns	
4	Received Steering Pulse Width	t_{RSW}		244		ns	
5	Received Data Delay	t_{RDD}			100	ns	
8	Received Data Set-Up Time	t_{RDS}	100			ns	
9	Received Data Hold Time	t_{RDH}	100			ns	
10	C1.5i Period	$t_{PC1.5}$		648		ns	
11	C1.5i Pulse Width High or Low	$t_{WC1.5}$		324		ns	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

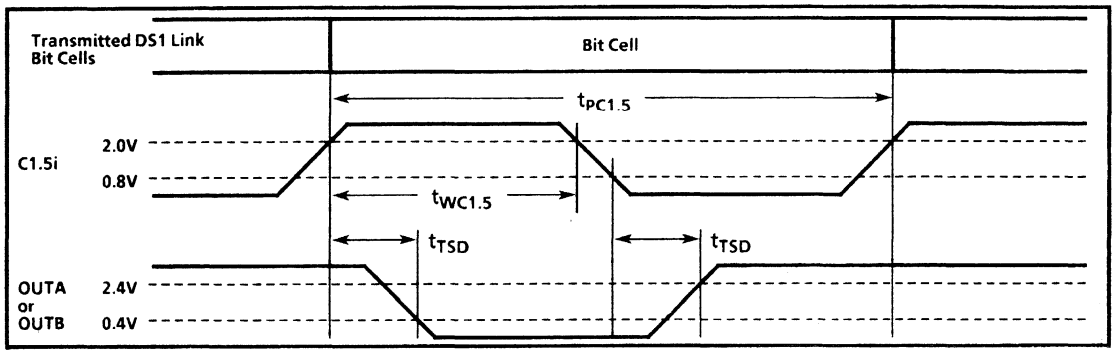


Figure 9 - Transmit Timing for DS1 Link

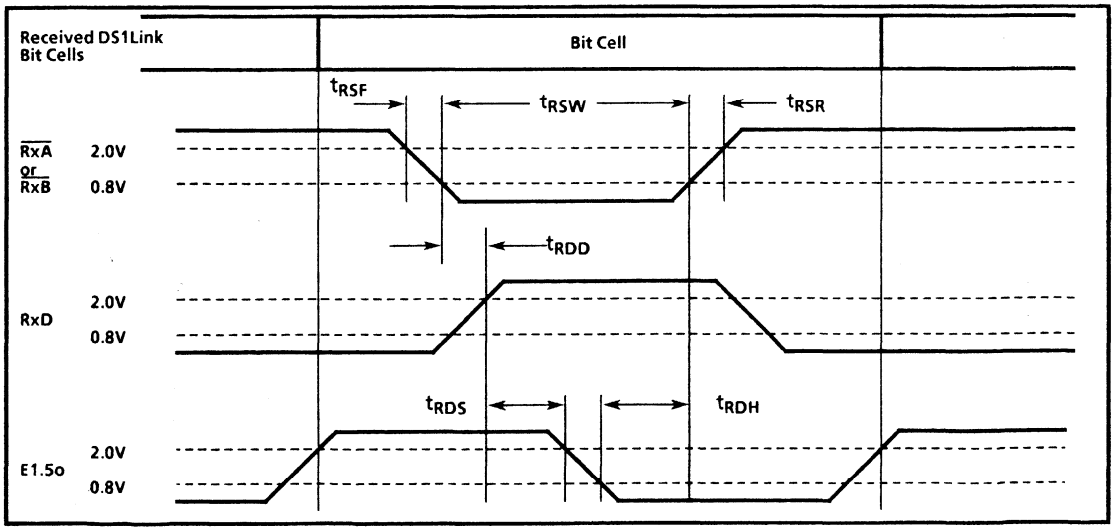


Figure 10 - Receive Timing for DS1 Link (see Note 1)

***Note 1:** $\overline{RxA}$ and $\overline{RxB}$ are derived from RxT and RxR which must meet CCITT G.732. The parameters t_{RDS} and t_{RDH} are related to device functionality. Network constraints may require tighter tolerances than the device specifications. The frequency of E1.5o must be adjusted with the external inductor to meet the device and/or the network tolerances.

AC Electrical Characteristics† - DS1 Link Timing (Figure 11 & 12)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit FDL set up time	t_{DLS}			100	ns	
2	Transmit FDL hold time	t_{DLH}			100	ns	
3	Receive FDL output delay	t_{DLOD}			100	ns	
4	FDL Clock Period	t_{DLCP}		250		µs	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

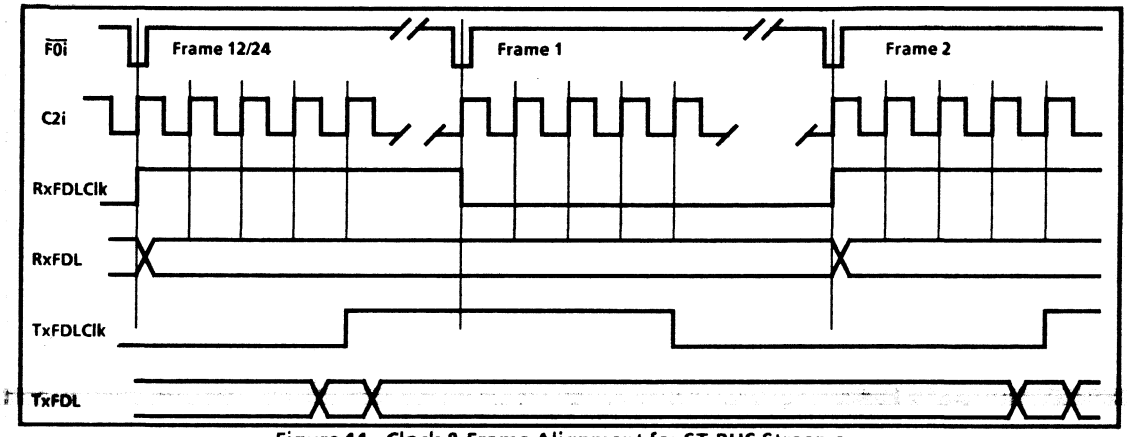


Figure 11 - Clock & Frame Alignment for ST-BUS Streams

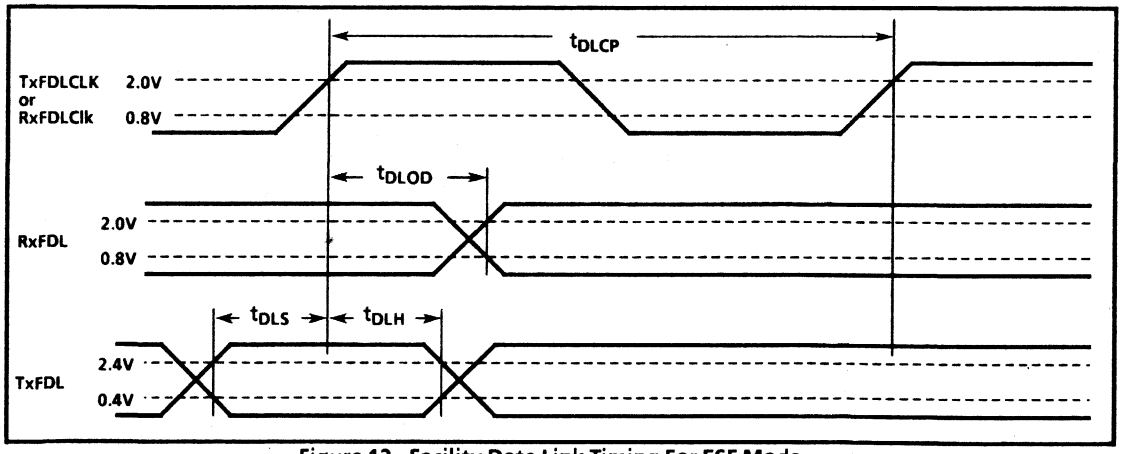


Figure 12 - Facility Data Link Timing For ESF Mode

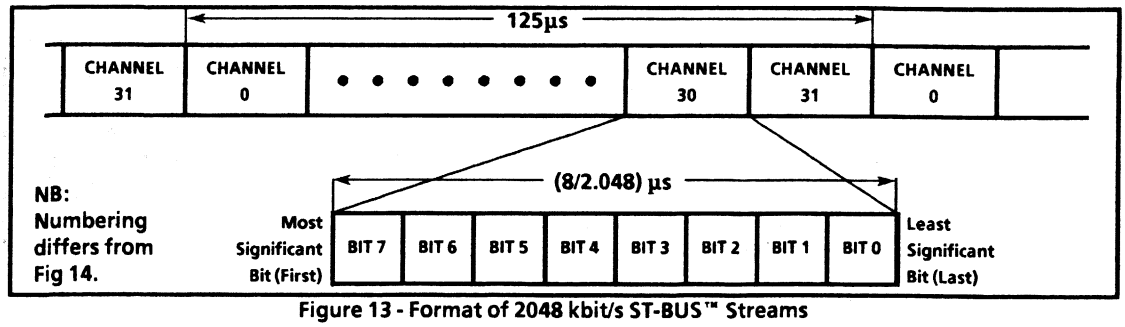


Figure 13 - Format of 2048 kbit/s ST-BUS™ Streams

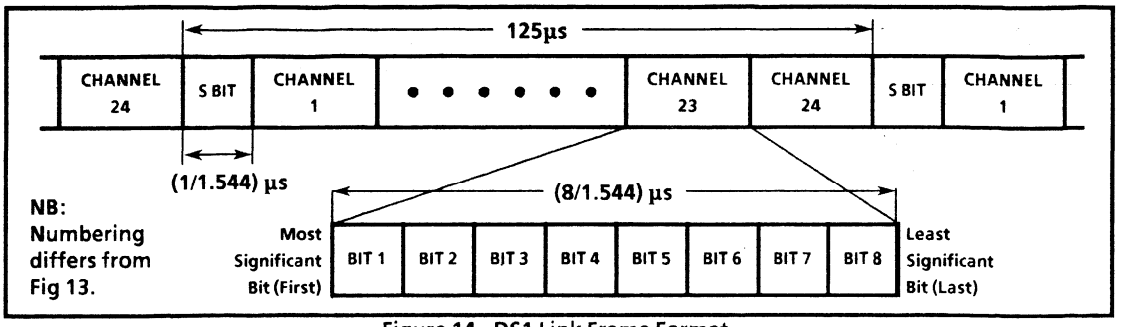


Figure 14 - DS1 Link Frame Format

Pin #	Name	Description
2	NC	**No Connect.**
3	E1.5o	**1.544 MHz Extracted Clock.** The extracted clock is used to clock RxD, $\overline{RxA}$ and $\overline{RxB}$ into the chip. The falling edge of this clock is nominally aligned with the center of the received bit on RxD, $\overline{RxA}$ and $\overline{RxB}$.
4	V_{DD}	**System Power Supply.** + 5V. +/- 10 %.
5	$\overline{RxA}$	**Received Split Phase Unipolar Signal.** Decoded by the device from the received bipolar line signal to represent one polarity of the signal.
6 7	RxT RxR	**Receive Tip and Ring Inputs.** Bipolar split phase inputs from the tip and ring leads of the input transformer. Impedance to Gnd ≈ 1KΩ. Impedance between pins = 430Ω.
8	$\overline{RxB}$	**Received Split Phase Unipolar Signal.** Decoded by the device from the received bipolar line signal to represent one polarity of the signal.
9	RxD	**Received Data.** The NAND of $\overline{RxA}$ and $\overline{RxB}$ used as the RZ version of the received data for input to the DS1 receiver and the clock extractor.
10	CSTi1	**Control ST-BUS Input #1.** This is a 32 channel control stream that contains 24 per-channel control words.
11	CSTi0	**Control ST-BUS Input #0.** This is a 32 channel control stream that contains 24 per-channel control words, and two master control words for overall chip operation.
12	E8Ko	**8 KHz Extracted Clock.** The E1.5o clock is internally divided by 193 to produce an 8KHz clock. This clock is phase-locked to the received line data rate. It is to be used for synchronizing a system to the DS1 data rate.
13	XCtl	**External Control.** The state of bit 3 MCW1 on CSTi0 is output on this pin. The state of XCtl is updated once per frame.
14	XSt	**External Status .** The state of this pin is sampled once a frame and the result is multiplexed on to bit 4 of MSW1 in CSTo. This is a Schmitt trigger input with thresholds of 2.5 volts high and 2.0 volts low.
15	CSTo	**Control ST-BUS Output.** This is a 32 channel control stream that contains 24 per-channel status words, and 2 master status words from overall chip operation.
16	NC	**No connect.**
17	DSTi	**Data ST-BUS Input.** Data is input to the chip on 24 of the 32 channels on this ST-BUS. Bit 2 of per channel control word 1 determines if there is a net inversion between DSTi and OUTA and OUTB.
18	C2i	**2.048 MHz System Clock.** This is the master clock for the ST-BUS section of the chip.All data on the ST-BUS is clocked in on the falling edge of C2i and out on the rising edge.
19	E1.5o	**1.544 MHz Extracted Clock.** The extracted clock is used to clock RxD, $\overline{RxA}$ and $\overline{RxB}$ into the chip. The falling edge of this clock is nominally aligned with the center of the received bit on RxD, $\overline{RxA}$ and $\overline{RxB}$.

Pin #	Name	Description
20	$\overline{F0i}$	**Frame Pulse Input.** This is the frame synchronization signal for the ST-BUS. The rising edge of C2i should nominally be in the center of the frame pulse. It is approximately 244 nsec wide, with a period of 125 μsec.
21	Vss	**System ground.**
22	NC	**No Connect.**
23	NC	**No Connect.**
24	NC	**No Connect.**
25	OUTA	**Transmit Split Phase Unipolar Signal** suitable for use with an external line transformer to construct the bipolar line signal
26	$\overline{TxSF}$	**Transmit Superframe Pulse Input.** An input pulse once every superframe will set the transmitted superframe to 1. The chip will free run if this pin is held high. The period is 12 frames long in DS1 mode and 24 frames long in ESF mode.
27	$\overline{RxSF}$	**Received Superframe Pulse Output.** Once every superframe there is an output pulse similar to frame pulse that designates the next frame of data on the ST-BUS to be from frame 1 of the received superframe. The period is 12 frames long in DS1 modes and 24 frames long in ESF mode.
28	C1.5i	**1.544 MHz clock input.** This is the transmit line clock. It must be phase-locked to the system clock. This is the clock used to output data on OUTA, OUTB. Data is clocked out on the rising edge of C1.5i.
29	OUTB	**Transmit Split Phase Unipolar Signal** suitable for use with an external line transformer to construct the bipolar line signal.
30	RxFDL	**Received Facility Data Link.** A 4 KHz serial output stream that is demultiplexed from the FDL in ESF mode, or the received F_S bit pattern when in SLC96 mode. It is clocked out on the rising edge of RxFDLClk.
31	DSTo	**Data ST-BUS Output.** Received data is decoded, buffered and output on 24 of the 32 channels on this ST-BUS. Bit 2 of per channel control word 1 determines if there is a net inversion between the data received at RxD and the data output on DSTo.
32	RxFDLClk	**Receive Facility Data Link Clock.** A 4 KHz clock used to output FDL information. Data is output on the rising edge of the clock.
33	Vss	**System Ground.**
34	TxFDLClk	**Transmit Facility Data Link Clock.** A 4 KHz clock used to input FDL information. Data is clocked in on the rising edge of the clock.
35	V_{CC}	**System Supply.** 12 Volts, +/- 10 %
36	TxFDL	**Transmit Facility Data Link.** A 4 KHz serial input stream that is muxed into the FDL position in the ESF mode, or the F_S pattern when in SLC96 mode. It is clocked in on the rising edge of TxFDLCLK.
37 38	LA LB	An external tuneable inductor is connected between these two pins to adjust the free running frequency of the extracted clock. The inductor is 43 to 48.5 μH.
39	NC	**No Connect.**
40	NC	**No Connect.**

Functional Timing Diagrams

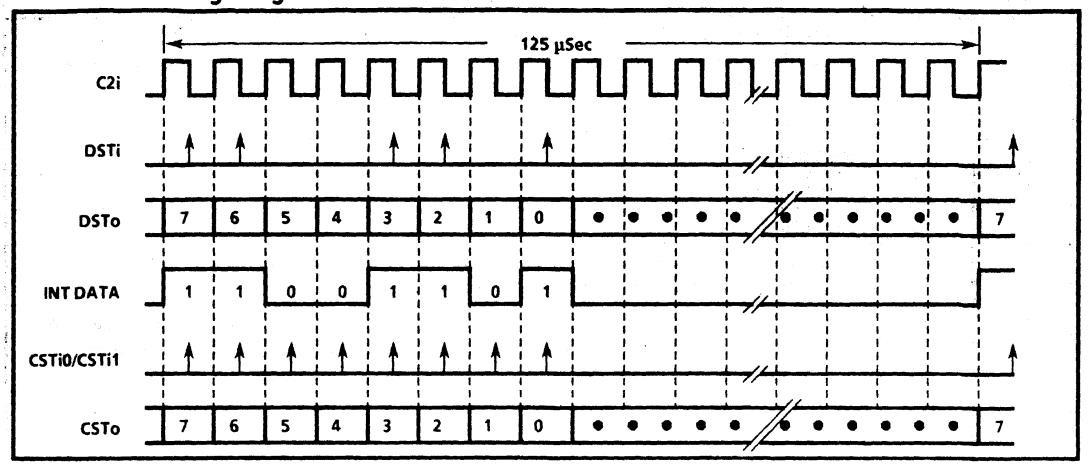


Figure 15 - ST-BUS Timing

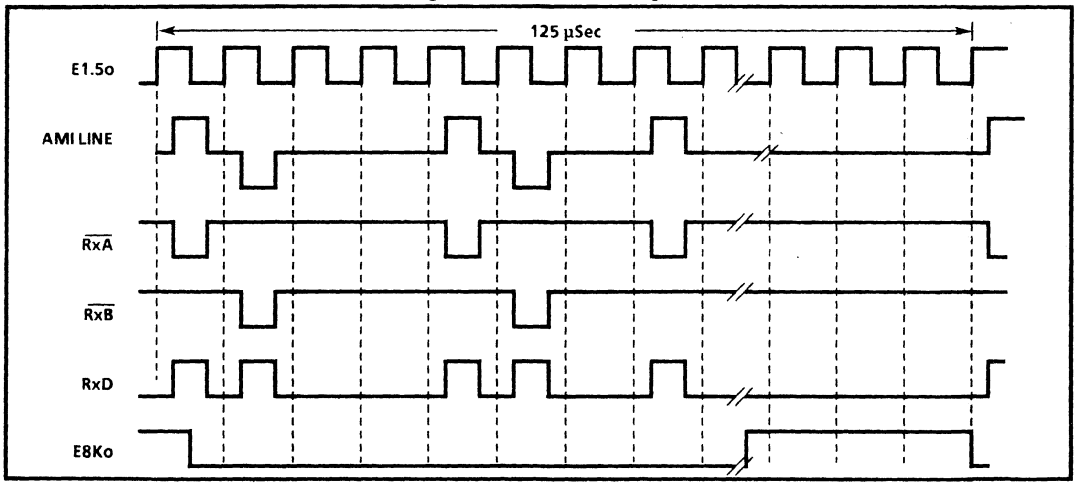


Figure 16 - DS1 Receive Timing

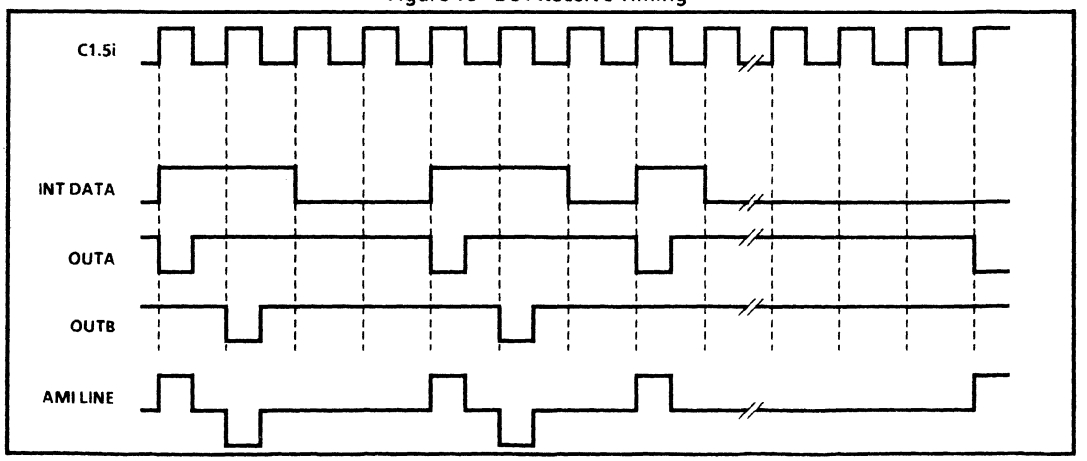


Figure 17 - DS1 Transmit Timing

Functional Description

The MH89760 is a thick film hybrid solution for a T1 interface. It contains both transmitter and receiver circuits, a received elastic buffer, bipolar line drivers and receivers, and clock extraction circuits. All of the formatting and rate adaption between the 2.048 Mbit/sec ST-BUS and the 1.544 Mbit/sec T1 line is done by the chip on board the hybrid. All of the options on the device are programmed or monitored through ST-BUS inputs and outputs. These options include ESF, D3/D4, or SLC-96 mode, common channel or robbed bit signalling, zero code suppression, alarms, and local and remote loop back.

The ST-BUS is a TDM bus structure that operates at 2.048 Mbits/sec. This serial stream is divided into 125 µsec frames that are made up of 32 8 bit channels. A serial stream that is made up of these 32 8 bit channels is known as an ST-BUS link, and one of these 64 Kbit/sec channels is known as an ST-BUS channel. The system side of the device is made up of ST-BUS inputs and outputs, i.e. control inputs and outputs (CSTi/o) and data inputs and outputs (DSTi/o). These signals are functionally represented in Figure 15. The line side of the device is made up of the split phase inputs and outputs that connect to the line coupling transformer, i.e. OUTA OUTB, and $\overline{RxA}$ $\overline{RxB}$. Functional transmit and receive timing is shown in Figures 16 and 17.

Detailed Description

Data ST-BUS Interface

The 24 channels of data for transmission on the line are input/output on DSTi/DSTo. All ST-BUS links contain 32 channels, therefore, there are eight unused channels on DSTi/DSTo. The valid DS1 channels for transmit and receive are shown in Figure 20.

Control ST-BUS Interface

Control of the T1 device is done by CSTi0 and CSTi1. These two serial inputs have two components. The first is the control information related to each of the 24 information channels. The second is the control information related to the overall operation of the device. The relationship between the CSTi channels and the DS1 channels is also shown in Figure 20.

Control ST-BUS Input 0

There are two master control words in CSTi0 in timeslots 15 and 31. These two eight bit words are used to:

1) Select the different operating modes of the device ESF, D3/D4 or SLC-96.

2) To activate the features that are needed in a certain application; common channel signalling, zero code suppression, signalling debounce, fast framing.

3) To turn on in service alarms diagnostic loop arounds and the external control function.

Tables 1 and 2 contain a complete explanation of how each of the control bits in master control words one and two operate.

Bit	Name	Description
7	Debounce	When set the debouncing of the signalling bits is prevented. When clear the signalling bits are debounced for 6 to 9 msec.
6	TSPZCS	When this bit is set data input on DSTi is transmitted undisturbed. i.e. transparent zero code suppression.
5	B8ZS	When this bit is set B8ZS zero code suppression is enabled. When clear bit 7 of DS1 channels containing all 0's is forced high
4	8KHSel	When set the E8Ko pin is held high. When clear E8Ko operates normally.
3	XCtl	When set the XCtl pin is held high, and when clear XCtl is held low.
2	ESFYLW	When set this bit causes a sequence of 8 1's followed by 8 0's to be sent in the outgoing facility data link. Transmit facility data link operates normally when clear.
1	Robbed bit	When this bit is set robbed bit signalling is disabled on all channels. When it is clear robbed bit signalling is enabled for all channel.
0	YLALR	When set bit 2 of all DS1 channels is set low. When clear bit 2 operates normally.

Table 1 - Master Control Word 1

DSTi	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

ST-BUS CHANNEL VERSUS DS1 CHANNEL TRANSMITTED

DSTo	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

ST-BUS CHANNEL VERSUS DS1 CHANNEL RECEIVED

CSTi0	0 PCCW1	1 PCCW1	2 PCCW1	3 X	4 PCCW1	5 PCCW1	6 PCCW1	7 X	8 PCCW1	9 PCCW1	10 PCCW1	11 X	12 PCCW1	13 PCCW1	14 PCCW1	15 MCW1	16 PCCW1	17 PCCW1	18 PCCW1	19 X	20 PCCW1	21 PCCW1	22 PCCW1	23 X	24 PCCW1	25 PCCW1	26 PCCW1	27 X	28 PCCW1	29 PCCW1	30 PCCW1	31 MCW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

ST-BUS CHANNEL VERSUS DS1 CHANNEL CONTROLLED

CSTi1	0 PCCW2	1 PCCW2	2 PCCW2	3 X	4 PCCW2	5 PCCW2	6 PCCW2	7 X	8 PCCW2	9 PCCW2	10 PCCW2	11 X	12 PCCW2	13 PCCW2	14 PCCW2	15 X	16 PCCW2	17 PCCW2	18 PCCW2	19 X	20 PCCW2	21 PCCW2	22 PCCW2	23 X	24 PCCW2	25 PCCW2	26 PCCW2	27 X	28 PCCW2	29 PCCW2	30 PCCW2	31 X
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

ST-BUS CHANNEL VERSUS DS1 CHANNEL CONTROLLED

CSTo	0 PCSW	1 PCSW	2 PCSW	3 PSW	4 PCSW	5 PCSW	6 PCSW	7 X	8 PCSW	9 PCSW	10 PCSW	11 X	12 PCSW	13 PCSW	14 PCSW	15 MSW1	16 PCSW	17 PCSW	18 PCSW	19 X	20 PCSW	21 PCSW	22 PCSW	23 X	24 PCSW	25 PCSW	26 PCSW	27 X	28 PCSW	29 PCSW	30 PCSW	31 MSW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

ST-BUS VERSUS DS1 CHANNEL STATUS

Figure 16 - ST-BUS Channel Allocations

PCCW = PER CHANNEL CONTROL WORD
PCSW = PER CHANNEL STATUS WORD
MCW = MASTER CONTROL WORD
MSW = MASTER STATUS WORD
PSW = PHASE STATUS WORD
X = UNUSED CHANNEL

Bit	Name	Description
7	RMLOOP	When set the received signal is looped around to the transmit, interrupting the normal output data. The input and output data is clocked with E1.5. The receiver still monitors the input signal.
6	DGLOOP	When set the transmitted signal is looped around to the received side.The normal received data is interrupted.
5	ALL1'S	When set the chip sends an unframed all 1's signal to the far end.
4	ESF/D4	When this bit is set the chip is in ESF mode, and in D3/D4 mode when it is clear.
3	ReFR	If set, for at least 1 frame, and then cleared the chip will begin to search for a new frame position when the chip detects the change in state from high to low. Only the change from high to low will cause a reframe, not a continuous low level.
2	SLC96	The chip is in SLC96 mode when this bit is set. This enables input and output of the F_S bit pattern using the same pins as the Facility data link uses in ESF mode. The chip will use the same framing algorithm as D3/D4 mode. The user must insert the valid F_S bits in 2 out of 6 superframes to allow the receiver to find superframe sync. , and the transmitter to insert ABCD bits in every 6th frame. The SLC96 FDL completely replaces the F_S pattern in the outgoing S bit position. Inactive in ESF mode
1	FstFr	When set, the chip disregards the CRC calculation when searching for synchronization. When this bit is clear the chip operates normally.
0	Maint.	When set, the out of sync. threshhold is 4 F_T error out of 12, when clear it is 2 of 4.

Table 2 - Master Control Word 2

The major operating modes of the device are enabled by bits 2 and 4 of Master Control Word 2. When using ESF mode bit 4 must be set (logic 1), bit 2 is undefined. Extended super frame mode enables the transmission of the S bit pattern shown in Table 3. This includes the frame/superframe pattern, the CRC-6, and the Facility Data Link (FDL). The device generates the frame/multiframe pattern, calculates the CRC, and inserts the data provided on TxFDL into the FDL. ESF mode will also insert ABCD signalling bits into the 24 frame multiframe. The DS1 frame begins 25 C1.5i bits from frame pulse.

The receiver locks on to the incoming frame, calculates the CRC and compares it to the CRC received in the next multiframe, extracts the FDL information and clocks it out of the device on RxFDL. There are two modifications that can be made to the frame synchronization circuit. Firstly, the CRC check can be turned off by Master Control Word 2. This enables the device to synchronize faster. Secondly, the device can be forced to resynchronize itself. The reframe bit is used to force a new frame position if the system thinks that the receiver is synchronized to the wrong position. The decision to force a reframe is made by monitoring the number of errors in the received CRC or by the mimic indicator in Master Status Word 1. When the device attains synchronization the mimic bit in Master Status Word 1 tells the user that the device found another possible candidate when it was searching for the framing pattern. The presence of a mimic can also be considered when the device is forced to reframe itself.

FRAME #	FPS	FDL	CRC	SIGNALLING †
1		X		
2			CB1	
3		X		
4	0			
5		X		
6			CB2	A
7		X		
8	0			
9		X		
10			CB3	
11		X		
12	1			B
13		X		
14			CB4	
15		X		
16	0			
17		X		
18			CB5	C
19		X		
20	1			
21		X		
22			CB6	
23		X		
24	1			D

Table 3 - ESF Frame Pattern

Standard D3/D4 framing is enabled when bit 4 of Master Control Word 2 is reset (logic 0). In this mode the device searches for the framing pattern shown in Table 4. This mode only supports AB bit signalling, and does not contain a CRC check. The fast frame option in Master Control Word 2 has no effect but the device can be forced to reframe.

FRAME #	F_T	F_S	SIGNALLING †
1	1		
2		0	
3	0		
4		0	
5	1		
6		1	A
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	B

Table 4 - D3/D4 Framer

† These signalling bits are only valid if the robbed bit signalling is active.

If the device has been programmed for D3/D4 mode it can also be made compatible with SLC-96 by setting bit two of Master Control Word 2. This allows the user to insert and extract the signalling framing pattern on the DS1 bit stream using the FDL input and output and their associated clocks. The user must format this 4Kbits of information externally to meet all of the requirements of the SLC-96 specification. The device multiplexes and demultiplexes this information into the proper position, but it does not format or interpret it. This mode of operation can also be used for any other application that uses all or part of the signalling framing pattern. As long as the device receives at least two proper sets of signalling framing bits, after synchronization, the device will be able extract the AB signalling bits.

The debouncing of the ABCD signalling bits can be disabled by bit 7 of Master Control Word 1 if the signalling bits are to be used as a data link, in a custom application. Debouncing can also be disabled if the debounce function has been done before the signalling information had been sent by the far end.

The combination of bits 5 and 6 in Master Control Word 1 allow one of three zero code suppression schemes to be selected. The three choices are: none, binary 8 zero suppression (B8ZS), or jammed bit (bit 7 forced high). No zero code suppression allows the device to interface with system that have already applied some form of zero code suppression to the data input on DSTi. B8ZS zero code suppression replaces all strings of 8 zeros with a known bit pattern and a specific pattern of bipolar violations. This bit pattern and violation pattern is shown in Figure 21. The receiver monitors the received bit pattern and the bipolar violation pattern and replaces all matching strings with 8 zeros.

Robbed bit signalling can be disabled for all channels by bit 1 of Master Control Word 1. By doing this the user can implement some type of common channel signalling by inserting the information in the proper channel of DSTi. The most common approach will be to use a common channel signalling protocol in channel 24 to create a 23 B + D type of interface.

Remote and digital loop around are used as diagnostic features to assist in locating the source of a fault condition. Remote loop around sends the far end data back to the far end unaltered so that

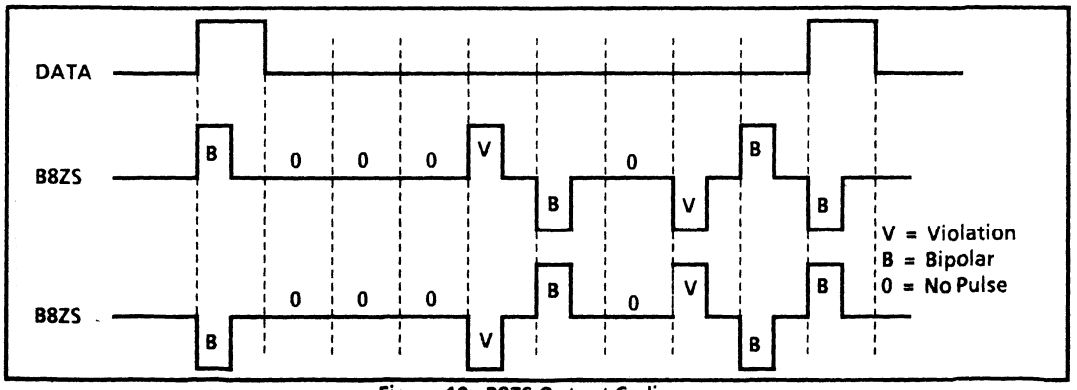


Figure 19 - B8ZS Output Coding

the transmission line can be tested. The received signal is still monitored so that the activation/deactivation signal for remote loop around can be contained in the DS1 signal. Digital loop around is used to test the near end interface equipment when there is no transmission line or when there is a suspected failure of the line.

The all ones transmit alarm is also known as the blue alarm or the keep alive signal. It can be activated separately from the digital loop around so that the transmission line sends an all 1's signal and the normal data can be looped around to the receiver by digital loop around.

In addition to the two master control words in CSTi0 there are also 24 per channel control words. The location of the 24 per channel control words is shown in Figure 20 and the control bits are explained in Table 5. Each control word has three bits that invert or do not invert the DS1 channel, cause a loopback of the DS1 channel, and enable or disable robbed bit signalling. The ability to invert or not invert a particular channel through the device is useful when a digital trunk is to carry a mixture of voice and data. Robbed bit signalling disable is used when a digital trunk carries common channel signalling and robbed bit signalling at the same time.

Control ST-BUS INPUT 1

Control ST-BUS input number 1 contains 24 additional per channel control words. These 24 ST-BUS channels contain the ABCD signalling bits that the device uses at transmit time. The position of these 24 per channel control words in the ST-BUS is shown in Figure 20 and the position on the ABCD signalling bits is shown in Table 6. Even though the device only inserts the signalling information in every 6th DS1 frame this information must be input every ST-BUS frame.

Control ST-BUS Output

The control ST-BUS output contains master status words one and two, 24 per channel status word, and a phase status word The master status words contain all of the information needed to determine the state of the interface and how well it is running. The information provided by the device is: frame and super frame synchronization, slip, bipolar violation counter, alarms, CRC error count, F_T error count, and synchronization pattern mimic. The phase status word provides a 9 bit digital phase reading between the DS1 frame boundary and the ST-BUS frame boundary. The ninth bit of this word is in Master Status Word 2. Tables 7 and 8 gives a description of each of bits in master status words one and two, and Table 9 gives a description of the phase status word.

The device detects the yellow alarm for both DS1 frame format and ESF format. The D3/D4 mode the yellow alarm will be detected in 600 msec and released in 200 msec. It is also detectable in the presence of errors on the line. The ESF yellow alarm will become active when the device has detected a string of 8 zeros followed by 8 ones. It is not

Bit	Name	Description
7-3	IC	Internal connections. Must be kept at 0 for normal operation
2	Polarity	When this bit is set the specified channel is not inverted on the receive, and the transmit side of the chip. When clear all bits are inverted through the chip on transmission and reception.
1	Loop	When set the received DS1 channel is replaced with the transmitted DS1 channel. Only one DS1 channel may be looped back in this manner at a time. The transmitted DS1 channel remains unaffected. When clear the transmit and receive DS1 sections operate normally.
0	Data	When set the controlled DS1 channel has robbed bit signalling insertion prevented. When clear the controlled channel is available for robbed bit signalling. If bit 1 of master control word 1 is clear, i.e. robbed bit.

Table 5 - Per Channel Control Word 1

Bit	Name	Description
7-4	Unused	Keep at 0 for normal operation
3 2 1-0	A B C,D	These are the 2 signalling bits inserted into the DS1 stream before being output from the chip, when in ESF mode. In the modes where there are only two signalling bits the value of C&D are ignored.

Table 6 - Per-Channel Control Word 2

Bit	Name	Description
7	YLALR	This bit is set when the chip is receiving a 0 in bit position 2 of every DS1 channel.
6	Mimic	This bit is set if the frame search algorithm found more than one possible frame candidate when it went into frame synchronization. Only active in ESF mode.
5	ERR	The state of this bit changes every time the chip detects 4 errors in the F_t portion of the S bit pattern.
4	ESFYLW	When set the received facility data link has detected a yellow alarm.
3	$\overline{\text{MFSYNC}}$	This bit is set when the chip has not detected the synchronization of the signalling frame. Applicable only to D3/D4 modes of operation.
2	BPV	The state of this bit changes every time the chip counts 256 bipolar violations.
1	SLIP	This bit changes state every time the chip performs a controlled slip.
0	$\overline{\text{SYN}}$	This bit is set when the chip has not achieved frame synchronization. The bit is clear when the chip is synchronized to the received DS1 data stream.

Table 7 - Master Status Word 1

Bit	Name	Description
7	BIAlm	This bit is set if the receiver has detected 2 frames of 1's and an out of frame condition. It is reset by any 250 micro second interval that contains a zero.
6	FrCnt	The state of this bit indicates whether the phase reading in the phase status word is from frame 0 or frame 1.
5	XSt	The state of the External Status is sampled once per frame and multiplexed into this bit position. Schmitt trigger input of 2.5 volts high and 2.0 volts low.
4-3	BPVCnt	These two bits are from the 8 bit bipolar violation counter. They change state every 128 and every 64 bipolar violations.
2-0	CRCCNT	These three bits count received CRC errors. The counter will roll around when it reaches terminal count.

Table 8 - Master Status Word 2

Bit	Name	Description
7-3	ChannelCnt	The value of these 5 bits indicate the relative position, within a frame, between the E8Ko and the ST-BUS frame. The 5 bits indicate the channel number.
2-0	BitCnt	The value of these three bits indicate the relative positions, within a channel, between the E8Ko and the ST-BUS. The 3 bits indicate the bit number.

Table 9 - Phase Status Word

detectable in the presence of errors on the line. This means that the ESF yellow alarm will drop out for relatively short periods of time, so the system will have to integrate the ESF yellow alarm. The blue alarm signal, in Master Status Word 2 , will also drop out if there are errors on the line.

The mimic bit in Master Status Word 1 is set when the receiver goes into synchronization. This is used to indicate that there was another possible candidate when the circuit was searching for the frame synchronization pattern. The mimic bit, the super frame sync and the CRC errors can be used separately or together to decide if the receiver should be forced to reframe.

The bipolar violation bit in Master Status Word 1, and the CRC error counter in Master Status Word 2 have a maximum refresh time of 96 msec. This means that they can not change state faster than every 96 msec. Using BPV as an example, if there are 256 violations in 80 msec the BPV bit will not change state until 96 msec. Any more errors in that extra 16 msec are not counted. If there are 256 errors in 200 msec then the BPV bit will change state after 200 msec. The other two bits of BPV information in Master Status Word 2 are not limited

Bit	Name	Description
7-4	Unused	Will be output as 0's
3 2 1 0	A B C D	These are the 4 signalling bits as extracted from the received DS1 bit stream. They are debounced for 6 to 9 msec, depending on the state of the signalling debounce control, bit 7 MCW1. They are output in the same timeslots, and bit positions, as their Per-Channel Control Word 2 counterparts.

Table 10 - Per-Channel Status Word

in quite the same manner. They are the next most significant bits in the BPV counter and can change at almost any rate because it is only the terminal count that is limited to every 96 msec. Intermediate counts can change at any time.

In practical terms this puts an upper limit on the error rate that can be calculated from the CRC and BPV information, but this rate is well above any normal operating condition.

Channel three of CSTo contains the Phase Status Word. These eight bits tell the user what phase relationship exists between the DS1 line and the ST-BUS. The first five bits indicate which channel the DS1 frame starts in and the last three bits contains which bit it starts in. Master Status Word 1 also contains a bit called frame count (FrCnt) that completes the phase indicator for a resolution of one bit over two frames. The Phase Status Word can be used to control a VCXO, in a large switching system, to produce a digitally controlled system phase locked loop. The key to the operation of such a phase locked loop is that there is 32 µsec of guaranteed jitter buffer, eight ST-BUS channels.

The amount of jitter on the received DS1 line can be determined by monitoring the 8 bit Phase Status Word and the frame counter in Master Status Word 1. If the amount of jitter present is less than eight ST-BUS channels peak to peak, then the frequency of the system clock is exactly right. If the phase relationship begins to wander then the frequency of the VCXO can be adjusted accordingly. The 32 usec of jitter buffering on the device allows the system phase locked loop to ignore the short term variations in the line speed and only adjust the systems VCXO with the longer term changes in the line speed, there by filtering the received jitter from the system clocks.

The ABCD signalling bits are output from the device in the 24 per channel status words. Their location in CSTo is shown in Figure 20 and the bit positions are shown in Table 10. The internal debouncing of the signalling bits can be turned on and off by Master Control Word 1. This enables the signalling path to be used as a low speed data link. When in D3/D4 mode the AB bits are valid and when in ESF mode the ABCD bits are valid. Even though the signalling bits are only received once every six frames the device stores the signalling so that it can be sent on the ST-BUS every frame. The ST-BUS will always contain the most recent signalling bits.

Line Interface

Line Transmitter

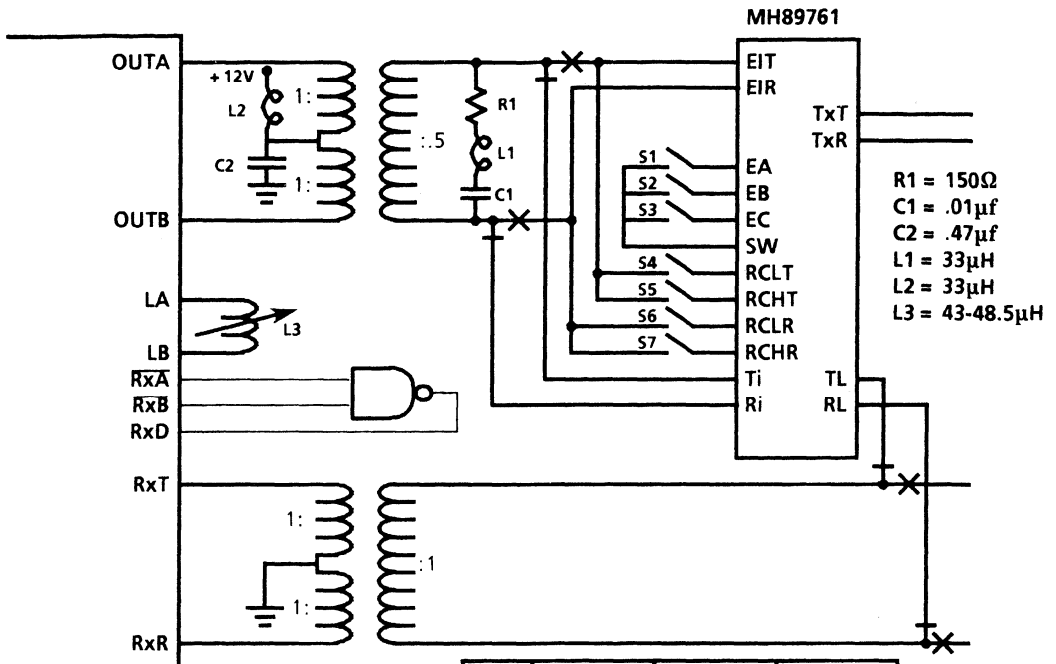
The transmit line interface is made up of two open collector drivers that represent the two pulse polarities (OUTA and OUTB). These are called split phase unipolar signals. The open collector drivers on the device will interface directly with a line transformer as shown in Figure 20. The capacitor and inductor on the center tap of the transmit transformer filter the 12 volt supply, and the series RLC across the output of the transformer shape the pulse to meet the AT&T or CCITT pulse templates.

Line Receiver

The receiver inputs are RxR and RxT. They are also shown in Figure 21. The transformer and the line receiver circuit converts the Alternate Mark Inversion line code into split phase unipolar signals $\overline{RxA}$, and $\overline{RxB}$. These two signals must be combined with a NAND gate to produce RxD. RxD is the data input for the receiver, and $\overline{RxA}$ and $\overline{RxB}$ are used to detect and count Bipolar Violations. The device presents a 430 ohm impedance to the receive transformer so that it will match a 100 ohm twisted pair line when it is reflected through the transformer.

Transmit Line Equalizer

To complete the interface to the transmit line the device requires a pre-equalizer and line impedance matching network. These two functions can be combined into one circuit that is a 6 dB pad with frequency compensation. The 6 dB of attenuation reduces the pulse size from the transformer to three volts and the frequency compensation pre-equalizes the signal before transmission. Mitel's MH89761 provides this function, as well as a separate plain 6 dB pad that can be used for external loop around. Figure 20 shows where the equalizer is used and how it is connected



	0-150'	150-450'	450-750'
S1	CLOSE	OPEN	OPEN
S2	OPEN	CLOSE	OPEN
S4	OPEN	OPEN	CLOSE
S4	OPEN	CLOSE	OPEN
S5	OPEN	OPEN	CLOSE
S6	OPEN	CLOSE	OPEN
S7	OPEN	OPEN	CLOSE

Equalizer settings

Note: The equalizer has been optimized for 22 gauge quad cable. The exact distances may vary with the type of cable and the output transformer.

Figure 20 - Input/Output Configuration

Clock Extractor

With the addition of an external tunable inductor (43µH to 48.5µH) the device extracts the received (E1.5o) clock from RxD. This clock is used to clock in the data on RxD, $\overline{RxA}$, and $\overline{RxB}$. Internally this signal is divided by 193 to produce the extracted 8 KHz signal (E8Ko). Figure 8 shows that this signal has a fixed relationship to the received DS1 frame. It is this relationship that is used to generate the Phase Status Word in CSTo. E8Ko is used to sample the ST-BUS counters once per frame to produce the 9 bit phase status.

Elastic Buffer

The received elastic buffer performs three functions. First, it enables the device to absorb jitter, second, it allows the device to perform controlled slips, and third, it aligns the transmit and receive data on the ST-BUS.

The amount of received jitter that the device can handle is approximately 32 µsec or exactly eight channels on the ST-BUS. Because the elastic RAM buffer is two frames, there may be times when the device will actually handle more than 32 µsec of jitter. However, worst case alignment of the DS1 frame and the ST-BUS frames will only allow 32 µsec of jitter tolerance. The maximum throughput delay is limited to 1.3 frames. It is limited to assist in keeping the throughput delay of the overall system to a minimum. One and one third frames of delay will still allow the device to perform a controlled slip of exactly one frame and still reduce the throughput delay.

When the device slips, the elastic buffer either repeats or skips one frame of information. If data is arriving too fast then one frame of data will be skipped. If the data is arriving too slow then one frame of data will be repeated. There is no loss of frame sync, multiframe sync, or any errors in the signalling bits when this occurs. The information on the FDL pins in ESF or SLC-96 mode will also undergo slips at the same time.

Clock Generation

The MH89760 requires three clock inputs. One for the T1 transmitter, and two for the ST-BUS. The ST-BUS requires a 2.048 MHz clock (C2i) and an 8KHz framing signal ($\overline{F0i}$). Figure 2 illustrates the relationship between the two and how it separates the ST-BUS into 32 channels. The ST-BUS clocks can easily be generated with dividers but the 1.544 MHz transmit clock (C1.5i) must be generated by a phase-locked loop. In order for the transmitter to operate properly C1.5i must be phase-locked to C2i. That is, there must be 193 clock cycles of C1.5i for every 256 clock cycles of C2i. The function is provided by the MT8940 Digital Phase-Locked Loop. Figure 21 shows how DPLL #1 can be setup to generate the C1.5i clock phase-locked to $\overline{F0i}$. These phase-locked clocks are required so that the device can convert from the 2.048 MHz ST-BUS to the 1.544 MHz DS1 rate.

Figure 21 also shows how DPLL #2 is set up to generate the ST-BUS clocks that are phase-locked to the received data rate. If E8Ko is connected to C8Kb on the MT8940 DPLL #2 will generate ST-BUS clocks that are phase-locked to the T1 line.

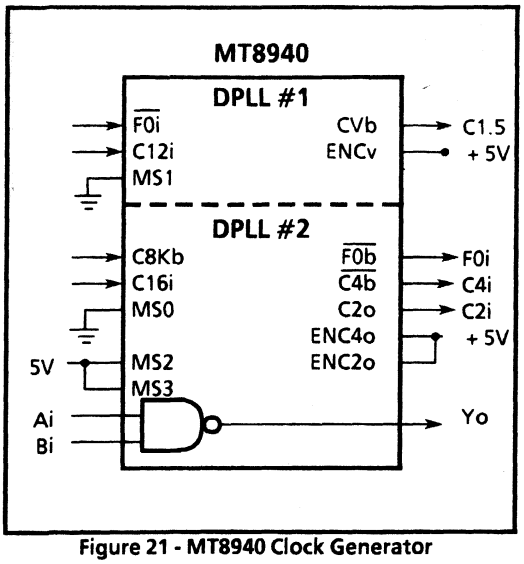


Figure 21 - MT8940 Clock Generator

Framing Algorithm

Figure 22 shows a state diagram of the framing algorithm. The dotted lines show which feature can be switched in and out depending upon the operating mode of the device.

The main feature of the framer is that it performs its function "off line". That is, the framer repositions the receive circuit only when it has detected a valid frame position. When the framer exits maintenance mode the receive counters remain where they are until the framer has found a new frame position. This means that if the user forces a reframe when the device was really in the right place, there will not be any disturbance in the circuit because the framer has no effect on the receiver until it has found synchronization. The out of synchronization criterion can be controlled by bit 0 in Master Control Word 2. This bit changes the out of frame conditions for the maintenance state.

The out of sync threshhold can be changed from 2 out of 4 errors in F_T to 4 out of 12 errors in F_T. The worst case average reframe time is 24 msec. for ESF mode, and 12msec. for D3/D4 modes. This number is a calculation of how long it would take to reframe if the device had to examine the maximum number of bit locations, but did not find any misleading mimics.

Figure 23 is a bar graph of percent probability versus reframe time, for random data input. The chart shows the results for ESF mode with CRC check, and D3/D4 modes of operation. The average reframe time with random data is 24 msec. for ESF, and 13 msec. D3/D4 modes. The probability of a reframe time of 35 msec. or less is 88% for ESF mode, and 97% for D3/D4 modes. In ESF mode it is recommended that the CRC check be enabled unless the line has a high error rate. With the CRC check disabled the average reframe time is greater because the framer must also check for mimics (more than one possible frame position).

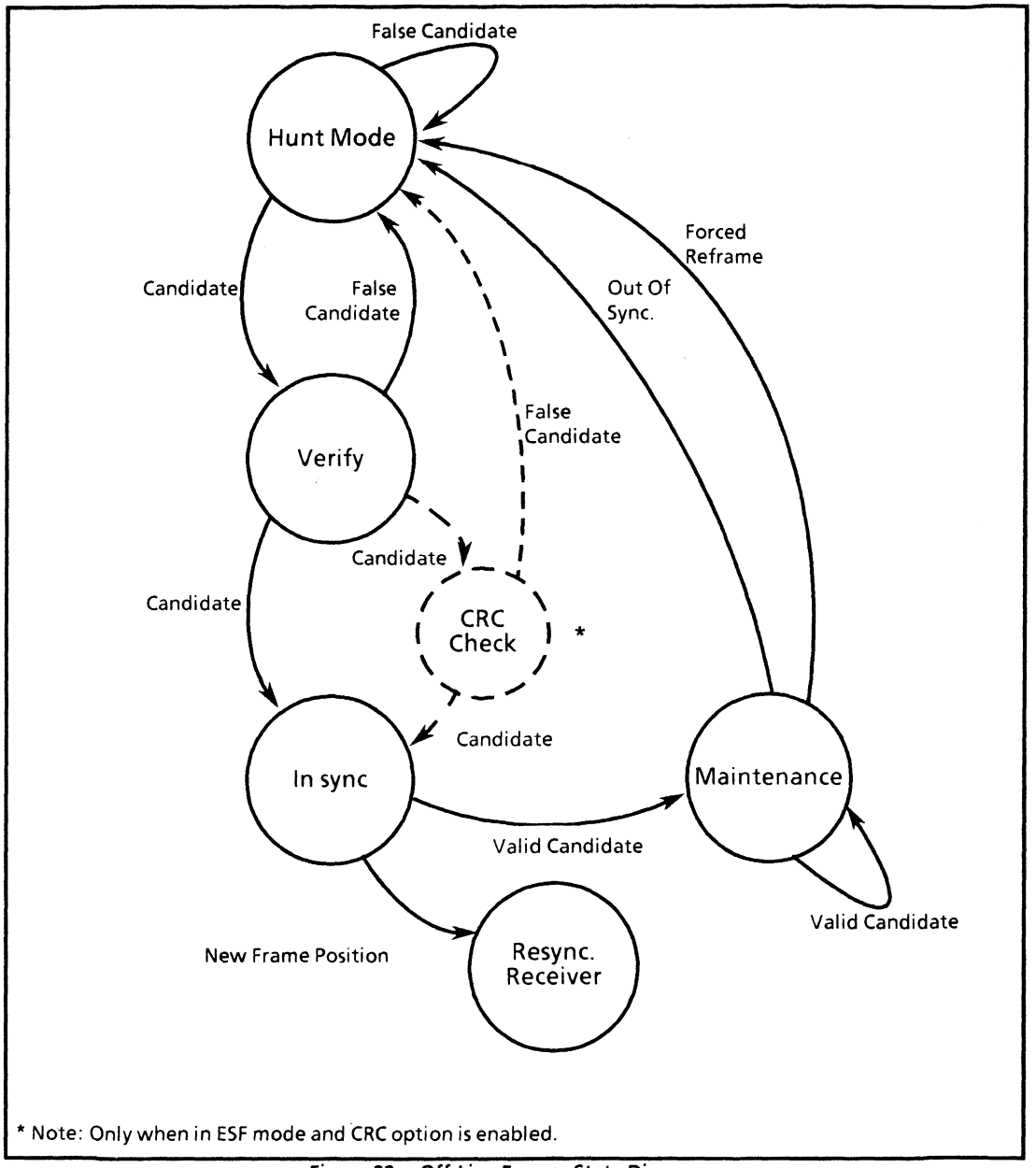


Figure 22 - Off-Line Framer State Diagram

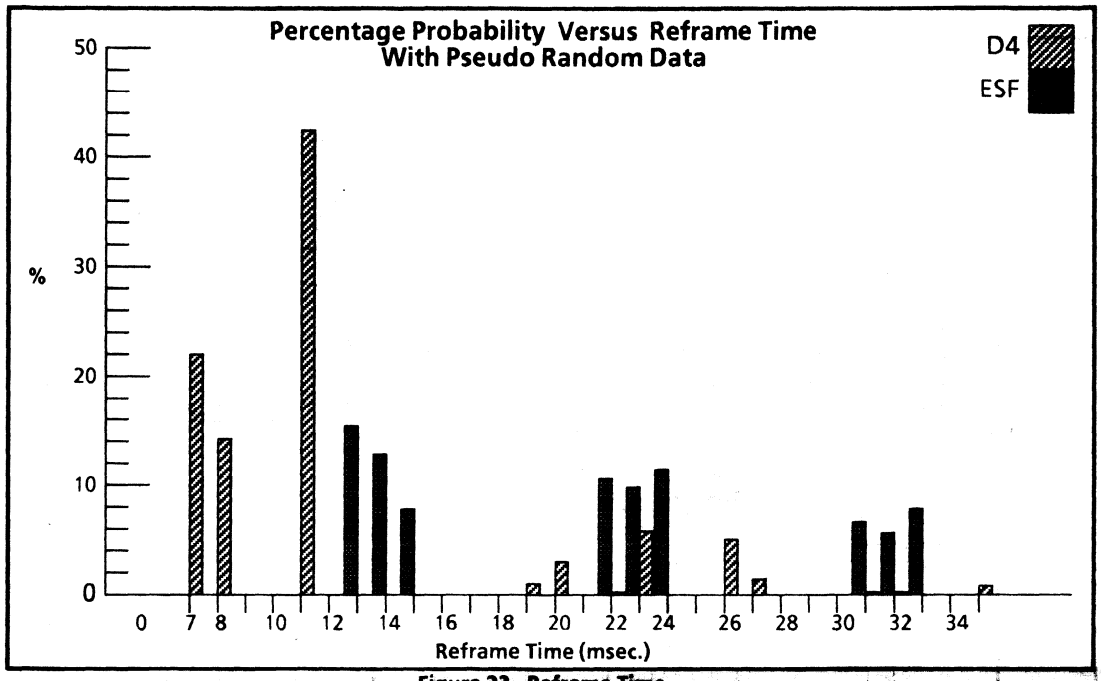


Figure 23 - Reframe Time

Applications

Figure 24 shows the external components that would be required in a typical ESF application. The MT8952 is handling the information on the facility data link with HDLC, the control, the MT8980 is used to control and monitor the device as well as switch data to DSTi and DSTo, the generation of the 1.544 MHz clock that is phase-locked to the ST-BUS, and the generation of the ST-BUS clocks phase-locked to the received clock rate is done by the MT8940. The line pre-equalization is done with the MH89761.

The typical connections shown in Figure 24 illustrates how the ST-BUS architecture is used to switch data to the MH89760, and to control and monitor the MH89760. The MT8980 is used in switching mode to transfer data to the T1 interface and in message mode to control and monitor the interface. That is, to setup and monitor master control and status words, and per channel control and status words. The components in Figure 24 produce a three port device. A line port to interface to the 1.544 MHz T1 line, an ST-BUS port to send and receive PCM or data from the system, and a microprocessor port to control and monitor all of the functions of the interface such as synchronization, alarms, and signalling.

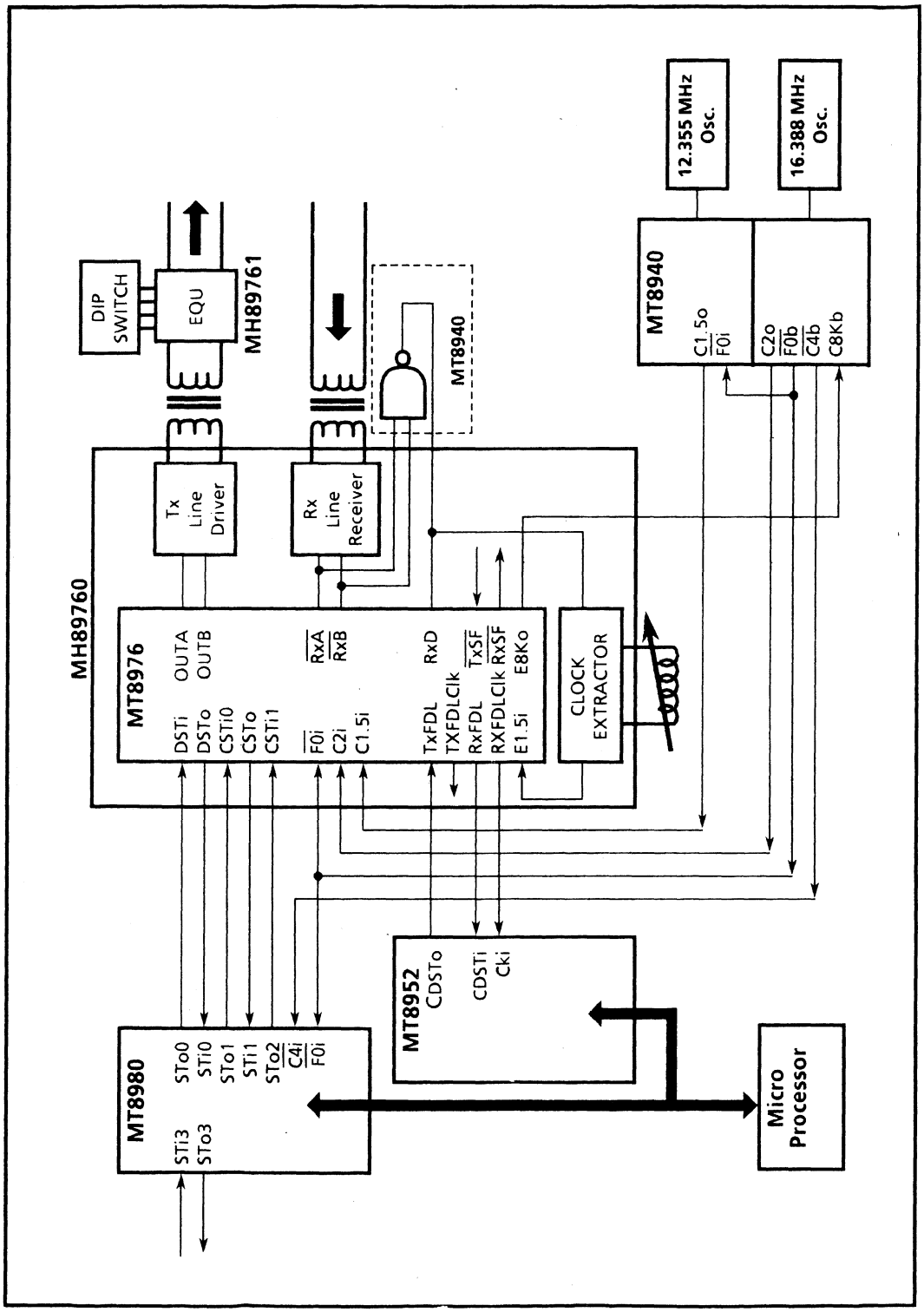


Figure 24 - Typical ESF Configuration

MH89761

T1 Digital Trunk Transmit Equalizer

Advance Information

9161-002-074 NA ISSUE 1 July 1986

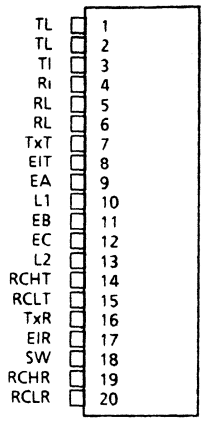
Features

- Compatible with the MH89760
- Programmable for short, medium, or long line lengths up to 655 ft.
- Transmit equalizer and 6dB loop around circuit

Description

The MH89761 is programmable transmit equalizer for use with a T1 line interface, specifically the MH89760. The MH89761 contains a three setting transmit equalizer and a 6 dB pad, for external loop around, with 100Ω input and output impedances. It is fabricated in thick film hybrid technology and is 2 inches high by 0.5 inches wide. The MH89761 is designed to drive 22 gauge twisted pair from the multiplex equipment to the crossconnect point. Figure 1 shows how the MH89761 is connected to the transmit side of a T1 interface. The seven switches control the distance settings of the equalizer. Ti, Ri, TL, and RL are the inputs and outputs of the 6 dB pad. The 4 pole double throw relay connected to the transformer inputs and outputs shows how the transmit signal is switched between the equalizer for normal operation, and the 6dB pad for loop around.

Pin Connections



Ordering Information

MH89761 20 pin SIP Hybrid
-40°C to 85°C

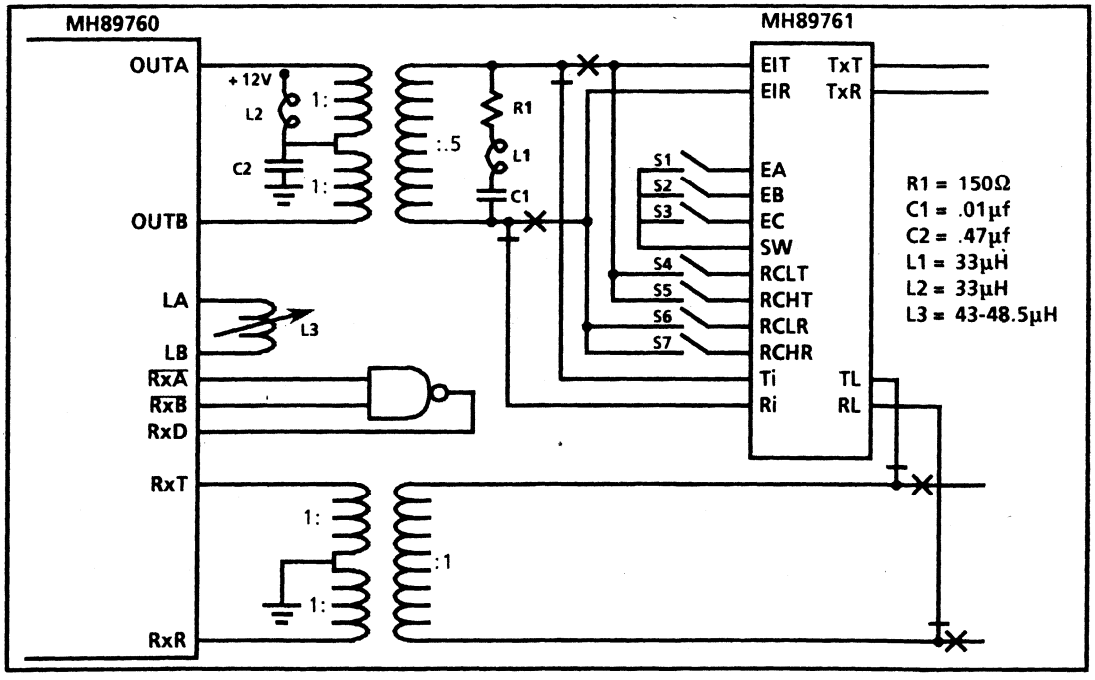
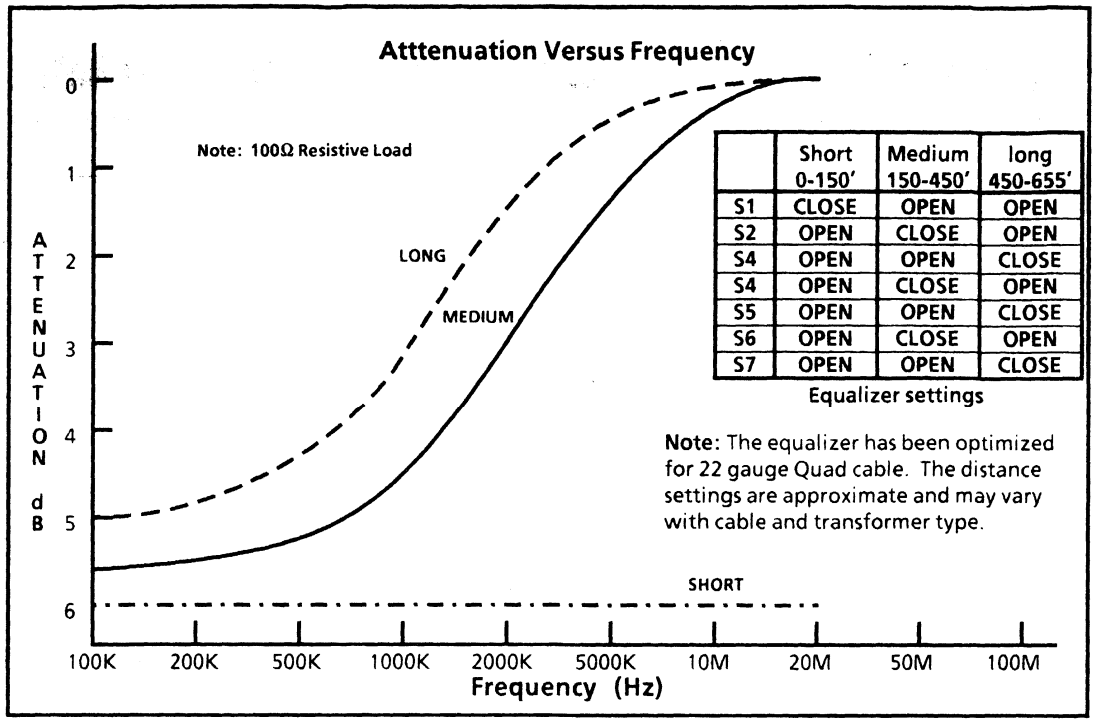


Figure 1 - Connection Diagram



	Short 0-150'	Medium 150-450'	long 450-655'
S1	CLOSE	OPEN	OPEN
S2	OPEN	CLOSE	OPEN
S4	OPEN	OPEN	CLOSE
S4	OPEN	CLOSE	OPEN
S5	OPEN	OPEN	CLOSE
S6	OPEN	CLOSE	OPEN
S7	OPEN	OPEN	CLOSE

Equalizer settings

Note: The equalizer has been optimized for 22 gauge Quad cable. The distance settings are approximate and may vary with cable and transformer type.

Figure 2 - Typical Frequency Response of the Equalizers

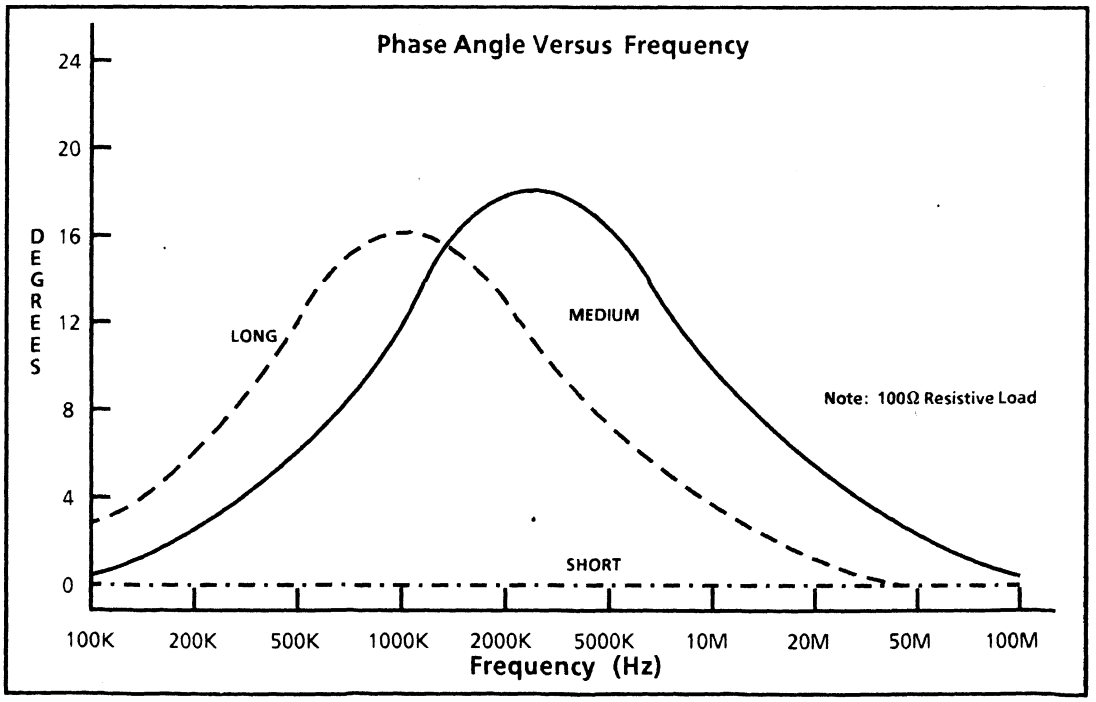


Figure 3 - Typical Phase Response of the Equalizers

ST-BUS™ FAMILY ISO-CMOS MT8978
CEPT Digital Trunk Interface Circuit

9161-002-012-NA ISSUE 4 JUNE 1986

Features

- Compatible with CCITT Recommendation G 732
- ST-BUS™ Compatible
- Interface to bidirectional 2048 kbit/s CEPT link
- 2 Frame Elastic Buffer
- Insertion of signalling and alignment
- Optional ADI encoding and decoding
- Per-channel control
- Programmable digital attenuation of PCM signals
- HDB3 encoding and decoding
- Optional Debounce of received signalling
- External control and status pins
- Single 5 V power supply
- TTL-compatible inputs and outputs

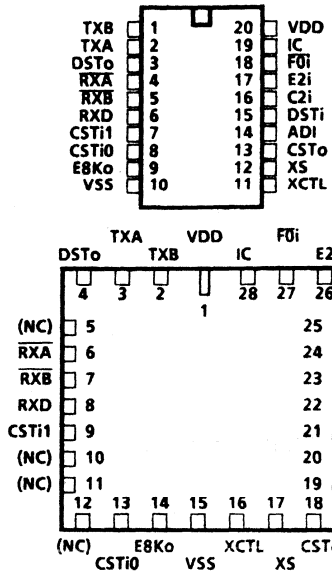
Applications

- High speed data links using CEPT 2048 kbit/s link
- PBX or computer to CEPT 2048 kbit/s link
- Channel banks

Description

The MT8978 is an interface circuit for use between serial 2048 kbit/s ST-BUS™ time-division multiplexed streams and a bidirectional 2048 kbit/s CEPT primary TDM transmission link. All functions, except clock extraction and line driving and sensing, are provided. The MT8978 is fabricated using Mitel's ISO-CMOS technology.

Pin Connections



Ordering Information

MT8978AC	20-Pin Ceramic
MT8978AY	28-Pin LCC

-40°C to + 85°C

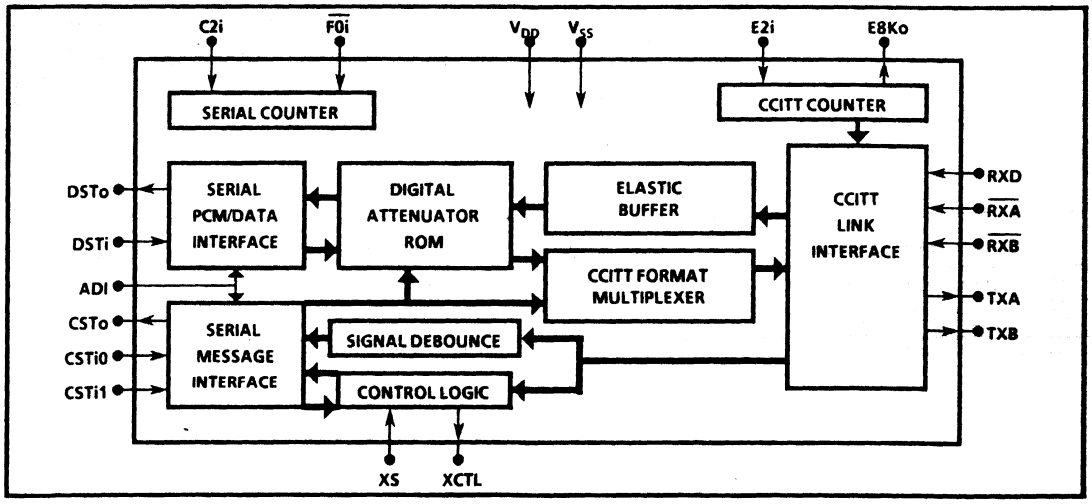


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7	V
2	Voltage at Digital Inputs	V_I	-0.3	V_{DD} + 0.3	V
3	Current at Digital Inputs	I_I		30	mA
4	Voltage at Digital Outputs	V_O	-0.3	V_{DD} + 0.3	V
5	Current at Digital Outputs	I_O		30	mA
6	Storage Temperature	T_{ST}	-65	150	°C
7	Power Dissipation	P		800	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		85	°C	
2	Supply Voltage	V_{DD}	4.5	5	5.5	V	
3	Input Voltage High	V_H	2.4		V_{DD}	V	For 400 mV noise margin
4	Input Voltage Low	V_L	V_{SS}		0.4	V	For 400 mV noise margin

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Power Dissipation	P		31.5	82.5	mW	Outputs unloaded
2	Supply Current	I_{DD}		8	15	mA	Outputs unloaded
3	Input High Voltage	V_{IH}	2.0		V_{DD}	V	
4	Input Low Voltage	V_{IL}	0		0.8	V	
5	Input Leakage	I_{IL}		1	10	uA	
6	Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = 10 mA @ V_{OH} = 2.4 V
7	Output High Current	I_{OH}	10	20		mA	Source. V_{OH} = 2.4 V
8	Output Low Voltage	V_{OL}	V_{SS}		0.4	V	I_{OL} = 2 mA @ V_{OL} = 0.4 V
9	Output Low Current	I_{OL}	2	10		mA	Sink. V_{OL} = 0.4 V
10	High Impedance Leakage	I_{OZ}		1	10	uA	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Capacitances

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Pin Capacitance	C_I		8		pF	
2	Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figures 2 and 3)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C2i Clock Period	t_{P20}	400	488	600	ns	
2	C2i Clock Width High or Low	t_{W20}	200	224	300	ns	
3	Frame Pulse Set Up Time*	t_{FPS}	65	-10		ns	
4	Frame Pulse Hold Time*	t_{FPH}	50	5		ns	
5	Frame Pulse Width*	t_{FPW}	100	224		ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Frame pulse is repeated every 125 µs in synchronisation with the clock.

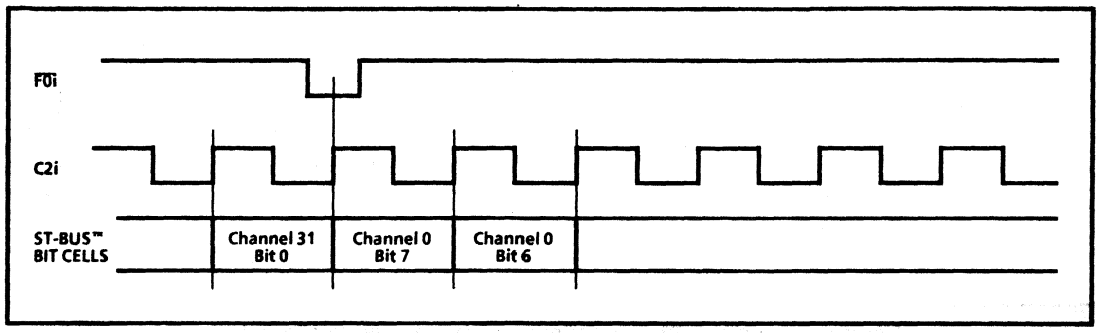


Figure 2 - Clock and Frame Alignment for 2048 kbit/s ST-BUS™ Streams

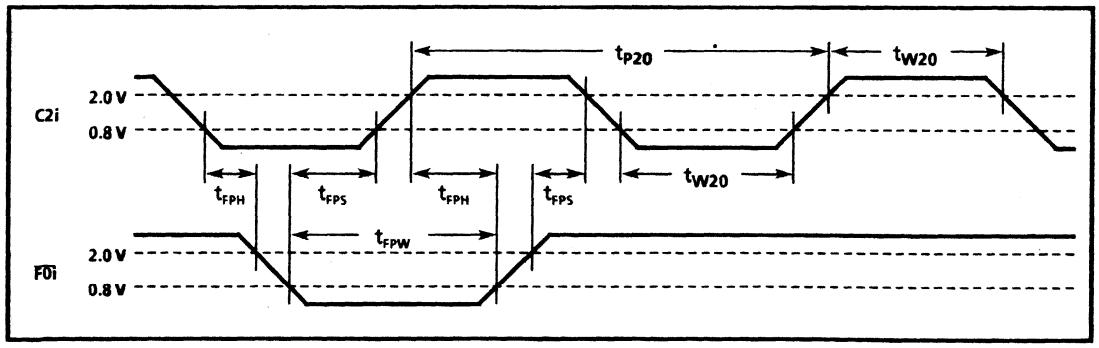


Figure 3 - Clock and Frame Timing for 2048 kbit/s ST-BUS™ Streams

AC Electrical Characteristics† - Timing for CEPT Link Bit Cells (Figure 4)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	E2i Clock Period	t_{PEC}	400	488	600	ns	
2	E2i Clock Width High or Low	t_{WEC}	200	224	300	ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

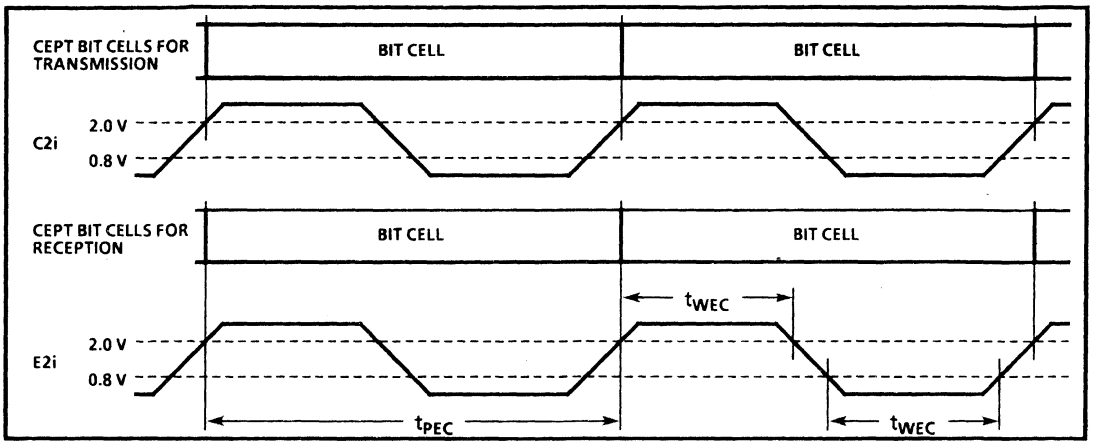


Figure 4 - Timing of CEPT Link Bit Cells for Transmission and Reception

AC Electrical Characteristics† - 2048 kbit/s ST-BUS™ Streams (Figure 5)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Serial Output Delay	t_{SOD}		50	125	ns	150 pF load
2	Serial Input Set-up Time	t_{SIS}	30	0		ns	
3	Serial Input Hold Time	t_{SIH}	55	10		ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

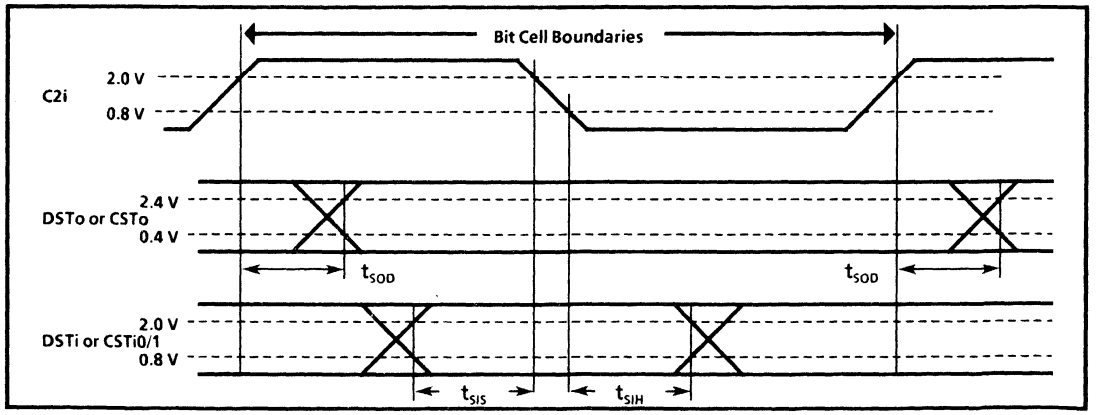


Figure 5 - 2048 kbit/s ST-BUS™ Streams

AC Electrical Characteristics† - XCTL, XS AND E8Ko (Figures 6, 7 and 8)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	External Control Delay	t_{XCD}		35	100	ns	50 pF load
2	External Status Set-up Time	t_{XSS}	50	0		ns	
3	External Status Hold Time	t_{XSH}	50	0		ns	
4	E8Ko Output Delay	t_{8OD}		45	115	ns	50 pF load
5	E8Ko Output Low Width	t_{8OL}		62.5		us	50 pF load
6	E8Ko Output High Width	t_{8OH}		62.5		us	50 pF load
7	E8Ko Output Transition Time	t_{8OT}		10		ns	50 pF load

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

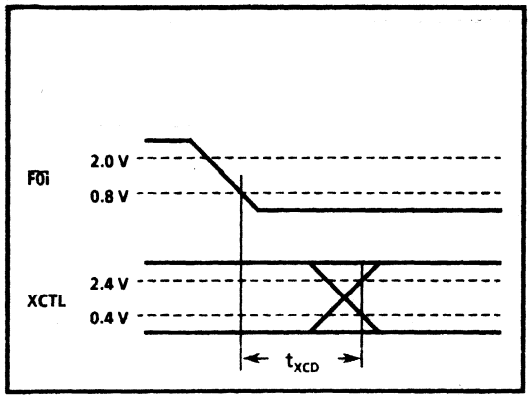


Figure 6 - XCTL Timing

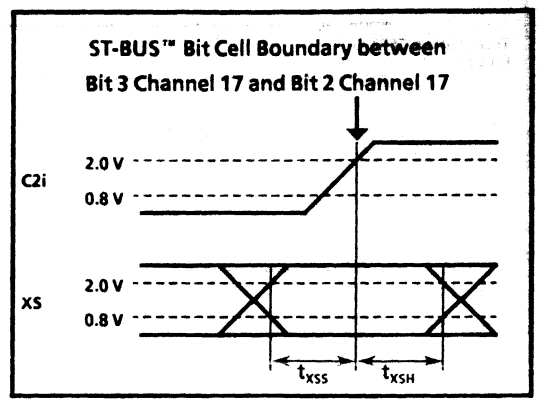


Figure 7 - XS Timing

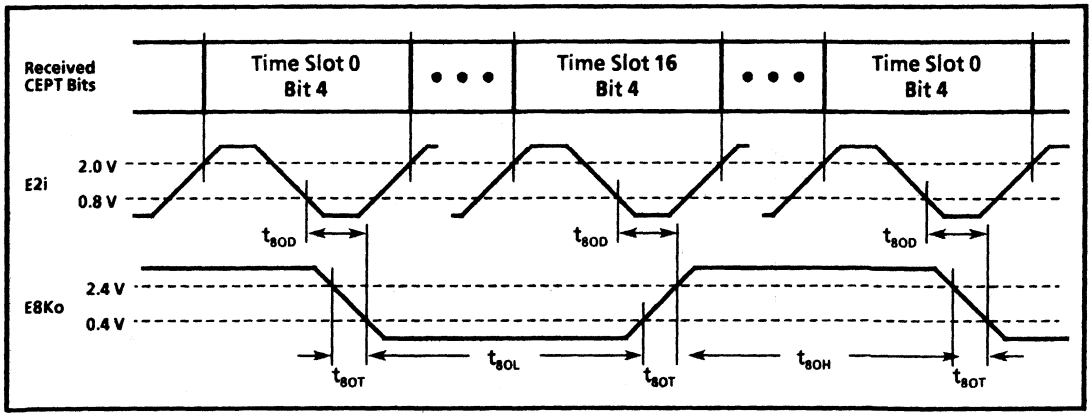


Figure 8 - E8Ko Timing

AC Electrical Characteristics† - CEPT Link Timing (Figures 9 and 10)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit Steering Delay*	t_{TSD}		50	150	ns	200 pF load
2	Transmit Sterring Transistion Time	t_{TST}	30			ns	
3	Receive Data Set-up Time	t_{RDS}	60			ns	
4	Receive Data Hold Time	t_{RDH}	30			ns	
5	Receive Steering Set-up Time	t_{RSS}	60			ns	
6	Receive Steering Hold Time	t_{RSH}	60	10		ns	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* The difference between t_{TSD} for TXA and TXB is typically 20 ns.

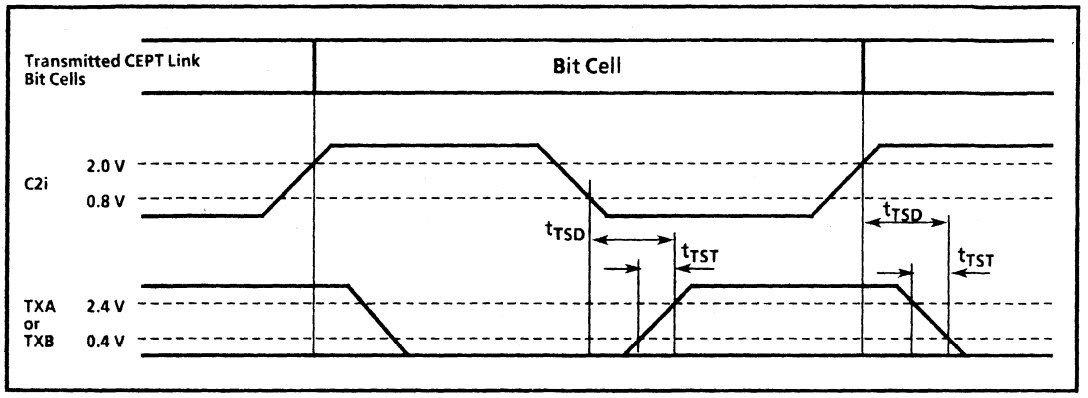


Figure 9 - Transmit Timing for CEPT Link

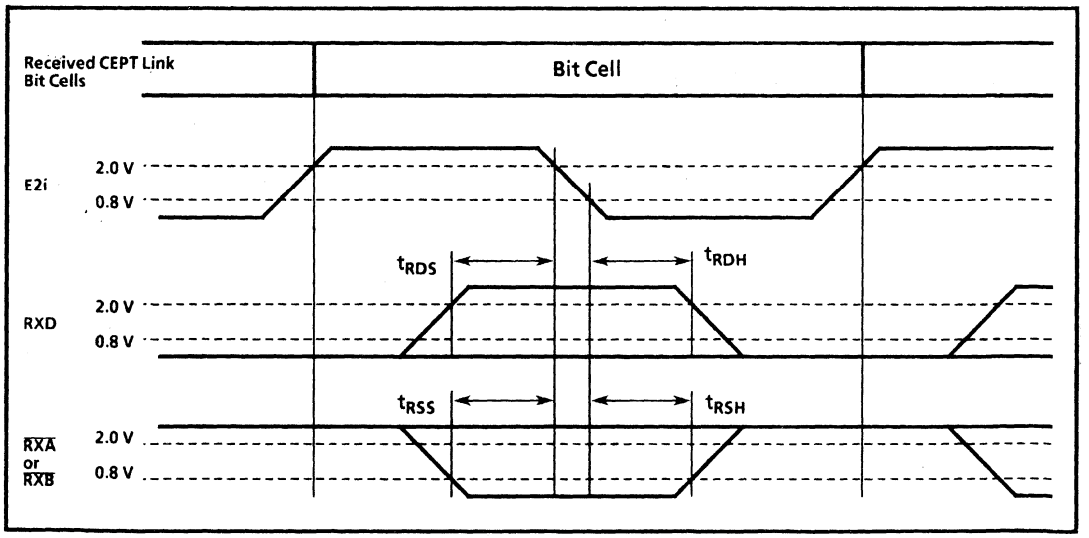


Figure 10 - Receive Timing for CEPT Link

Pin Description

Pin #	Name	Description
1/2	TXA / TXB	**Transmit A & B (Outputs).** These two outputs can be used to control the line driver for the CEPT link.
3	DSTo	**Data ST-BUS™ Out (Output).** This ST-BUS™ stream output contains the 30 PCM or data channels received on 30 of the 32 time slots of the CEPT link.
4/5	$\overline{RXA}$ / $\overline{RXB}$	**Receive A & B (Inputs).** Split phase unipolar inputs used to sense bipolar violation and zero code on the HDB3-encoded CEPT link.
6	RXD	**Receive Data (Input).** This is the input for the data received on the CEPT link. It is produced by gating $\overline{RXA}$ and $\overline{RXB}$ with an external NAND gate.
7	CSTi1	**Control ST-BUS™ In 1 (Input).** This is the input for the ST-BUS™ stream which contains the signalling and alignment information.
8	CSTi0	**Control ST-BUS™ In 0 (Input).** This is the input for the ST-BUS™ stream which controls the chip and contains the information for the digital attenuation of each channel.
9	E8Ko	**Extracted 8 kHz (Three-state Output).** This output provides an optional 8 kHz clock synchronized to the extracted clock input, E2i. A control bit in the CSTi0 stream determines whether this output is active or is high impedance.
10	V_{SS}	**Power Input.** Negative supply (ground).
11	XCTL	**External Control (Output).** This output provides the data received on one of the bits on a channel on CSTi0.
12	XS	**External Status (Input).** Data presented on this input is transmitted as a bit on one of the channels on CSTo.
13	CSTo	**Control ST-BUS™ Out (Output).** This output gives an ST-BUS™ stream which contains signalling and status information.
14	ADI	**Alternate Digit Inversion (Input).** If this input is high, then CEPT time slots which are specified on CSTi0 to be speech are ADI [Alternate Digit Inversion] coded and decoded. This feature allows either ADI or non-ADI codecs to be used on DSTi and DSTo.
15	DSTi	**Data ST-BUS™ In (Input).** This is the input for the ST-BUS™ stream which contains the 30 PCM or data channels for transmission on 30 of the 32 time slots of the CEPT link.
16	C2i	**2.048 MHz Clock (Input).** This is the input to the counter for the ST-BUS™ streams.
17	E2i	**Extracted 2048 kHz Clock (Input).** This is the input for the 2048 kHz clock extracted from the data received on the CEPT link. This clock controls the sampling of received data at the CEPT link interface.
18	$\overline{F0i}$	**Framing Signal Type 0 (Input).** This is the input for the frame synchronization pulse for the ST-BUS™ streams. A low on this input causes the serial counter to reset on the next positive transition of the C2i clock input.
19	IC	**Internal Connection.** Tie to V_{SS} for normal operation.
20	V_{DD}	**Power Input.** Positive supply.

Functional Description

The MT8978 provides an interface between a bidirectional 2048 kbit/s CEPT primary TDM transmission link and 2048 kbit/s ST-BUS™ PCM/Data and control streams.

The serial PCM voice or data arriving at DSTi is converted to 8-bit bytes at the serial PCM/Data interface. These bytes can be ADI [Alternate Digit Inversion] coded if required. Each channel can be digitally attenuated before being merged with the signalling and alignment channels in the CEPT format multiplexer. The data is HDB3 [High Density Bipolar No. 3] coded and the bipolar steering for the line driver is output on TXA and TXB.

Data arriving on the CEPT link is HDB3-decoded, then separated into PCM/Data channels and signalling channels. The PCM/Data stream is passed through an elastic buffer to allow for fluctuations in the data rates. It may be digitally attenuated or ADI decoded before emerging on the DSTo pin.

The signalling information from the CEPT link is debounced before being merged with the status information for the chip which contains the data representing the state of the XS pin. The multiplexed status and signalling information emerges as the ST-BUS™ stream on CSTo.

The CSTi1 ST-BUS™ stream is used to provide signalling and alignment information for the CEPT link, while the CSTi0 stream is used to control independent PCM/Data time slots and the XCTL pin.

Synchronization of the system using the interface may be simplified by the E8Ko pin. This provides a clock with a period corresponding to 256 cycles of the extracted clock, E2i. This period is equivalent to the time taken for a frame of 32 time slots to arrive on the CEPT link.

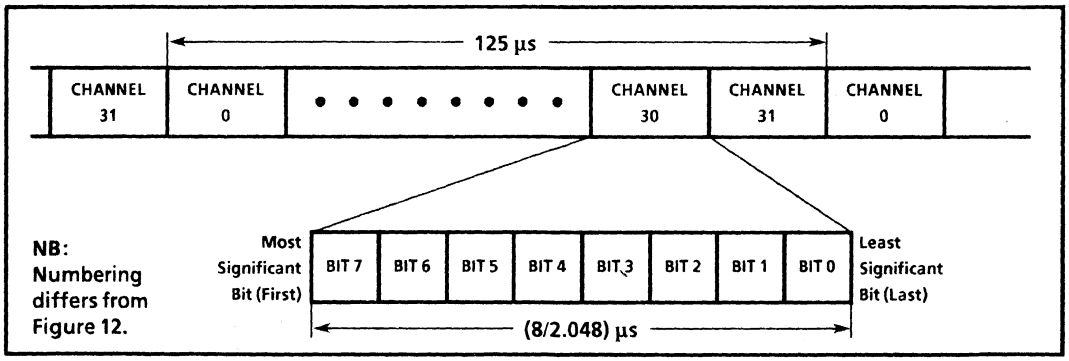


Figure 11 - ST-BUS™ Stream Format

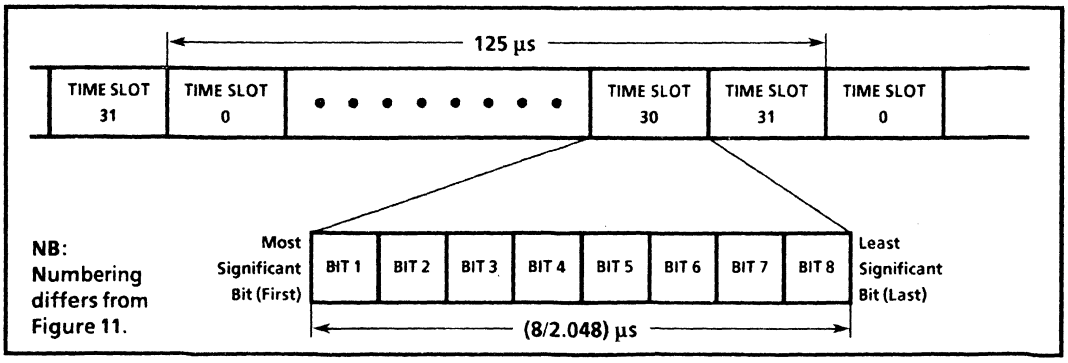


Figure 12 - CEPT Link Frame Format

Frame Formats

Frames on the ST-BUS™ streams consist of 32 channels, numbered from 0 to 31, and each channel contains 8 bits numbered from 7 to 0. Bit 7 of channel 0 is the first bit transmitted in each frame. and frames are 125 µs long (see Figure 11).

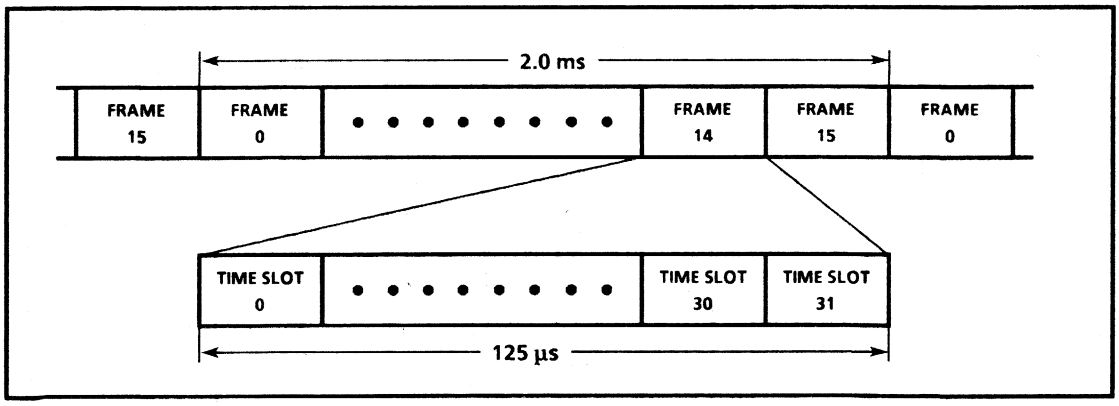
Frames on the CEPT link are similar to frames on the ST-BUS™, but consist of 32 time slots numbered 0 to 31 and the individual bits within each time slot are numbered from 1 to 8 (see Figure 12). Within each frame, time slots 0 and 16 are reserved for alignment and signalling. This leaves time slots 1 to 15 and 17 to 31 transparent for voice or data. These form telephone channels 1 to 30.

Frame-alignment frames and non-frame-alignment frames occur alternatively on the CEPT link. Frame-alignment frames contain the frame alignment signal (0011011) on bits 2 to 8 of time slot 0, whereas in non-frame-alignment frames bit 2 of time slot 0 is 1 and bits 3 to 8 are used to give an alarm and for national signalling. Bit 1 of both types of frame is used for international signalling (see Figure 13).

Frames are numbered from 0 to 15 and are grouped together to form multiframes as shown in Figure 14. Frame 0 of the 16-frame multiframe can be identified by the presence of 4 zeros on bits 1 to 4 of time slot 16. The remaining bits carry multiframe signalling. Time slot 16 of frames 1 to 15 of the multiframe carry the A, B, C and D signalling bits associated with the 30 telephone channels (time slots 1 to 15 and 17 to 31), as shown in Figure 15.

	Bit Number							
	1	2	3	4	5	6	7	8
Time slot 0 containing the frame alignment signal	Reserved for international use	0	0	1	1	0	1	1
Time slot 0 not containing the frame alignment signal	Reserved for international use	1	Alarm indication to the remote PCM multiplex equipment	Reserved for national use				

Figure 13 - Allocation of Bits in Time Slot 0 of the CEPT Link



Figrure 14 - CEPT Link Multiframe Format

Time slot 16 of frame 0		Time slot 16 of frame 1			Time slot 16 of frame 15	
0000	XYXX	ABCD bits for telephone channel 1 (time slot 1)	ABCD bits for telephone channel 16 (time slot 17)	• • •	ABCD bits for telephone channel 15 (time slot 15)	ABCD bits for telephone channel 30 (time slot 31)

Figure 15 - Allocation of Bits in Time Slot 16 of the CEPT Link

Note: No Functional Timing Relationship is Implied by these Figures

DSTi	0 X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16 X	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CEPT		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

Figure 16. Relationship between Input DSTi Time Slots and Transmitted CEPT Channels

(X Denotes Unused DSTi Channels)

DSTO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CEPT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Figure 17. Relationship between Received CEPT Time Slots and Output DSTo Channels

CSTi0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15 C	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31 C
CEPT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 18. Relationship between Input CSTi0 Channels and Controlled CEPT Time Slots

CSTI1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18 X	19 X	20 X	21 X	22 X	23 X	24 X	25 X	26 X	27 X	28 X	29 X	30 X	31 X
CEPT FRAME# channel #	0 16	1 16	2 16	3 16	4 16	5 16	6 16	7 16	8 16	9 16	10 16	11 16	12 16	13 16	14 16	15 16	A 0	N 0														

Figure 19. Relationship between Input CSTi1 channels and Transmitted CEPT Frames

(x Denotes Unused CSTi1 Channels)

(A denotes Frame-Alignment Frames - N denotes Non-Frame Alignment Frames)

CSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18 S	19 T	20 T	21 T	22 T	23 T	24 T	25 T	26 T	27 T	28 T	29 T	30 T	31 T
CEPT FRAME# channel #	0 16	1 16	2 16	3 16	4 16	5 16	6 16	7 16	8 16	9 16	10 16	11 16	12 16	13 16	14 16	15 16	A 0	N 0														

Figure 20. Relationship between Received CEPT Frames and Output CSTo Channels

(T Denotes CSTo Channels which are reserved for testing)

(A Denotes Frame-Alignment Frames - N Denotes Non Frame-Alignment Frames - S Denotes Master Status Channel)

BIT	NAME	DESCRIPTION
7	DATA	If 1, then the controlled time slot on the CEPT 2048 kbit/s link is treated as a data channel; i.e. no ADI encoding or decoding is performed on transmission or reception and the data is not attenuated. If 0, then the ADI pin determines whether or not ADI encoding and decoding is performed and bits 0-5 determine the transmit and receive attenuation. (This bit has precedence over the ADI pin).
6	LOOP	If 1, then the controlled time slot on the transmitted CEPT 2048 kbit/s link is looped internally to replace the data on the corresponding received time slot. If 0, then this function is disabled. This function only operates if frame synchronization is received from the CEPT link and only a single time slot can be looped within the frame.
5,4,3	RXPAD4,2,1	Per time slot receive attenuation control bits RXPAD4 RXPAD2 RXPAD1 Gain (dB) 0 0 0 0 0 0 1 -1 0 1 0 -2 0 1 1 -3 1 0 0 -4 1 0 1 -5 1 1 0 -6 1 1 1 1
2,1,0	TXPAD4,2,1	Per time slot transmit attenuation control bits TXPAD4 TXPAD2 TXPAD1 Gain (dB) 0 0 0 0 0 0 1 -1 0 1 0 -2 0 1 1 -3 1 0 0 -4 1 0 1 -5 1 1 0 -6 1 1 1 1

Table 1 - Data Format on CSTi0 Channels Used for Controlling Time Slots on the CEPT Link

BIT	NAME	DESCRIPTION
7	Test Bit	Keep at 1 for normal operation.
6	LOOP	If 1, then time slot 16 on the transmitted CEPT 2048 kbit/s link is looped internally to replace the data received on time slot 16. If 0, then this function is disabled. This function only operates if frame synchronization is received from the CEPT link and only a single time slot can be looped within the frame.
5-4	Test Bits	Keep at 1 for normal operation.
3, 2, 1 & 0	NDBD, NDBC, NDBB & NDBA	If 1, then no debouncing is applied to the received D, C, B or A signalling bits. If 0, then the received D, C, B or A signalling bits are debounced for between 6 and 8 ms.

Table 2 - Data Format on CSTi0 Channel 15 - Master Control 1

NB. If Common Channel Signalling is selected (see Table 3) then the bits on CSTi0 Channel 15 are redefined in accordance with Table 1.

Monitoring and Control

30 of the 32 channels on the ST-BUS™ stream which is input at the DSTi pin, are transmitted on the CEPT link. Figure 16 shows the correspondence between the channels at DSTi and the time slots on the CEPT link.

The 30 telephone channels received on the CEPT link on time slots 1 to 15 and 17 to 31 are output on the corresponding channels of the DSTo pin as shown in Figure17.

The ST-BUS™ stream which is input at the CSTi0 pin, contains information which controls the CEPT time slots and for master control (see Figure 18). The information which controls the CEPT time slots is input on channels 0 to 14 and 16 to 31 (see Table 1), one channel ahead of the corresponding telephone channel. Master control information is input on channels 15 and 31 (see Table 2 and 3).

The ST-BUS™ stream which is input at the CSTi1 pin, contains the CEPT alignment and signalling information (see Figure 19). Channels 0 to 15 contain the information output on time slot 16 of frames 0 to 15 of the CEPT link's multiframes (see Table 4 and 5). Channels 16 and 17 contain the information transmitted on time slot 0 of the frame-alignment and non-frame-alignment frames of the CEPT link, respectively (see Table 6 and 7).

Channels on CSTo are assigned in a similar way to channels on CSTi1 (see Figure 20). Channels 0 to 15 contain the data received on time slot 16 of frames 0 to 15 of the multiframes (see Table 8 and 9). Channels 16 and 17 contain the data received from the CEPT link on time slot 0 of frame-alignment and non-frame-alignment frames, respectively (see Table 10 and 11). Channel 18 contains the master status information for the chip (see Table 12).

BIT	NAME	DESCRIPTION
7	Test Bit	Keep at 1 for normal operation.
6	Test Bit	Keep at 0 for normal operation.
5	CCS	If 1, then the MT8978 operates in its common channel signalling mode. Channel 16 on the DSTi pin is transmitted on time slot 16 of the CEPT link, and time slot 16 from the received CEPT link is output on channel 16 on the DSTo pin. Channel 15 on the CSTi0 pin contains the information for the control of time slot 16. Channels 0 to 15 on CSTi1 and CSTo are unused. If 0, then this mode is disabled.
4	8KHZSEL	If 1, then an 8 kHz signal synchronized to the received CEPT 2048 kbit/s link is output on the E8Ko pin. This feature only operates when frame synchronization is received from the CEPT link. If 0, then the E8Ko pin goes into its high impedance state.
3	TXAIS	If 1, then an unframed all 1 s alarm signal is transmitted on all time slots. If 0, then the time slots function normally.
2	TXTS16AIS	If 1, then an all 1 s alarm signal is transmitted on time slot 16. If 0, then time slot 16 functions normally.
1	XCTL	If 1, then the XCTL pin is driven high. If 0, then the XCTL pin is driven low.
0	(N/A)	(unused)

Table 3 - Data Format on CSTi0 Channel 31 - Master Control 2

BIT	NAME	DESCRIPTION
7-4	MA1-4	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 1 to 4 of time slot 16 of frame 0 of the multiframe. They should be kept at 0 to allow multiframe alignment to be detected.
3	X1	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 5 of time slot 16 of frame 0 of the multiframe. It is a spare signalling bit which should be kept at 1 if unused.
2	Y	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 6 of time slot 16 of frame 0 of the multiframe. It is used to indicate the loss of multiframe alignment to the remote end of the link. A 1 on this bit is the signal that multiframe alignment on the received link has been lost. A 0 indicates that multiframe alignment is detected.
1,0	X2,X3	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 7 and 8 respectively, of time slot 16 of frame 0 of the multiframe. They are spare signalling bits which should be kept at 1 if unused.

Table 4 - Data Format on CSTi1 Channel 0 Used for Multiframe Alignment (Frame 0) on the Transmitted CEPT Link - cf Figure 15

BIT	NAME	DESCRIPTION
7, 6, 5 & 4	A(N), B(N), C(N) & D(N)	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 1 to 4 of time slot 16 in frame N, and are the A, B, C and D signalling bits associated with telephone channel N. The value of N lies in the range 1 to 15 and refers to the channel on the CSTi1 pin where the bits are supplied, the telephone channel with which the bits are associated, and the frame on the CEPT link on which the bits are transmitted. For example, the bits input on the CSTi1 pin on channel 3 are associated with telephone channel 3, which is time slot 3 of the CEPT link, and are transmitted on bit positions 1 to 4 of time slot 16 in frame 3 of each multiframe on the CEPT link (see Figure 15). If bits B, C or D are not used they should be given the values 1, 0 and 1 respectively. The combination 0000 for ABCD bits should not be used for telephone channels 1 to 15, as this would interfere with multiframe alignment.
3, 2, 1 & 0	A(N + 15), B(N + 15), C(N + 15) & D(N + 15)	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 5 to 8 of time slot 16 in frame N, and are the A, B, C and D signalling bits associated with telephone channel N + 15. The value of N lies in the range 1 to 15 and refers to both the channel on the CSTi1 pin where the bits are supplied and the frame on the CEPT link on which the bits are transmitted, and indirectly indicates the telephone channel with which the bits are associated. For example, the bits input on the CSTi1 pin on channel 3 are associated with telephone channel 18, which is time slot 19 of the CEPT link, and are transmitted on bit positions 5 to 8 of time slot 16 in frame 3 of each multiframe on the CEPT link (see Figure 15).

Table 5 - Data Format on CSTi1 Channels Used for Channel Associated Signalling (Frames 1 to 15) on the Transmitted CEPT Link - cf Figure 15

BIT	NAME	DESCRIPTION
7	IU0	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 1 of time slot 0 of frame-alignment frames (see Figure 13). It is reserved for international signalling and should be kept at 1 when not in use.
6-0	FAF2-8	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 2 to 8 of time slot 0 of frame-alignment frames (see Figure 13). These bits form the frame alignment pattern and should be set to 0011011.

Table 6 - Data Format on CSTi1 Channel 16 Used for Frame-Alignment Frames on the Transmitted CEPT Link - cf Figure 13

BIT	NAME	DESCRIPTION
7	IU1	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 1 of time slot 0 of non-frame-alignment frames (see Figure 13). It is reserved for international signalling and should be kept at 1 when not in use.
6	NFAF	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 2 of time slot 0 of non-frame-alignment frames (see Figure 13). In order to differentiate between frame-alignment frames and non-frame-alignment frames, this bit should be kept at 1.
5	ALM	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 3 of time slot 0 of non-frame-alignment frames (see Figure 13). It is used to signal an alarm to the remote end of the CEPT link. The bit should be set to 1 to signal an alarm and should be kept at 0 under normal operation.
4-0	NU1-5	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 4 to 8 of time slot 0 of non-frame-alignment frames (see Figure 13). These bits are reserved for national signalling, and on crossing national borders they should be set to 1.

Table 7 - Data Format on CSTi1 Channel 17 Used for Non-Frame-Alignment Frames on the Transmitted CEPT Link - cf Figure 13

BIT	NAME	DESCRIPTION
7	$\overline{\text{TFSYN}}$	This bit goes to 1 to signal that the device has lost frame synchronization on the received CEPT 2048 kbit/s link. It goes to 0 when frame synchronization is detected.
6	$\overline{\text{MFSYN}}$	This bit goes to 1 to signal that the device has lost multiframe synchronization on the received CEPT 2048 kbit/s link. It goes to 0 when multiframe synchronization is detected.
5	ERR	This bit changes states after 16 or more errors on the frame alignment synchronization byte within a sample periode of 128 ms.
4	SLIP	This bit changes state when a slip occurs between the received CEPT 2048 kbit/s link and the 2048 kbit/s TDM busses.
3	RXAIS	This bit goes to 1 to signal that an unframed all-ones alarm signal has been detected on the received CEPT 2048 kbit/s link. It goes to 0 when the alarm indicator signal is removed.
2	RXTS16AIS	This bit goes to 1 to signal that an all-ones alarm signal has been detected on channel 16 of the received CEPT 2048 kbit/s link. It goes to 0 when the alarm indicator signal of channel 16 is removed.
1	XS	This bit contains the data sampled once per frame at the XS pin.
0	(N/A)	(unused)

Table 12 - Data Format on CSTo Channel 18 - Master Status

Notes

ST-BUS™ FAMILY MH89780
CEPT Digital Trunk Hybrid
Preliminary Information

9161-002-040 NA ISSUE 2 JUNE 1986

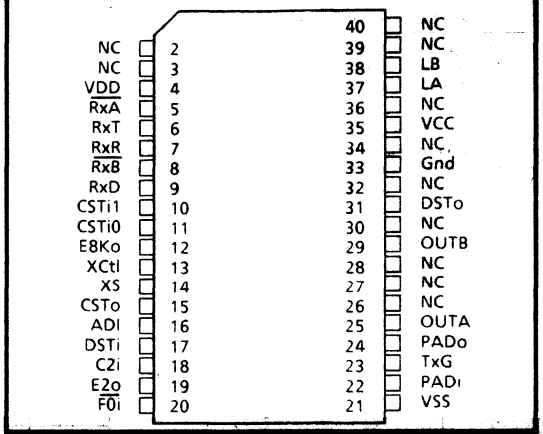
Features

- MITEL ST-BUS compatible
- Interface between a 2048 kb/s,(ST-BUS), serial stream and a bidirectional CEPT Digital Trunk
- Compatible with CCITT G.732
- Insertion of framing/alignment information
- 2 frame Elastic Buffer
- Optional insertion/detection of signalling
- Frame and Multi Frame error/alarm detection
- HDB3 Zero code replacement
- AMI coding and decoding
- Optional ADI coding and decoding
- Per channel: digital attenuation, & loop back
- DMI and CPI compatible
- 2.048 Mhz Clock Extraction from received line
- Line Driver and Receiver
- 8Khz network synchronization output

Applications

- PBX or computer to CEPT Digital Trunk
- High speed data link using CEPT Digital trunk
- TDM multiplexers

Pin Connections



Ordering Information

MH89780 40 pin DIL Hybrid
0°C to 70°C

Description

The MH89780 provides a complete interface between 2048 Kb/s (ST-BUS) serial data and a 2048 kb/s bidirectional CEPT link. In an ST-BUS based system, this thick film hybrid converts the 30 active ST-BUS channels to 30 channels, plus signalling and frame alignment, yielding 2048 kb/s CEPT format.

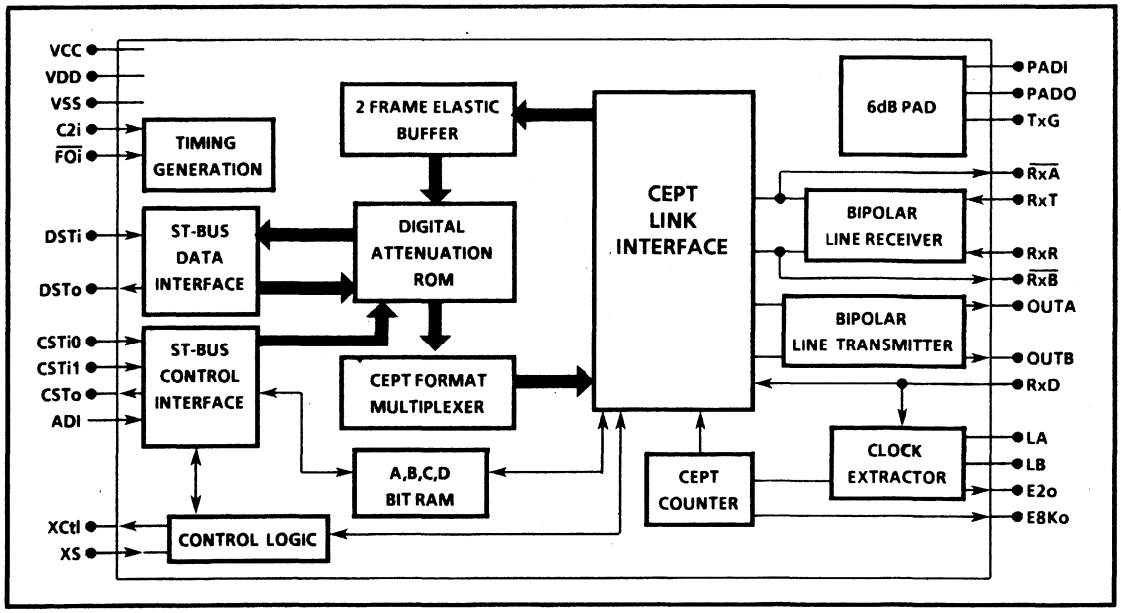


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power Supplies	V_{CC}	-0.3	15	V
	With respect to V_{SS}	V_{DD}	-0.3	7	V
2	Voltage on any pin other than supplies		V_{SS}-0.3	V_{DD} + 0.3	V
3	Current at any pin other than supplies			40	mA
4	Storage Temperature	T_{ST}	-20	85	°C
5	Package Power Dissipation	P		800	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Operating Temperature	T_{OP}	0		70	°C	
2	I	Power Supplies	V_{CC}	11.4	12	12.6	V	
	N		V_{DD}	4.5	5.0	5.5	V	
3	P	Input High Voltage	V_{IH}	2.4		V_{DD}	V	For 400 mV noise margin
	U		V_{IH}		3.0		V	RxT and RxR
4	T	Input Low Voltage	V_{IL}	V_{SS}		0.4	V	For 400 mV noise margin
	S		V_{IL}			0.3	V	RxT and RxR

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Clocked operation over recommended temperature ranges and power supply voltages

		Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Inputs	Supply Current	I_{CC}		10	20	mA	Outputs Unloaded
			I_{DD}		15	30	mA	Outputs Unloaded
2		Input High Voltage	V_{IH}	2.0			V	Digital Inputs
3		Input Low Voltage	V_{IL}			0.8	V	Digital Inputs
4		Input Leakage Current	I_{IL}		± 1	± 10	µA	Digital Inputs V_{IN} = 0 to V_{DD}
5	Outputs	Output High Voltage Digital	V_{OH}	2.4			V	I_{OL} = 10mA
6		Output High Leakage	I_{OZ}			500	nA	V_O = 0 to V_{DD}
7		Output High Current Digital	I_{OH}	10	20		mA	Source Current V_{OH} = 2.4V
		E2o	I_{OH}	8	16		mA	Source Current V_{OH} = 3.0V
8		Output Low Voltage Digital	V_{OL}			0.4	V	I_{OL} = 2mA
		OUTA or OUTB	V_{OL}			.25	V	I_{OL} = 10mA
9		Output Low Current Digital	I_{OL}	2	10		mA	Sink Current V_{OL} = 0.4V
		E2o	I_{OL}	6	30		mA	Sink Current V_{OL} = 2.0V
10		Input Impedance RxT to RxR			400		Ω	
		RxT or RxR to Gnd			1K		Ω	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Functional Timing Diagram

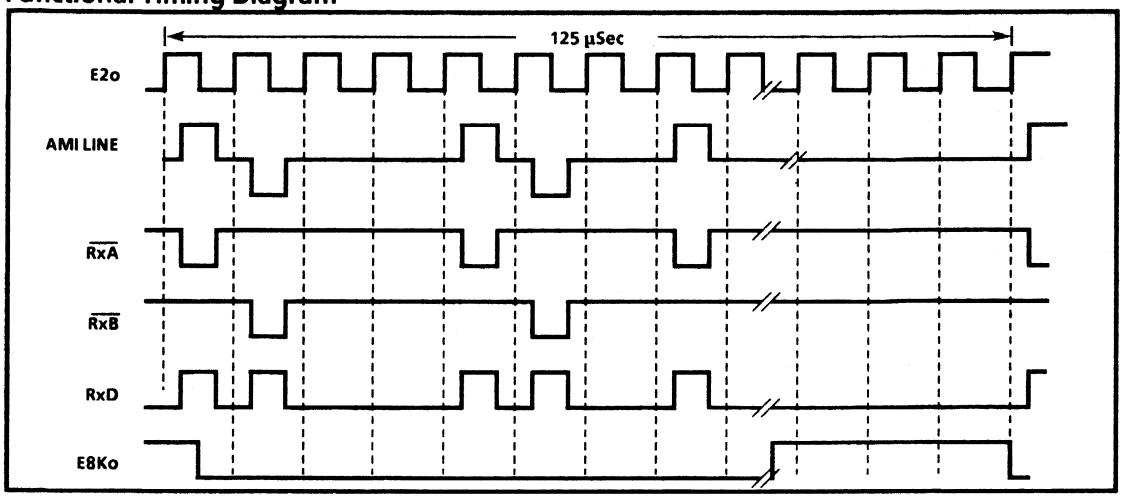


Figure 2a. CEPT Receive Timing

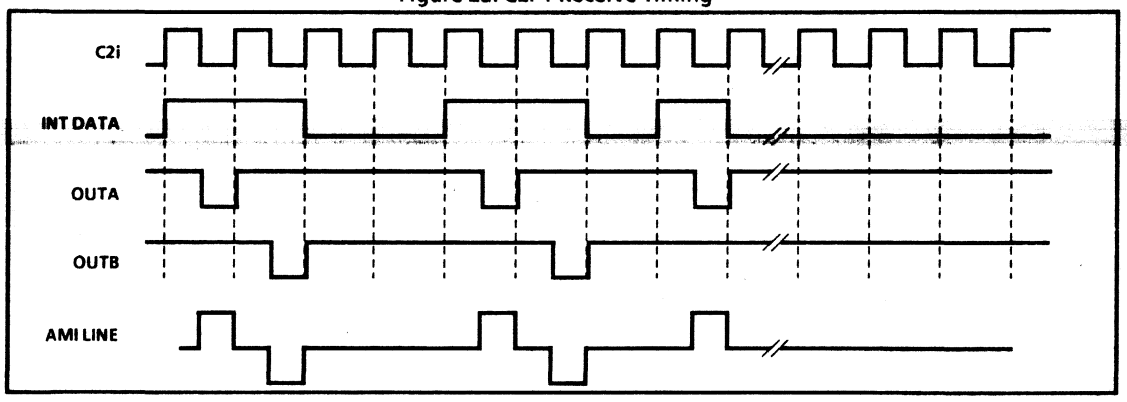


Figure 2b. CEPT Transmit Timing

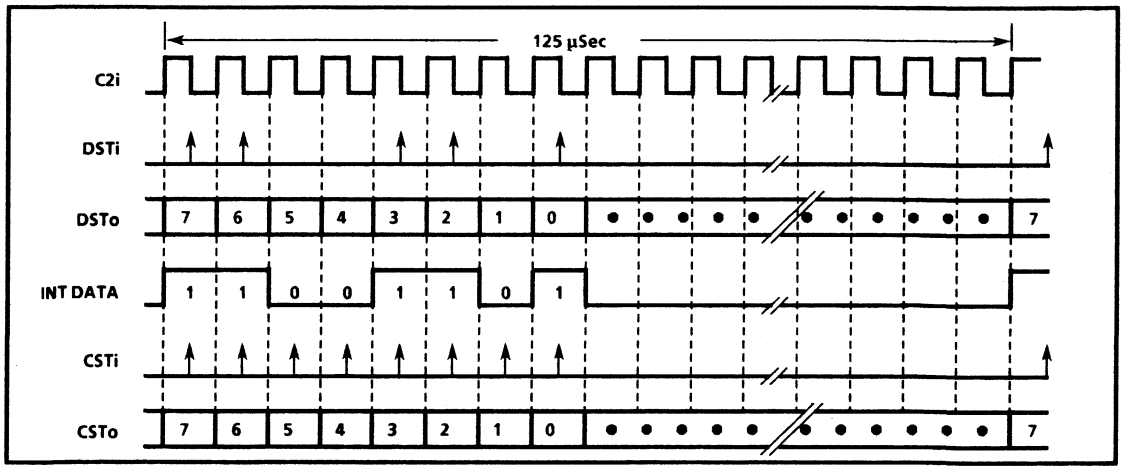


Figure 3. ST-BUS Timing

AC Electrical Characteristics† - Capacitance

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Pin Capacitance	C_I		10		pF	
2	Output Pin Capacitance	C_O		10		pF	

† Timing is over recommended temperature & power supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figure 4 & 5)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C2i Clock Period	t_{p20}	400	488	600	ns	
2	C2i Clock Width High or Low	t_{W20}	200	244	300	ns	
3	C2i Clock Transition Time	t_{T20}		20		ns	
4	Frame Pulse Set Up Time	t_{FPS}	50			ns	
5	Frame Pulse Hold Time	t_{FPH}	50			ns	
6	Frame Pulse Width	t_{FPW}		244		ns	

NB: Frame Pulse is repeated every 125µs in synchronization with the clock

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

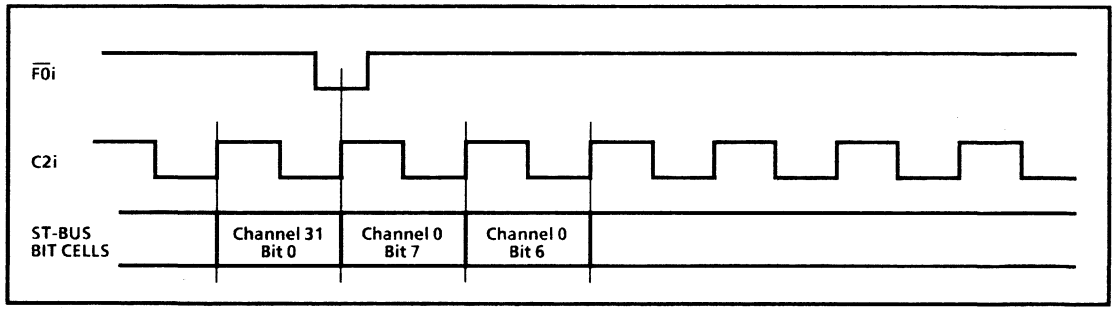


Figure 4. Clock & Frame Alignment for ST-BUS Streams

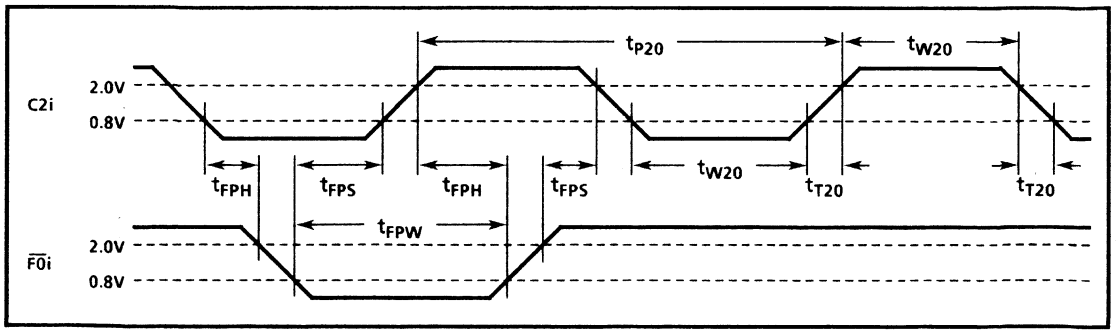


Figure 5. Clock & Frame Pulse Timing for ST-BUS Streams

AC Electrical Characteristics† - Timing For CEPT Link Bit Cells (Figure 6)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	E2o Clock Period	t_{P2EC}		488		ns	
2	E2o Clock Width High or Low	t_{W2EC}		244		ns	
3	E2o Clock Rise Time	t_{R2EC}		60			50 pF load
4	E2o Clock Fall Time	t_{F2EC}		20			50 pF load

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

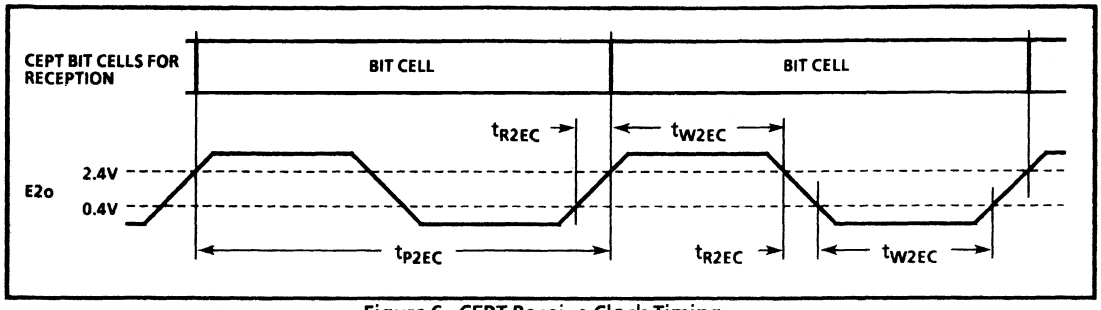


Figure 6. CEPT Receive Clock Timing

AC Electrical Characteristics† - 2048 Kbit/s ST-BUS Streams (Figure 7)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Serial Output Delay	t_{SOD}			125	ns	150pF load
2	Serial Input Set-Up Time	t_{SIS}	30			ns	
3	Serial Input Hold Time	t_{SIH}	55			ns	

†Timing is over recommended temperature & power supply voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

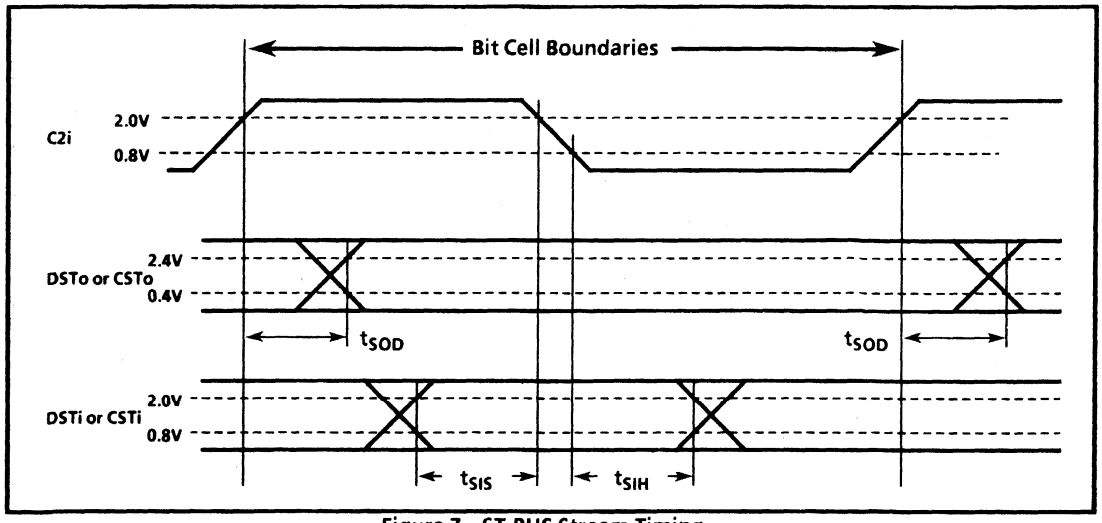


Figure 7. ST-BUS Stream Timing

AC Electrical Characteristics† - XCTL, XS, & E8Ko (Figure 8, 9, & 10)

	CHARACTERISTIC	SYM	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS
1	External Control Delay	t_{XCD}	0	100		ns	50pF load
2	External Status Set-Up Time	t_{XSS}		100		ns	
3	External Status Hold Time	t_{XSH}		100		ns	
4	8KHZ Output Delay	t_{8OD}	0	100		ns	50pF load
5	8KHZ Output Low Width	t_{8OL}		62.5		µs	50pF load
6	8KHZ Output High Width	t_{8OH}		62.5		µs	50pF load
7	8KHZ Rise Time	t_{8R}		20		ns	50pF Load
8	8KHZ Fall Time	t_{8F}		20		ns	50pF Load

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

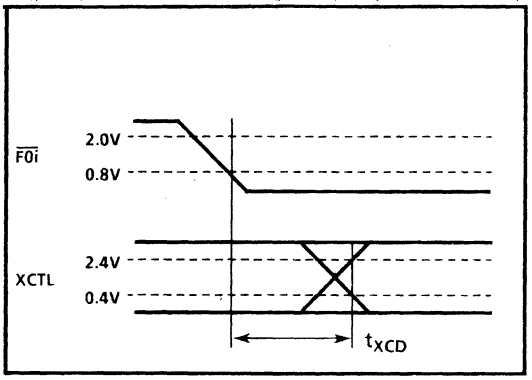


Figure 8. - XCTL Timing

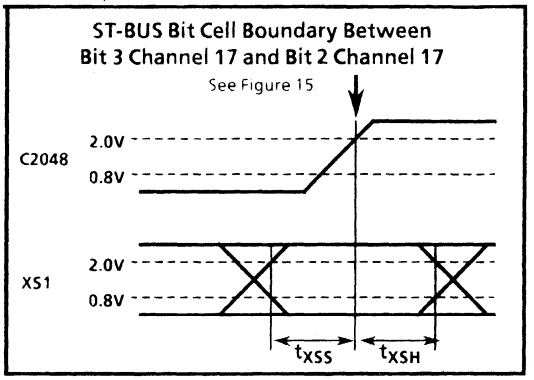


Figure 9. - XS Timing

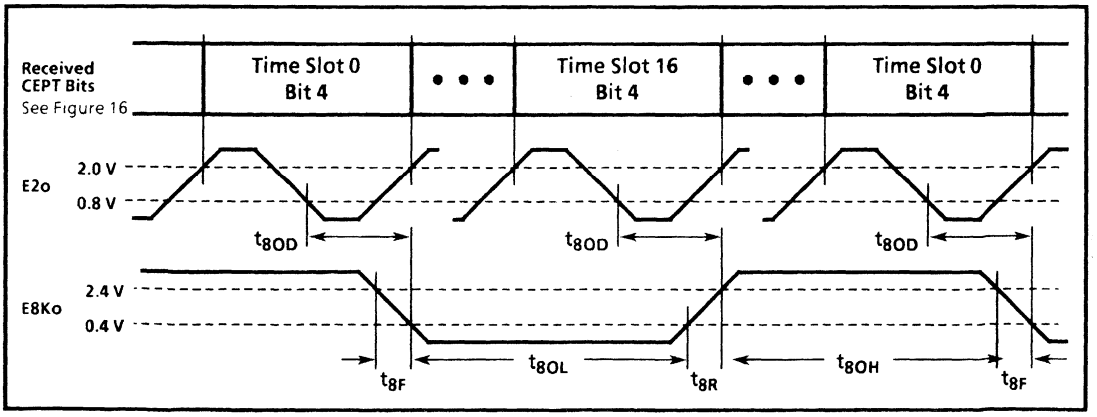


Figure 10. - E8Ko Timing

AC Electrical Characteristics† - CEPT Link Timing (Figure 11 & 12)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Transmit Steering Delay	t_{TSD}	0	150		ns	See Figure 13 see Note 1
2	Received Steering Rise Time	t_{RSR}		20		ns	
3	Received Steering Fall Time	t_{RSF}		20		ns	
4	Received Steering Pulse Width	t_{RSW}		244		ns	
5	Received Data Delay	t_{RDD}			100	ns	
6	Received Data Rise Time	t_{RDR}		20		ns	See Figure 14
7	Received Data Fall Time	t_{RDF}		20		ns	See Figure 14
8	Received Data Set-Up Time	t_{RDS}	100			ns	
9	Received Data Hold Time	t_{RDH}	100			ns	

Note 1: The difference between t_{TSD} for OUTA and OUTB is typically 20 ns.

†Timing is over recommended temperature & power supply voltage ranges.

‡Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

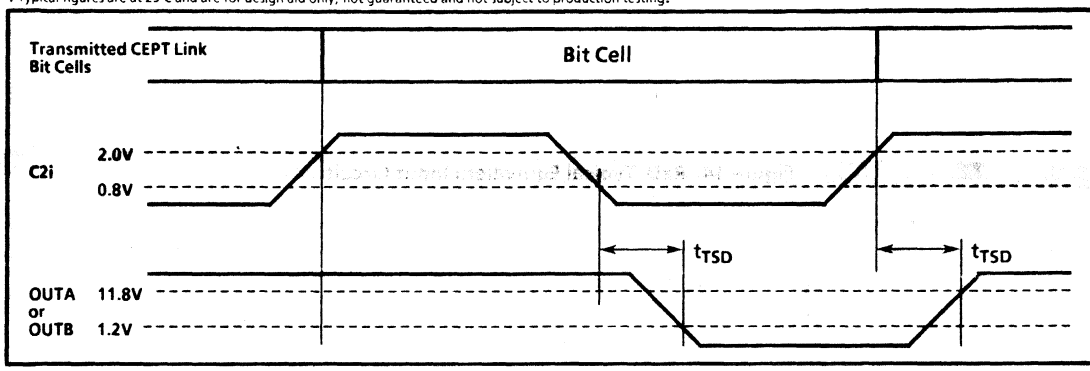


Figure 11. Transmit Timing for CEPT Link

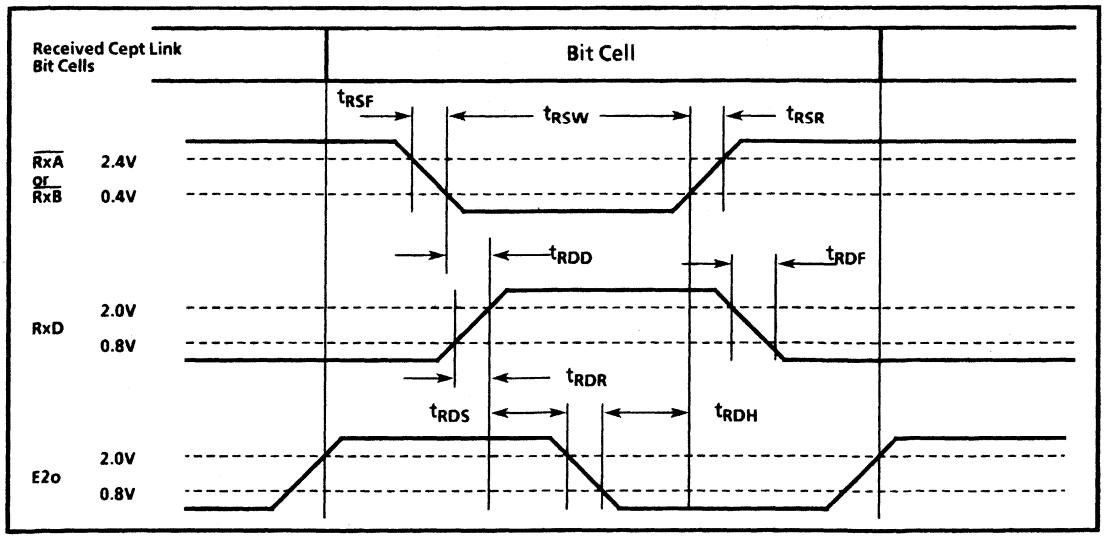


Figure 12. Receive Timing for CEPT Link (see Note 2)

***Note 2:** $\overline{RxA}$ and $\overline{RxB}$ are derived from RxT and RxR which must meet CCITT G.732. The parameters t_{RDS} and t_{RDH} are related to device functionality. Network constraints may require tighter tolerances than the device specifications. The frequency of E2o must be adjusted with the external inductor to meet the device and/or the network tolerances.

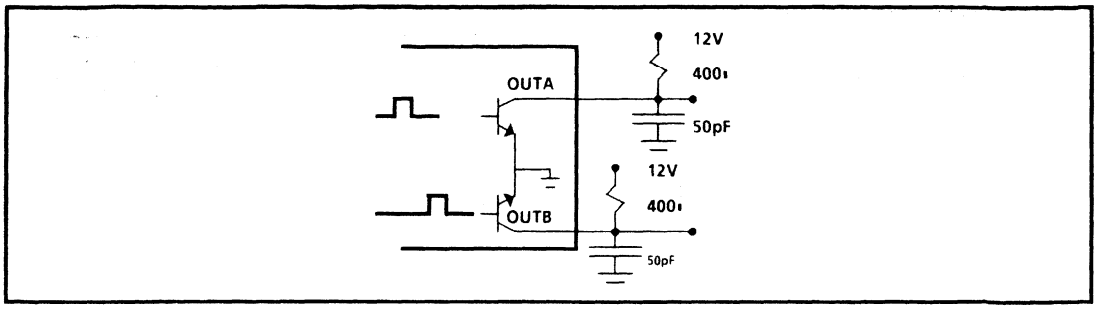


Figure 13. OUTA and OUTB Test Circuit

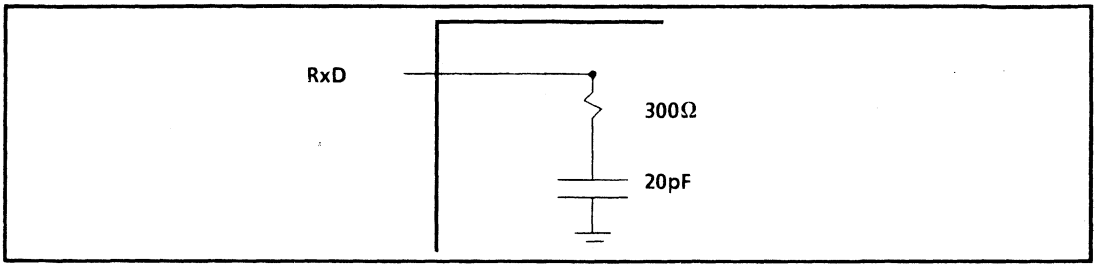


Figure 14. RxD Typical Equivalent Input Circuit

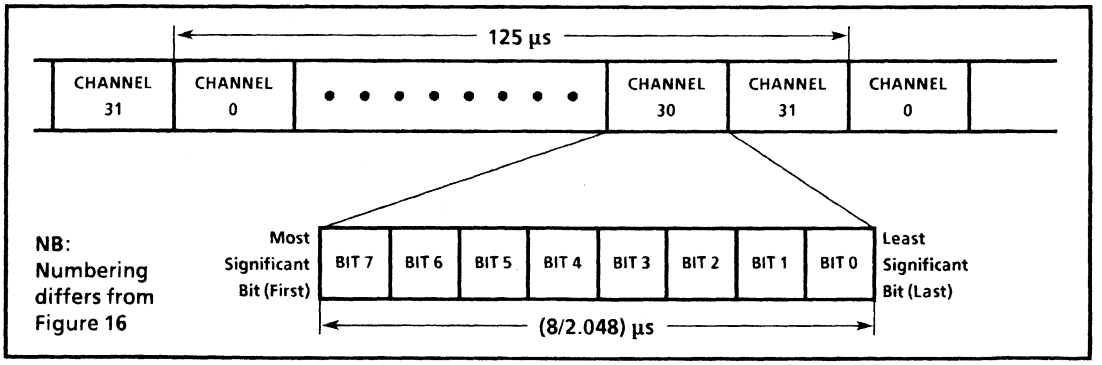


Figure 15. ST-BUS™ Stream Format

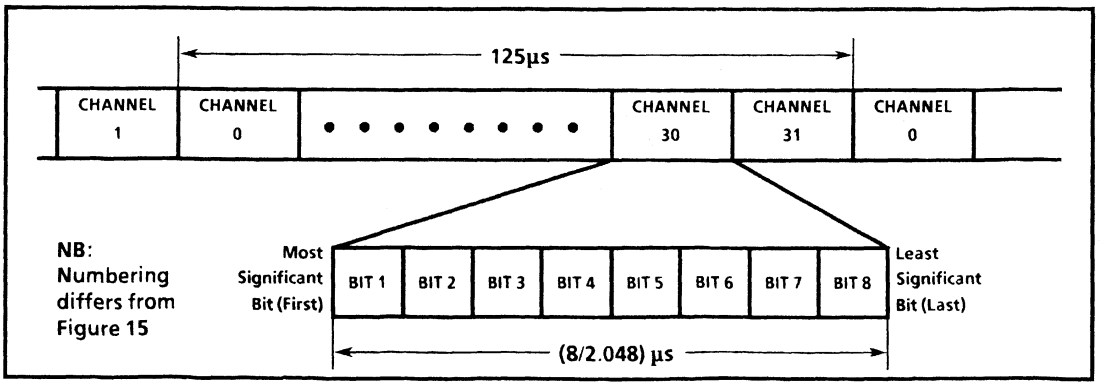


Figure 16. CEPT Link Frame Format

Pin Description

Pin #	Name	Description
2-3	NC	
4	V_{DD}	Digital power supply voltage, + 5 volts.
5	$\overline{RxA}$	Decoded receive side unipolar split phase return to zero output. $\overline{RxA}$ and $\overline{RxB}$ should be connected to the inputs of an external NAND gate used to generate RxD.
6	RxT	Receiver bipolar split phase input from the tip lead of the input transformer.
7	RxR	Receiver bipolar split phase input from the ring lead of the input transformer.
8	$\overline{RxB}$	Decoded receive side unipolar split phase return to zero output. $\overline{RxA}$ and $\overline{RxB}$ should be connected to the inputs of an external NAND gate used to generate RxD.
9	RxD	Received data in a unipolar return to zero format. It is generated by gating $\overline{RxA}$ and $\overline{RxB}$ with an external NAND gate.
10 11	CSTi1 CSTi0	These 2 Control ST-BUS inputs carry per channel settings, signalling, frame synchronization, and interface control information to the interface chip.
12	E8Ko	An 8Khz output that can be used for synchronization to the network. It is enabled by bit 4 on channel 31 of CSTi0.
13	XCtl	External control output is controlled from bit 1 of channel 31 in CSTi0.
14	XS	Uncommitted scan point input . The received status information is output on bit 1 of channel 18 of CSTo.
15	CSTo	A 32 channel message output (30 active) that carries received signalling information and the 2048 Kb/s interface status information.
16	ADI	Alternate digit inversion input , when high, applies ADI coding and decoding to the non data channels . A data channel is defined by bit 8 ch 1-15/17-31 of CSTi0.
17	DSTi	32 channel 2048 Kb/s Data ST-BUS serial input (30 active)
18	C2i	2.048 Mhz master clock input.
19	E2o	2.048 Mhz extracted clock output that is derived from the RxD input.
20	$\overline{F0i}$	8Khz framing pulse, that is 244nsec. wide, used to indicate the start of a 32 channel frame.
21	V_{SS}	System ground.
22 23 24	PADi TXG PADo	These three pins are the input, output, and the ground connections for a 6dB PAD. Input and output impedance is 75Ω.
25	OUTA	Open collector output from the bipolar steering network.
26-28	NC	
29	OUTB	Open collector output from the bipolar steering network.
30	NC	
31	DSTo	32 channel 2048 Kb/s Control ST-BUS serial output (30 active).
32	NC	
33	Gnd	System ground.
34	NC	
35	VCC	Analog power supply voltage, + 12 volts.
36	NC	
37 38	LA LB	An external, manually controlled, inductor is connected between these two pins to adjust the free running frequency of the clock extractor circuit.
39-40	NC	

Functional Description

The MH89780 is a thick film hybrid circuit, which can be used to interface PBX's, computers, or TDM multiplexors to a CEPT digital trunk. It does the conversion from the CEPT format, on the digital line, to the 2.048 Mbit/s serial format of the ST-BUS. The device is capable of accepting inputs from any ST-BUS compatible device, i.e. MT8960/65 voice codec, MT8950 data codec, MT8980/81 digital switch, MH89700 Digital Line Interface Module.

Functions provided by the MH89780 under software control are: digital gain control of transmit and receive paths, per channel loop back, channel definition i.e. a data channel or a voice channel, signalling mode, i.e. common channel or channel associated signalling, debounce of signalling bits in channel associated signalling mode, and transmission/ monitor of all 1's alarms. Information provided by the MH89780 includes; frame synchronization, multiframe synchronization, received all 1's alarms, data slips, and synchronization byte error monitoring. Other functions included on the MH89780 are, 2 frame received elastic buffer, clock extraction to produce a synchronized 2048 MHz clock from the received data, bipolar line drivers and receivers that will interface directly to pulse line transformers, and one uncommitted scan point and drive point for custom applications.

Data enters the device through the serial input Data ST-BUS input (DSTi). The CEPT format is multiplexed into the data stream, and output onto the transmission line through the bipolar line transmitter. Digital attenuation is also added before transmission. All of the control signalling and alarm conditions are inserted by the CEPT link interface and the CEPT format mux.

The received data is decoded by the bipolar line receiver and clocked into the CEPT link interface by the extracted clock (E2o). The E2o clock is supplied by the on board clock extraction circuit. After all of the synchronization, signalling and alarm information has been removed by the CEPT link interface, for output onto the control interface, the information channels enter the elastic buffer. The elastic buffer absorbs the short term variations, or jitter, of the CEPT received data rate. This is required because the system clock frequency, C2i, is very stable with respect to the extracted clock. The elastic buffer also allows the implementation of controlled slips. After passing through the elastic buffer digital attenuation is applied before the information is clocked out of the device by the ST-BUS Data Interface.

	Bit Number							
	1	2	3	4	5	6	7	8
Time slot 0 containing the frame alignment signal	Reserved for international use	0	0	1	1	0	1	1
Time slot 0 containing the nonframe alignment signal	Reserved for international use	1	Alarm indication to the remote PCM multiplex equipment	See Note #3	See Note #3	See Note #3	See Note #3	See Note #3

Figure 17. Allocation of Bits in Time Slot 0 of the CEPT Link

Note 3 : Reserved for National use

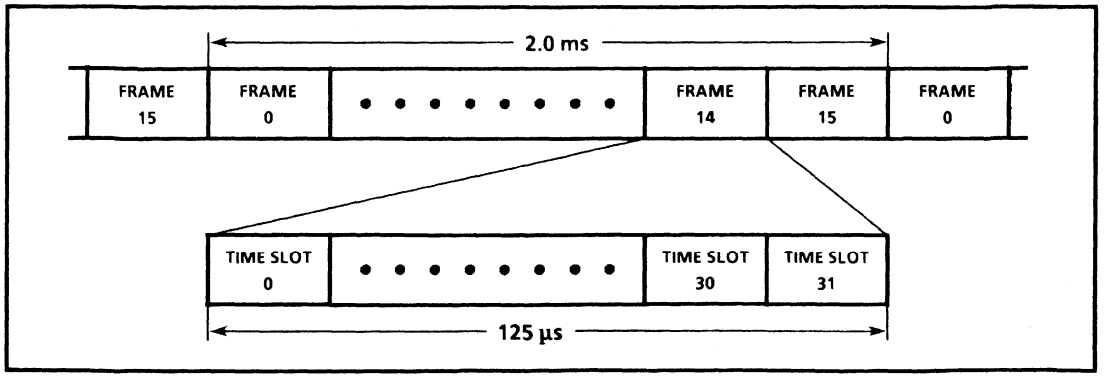


Figure 18. CEPT Link Multiframe Format

Formats

The ST-BUS and the CEPT frame formats are almost the same, and as such they are almost directly compatible. Both systems operate at 2.048MHz and they both contain 32, 8 bit channels for a total of 256 bits per frame. All I/O is done via the serial ST-BUS streams. Note that the ST-BUS and the CEPT bit assignment is different, as shown in Figures 15 and 16.

ST-BUS

The ST-BUS is configured as 32, 8 bit channels with synchronization being supplied by the external 8 Khz frame pulse. Figure 4 shows how the frame pulse ($\overline{F0i}$) defines the ST-BUS frame boundaries. All data is clocked into the device on the falling edge of C2i and clocked out on the rising edge.

CEPT

The CEPT format consists of 32, 8 bit channels, which is defined as one frame. Of the 32 channels in a frame, 30 are defined as information channels, time slots 1-15 and 17-31. Channel 0 is multiplexed as synchronization and signalling, and channel 16 is used for channel associated signalling. Synchronization is included within the CEPT bit stream in the form of a bit pattern inserted into channel 0. The contents of channel 0 alternate between the frame alignment pattern and the non frame alignment pattern. Figure 17 shows the bit assignment in alternate frames of channel 0.

Time slots 1 to 15 and 17 to 31 are the information channels, each containing 64 Kbits of bandwidth. These time slots correspond to voice channels 1-30. The CEPT format has 4 signalling bits, A,B,C,D. Signalling bits for all 30 information channels are transmitted in timeslot 16. In order to accomplish this, a 16 frame multiframe is defined by sending four zeros in the high order nibble of channel 16 once every 16 frames, i.e., frame 0 (see Figure 18). Channel 16 of frames 1 to 15 of the multiframe contain the signalling bits for two information channels. Each frame (n) contains the signalling bits for channel n and channel n + 15, except frame 0 which contains the four zeros, that defines frame 0 of the multiframe, and the XYXX bits.

Data Interface

The MH89780 receives information channels on the DSTi pin. Of the 32 available timeslots on this serial input 30 are defined as information channels. They are timeslots 1-15 and 17-31. These 30 time slots are the 30 channels of the CEPT format numbered 1-15 and 16-30. Channels 0 and 16 are unused to allow the synchronization and signalling information to be inserted, from the Control Interface (CSTi0 and CSTi1), by the MH89780. The relationship between the input and output ST-BUS stream and the CEPT line is illustrated in Figures 20 and 21. Channel 16 becomes an active channel when the MH89780 is in CCS (Common Channel Signalling) mode. In this mode channel 16 on DSTi is transmitted on channel 16 of the CEPT link unaltered.

Control Interface

Control Input 0

All the necessary control and signalling information is input through the two CSTi inputs. Control input number 0 (CSTi0) contains the control information that is associated with each information channel. Each control channel contains the per channel digital attenuation information, the individual loopback control bit, and the voice or data channel identifier, see Table 1. When a channel is in data mode the digital attenuation is disabled, and Alternate Digit Inversion is disabled, independent of the state of the ADI pin. It should be noted that the control word for a given information channel is input one time slot early, i.e., channel 0 of CSTi0 controls channel 1 of DSTi. Channels 15 and 31 of CSTi0 contain Master Control Words 1 and 2, see Tables 2 and 3 for the respective bit functions. Figure 22, shows the relationship between the CSTi0 channels and the CEPT channel controlled.

Time slot 16 of frame 0		Time slot 16 of frame 1			Time slot 16 of frame 15	
0000	XYXX	ABCD bits for telephone channel 1 (time slot 1)	ABCD bits for telephone channel 16 (time slot 17)	• • •	ABCD bits for telephone channel 15 (time slot 15)	ABCD bits for telephone channel 30 (time slot 31)

Figure 19. Allocation of Bits in Time Slot 16 of the CEPT Link

BIT	NAME	DESCRIPTION
7	DATA	If 1, then the controlled time slot on the CEPT 2048 kbit/s link is treated as a data channel; i.e., no ADI encoding or decoding is performed on transmission or reception, and digital attenuation is disabled. If 0, then the ADI pin determines whether or not ADI encoding and decoding is performed.
6	LOOP	If 1, then the controlled time slot on the transmitted CEPT 2048 kbit/s link is looped internally to replace the data on the corresponding received time slot. If 0, then this function is disabled. This function only operates if frame synchronization is received from the CEPT link. If more than one channel is looped per frame only the first one will be active.
5,4,3	RXPAD4,2,1	Per time slot receive attenuation control bits RXPAD4 RXPAD2 RXPAD1 Gain (dB) 0 0 0 0 0 0 1 -1 0 1 0 -2 0 1 1 -3 1 0 0 -4 1 0 1 -5 1 1 0 -6 1 1 1 1
2,1,0	TXPAD4,2,1	Per time slot transmit attenuation control bits TXPAD4 TXPAD2 TXPAD1 Gain (dB) 0 0 0 0 0 0 1 -1 0 1 0 -2 0 1 1 -3 1 0 0 -4 1 0 1 -5 1 1 0 -6 1 1 1 1

Table 1. Data Format on CSTi0 Channels used for Controlling Time Slots on the CEPT Link

BIT	NAME	DESCRIPTION
7	Test Bit	Keep at '1' for normal operation.
6	LOOP	If '1', then time slot 16 on the transmitted CEPT 2048 kbit/s link is looped internally to replace the data received on time slot 16. If '0,' then this function is disabled. This function only operates if frame synchronization is received from the CEPT link and only a single time slot can be looped within the frame.
5,4	Test Bits	Keep at '1' for normal operation.
3,2, 1 & 0	NDBD, NDBC, NDBB & NDBA	If '1', then no debouncing is applied to the received A, B, C or D signalling bits. If '0', then the received A, B, C or D signalling bits are debounced for between 6 and 8 ms.

Table 2. Data Format on CSTi0 Channel 15 - Master Control 1

BIT	NAME	DESCRIPTION
7	Test Bit	Keep at 1 for normal operation.
6	Test Bit	Keep at 0 for normal operation.
5	CCS	If 1, then the MH89780 operates in its common channel signalling mode. Channel 16 on the DSTi pin is transmitted on time slot 16 of the CEPT link, and time slot 16 from the received CEPT link is output on channel 16 on the DSTo pin. Channel 15 on the CSTi0 pin contains the information for the control of time slot 16. Channels 0 to 15 on CSTi1 and CSTo are unused. If 0, the device is in channel associated signalling mode where channel 16 is used to transmit the ABCD signalling bits.
4	8KHZSEL	If 1, then an 8 kHz signal synchronized to the received CEPT 2048 kbit/s link is output on the E8Ko pin. This feature is only valid when frame synchronization is received from the CEPT link. If 0, then the E8Ko pin goes into its high impedance state.
3	TXAIS	If 1, then an all 1's alarm signal is transmitted on all time slots. If 0, then the time slots functions normally.
2	TXTS16AIS	If 1, then an all 1 s alarm signal is transmitted on time slot 16. If 0, then time slot 16 functions normally.
1	XCTL	If 1, then the XCTL pin is driven high. If 0, then the XCTL pin is driven low.
0	(N/A)	(unused)

Table 3. Data Format on CSTi0 Channel 31-Master Control 2

Control Input 1

Control input stream number 1 (CSTi1) contains the synchronization information and the ABCD signalling bits for insertion into channel 16 of the CEPT stream. Channel 0 contains the four zeros of the multiframe alignment pattern plus the XYXX bits, see Table 4. Channels 1 to 15 contain the ABCD signalling bits as defined in CEPT format, see table 5, i.e., channel 1 of CSTi1 contains the ABCD bits for DSTi time slots 1 and 17. Channel 16 contains the frame alignment pattern, and channel 17 contains the nonframe alignment pattern, see Figure 17. Figure 23, shows the relationship between the CSTi1 and the CEPT stream.

BIT	NAME	DESCRIPTION
7-4	MA1-4	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 1 to 4 of time slot 16 of frame 0 of the multiframe. They should be kept at '0' to allow multiframe alignment to be detected.
3	X1	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 5 of time slot 16 of frame 0 of the multiframe. It is a spare bit which should be kept at '1' if unused.
2	Y	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 6 of time slot 16 of frame 0 of the multiframe. It is used to indicate the loss of multiframe alignment to the remote end of the link. A '1' on this bit is the signal that multiframe alignment on the received link has been lost. A '0' indicates that multiframe alignment is detected.
1,0	X2,X3	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 7 and 8 respectively, of time slot 16 of frame 0 of the multiframe. They are spare bits which should be kept at '1' if unused

Table 4 - Data Format on CSTi1 Channel 0 used for Multiframe Alignment (Frame 0) on the Transmitted CEPT Link - cf Fig. 19

BIT	NAME	DESCRIPTION
7, 6, 5 & 4	A(N), B(N), C(N) & D(N)	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 1 to 4 of time slot 16 in frame N, and are the A, B, C and D signalling bits associated with telephone channel N. The value of N lies in the range 1 to 15 and refers to the CSTi1 channel from which the bits are sourced, the telephone channel with which the bits are associated, and the frame on the CEPT link on which the bits are transmitted. For example, the bits input on the CSTi1 pin on channel 3 are associated with telephone channel 3, which is time slot 3 of the CEPT link, and are transmitted on bit positions 1 to 4 of time slot 16 in frame 3 of each multiframe on the CEPT Link (See Fig. 19). If bits B, C or D are not used they should be given the values '1', '0' and '1' respectively. The combination 0000 for ABCD bits should not be used for telephone channels 1 to 15, as this would interfere with multiframe alignment.
3, 2, 1 & 0	A(N + 15), B(N + 15), C(N + 15) & D(N + 15)	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 5 to 8 of time lot 16 in frame N, and are the A, B, C and D signalling bits associated with telephone channel N + 15. The value of N lies in the range 1 to 15 and refers to both the channel on the CSTi1 pin where the bits are supplied and the frame on the CEPT link on which the bits are transmitted, and indirectly indicates the telephone channel with which the bits are associated. For example, the bits input on the CSTi1 pin on channel 3 are associated with telephone channel 18, which is time slot 19 of the CEPT link, and are transmitted on bit positions 5 to 8 of time slot 16 in frame 3 of each multiframe on the CEPT link (See Fig. 19).

Table 5. Data Format on CSTi1 Channels used for Channel Associated Signalling (Frames 1 to 15) on the Transmitted CEPT Link - cf Figure 19

BIT	NAME	DESCRIPTION
7	IU0	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 1 of time slot 0 of frame-alignment frames (see Fig. 17). It is reserved for international use and should be kept at '1' when not used.
6-0	FAF2-8	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 2 to 8 of time slot 0 of frame-alignment frames (see Fig. 17). These bits form the frame alignment pattern and should be set to '0011011'

Table 6 - Data Format on CSTi1 Channel 16 used for Frame-Alignment Frames on the Transmitted CEPT Link - cf Figure 17

BIT	NAME	DESCRIPTION
7	IU1	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 1 of time slot 0 of non-frame-alignment frames (see Fig. 17). It is reserved for international use and should be kept at '1' when not used.
6	NFAF	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 2 of time slot 0 of non-frame-alignment frames (see Fig. 17). In order to differentiate between frame-alignment frames and non-frame-alignment frames, this bit should be kept at '1'.
5	ALM	This bit is transmitted on the CEPT 2048 kbit/s link in bit position 3 of time slot 0 of non frame-alignment frames (see Fig. 17). It is used to signal an alarm to the remote end of the CEPT link. The bit should be set to '1' to signal an alarm and should be kept at '0' under normal operation.
4-0	NU1-5	These bits are transmitted on the CEPT 2048 kbit/s link in bit positions 4 to 8 of time slot 0 of non frame-alignment frames (see Fig. 17). These bits are reserved for national use, and on crossing international borders they should be set to '1'

Table 7. Data Format on CSTi1 Channel 17 used for Non-Frame-Alignment Frames on the Transmitted CEPT Link - cf Fig. 17

Control Output

Control output (CSTo) contains the multiframe pattern from channel 16 of frame 0, see Table 8. Signalling bits, ABCD, for each CEPT channel are sourced from channel 16 of frames 1-15 and are output in time slots 1-15, as shown in Table 9. The frame alignment pattern and nonframe alignment pattern, received from channel 0 of alternate frames are output in time slots 16 and 17, as shown in Tables 10, and 11. The master status word returns to the user all the information needed to determine the operating condition of the CEPT interface i.e., frame synchronization, multiframe synchronization, frame alignment byte errors, slips, alarms, and the external status pin, see Table 12. Figure 24, shows the relationship between the CSTo channels, and the CEPT channels. The error bit in the Master Status word is an indicator of the number of errors that have been received in the frame alignment byte. If there are 16 or more errors received in the frame alignment byte in a period of 128 mSec, then the state of the error bit changes. i.e., If this bit toggles after 1024 mSec there were at least 16 errors in that time period.

BIT	NAME	DESCRIPTION
7-4	MA1-4	These are the bits which are received from the CEPT 2048 kbit/s link in bit positions 1 to 4 of time slot 16 of frame 0 of the multiframe. They should all be '0'.
3	X1	This is the bit which is received on the CEPT 2048 kbit/s link in bit position 5 of time slot 16 of frame 0 of the multiframe. It is a spare bit which should be '1' if unused. It is not debounced.
2	Y	This is the bit which is received on the CEPT 2048 kbit/s link in bit position 6 of time slot 16 of frame 0 of the multiframe. It is used to indicate the loss of multiframe alignment at the remote end of the link. A '1' on this bit is the signal that multiframe alignment at the remote end of the link has been lost. A '0' indicates that multiframe alignment is detected. It is not debounced.
1,0	X2,X3	These are the bits which are received on the CEPT 2048 kbit/s link in bit positions 7 and 8 respectively, of time slot 16 of frame 0 of the multiframe. They are spare bits which should be '1' if unused. They are not debounced

Table 8 - Data Format on CSTo Channel 0, from Multiframe Alignment Frames (Frame 0 Channel 16) on the Received CEPT Link - cf Figure 19

BIT	NAME	DESCRIPTION
7, 6, 5 & 4	A(N), B(N), C(N) & D(N)	These are the bits which are received from the CEPT 2048 kbit/s link in bit positions 1 to 4 of time slot 16 in frame N, and are the A, B, C and D signalling bits associated with telephone channel N. The value of N lies in the range 1 to 15 and refers to the channel on the CSTo pin on which the bits are output, the telephone channel with which the bits are associated and the frame on the CEPT link on which the bits are received.For example, the bits output on the CSTo pin on channel 3 are associated with telephone channel 3, which is time slot 3 of the CEPT link, and are received on bits positions 1 to 4 of time slot 16 in frame 3 of each multiframe on the CEPT link (see Fig. 19). If bits B, C or D are not used they should have the values '1, 0' and '1' respectively. The combination '0000' for ABCD bits should not be found for telephone channels 1 to 15 as this implies interference with multiframe alignment.
3, 2, 1 & 0	A(N + 15), B(N + 15), C(N + 15) & D(N + 15)	These are the bits which are received from the CEPT 2048 kbit/s link in bit positions 5 to 8 of time slot 16 in frame N, and are the A, B, C and D signalling bits associated with telephone channel N + 15. The value of N lies in the range 1 to 15 and refers to both the channel on the CSTo pin where the bits are output and the frame on the CEPT link on which the bits are received, and indirectly indicates the telephone channel with which the bits are are associated. The associated channel is N + 15. For example, the bits output on the CSTo pin on channel 3 are associated with telephone channel 18, which is time slot 19 of the CEPT link, and are received on bits positions 5 to 8 of time slot 16 in frame 3 of each multiframe on the CEPT link (see Fig. 19).

Table 9. Data Format on CSTo Channels used for Channel Associated Signalling (Frames 1 to 15 Channel 16) on the Received CEPT Link - cf Figure 19

BIT	NAME	DESCRIPTION
7	IU0	This is the bit which is received from the CEPT 2048 kbit/s link in bit position 1 of time slot 0 of frame-alignment frames (see Fig. 17). It is reserved for international use and should have the value '1' when unused.
6-0	FAF2-8	These are the bits which are received from the CEPT 2048 kbit/s link in bit positions 2 to 8 of time slot 0 of frame-alignment frames (see Fig. 13). These bits form the frame alignment pattern and should have the values of '0011011'.

Table 10. Data Format on CSTo Channel 16 from Frame-Alignment Frames on the Received CEPT Link - cf Figure 17

BIT	NAME	DESCRIPTION
7	IU1	This is the bit which is received from the CEPT 2048 kbit/s link in bit position 1 of time slot 0 of non frame-alignment frames (see Fig. 17). It is reserved for international use and should have the value '1' when unused.
6	NFAF	This is the bit which is received from the CEPT 2048 kbit/s link in bit position 2 of time slot 0 of non-frame-alignment frames (see Fig. 17). This bit should be '1' in order to differentiate between frame-alignment frames and non-frame-alignment frames.
5	ALM	This is the bit which is received from the CEPT 2048 kbit/s link in bit position 3 of time slot 0 of non-frame-alignment frames (see Fig. 17). It is used to signal an alarm **from the remote end of the CEPT link. This bit should have the value '0' under** normal operation and should go to '1 'to signal an alarm.
4-0	NU1-5	These are the bits which are received on the CEPT 2048 kbit/s link in bit positions 4 to 8 of time slot 0 of non-frame-alignment frames (see Fig. 17). These bits are reserved for national use, and on crossing international borders they should have the value '1'.

Table 11. Data Format on CSTo Channel 17 from Non Frame-Alignment Frames on the Received CEPT Link - cf Figure 17

BIT	NAME	DESCRIPTION
7	$\overline{\text{TFSYN}}$	This bit goes to 1 to indicate a loss of frame synchronization by the MH89780. It goes to '0' when frame synchronization is detected.
6	$\overline{\text{MFSYN}}$	This bit goes to 1 to indicate a loss of multiframe synchronization by the MH89780. It goes to '0' when multiframe synchronization is detected.
5	ERR	This bit changes state after 16, or more, errors of the master frame synchronization byte in a sample period of 128 msec.
4	SLIP	This bit changes state when a slip occurs between the received CEPT 2048 kbit/s link and the 2048 kbit/s ST-BUS.
3	RXAIS	This bit goes to 1 to signal that an unframed all-ones alarm signal has been detected on the received CEPT 2048 kbit/s link. It goes to 0 when the all-ones alarm signal is removed.
2	RXTS16AIS	This bit goes to 1 to signal that an all-ones alarm signal has been detected on channel 16 of the received CEPT 2048 kbit/s link. It goes to 0 when the all-ones alarm signal is removed.
1	XS	This bit contains the data sampled once per frame at the XS pin.
0	(NA)	(UNUSED).

Table 12. Data Format on CSTo Channel 18 - Master Status

Note: No Functional Timing Relationship is Implied by these Figures

DSTi	0 X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16 X	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CEPT		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

Figure 20. Relationship between Input DSTi Time Slots and Transmitted CEPT Channels
(X Denotes Unused DSTi Channels)

DSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CEPT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Figure 21. Relationship between Received CEPT Time Slots and Output DSTo Channels

CSTi0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15 C	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31 C
CEPT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 22. Relationship between Input CSTi0 Channels and Controlled CEPT Time Slots
(C Denotes Master Control Channels)

CSTi1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18 X	19 X	20 X	21 X	22 X	23 X	24 X	25 X	26 X	27 X	28 X	29 X	30 X	31 X
CEPT FRAME#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	A	N														
channel #	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	0	0														

Figure 23. Relationship between Input CSTi1 channels and Transmitted CEPT Frames
(x Denotes Unused CSTi1 Channels)
(A denotes Frame-Alignment Frames - N denotes Non-Frame Alignment Frames)

CSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18 S	19 T	20 T	21 T	22 T	23 T	24 T	25 T	26 T	27 T	28 T	29 T	30 T	31 T
CEPT FRAME#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	A	N														
channel #	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	0	0														

Figure 24. Relationship between Received CEPT Frames and Output CSTo Channels
(T Denotes CSTo Channels which are reserved for testing)
(A Denotes Frame-Alignment Frames - N Denotes Non Frame-Alignment Frames - S Denotes Master Status Channel)

BIPOLAR RECEIVER

The receiver circuit interfaces to the CEPT line through a pulse transformer. A recommended input transformer is shown in the application circuit of Figure 25. The receiver decodes the AMI line into split phase signals $\overline{RxA}$ and $\overline{RxB}$, these two signals must be combined in an external NAND gate to form RxD. The received data is clocked into the interface on the falling edge of E2o. Figure 2a shows the functional timing of the bipolar receiver. With the receive transformer shown in the application circuit of Figure 25, the 300Ω internal impedance presents a 75Ω impedance to the line.

CLOCK EXTRACTOR

The MH89780 contains the clock extraction circuit that generates E2o. This is the clock that is used by the interface to clock information from the RxD input. The falling edge of E2o is aligned with the nominal center of the received data, RxD. In order to tune the clock extractor to 2.048 MHz an external tunable inductor is connected between LA and LB. This completes the tank circuit of the current injection oscillator used in the clock extraction circuit. The range of the inductor should be from 32 to 39μH.

The extracted 8KHz output (E8Ko) is derived from the E2o clock by dividing it by 256. It can be used by an external phase-locked loop to generate the system clock and frame pulse that is synchronized to the network.

To set up the clock extractor the data input at RxD is removed and the free running frequency of the clock extractor is adjusted to 2.048MHz with the tuneable inductor.

BIPOLAR TRANSMITTER

The MH89780 contains the steering logic to perform the AMI line coding, and provides the user with bipolar open collector output drivers. These outputs are suitable for interfacing with a center tapped pulse transformer. OUTA and OUTB are the bipolar steering outputs. Figure 2b illustrates how the two outputs correspond to the opposite polarities of the Alternate Mark Inversion line code. Each output steers the circuit into producing the pulse of the proper polarity. Figure 2b also shows the functional timing of the bipolar transmitter. This type of output is directly compatible with a pulse line transformer similar to that shown in Figure 25.

6DB PAD

There is a 6dB pad available on the hybrid that is used for attentuation and line matching. The input and output impedance of the 6dB pad is 75 ohms. The application circuit in Figure 25 shows a + 12V center tapped transmit transformer. This transformer will produce a 6.0V output pulse height. The 6dB pad will reduce the pulse height to 3.0V , as specified by CCITT G.732, and also present a 75Ω output impedance to the transmit line.

APPLICATIONS

The diagram in Figure 25 illustrates a typical CEPT interface. The only external components required are 2 transformers, a tuneable inductor, and a NAND gate. All of the ST-BUS signals could typically be sourced from an MT8980/81 Digital Time Space Switch. They could also be sourced directly from other ST-BUS devices like the MT8960 voice codec. The relay marked KA shows how an external loop around can be implemented.

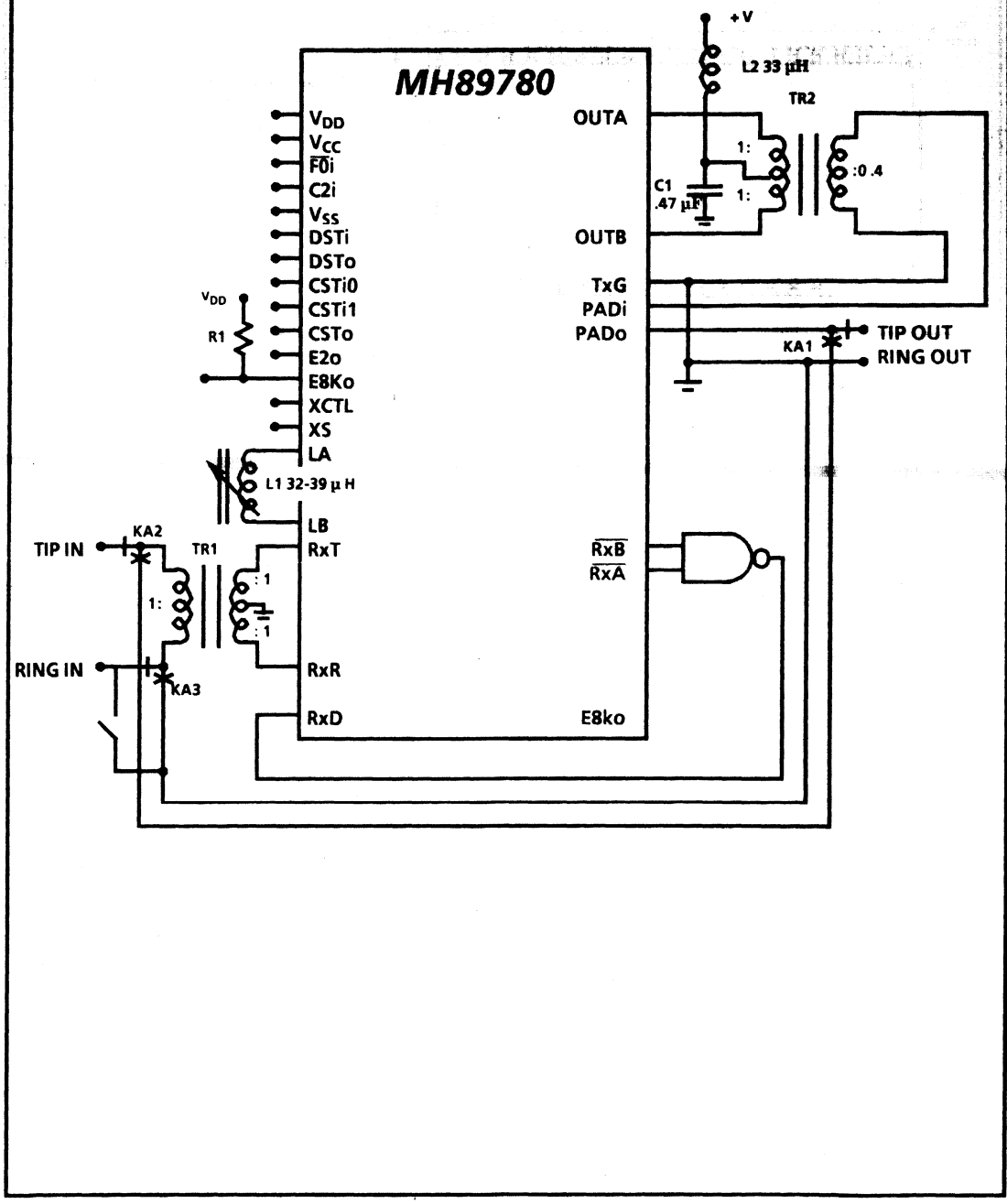


Figure 25. Typical Application Circuit

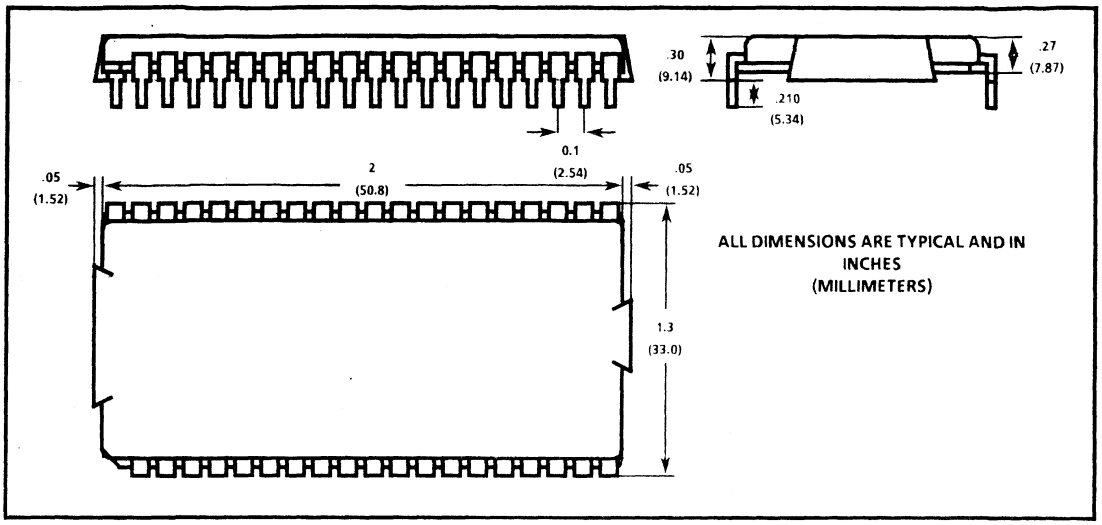


Figure 26. Physical Dimensions of 40 Pin Dual in Line Hybrid Package

ISO-CMOS ST-BUS™ FAMILY MT8980D
Digital Time/Space Crosspoint Switch
Preliminary Information

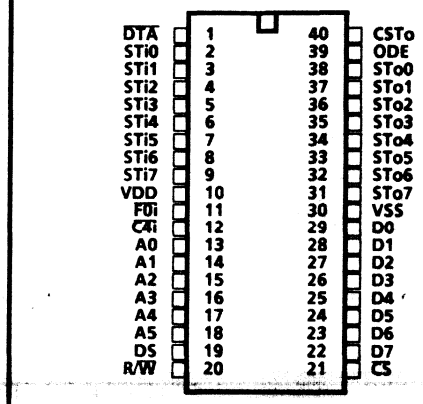
9161-002-071 NA ISSUE 1 June 1986

Features
- MITEL ST-BUS™ Compatible
- 8-Line x 32-Channel Inputs
- 8-Line x 32-Channel Outputs
- 256 Ports Non-Blocking Switch
- Single Power Supply (+ 5 V)
- Low Power Consumption: 30 mW Typ
- Microprocessor-Control Interface
- Three-state Serial Outputs

Description

This VLSI ISO-CMOS device is designed for switching PCM-encoded voice or data, under microprocessor control, in a modern digital exchange, PBX or Central Office. It provides simultaneous connections for up to 256 64 kbit/s channels. Each of the eight serial inputs and outputs consist of 32 64 kbit/s channels multiplexed to form a 2048 kbit/s ST-BUS™ stream. In addition, the MT8980 provides microprocessor read and write access to individual ST-BUS channels.

Pin Connections



Ordering Information

MT8980DC	40 Pin Ceramic DIL (Cerdip)
MT8980DE	40 Pin Plastic DIL
MT8980DP	44 Pin Plastic PLCC
	-40°C to + 85°C

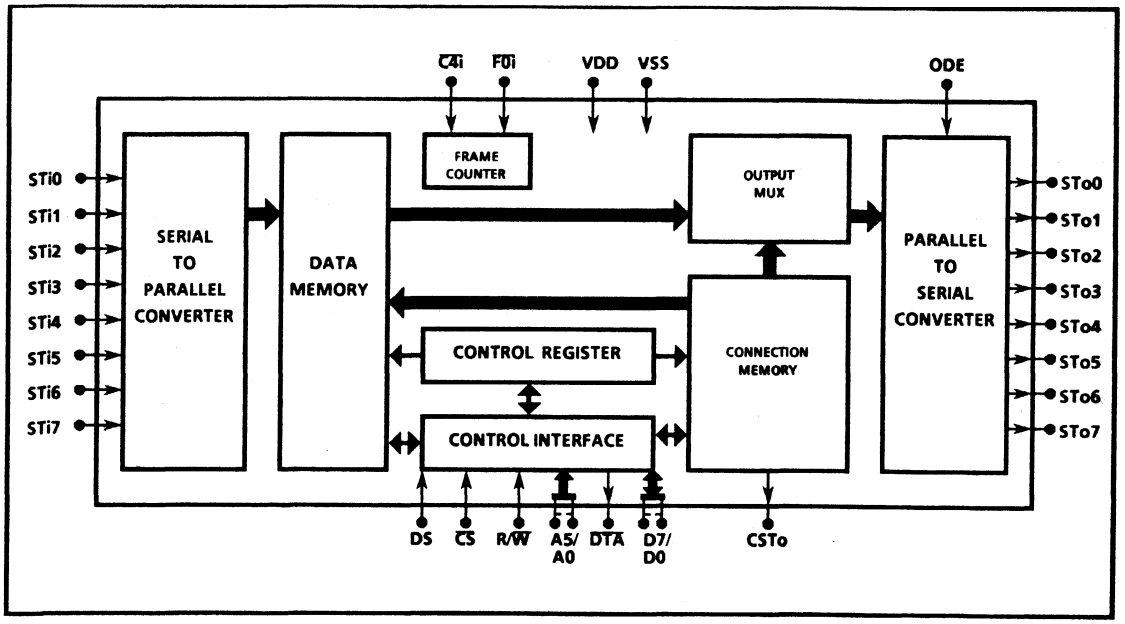


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	V_{DD} - V_{SS}		- 0.3	7	V
2	Voltage on Digital Inputs	V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Voltage on Digital Outputs	V_O	V_{SS} - 0.3	V_{DD} + 0.3	V
4	Current at Digital Outputs	I_O		40	mA
5	Storage Temperature	T_S	- 65	+ 150	°C
6	Package Power Dissipation	P_D		2	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

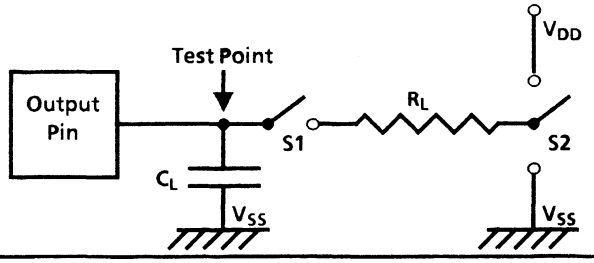
		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Operating Temperature	T_{OP}	-40		+ 85	°C	
2		Positive Supply	V_{DD}	4.75		5.25	V	
3		Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	I	Supply Current	I_{DD}		6	10	mA	Outputs unloaded
2	N	Input High Voltage	V_{IH}	2.0			V	
3	P	Input Low Voltage	V_{IL}			0.8	V	
4	U	Input Leakage	I_{IL}			5	μA	V_I between V_{SS} and V_{DD}
5	T S	Input Pin Capacitance	C_I		8		pF	
6	O	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 10 mA
7	U	Output High Current	I_{OH}	10	15		mA	Sourcing. V_{OH} = 2.4V
8	T	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
9	P	Output Low Current	I_{OL}	5	10		mA	Sinking. V_{OL} = 0.4V
10	U	High Impedance Leakage	I_{OZ}			5	μA	V_O between V_{SS} and V_{DD}
11	T S	Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



S1 is open circuit except when testing output levels or high impedance states.
S2 is switched to V_{DD} or V_{SS} when testing output levels or high impedance states.

Figure 2 - Output Test Load

AC Electrical Characteristics† - Clock Timing (Figures 3 and 4)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	Clock Period*	t_{CLK}	220	244	300	ns	
2		Clock Width High	t_{CH}	100	122	150	ns	
3		Clock Width Low	t_{CL}	110	122	150	ns	
4		Clock Transition Time	t_{CTT}		20		ns	
5		Frame Pulse Set upTime	t_{FPS}	20		200	ns	
6		Frame Pulse Hold Time	t_{FPH}	0.020		50	μs	
7		Frame Pulse Width	t_{FPW}		244		ns	

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* Contents of Connection Memory are not lost if the clock stops, however, ST-BUS outputs go into the high impedance state

NB: Frame Pulse is repeated every 512 cycles of $\overline{C4i}$

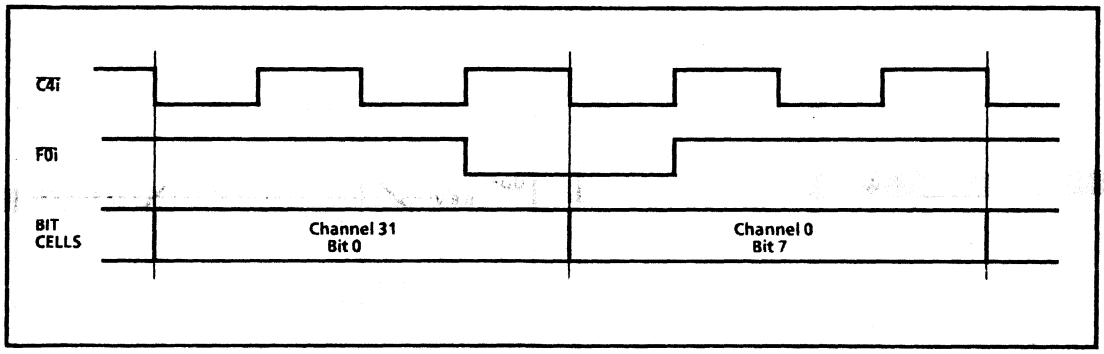


Figure 3 - Frame Alignment

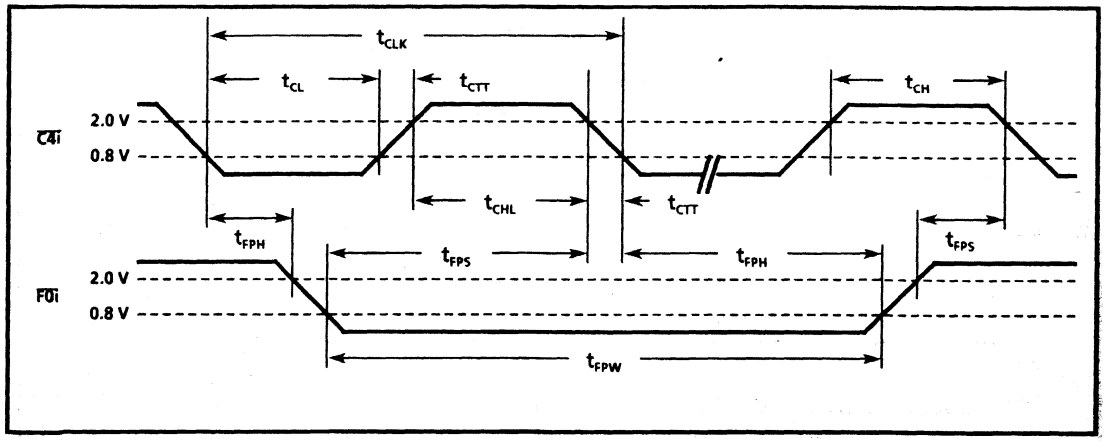


Figure 4 - Clock Timing

AC Electrical Characteristics† - Serial Streams (Figures 2, 5, 6 and 7)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	O U T P U T S	STo0/7 Delay - Active to High Z	t_{SAZ}	20	50	80	ns	RL = 1 KΩ*, CL = 150 pF
2		STo0/7 Delay - High Z to Active	t_{SZA}	25	60	125	ns	CL = 150 pF
3		STo0/7 Delay - Active to Active	t_{SAA}	30	65	125	ns	CL = 150 pF
4		STo0/7 Hold Time	t_{SOH}	25	45		ns	CL = 150 pF
5		Output Driver Enable Delay	t_{OED}		45	125	ns	RL = 1 KΩ*, CL = 150 pF
6		External Control Hold Time	t_{XCH}	0	50		ns	CL = 150 pF
7		External Control Delay	t_{XCD}		75	110	ns	CL = 150 pF
8	I N	Serial Input Set up Time	t_{SIS}		-40	-20	ns	
9		Serial Input Hold Time	t_{SIH}	90			ns	

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

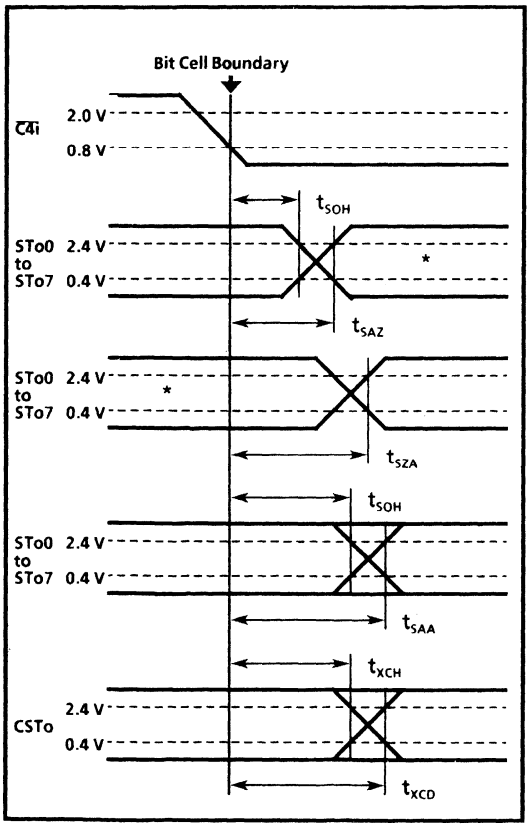


Fig. 5 - Serial Outputs and External Control

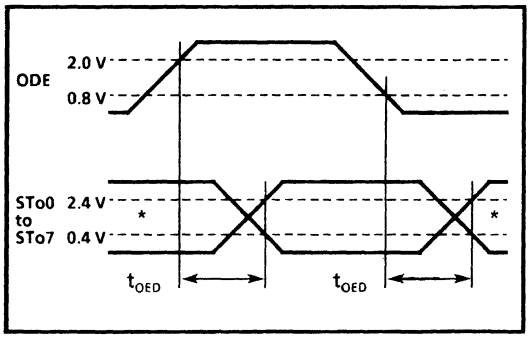


Fig. 6 - Output Driver Enable

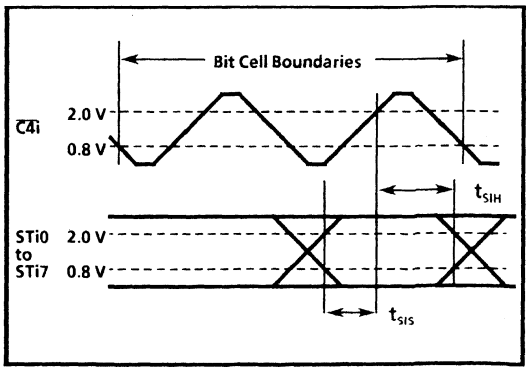


Fig. 7 - Serial Inputs

AC Electrical Characteristics† - Processor Bus (Figures 2 and 8)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Chip Select Set up Time	t_{CSS}	20	0		ns	
2	Read/Write Set up Time	t_{RWS}	25	5		ns	
3	Address Set up Time	t_{ADS}	25	5		ns	
4	Aknowledgement Delay Fast	t_{AKD}		40	100	ns	CL = 150 pf
	Slow	t_{AKD}	2.7		7.2	cycles	$\overline{C4i}$ cycles①
5	Fast Write Data Set up Time	t_{FWS}	0			ns	
6	Slow Write Data Delay	t_{SWD}		2.0	1.7	cycles	$\overline{C4i}$ cycles①
7	Read Data Set up Time	t_{RDS}			0.5	cycles	$\overline{C4i}$ cycles①, CL = 150 pf
8	Data Hold Time Read	t_{DHT}	20			ns	RL = 1 KΩ*, CL = 150 pf
	Write	t_{DHT}	20	10		ns	
9	Read Data To High Impedance	t_{RDZ}		50	90	ns	RL = 1 KΩ*, CL = 150 pf
10	Chip Select Hold Time	t_{CSH}	0			ns	
11	Read/Write Hold Time	t_{RWH}	0			ns	
12	Address Hold Time	t_{ADH}	0			ns	
13	Acknowledgement Hold Time	t_{AKH}	30	60	80	ns	RL = 1 KΩ*, CL = 150 pf

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

① Processor accesses are dependant on the $\overline{C4i}$ clock, and so some timings are expressed as multiples of the $\overline{C4i}$ clock period.

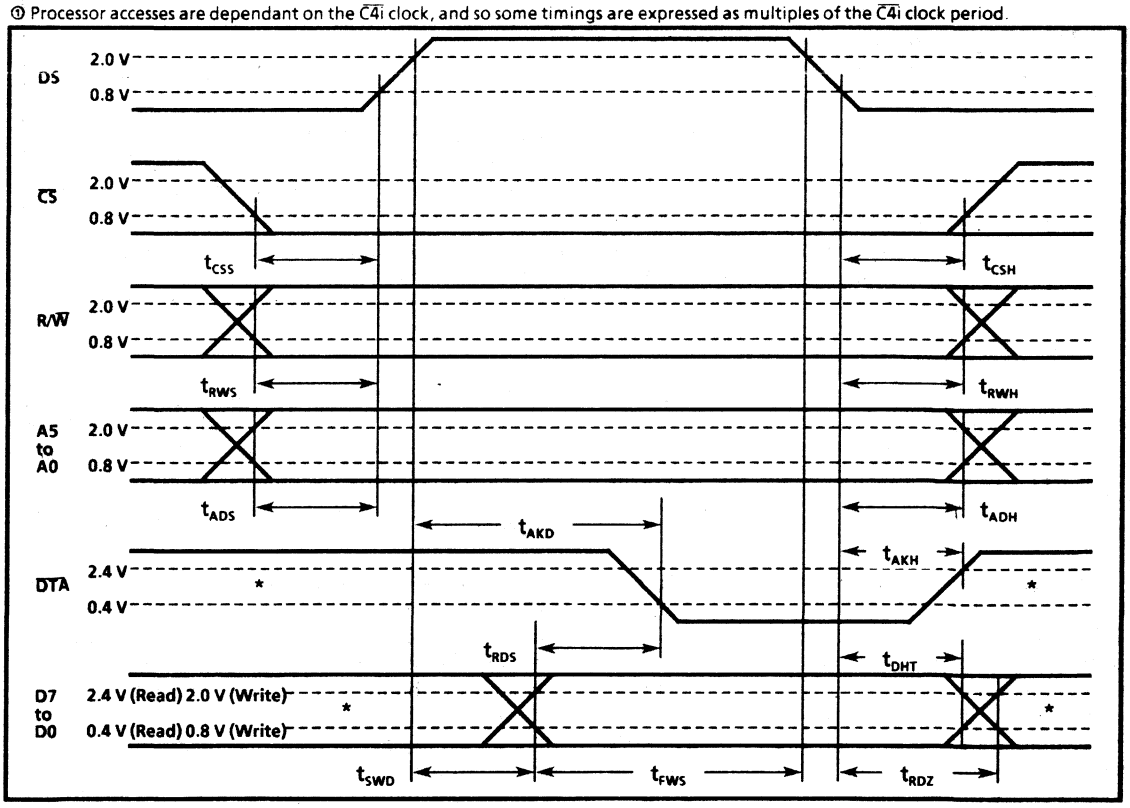


Figure 8 - Processor Bus

Pin Description

PIN	NAME	DESCRIPTION
1	$\overline{DTA}$	**Data Acknowledgement (Open Drain Pulldown Output).** This is the data acknowledgement on the microprocessor interface. This pin is pulled low to signal that the chip has processed the data.
2-9	STi0-STi7	**ST-BUS Input 0 to 7 (Inputs).** These are the inputs for the 2048 kbit/s ST-BUS™ input streams.
10	VDD	**Power Input.** Positive Supply.
11	$\overline{F0i}$	**Framing 0-Type (Input).** This is the input for the frame synchronisation pulse for the 2048 kbit/s ST-BUS™ streams. A low on this input causes the internal counter to reset on the next negative transition of $\overline{C4i}$.
12	$\overline{C4i}$	**4.096 MHz Clock (Input).** ST-BUS™ bit cell boundaries lie on the alternate falling edges of this clock.
13-18	A0-A5	**Address 0 to 5 (Inputs).** These are the inputs for the address lines on the microprocessor interface.
19	DS	**Data Strobe (Input).** This is the input for the active high data strobe on the microprocessor interface.
20	R/$\overline{W}$	**Read or Write (Input).** This is the input for the read/write signal on the microprocessor interface - high for read, low for write.
21	$\overline{CS}$	**Chip Select (Input).** This is the input for the active low chip select on the microprocessor interface.
22-29	D7-D0	**Data 7 to 0 (Three-state I/O Pins).** These are the bidirectional data pins on the microprocessor interface.
30	VSS	**Power Input.** Negative Supply (Ground).
31-38	STo7-STo0	**ST-BUS Output 7 to 0 (Three-state Outputs).** These are the pins for the eight 2048 kbit/s ST-BUS™ output streams.
39	ODE	**Output Drive Enable (Input).** If this input is held high, the STo0-STo7 output drivers function normally. If this input is low, the STo0-STo7 output drivers go into their high impedance state. **NB:** Even when ODE is high, channels on the STo0-STo7 outputs can go high impedance under software control.
40	CSTo	**Control ST-BUS Output (Complementary Output).** Each frame of 256 bits on this ST-BUS™ output contains the values of bit 1 in the 256 locations of the Connection Memory High.

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, MITEL has devised the ST-BUS™ (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS™ operate continuously at 2048 kbit/s and are arranged in 125 μs wide frames which contain 32 8-bit channels. MITEL manufactures a number of devices which interface to the ST-BUS™; a key device being the MT8980 chip.

The MT8980 can switch data from channels on ST-BUS™ inputs to channels on ST-BUS™ outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS™ inputs or write to channels on ST-BUS™ outputs (Message Mode). To the microprocessor, the MT8980 looks like a memory peripheral. The microprocessor can write to the MT8980 to establish switched connections between input ST-BUS™ channels and output ST-BUS™ channels, or to transmit messages

on output ST-BUS™ channels. By reading from the MT8980, the microprocessor can receive messages from ST-BUS™ input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the MT8980 allows systems to use distributed processing and to switch voice or data in an ST-BUS™ architecture.

Hardware Description

Serial data at 2048 kbit/s is received at the eight ST-BUS™ inputs (STi0 to STi7), and serial data is transmitted at the eight ST-BUS™ outputs (STo0 to STo7). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (e.g., MITEL's MT8964).

This serial input word is converted into parallel data and stored in the 256x8 Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS™ input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS™ output streams. When a channel is due to be transmitted on an ST-BUS™ output, the data for the channel can either be switched from an ST-BUS™ input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS™ stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the Control Register, which may be written to or read from via the Control Interface. The lower order bits come from the address lines directly.

The Control Register also allows the chip to broadcast messages on all ST-BUS™ outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state, which enables arrays of MT8980s to be constructed. It also controls the $\overline{CSTo}$ pin.

All ST-BUS™ timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

Software Control

The address lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register, to the High or Low sections of the Connection Memory or to the Data Memory.

If address line A5 is low, then the Control Register is addressed regardless of the other address lines (see Fig. 9). If A5 is high, then the address lines A4-A0 select the memory location

A5	A4	A3	A2	A1	A0	HEX ADDRESS	LOCATION
0	X	X	X	X	X	00 - 1F	Control Register *
1	0	0	0	0	0	20	Channel 0†
1	0	0	0	0	1	21	Channel 1†
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	3F	Channel 31†

* Writing to the Control Register is the only fast transaction.
† Memory and stream are specified by the contents of the Control Register.

Figure 9 - Address Memory Map

corresponding to channel 0-31 for the memory and stream selected in the Control Register.

The data in the Control Register consists of mode control bits, memory select bits, and stream address bits (see Fig. 10). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS™ input or output streams.

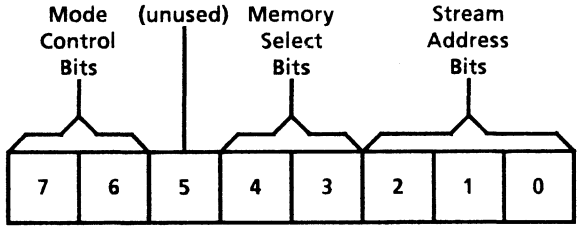
Bit 7 of the Control Register allows split memory operation - reads are from the Data Memory and writes are to the Connection Memory Low.

The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the ST-BUS™ output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

If bit 6 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally (see Fig. 11). If bit 2 is 1, the associated ST-BUS™ output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS™ input stream and channel where the byte is to be found (see Fig. 12).

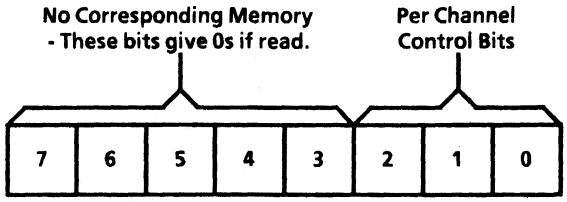
If the ODE pin is low, then all serial outputs are high-impedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS™ output stream and channel. Bit 0 = 1 enables the driver and bit 0 = 0 disables it (see Fig. 11).

Bit 1 of each Connection Memory High location (see Fig. 11) is output on the CSTo pin once every frame. To allow for delay in any external control circuitry the bit is output one channel before the



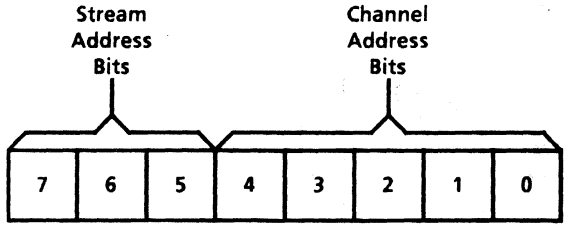
BIT	NAME	DESCRIPTION
7	Split Memory	When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. When 0, the Memory Select Bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.
6	Message Mode	When 1, the contents of the Connection Memory Low are outut on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
5	(unused)	
4-3	Memory Select Bits	0-0 - Not to be used 0-1 - Data Memory (read only from the microprocessor port) 1-0 - Connection Memory Low 1-1 - Connection Memory High
2-0	Stream Address Bits	The number expressed in binary notation on these bits refers to the input or output ST-BUS™ stream which corresponds to the subsection of memory made accessible for subsequent operations.

Figure 10 - Control Register Bits



BIT	NAME	DESCRIPTION
2	Message Channel	When 1, the contents of the corresponding location in Connection Memory Low are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
1	CSTo Bit	This bit is output on the CSTo pin one channel early. The CSTo bit for stream 0 is output first.
0	Output Enable	If the ODE pin is high and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.

Figure 11 - Connection Memory High Bits



BIT	NAME	DESCRIPTION
7-5*	Stream Address Bits*	The number expressed in binary notation on these 3 bits is the number of the ST-BUS™ stream for the source of the connection. Bit 7 is the most significant bit. E.g., if bit 7 is 1, bit 6 is 0 and bit 5 is 0, then the source of the connection is a channel on STi4.
4-0*	Channel Address Bits*	The number expressed in binary notation on these 5 bits is the number of the channel which is the the source of the connection (The ST-BUS™ stream where the channel lies is defined by bits 7, 6 and 5.). Bit 4 is the most significant bit. E.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.

*If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.

Figure 12 - Connection Memory Low Bits

corresponding channel on the ST-BUS™ streams, and the bit for stream 0 is output first in the channel; e.g., bit 1's for channel 9 of streams 0-7 are output synchronously with ST-BUS™ channel 8 bits 7-0.

Applications

Use in a Simple Digital Switching System

Fig. 13 and 14 show how MT8980s can be used with MT8964s to form a simple digital switching system. Fig. 13 shows the interface between the MT8980s and the filter/codecs. Fig. 14 shows the position of these components in an example architecture.

The MT8964 filter/codec in Fig. 13 receives and transmits digitised voice signals on the ST-BUS™ input D_R, and ST-BUS™ output D_X, respectively. These signals are routed to the ST-BUS™ inputs and outputs on the top MT8980, which is used as a digital speech switch.

The MT8964 is controlled by the ST-BUS™ input D_C originating from the bottom MT8980, which generates the appropriate signals from an output channel in Message Mode. This architecture optimises the messaging capability of the line circuit by building signalling logic, e.g. for on-off hook detection, which communicates on an ST-BUS™ output. This signalling ST-BUS™ output is monitored by a microprocessor (not shown) through an ST-BUS™ input on the bottom MT8980.

Fig. 14 shows how a simple digital switching system may be designed using the ST-BUS™ architecture. This is a private telephone network with 256 extensions which uses a single MT8980 as a speech switch and a second MT8980 for communication with the line interface circuits.

A larger digital switching system may be designed by cascading a number of MT8980s. Fig. 15 shows how four MT8980s may be arranged in a non-blocking configuration which can switch any channel on any of the ST-BUS™ inputs to any channel on the ST-BUS™ outputs.

Application Circuit with 6802 Processor

Fig. 16 shows an example of a complete circuit which may be used to evaluate the chip.

For convenience, a 4 MHz crystal oscillator has been used rather than a 4.096 MHz clock, as both

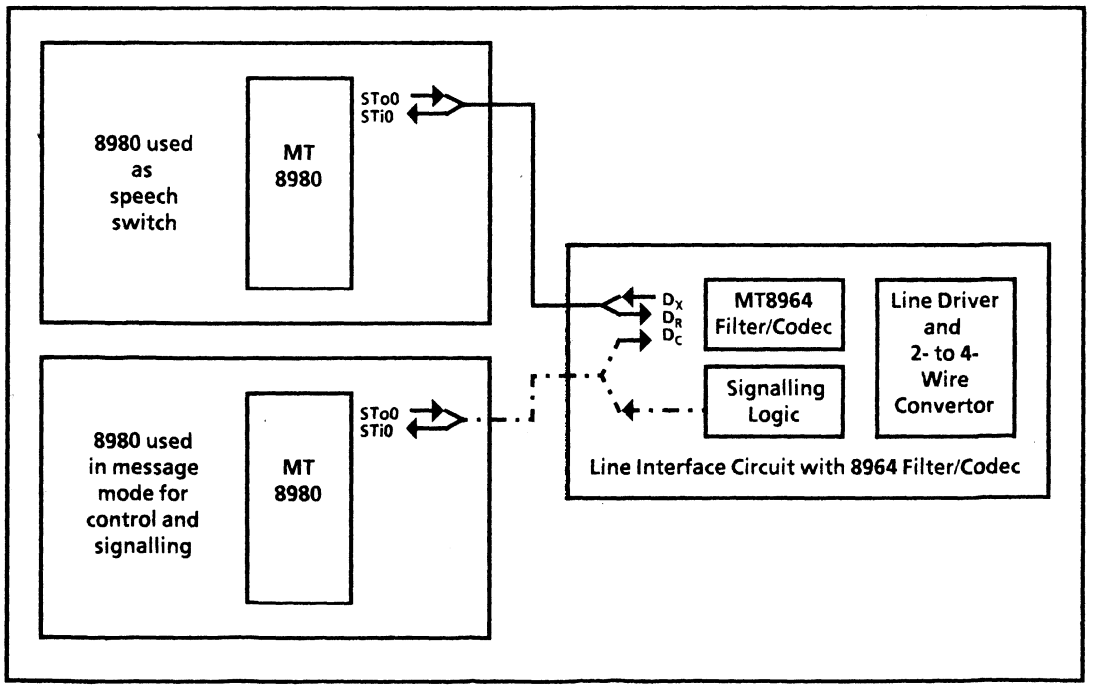


Figure 13 - Example of Typical Interface between 8980s and 8964s for Simple Digital Switching System

are within the limits of the chip's specifications. The RC delay used with the 393 counters ensures a sufficient hold time for the FP signal, but the values used may have to be changed if faster 393 counters become available.

The chip is shown as memory mapped into the MEK6802D3 system. Chip addresses 00-3F correspond to processor addresses 2000-203F. Delay through the address decoder requires the VMA signal to be used twice to remove glitches. The MEK6802D3 board uses a 10KΩ pullup on the MR pin, which would have to be incorporated into the circuit if the board was replaced by a processor.

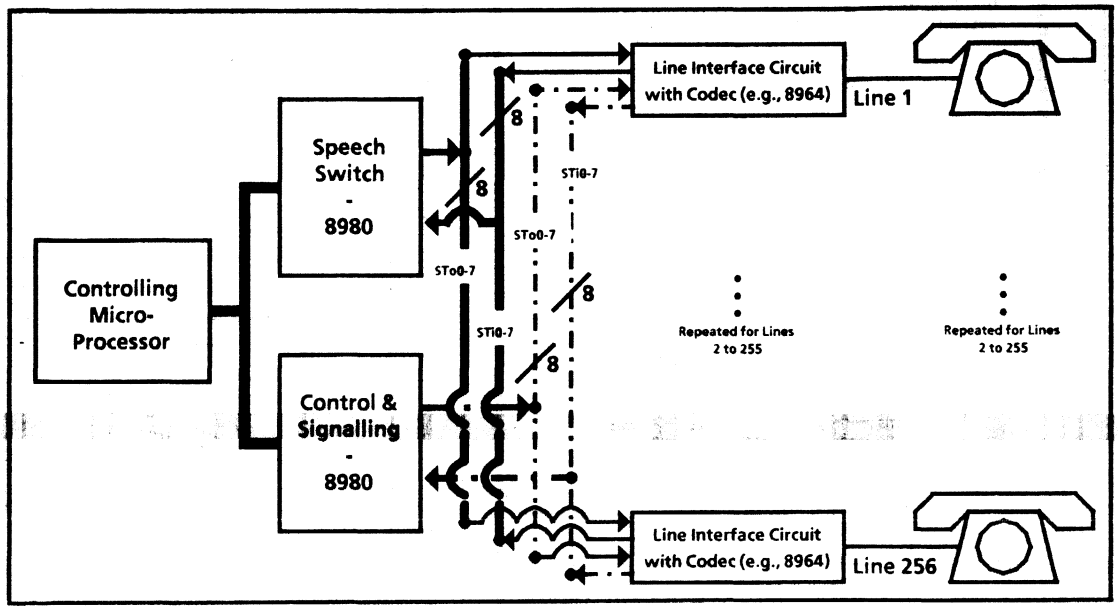


Figure 14 - Example Architecture of a Simple Digital Switching System

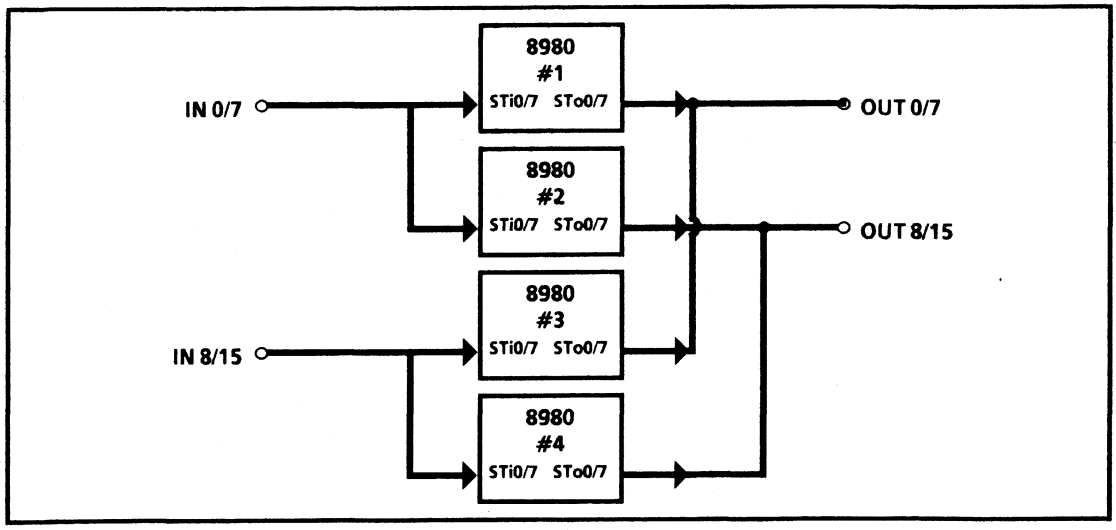


Figure 15 - Four 8980s Arranged in a Non-Blocking 16 x 16 Configuration

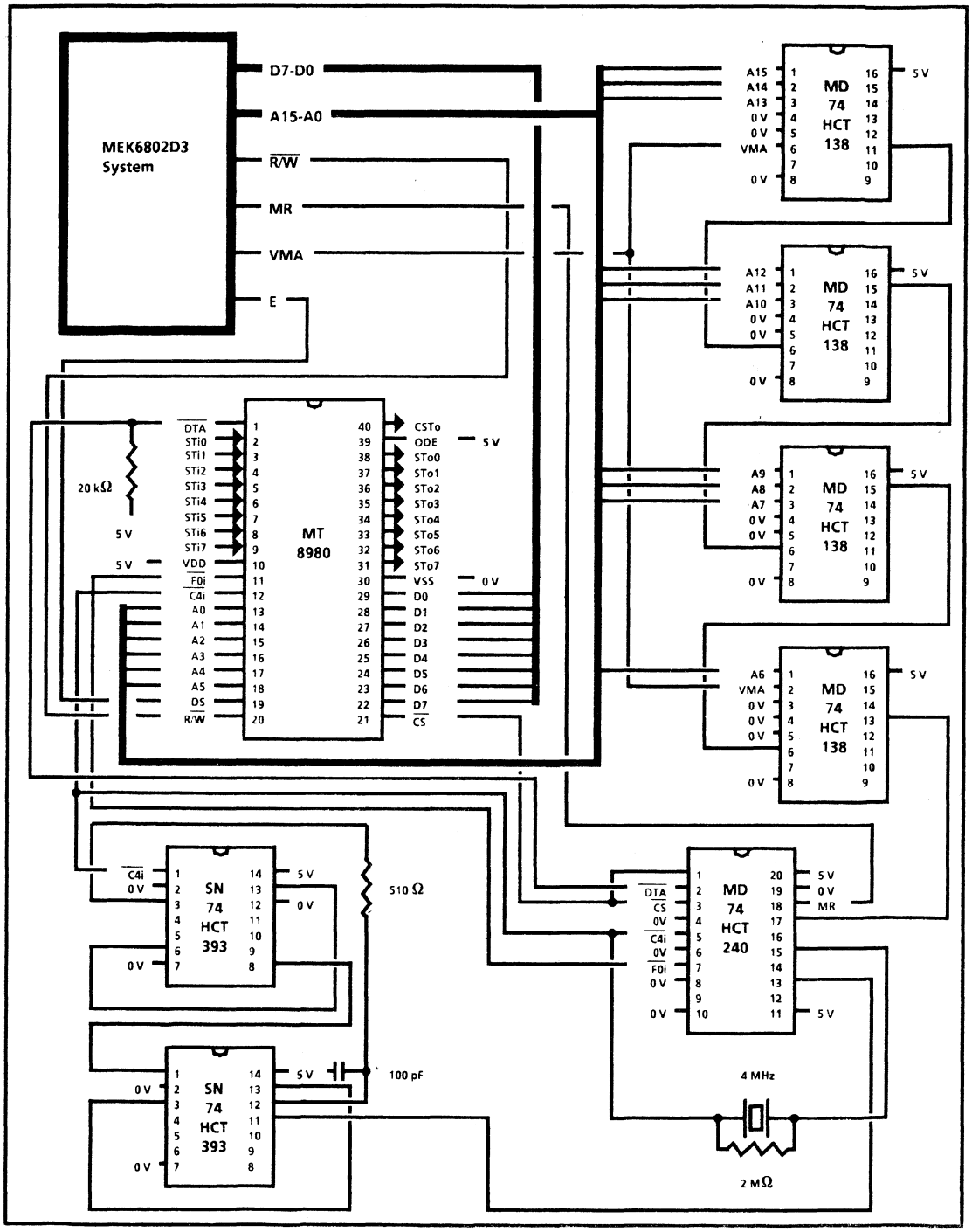


Fig. 16 - Application Circuit with 6802

ISO-CMOS ST-BUS™ FAMILY MT8981D
Digital Time/Space Crosspoint Switch
Preliminary Information

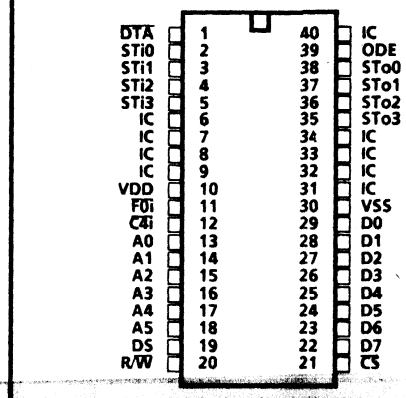
9161-002-072 NA ISSUE 1 JUNE 1986

Features
- MITEL ST-BUS™ Compatible
- 4-Line x 32-Channel Inputs
- 4-Line x 32-Channel Outputs
- 128 Ports Non-Blocking Switch
- Single Power Supply (+ 5 V)
- Low Power Consumption: 30 mW Typ
- Microprocessor-Control Interface
- Three-state Serial Outputs

Description

This VLSI ISO-CMOS device is designed for switching PCM-encoded voice or data, under microprocessor control, in a modern digital exchange, PBX or Central Office. It provides simultaneous connections for up to 128 64 kbit/s channels. Each of the four serial inputs and outputs consist of 32 64 kbit/s channels multiplexed to form a 2048 kbit/s ST-BUS™ stream. In addition, the MT8981 provides microprocessor read and write access to individual ST-BUS channels.

Pin Connections



Ordering Information

MT8981DC	40 Pin Ceramic DIL (Cerdip)
MT8981DE	40 Pin Plastic DIL
MT8981DP	44 Pin Plastic PLCC
	-40°C to + 85°C

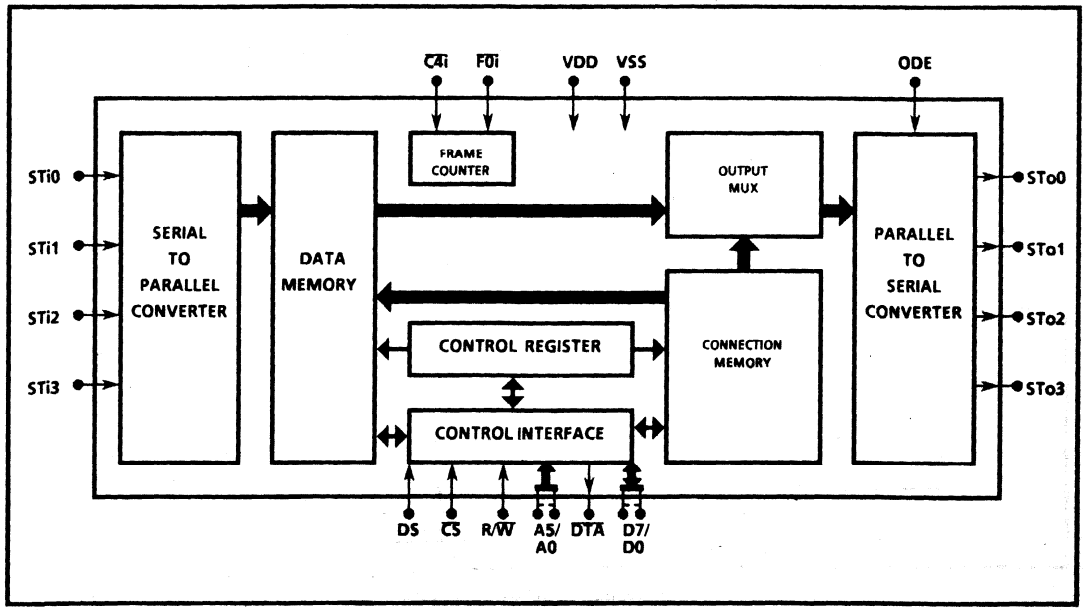


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	V_{DD} - V_{SS}		-0.3	7	V
2	Voltage on Digital Inputs	V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Voltage on Digital Outputs	V_O	V_{SS} - 0.3	V_{DD} + 0.3	V
4	Current at Digital Outputs	I_O		40	mA
5	Storage Temperature	T_S	-65	+150	°C
6	Package Power Dissipation	P_D		2	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

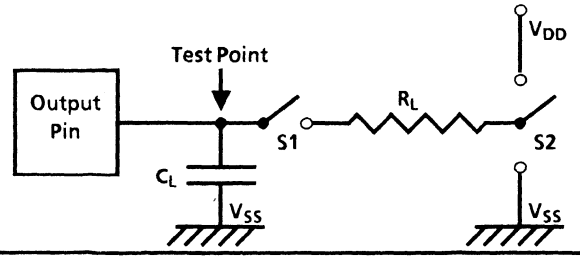
		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Operating Temperature	T_{OP}	-40		+85	°C	
2		Positive Supply	V_{DD}	4.75		5.25	V	
3		Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	I	Supply Current	I_{DD}		6	10	mA	Outputs unloaded
2	N	Input High Voltage	V_{IH}	2.0			V	
3	P	Input Low Voltage	V_{IL}			0.8	V	
4	U	Input Leakage	I_{IL}			5	μA	V_I between V_{SS} and V_{DD}
5	T S	Input Pin Capacitance	C_I		8		pF	
6	O	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 10 mA
7	U	Output High Current	I_{OH}	10	15		mA	Sourcing. V_{OH} = 2.4V
8	T	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
9	P	Output Low Current	I_{OL}	5	10		mA	Sinking. V_{OL} = 0.4 V
10	U	High Impedance Leakage	I_{OZ}			5	μA	V_O between V_{SS} and V_{DD}
11	T S	Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



S1 is open circuit except when testing output levels or high impedance states.

S2 is switched to V_{DD} or V_{SS} when testing output levels or high impedance states.

Figure 2 - Output Test Load

AC Electrical Characteristics† - Clock Timing (Figures 3 and 4)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	Clock Period*	t_{CLK}	220	244	300	ns	
2		Clock Width High	t_{CH}	100	122	150	ns	
3		Clock Width Low	t_{CL}	110	122	150	ns	
4		Clock Transition Time	t_{CTT}		20		ns	
5		Frame Pulse Set upTime	t_{FPS}	20		200	ns	
6		Frame Pulse Hold Time	t_{FPH}	0.020		50	μs	
7		Frame Pulse Width	t_{FPW}		244		ns	

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* Contents of Connection Memory are not lost if the clock stops, however, ST-BUS outputs go into the high impedance state

NB: Frame Pulse is repeated every 512 cycles of $\overline{C4i}$

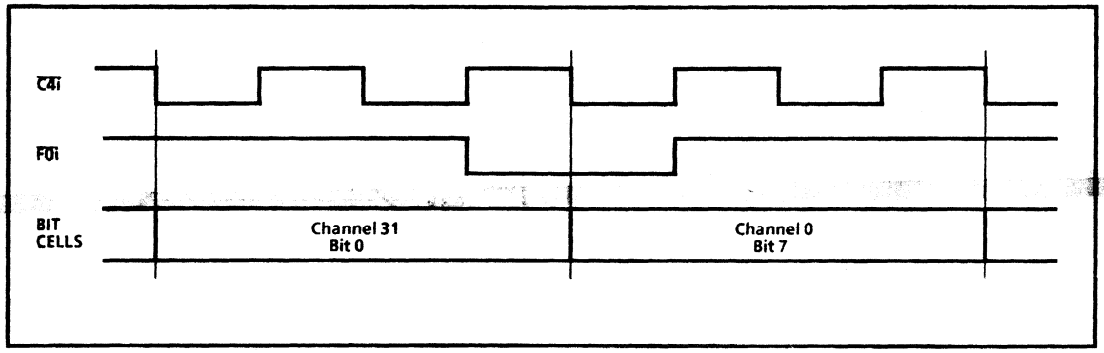


Figure 3 - Frame Alignment

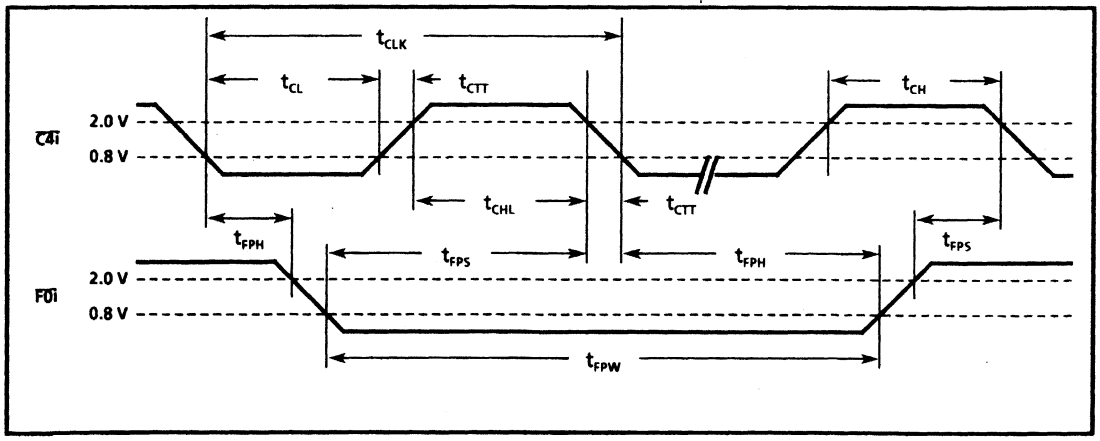


Figure 4 - Clock Timing

AC Electrical Characteristics† - Serial Streams (Figures 2, 5, 6 and 7)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	OUTPUTS	STo0/3 Delay - Active to High Z	t_{SAZ}	20	50	80	ns	RL = 1 KΩ*, CL = 150 pF
2		STo0/3 Delay - High Z to Active	t_{SZA}	25	60	125	ns	CL = 150 pF
3		STo0/3 Delay - Active to Active	t_{SAA}	30	65	125	ns	CL = 150 pF
4		STo0/3 Hold Time	t_{SOH}	25	45		ns	CL = 150 pF
5		Output Driver Enable Delay	t_{OED}		45	125	ns	RL = 1 KΩ*, CL = 150 pF
6		External Control Hold Time	t_{XCH}	0	50		ns	CL = 150 pF
7		External Control Delay	t_{XCD}		75	110	ns	CL = 150 pF
8	IN	Serial Input Set up Time	t_{SIS}		-40	-20	ns	
9		Serial Input Hold Time	t_{SIH}	90			ns	

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

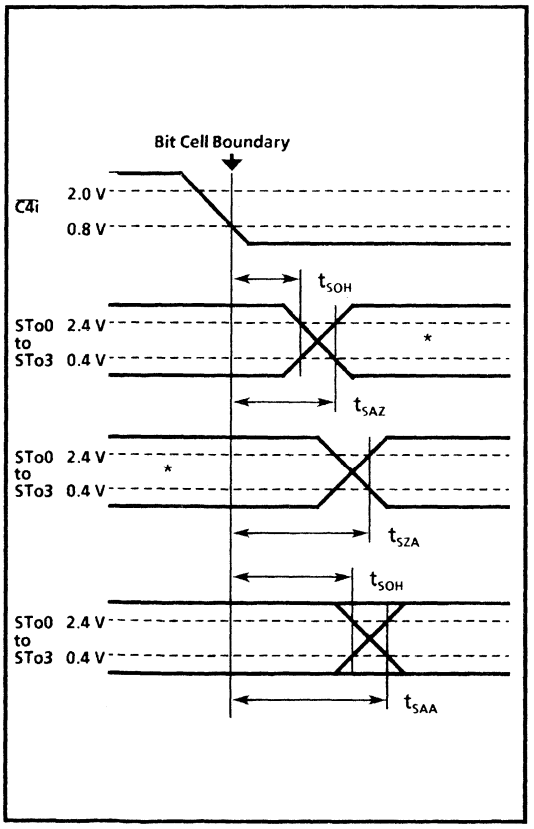


Fig. 5 - Serial Outputs

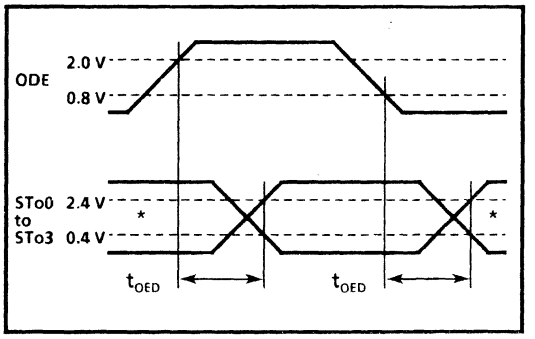


Fig. 6 - Output Driver Enable

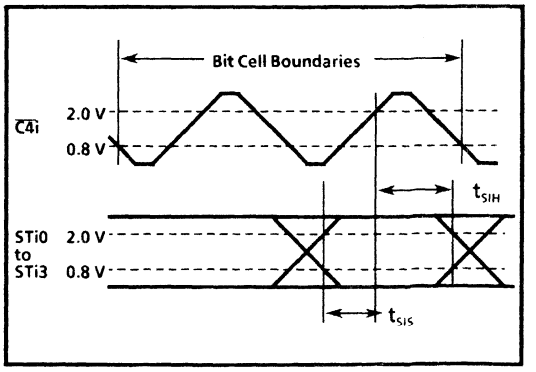


Fig. 7 - Serial Inputs

AC Electrical Characteristics† - Processor Bus (Figures 2 and 8)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Chip Select Set up Time	t_{CSS}	20	0		ns	
2	Read/Write Set up Time	t_{RWS}	25	5		ns	
3	Address Set up Time	t_{ADS}	25	5		ns	
4	Aknowledgement Delay Fast	t_{AKD}		40	100	ns	CL = 150 pf
	Slow	t_{AKD}	2.7		7.2	cycles	$\overline{C4i}$ cycles①
5	Fast Write Data Set up Time	t_{FWS}	0			ns	
6	Slow Write Data Delay	t_{SWD}		2.0	1.7	cycles	$\overline{C4i}$ cycles①
7	Read Data Set up Time	t_{RDS}			0.5	cycles	$\overline{C4i}$ cycles①, CL = 150 pf
8	Data Hold Time Read	t_{DHT}	20			ns	RL = 1 KΩ*, CL = 150 pf
	Write	t_{DHT}	20	10		ns	
9	Read Data To High Impedance	t_{RDZ}		50	90	ns	RL = 1 KΩ*, CL = 150 pf
10	Chip Select Hold Time	t_{CSH}	0			ns	
11	Read/Write Hold Time	t_{RWH}	0			ns	
12	Address Hold Time	t_{ADH}	0			ns	
13	Acknowledgement Hold Time	t_{AKH}	30	60	80	ns	RL = 1 KΩ*, CL = 150 pf

† Timing is over recommended temperature & Power Supply voltages

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

① Processor accesses are dependant on the $\overline{C4i}$ clock, and so some timings are expressed as multiples of the $\overline{C4i}$ clock period.

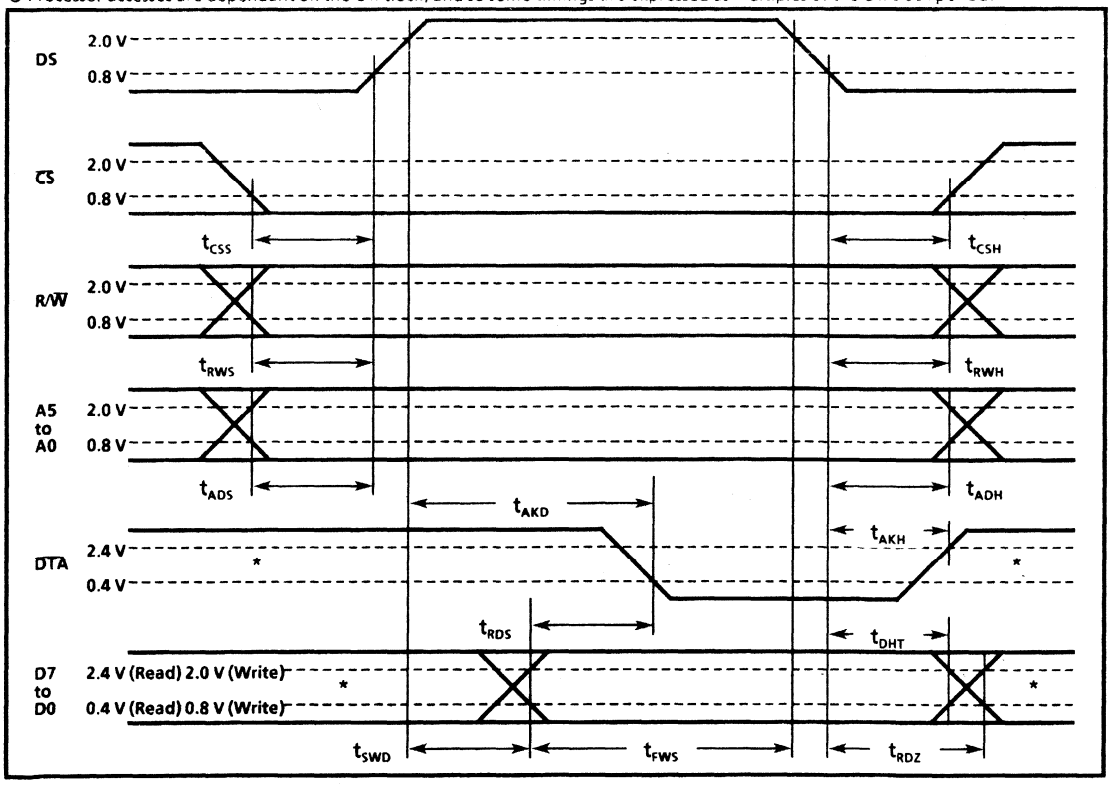


Figure 8 - Processor Bus

Pin Description

PIN	NAME	DESCRIPTION
1	$\overline{DTA}$	**Data Acknowledgement (Open Drain Pulldown Output).** This is the data acknowledgement on the microprocessor interface. This pin is pulled low to signal that the chip has processed the data.
2-5	STi0-STi3	**ST-BUS Input 0 to 3 (Inputs).** These are the inputs for the 2048 kbit/s ST-BUS™ input streams.
6-9	IC	**Internal Connections.** Must be connected to V_{DD}.
10	VDD	**Power Input.** Positive Supply.
11	$\overline{F0i}$	**Framing 0-Type (Input).** This is the input for the frame synchronisation pulse for the 2048 kbit/s ST-BUS™ streams. A low on this input causes the internal counter to reset on the next negative transition of $\overline{C4i}$.
12	$\overline{C4i}$	**4.096 MHz Clock (Input).** ST-BUS™ bit cell boundaries lie on the alternate falling edges of this clock.
13-18	A0-A5	**Address 0 to 5 (Inputs).** These are the inputs for the address lines on the microprocessor interface.
19	DS	**Data Strobe (Input).** This is the input for the active high data strobe on the microprocessor interface.
20	R/$\overline{W}$	**Read or Write (Input).** This is the input for the read/write signal on the microprocessor interface - high for read, low for write.
21	$\overline{CS}$	**Chip Select (Input).** This is the input for the active low chip select on the microprocessor interface.
22-29	D7-D0	**Data 7 to 0 (Three-state I/O Pins).** These are the bidirectional data pins on the microprocessor interface.
30	VSS	**Power Input.** Negative Supply (Ground).
31-34	IC	**Internal Connections.** Leave pins disconnected.
35-38	STo3-STo0	**ST-BUS Output 3 to 0 (Three-state Outputs).** These are the pins for the four 2048 kbit/s ST-BUS™ output streams.
39	ODE	**Output Drive Enable (Input).** If this input is held high, the STo0-STo3 output drivers function normally. If this input is low, the STo0-STo3 output drivers go into their high impedance state. **NB:** Even when ODE is high, channels on the STo0-STo3 outputs can go high impedance under software control.
40	IC	**Internal Connections.** Leave pin disconnected.

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, MITEL has devised the ST-BUS™ (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS™ operate continuously at 2048 kbit/s and are arranged in 125 μs wide frames which contain 32 8-bit channels. MITEL manufactures a number of devices which interface to the ST-BUS™; a key device being the MT8981 chip.

The MT8981 can switch data from channels on ST-BUS™ inputs to channels on ST-BUS™ outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS™ inputs or write to channels on ST-BUS™ outputs (Message Mode). To the microprocessor, the MT8981 looks like a memory peripheral. The microprocessor can write to the MT8981 to establish switched connections between input ST-BUS™ channels and

output ST-BUS™ channels, or to transmit messages on output ST-BUS™ channels. By reading from the MT8981, the microprocessor can receive messages from ST-BUS™ input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the MT8981 allows systems to use distributed processing and to switch voice or data in an ST-BUS™ architecture.

Hardware Description

Serial data at 2048 kbit/s is received at the four ST-BUS™ inputs (STi0 to STi3), and serial data is transmitted at the four ST-BUS™ outputs (STo0 to STo3). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (e.g., MITEL's MT8964).

This serial input word is converted into parallel data and stored in the 128x8 Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS™ input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS™ output streams. When a channel is due to be transmitted on an ST-BUS™ output, the data for the channel can either be switched from an ST-BUS™ input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS™ stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocessor control signals $\overline{CS}$, DTA, R/$\overline{W}$ and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the Control Register, which may be written to or read from via the Control Interface. The lower order bits come from the address lines directly.

The Control Register also allows the chip to broadcast messages on all ST-BUS™ outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state, which enables arrays of MT8981s to be constructed. It also controls the CSTo pin.

All ST-BUS™ timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

Software Control

The address lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register, to the High or Low sections of the Connection Memory or to the Data Memory.

If address line A5 is low, then the Control Register is addressed regardless of the other address lines (see Fig. 9). If A5 is high, then the address lines A4-A0 select the memory location

A5	A4	A3	A2	A1	A0	HEX ADDRESS	LOCATION
0	X	X	X	X	X	00 - 1F	Control Register *
1	0	0	0	0	0	20	Channel 0†
1	0	0	0	0	1	21	Channel 1†
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	3F	Channel 31†

* Writing to the Control Register is the only fast transaction.
† Memory and stream are specified by the contents of the Control Register.

Figure 9 - Address Memory Map

corresponding to channel 0-31 for the memory and stream selected in the Control Register.

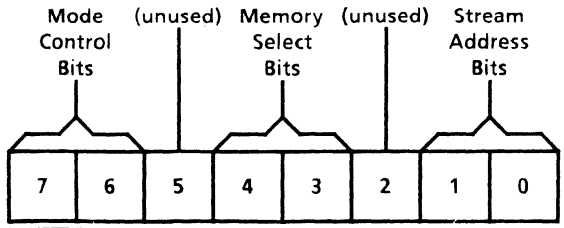
The data in the Control Register consists of mode control bits, memory select bits, and stream address bits (see Fig. 10). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS™ input or output streams.

Bit 7 of the Control Register allows split memory operation - reads are from the Data Memory and writes are to the Connection Memory Low.

The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the ST-BUS™ output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

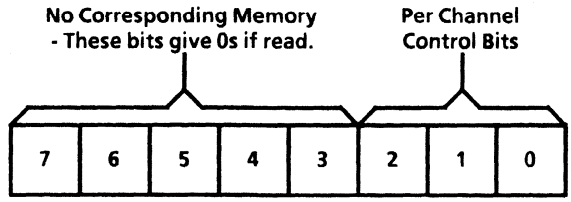
If bit 6 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally (see Fig. 11). If bit 2 is 1, the associated ST-BUS™ output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS™ input stream and channel where the byte is to be found (see Fig. 12).

If the ODE pin is low, then all serial outputs are high-impedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS™ output stream and channel. Bit 0 = 1 enables the driver and bit 0 = 0 disables it (see Fig. 11).



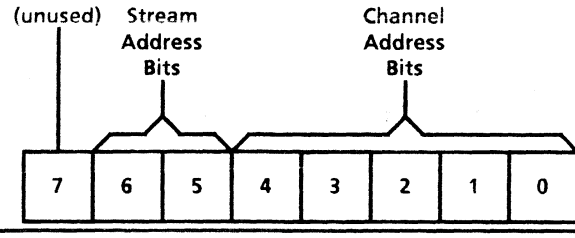
BIT	NAME	DESCRIPTION
7	Split Memory	When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. When 0, the Memory Select Bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.
6	Message Mode	When 1, the contents of the Connection Memory Low are outut on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
5	(unused)	
4-3	Memory Select Bits	0-0 - Not to be used 0-1 - Data Memory (read only from the microprocessor port) 1-0 - Connection Memory Low 1-1 - Connection Memory High
2	(unused)	Must be a 0.
1-0	Stream Address Bits	The number expressed in binary notation on these bits refers to the input or output ST-BUS™ stream which corresponds to the subsection of memory made accessible for subsequent operations.

Figure 10 - Control Register Bits



BIT	NAME	DESCRIPTION
2	Message Channel	When 1, the contents of the corresponding location in Connection Memory Low are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
1	(Unused)	
0	Output Enable	If the ODE pin is high and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.

Figure 11 - Connection Memory High Bits



BIT	NAME	DESCRIPTION
7	(Unused)	Must be a 0.
6-5*	Stream Address Bits*	The number expressed in binary notation on these 2 bits is the number of the ST-BUS™ stream for the source of the connection. Bit 6 is the most significant bit. E.g., if bit 6 is 1, and bit 5 is 0, then the source of the connection is a channel on STi2.
4-0*	Channel Address Bits*	The number expressed in binary notation on these 5 bits is the number of the channel which is the the source of the connection (The ST-BUS™ stream where the channel lies is defined by bits 6 and 5.). Bit 4 is the most significant bit. E.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.

*If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.

Figure 12 - Connection Memory Low Bits

Applications

Use in a Simple Digital Switching System

Fig. 13 and 14 show how MT8981s can be used with MT8964s to form a simple digital switching system. Fig. 13 shows the interface between the MT8981s and the filter/codecs. Fig. 14 shows the position of these components in an example architecture.

The MT8964 filter/codec in Fig. 13 receives and transmits digitised voice signals on the ST-BUS™ input D_R, and ST-BUS™ output D_X, respectively. These signals are routed to the ST-BUS™ inputs and outputs on the top MT8981, which is used as a digital speech switch.

The MT8964 is controlled by the ST-BUS™ input D_C originating from the bottom MT8981, which generates the appropriate signals from an output channel in Message Mode. This architecture optimises the messaging capability of the line circuit by building signalling logic, e.g. for on-off hook detection, which communicates on an ST-BUS™ output. This signalling ST-BUS™ output is monitored by a microprocessor (not shown) through an ST-BUS™ input on the bottom MT8981.

Fig. 14 shows how a simple digital switching system may be designed using the ST-BUS™ architecture. This is a private telephone network with 128 extensions which uses a single MT8981 as a speech switch and a second MT8981 for communication with the line interface circuits.

A larger digital switching system may be designed by cascading a number of MT8981s. Fig. 15 shows how four MT8981s may be arranged in a non-blocking configuration which can switch any channel on any of the ST-BUS™ inputs to any channel on the ST-BUS™ outputs.

Application Circuit with 6802 Processor

Fig. 16 shows an example of a complete circuit which may be used to evaluate the chip.

For convenience, a 4 MHz crystal oscillator has been used rather than a 4.096 MHz clock, as both are within the limits of the chip's specifications. The RC delay used with the 393 counters ensures a sufficient hold time for the FP signal, but the values used may have to be changed if faster 393 counters become available.

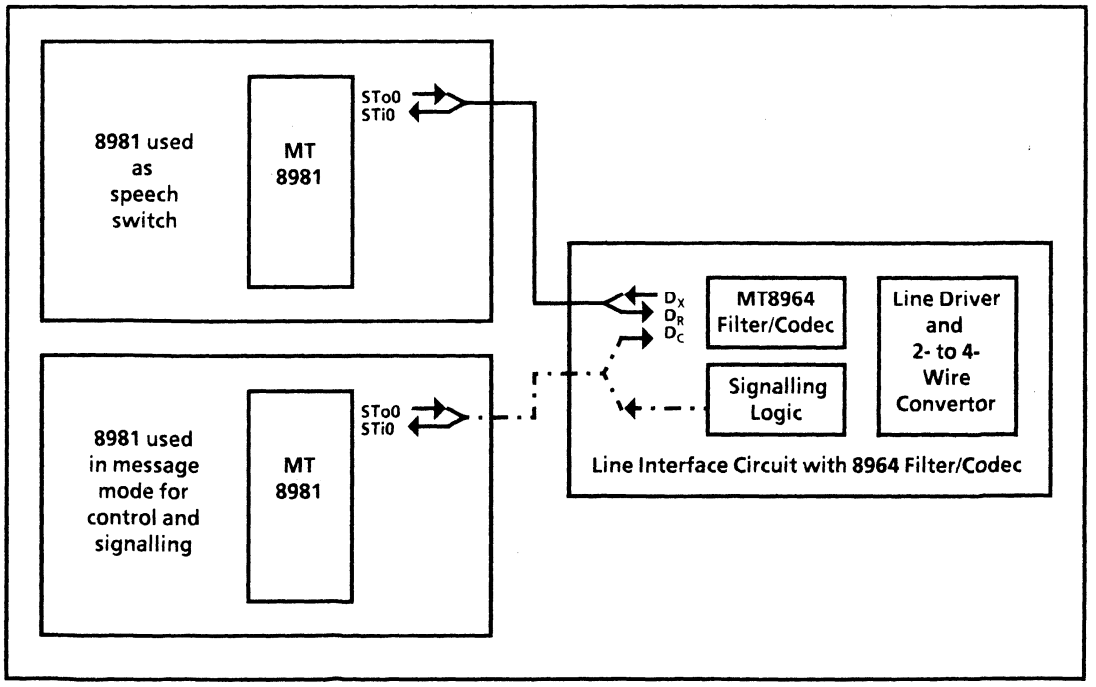


Figure 13 - Example of Typical Interface between 8981s and 8964s for Simple Digital Switching System

The chip is shown as memory mapped into the MEK6802D3 system. Chip addresses 00-3F correspond to processor addresses 2000-203F. Delay through the address decoder requires the VMA signal to be used twice to remove glitches. The MEK6802D3 board uses a 10KΩ pullup on the MR pin, which would have to be incorporated into the circuit if the board was replaced by a processor.

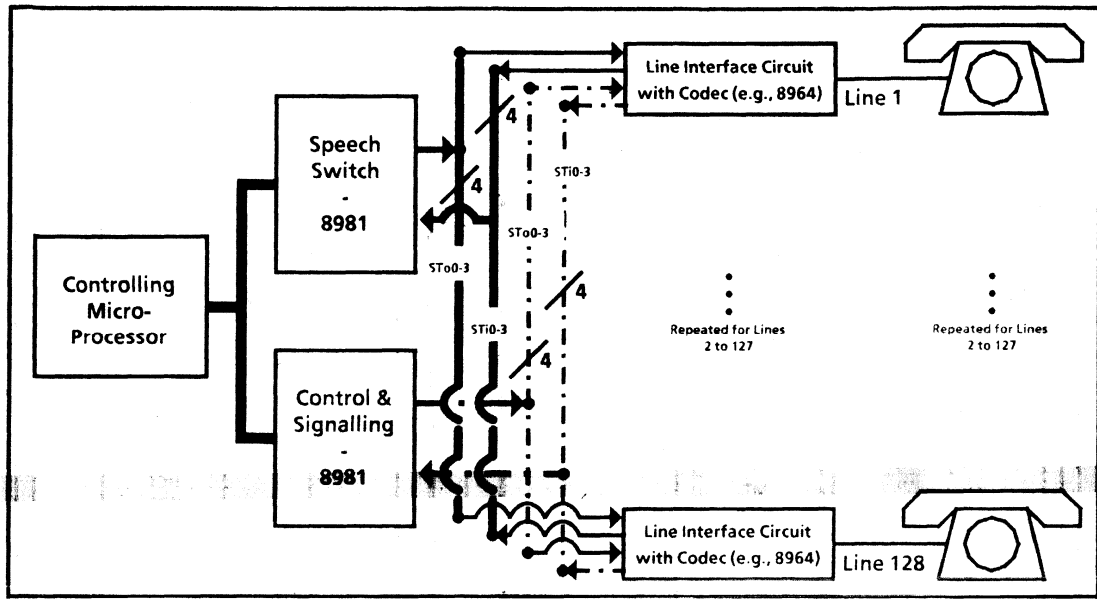


Figure 14 - Example Architecture of a Simple Digital Switching System

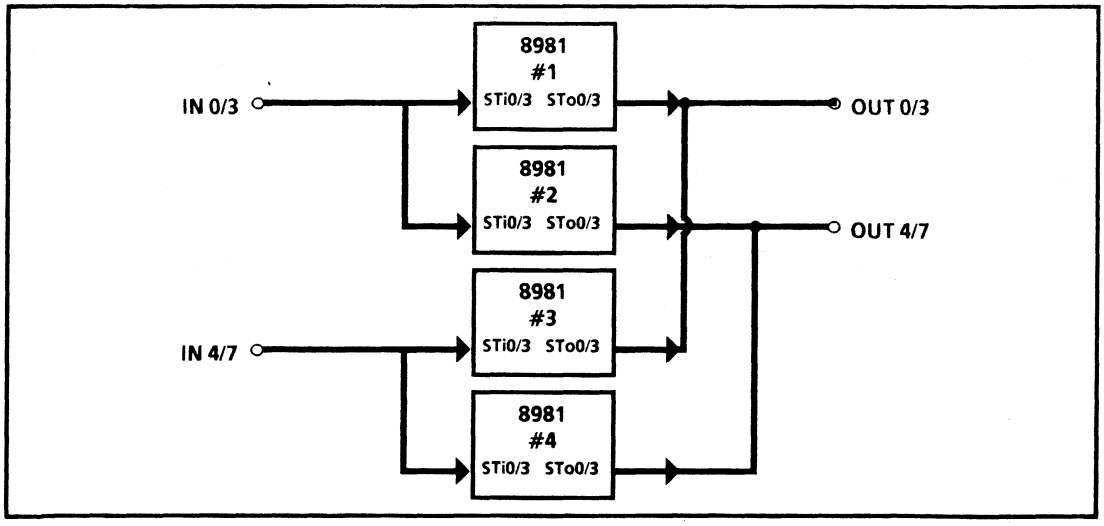


Figure 15 - Four 8981's Arranged in a Non-Blocking 8 x 8 Configuration

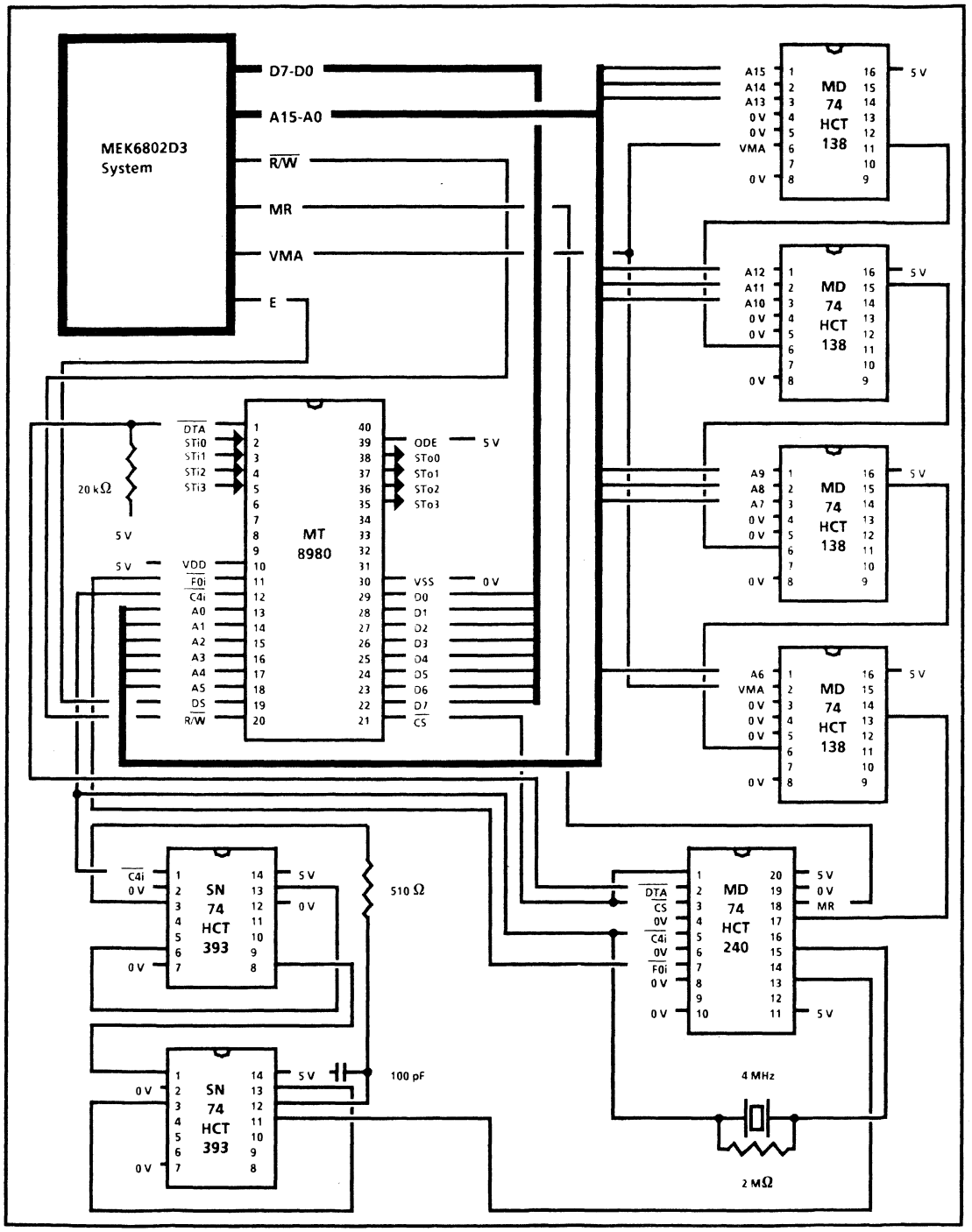


Fig. 16 - Application Circuit with 6802

MITEL

ISO²-CMOS ST-BUS™ MT8994/5
Digital Telephone (D-Phone)

Preliminary Information

9161-002-076-NA ISSUE 1 SEPTEMBER 1996

Features

- Integrated digital telephone circuit
- μ-Law/A-Law codec and filters
- Programmable transmit and receive gains
- DTMF generator and tone ringer
- Speaker-phone operation
- Interface to standard telephony transducers
- Sense/Drive ports
- Single 5 volts power supply
- Intel/Motorola bus interface
- ST-BUS compatible

Applications

- Featured digital telephone sets
- Voice/Data terminals
- Cellular radio sets

Description

The MT8994/5 is an integrated digital telephone circuit (D-Phone). Conversion of analog signals to digital PCM and vice versa is accomplished with an on-chip filter codec. Digital signal processing techniques provide speaker-phone operation and generation of ringing tone and DTMF signals. The D-Phone incorporates a bus interface compatible with Intel or Motorola microprocessors and includes an ST-BUS™ serial interface. The device is fabricated in Mitel's ISO²-CMOS technology which ensures low power consumption and high reliability.

Pin Connections

SPKR+	1	40	VDD
HSPKR−	2	39	SPKR−
CODECn	3	38	HSPKR+
PWRST	4	37	VSS SPKR
CS	5	36	VREF
AS,ALE	6	35	VBIAS
DS,RD	7	34	M−
R/W,WR	8	33	M+
AD7	9	32	MIC
AD6	10	31	F0i
AD5	11	30	DSTi
AD4	12	29	DSTo
AD3	13	28	C4i
AD2	14	27	SD6
AD1	15	26	SD5
AD0	16	25	SD4
NC	17	24	SD3
WD	18	23	SD2
IC	19	22	SD1
VSS	20	21	SD0

Ordering Information

MT8994/5AC μ-Law/A-Law 40 Pin Cerdip
MT8994/5AE μ-Law/A-Law 40 Pin Plastic DIL
0 °C to + 70 °C

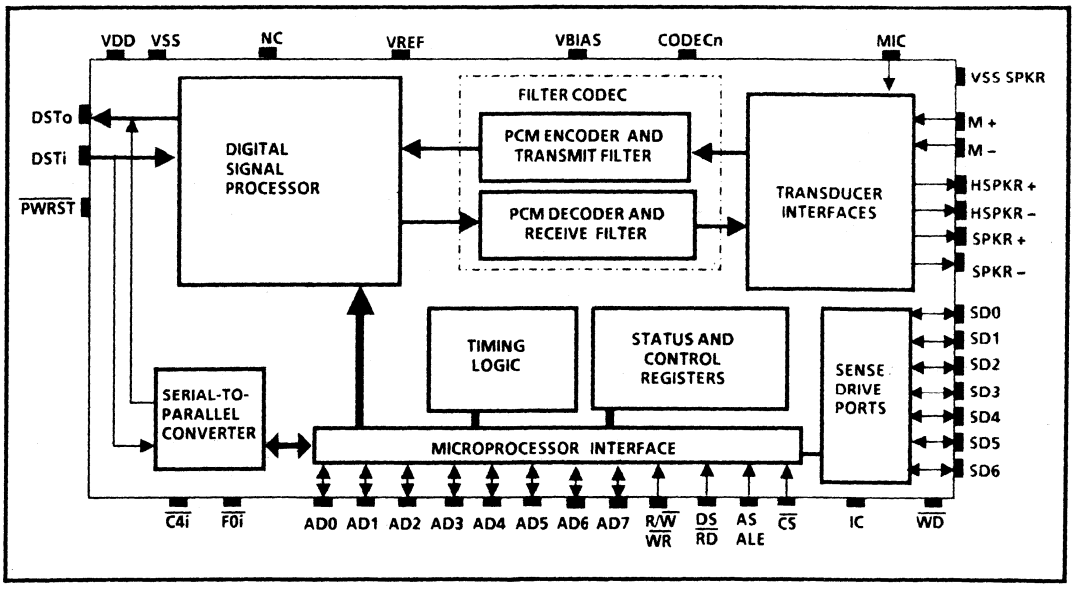


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings*

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		$V_{DD} - V_{SS}$	- 0.3	7	V
2	Voltage on any I/O pin		V_I/V_O	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current on any I/O pin		I_I/I_O		± 20	mA
4	Storage Temperature		T_S	- 65	+ 150	°C
5	Power Dissipation (package)	Plastic	P_D		0.6	W
		Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5	5.25	V	
2	Input Voltage (high)	V_{IH}	2.4		V_{DD}	V	Noise margin = 400 mV
3	Input Voltage (low)	V_{IL}	V_{SS}		0.4	V	Noise margin = 400 mV
4	Operating Temperature	T_O	0		+ 70	°C	
5	Clock Frequency	f_{CLK}		4096		kHz	

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current (clock disabled)	I_{DDC1}		1		mA	outputs unloaded
	(clock enabled)	I_{DDC2}		2		mA	
2	Supply Current (handset speaker enabled) No Load	I_{DDH1}		6		mA	no signal
	Load = 150Ω	I_{DDH2}		7		mA	- 20 dBm0, 1020 Hz
		I_{DDH3}		8		mA	0 dBm0, 1020 Hz
3	Supply Current (speaker driver enabled) No Load	I_{DDS1}		9		mA	no signal
	Load = 40Ω	I_{DDS2}		12		mA	- 20 dBm0, 1020 Hz
		I_{DDS3}		45		mA	0 dBm0, 1020 Hz
4	Input HIGH Voltage TTL inputs	V_{IH}	2.0			V	
5	Input LOW Voltage TTL inputs	V_{IL}			0.8	V	
6	Input Leakage Current	I_{IZ}			1	μA	$V_{IN} = V_{DD}$ to V_{SS}
7	Positive Going Threshold Voltage (PWRST only)	V_{T+}		1.7			V_{DD} = 5 V
	Negative Going Threshold Voltage (PWRST only)	V_{T-}		1.2			V_{DD} = 5 V
8	Output LOW Voltage TTL O/P	V_{OL}			0.4	V	I_{OL} = 3 mA
9	Output HIGH Voltage TTL O/P	V_{OH}	2.4			V	I_{OH} = 10 mA
10	Output HIGH Current TTL O/P	I_{OH}	10	15		mA	V_{OH} = 2.4 V
11	Output LOW Current TTL O/P	I_{OH}	3	5		mA	V_{OL} = 0.4 V
	SD0-6			3			V_{OL} = 0.4 V
	SD0-6			15			V_{OL} = 2.5 V
12	Output Voltage	V_{REF}		0.5		V	no load
		V_{BIAS}		2.5			
13	Output Leakage Current	I_{OZ}			1	μA	$V_{OUT} = V_{DD}$ to V_{SS}

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Pin Capacitance	C_{IN}		8		pF	
2	Output Pin Capacitance	C_{OUT}		8		pF	

† Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† -ST-BUS Timing (See Figure 2)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\overline{C4}$i Clock Period	t_{C4P}	243.9	244.1	244.3	ns	
2	$\overline{C4}$i Clock High period	t_{C4H}	110	122	134	ns	
3	$\overline{C4}$i Clock Low period	t_{C4L}	110	122	134	ns	
4	$\overline{C4}$i Clock Transition Time	t_T		20		ns	
5	$\overline{F0}$i Frame Pulse Setup Time	t_{F0iS}	50		150	ns	
6	$\overline{F0}$i Frame Pulse Hold Time	t_{F0iH}	50		150	ns	
7	$\overline{F0}$i Frame Pulse Width Low	t_{F0iW}	100		300	ns	
8	DSTo Delay	t_{DSToD}			145	ns	C_L = 150 pF
9	DSTi Setup Time	t_{DSTiS}	30			ns	
10	DSTi Hold Time	t_{DSTiH}	50			ns	

* Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

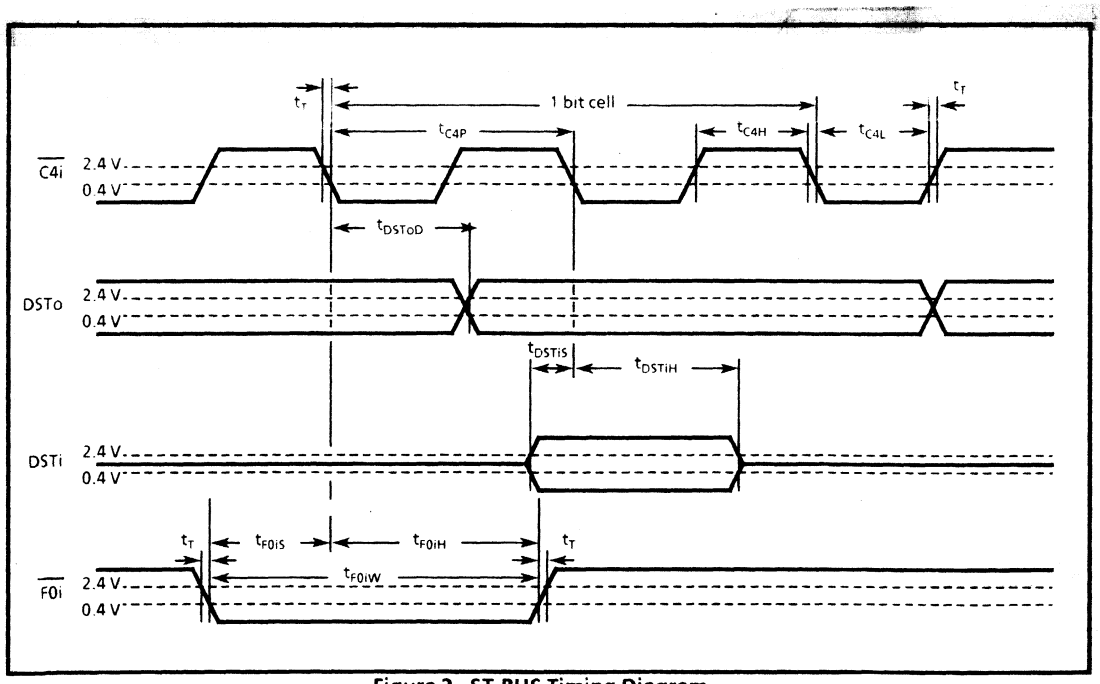


Figure 2 - ST-BUS Timing Diagram

AC Electrical Characteristics - Microprocessor Bus Timing† - (See Figures 3, 4 & 5)

	Characteristics	Sym	Min	Typ‡	Max	Units
1	Cycle Time	t_{CYC}	667			ns
2	Pulse Width, DS Low or $\overline{RD}$, $\overline{WR}$ High	PW_{EL}	200			ns
3	Pulse Width, DS High or $\overline{RD}$, $\overline{WR}$ Low	PW_{EH}	200			ns
4	Input Rise and Fall Time	t_r, t_f			30	ns
5	R/$\overline{W}$ Hold Time	t_{RWH}	10			ns
6	R/$\overline{W}$ Set up Time Before DS	t_{RWS}	30			ns
7	Chip Select Setup Time Before AS, ALE Fall	t_{CS}	50			ns
8	Chip Select Hold Time	t_{CH}	0			ns
9	Read Data Hold Time	t_{DHR}	10		100	ns
10	Write Data Hold Time	t_{DHW}	15			ns
11	Muxed Address Valid Time to AS, ALE Fall	t_{ASL}	40			ns
12	Muxed Address Hold Time	t_{AHL}	15			ns
13	Delay Time DS to AS, ALE Rise	t_{ASD}	50			ns
14	Pulse Width, AS, ALE High	PW_{ASH}	100			ns
15	Delay Time AS, ALE to DS Rise	t_{ASED}	60			ns
16	Peripheral Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}			150	ns
17	Peripheral Data Setup Time	t_{DSW}	100			ns

†Timing is over recommended temperature range & recommended power supply voltages. All values shown assume a 50 pF load on the data pins. Read means read from the D-Phone and Write means write to the D-Phone.

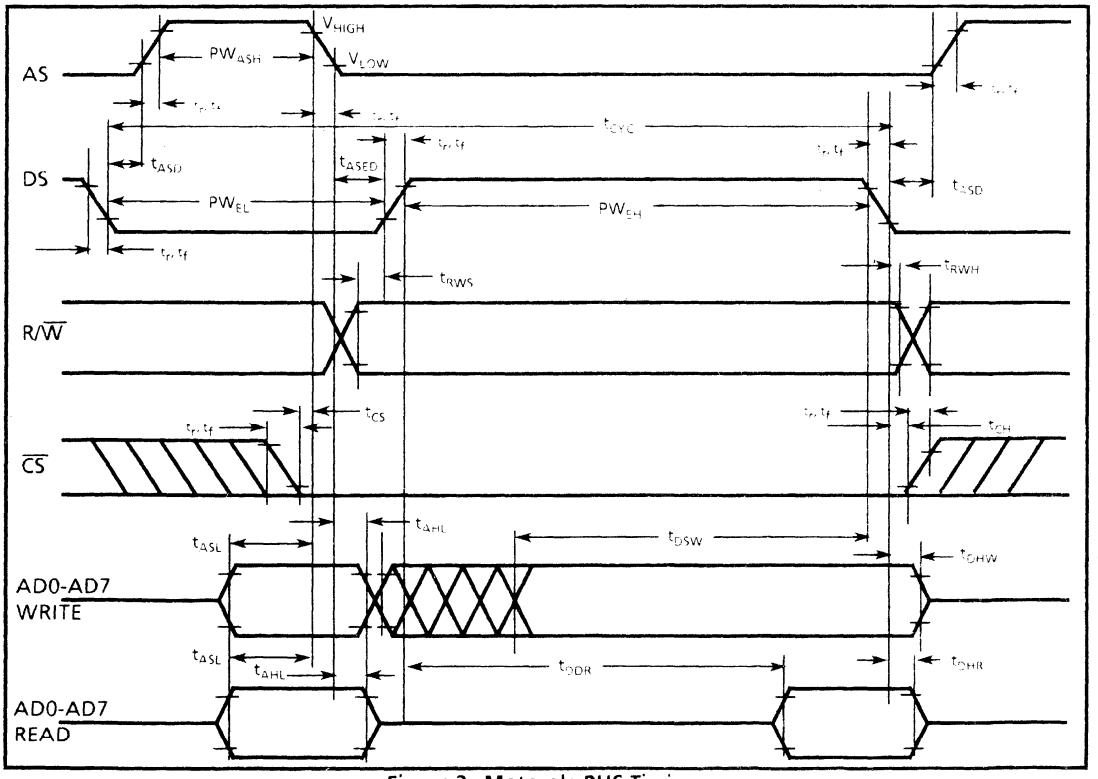


Figure 3 - Motorola BUS Timing

Note: $V_{HIGH} = (V_{DD} - 2.0)$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 5 %

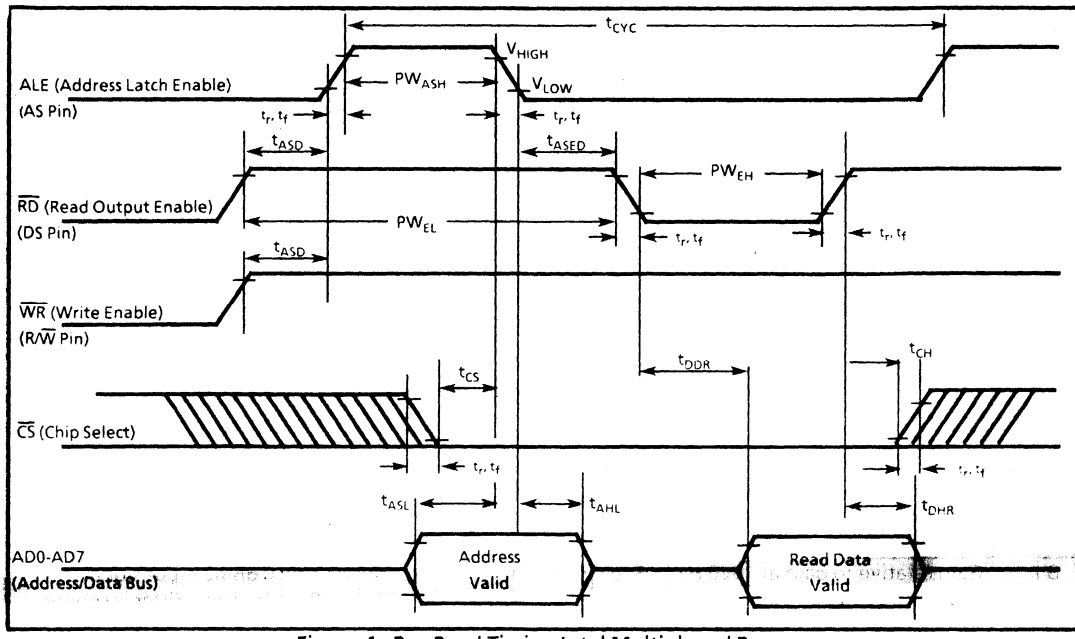


Figure 4 - Bus Read Timing Intel Multiplexed Bus

Note: V_{HIGH} = (V_{DD} - 2.0) V , V_{LOW} = 0.8 V, for V_{DD} = 5.0 V ±5 %

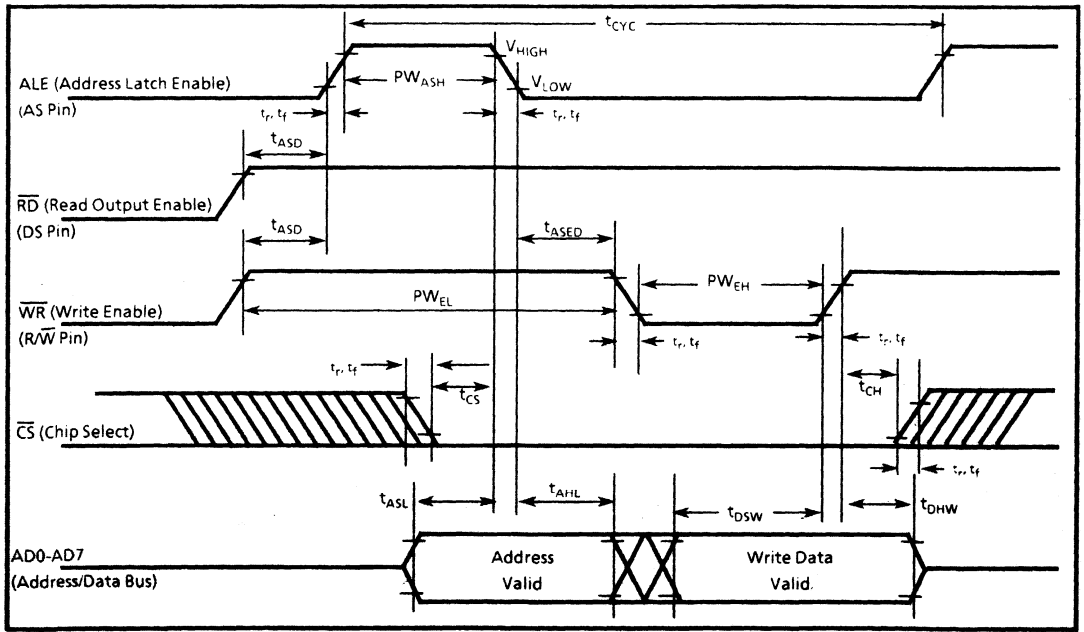


Figure 5 - Bus Write Timing Intel Multiplexed Bus

Note: V_{HIGH} = (V_{DD} - 2.0) V , V_{LOW} = 0.8 V, for V_{DD} = 5.0 V ±5 %

AC Electrical Characteristics † - Transmit Path (Microphone Interface, Transmit Filter And A/D)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Analog input to the codec equivalent to overload decision	V_{IN}		3.863 4.000		V_{pp} V_{pp}	μ-Law ① A-Law ①
2	Absolute Gain ②	G_{AX}	13.15 16.45	13.50 16.80	13.85 17.15	dB dB	μ-Law at 1020 Hz A-Law at 1020 Hz
3	Gain Tracking CCITT G.712 method 2 AT&T	GT_X	 – 0.25 – 0.5 – 1.5		 + 0.25 + 0.5 + 1.5	 dB dB dB	sinusoidal level 3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0
4	Quantization Distortion CCITT G.712 method 2 AT&T	D_{QX}	 35.3 29.3 24.3			 dB dB dB	 0 to – 30 dBm0 – 40 dBm0 – 45 dBm0
5	Idle Channel Noise	N_{CX} N_{PX}		18 – 70		dBrnC0 dBmp0	μ-Law A-Law
6	Harmonic Distortion	D_H			– 46	dB	Input signal 0 dBm0 at 1020 Hz
7	Envelope Delay 1000-2600 Hz Variation with 600-3000 Hz Frequency 400-3200 Hz	D_{DX}		60 150 250		μs μs μs	Input signal: 400-3200 Hz sinewave at 0 dBm0
8	Gain relative to gain at 1020 Hz < 50 Hz 60 Hz 200 Hz 300-3000 Hz 3200 Hz 3300 Hz 3400 Hz 4000 Hz >4600 Hz	G_{RX}	 – 1.8 – 0.15 – 0.275 – 0.35 – 0.8		 – 25 – 30 0.0 0.15 0.15 0.03 – 0.1 – 14 – 32	 dB dB dB dB dB dB dB dB dB	0 dBm0 input signal Transmit Filter response with High Pass Filter disabled (Refer to Section 2.3 and Table 6).
9	Power Supply Rejection	PSRR					

† Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
① 0 dBm0 = 0.948 V_{RMS} for μ-Law and 0.985 V_{RMS} for A-Law (V_{REF} = 0.5 volt and V_{BIAS} = 2.5 volts)
② The Transmit filter is adjustable from 0 to + 6 dB in 2 dB steps

AC Electrical Characteristics† - Receive Path (D/A, Receive Filter, Speaker-phone Speaker/ Handset Speaker Interface)

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Analog output to the codec equivalent to overload decision	V_{OUT}		3.863 4.000		V_{PP} V_{PP}	μ-Law A-Law
2	Absolute gain (Receive Filter and D/A) ③	G_{AR}	- 0.35 - 0.35	0.0 0.0	+ 0.35 + 0.35	dB dB	μ-Law at 1020 Hz A-Law at 1020 Hz
3	Deviation of attenuation adjustment (Receive Filter)	D_{AA}	- 0.1		0.1	dB	from nominal
4	Differential handset speaker driver gain	G_{DA}	- 14.25 - 13.65	- 13.90 - 13.30	- 13.55 - 12.95	dB dB	μ-Law across 150 Ω, See A-Law Figure 16
5	Side-tone ④	S_T		- 7.3 - 15.9		dB dB	μ-Law from MIC inputs A-Law to HSPKR outputs
6	Differential speaker-phone speaker driver gain	G_{SS}		9.6 13.3		dB dB	μ-Law A-Law - 10 dBm0 input signal, 40 ohm load across SPKR + and SPKR -
7	Gain tracking CCITT G.712 method 2 μ-Law (Speaker-phone speaker) A-Law (Speaker-phone speaker) μ-Law, A-Law (Handset speaker)	GT_R	 - 0.25 - 0.5 - 1.5 - 0.25 - 0.5 - 1.5 - 0.25 - 0.5 - 1.5		 + 0.25 + 0.5 + 1.5 + 0.25 + 0.5 + 1.5 + 0.25 + 0.5 + 1.5	 dB dB dB dB dB dB dB dB dB	 - 4 to - 40 dBm0 - 40 to - 50 dBm0 - 50 to - 55 dBm0 - 8 to - 40 dBm0 - 40 to - 50 dBm0 - 50 to - 55 dBm0 + 3 to - 40 dBm0 - 40 to - 50 dBm0 - 50 to - 55 dBm0
8	Quantization distortion CCITT G.712 method 2	D_{QR}	35.4 29.4 24.4			dB dB dB	- 5 to - 30 dBm0 - 40 dBm0 - 45 dBm0
9	Idle channel noise	N_{CR} N_{PRS} N_{PRHS}		22 - 62 - 85		dBrnC0 dBmp0 dBmp0	μ-Law SPKR +, SPKR - A-Law SPKR +, SPKR - A-Law and μ-Law across HSPKR +, HSPKR -
10	Gain relative to gain at 1020 Hz <200 Hz 200 Hz 300-3000 Hz 3200 Hz 3300 Hz 3400 Hz 4000 Hz >4600 Hz	G_{RR}	 - 0.5 - 0.15 - 0.275 - 0.35 - 0.8		 0.15 0.15 0.15 0.15 0.03 - 0.1 - 14 - 28	 dB dB dB dB dB dB dB dB	Receive Filter response with DIAL disabled (Refer to Section 3.1 and Table 7).
11	Power Supply Rejection	PSRR					

† Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
① 0 dBm0 refers to the input to the drivers from the codec, Rx filters and the PCM at DSTi.
② Distortion may degrade due to clipping at lower V_{DD} voltages or when valid input signal levels have been exceeded.
③ Note that Rx filter can be adjusted from 0 to - 7 dB in 1 dB steps.
④ Roll-off 6 dB/octave @ 2.5 kHz

AC Electrical Characteristics†- Receive Path (D/A, Receive Filter, Speaker-phone Speaker/ Handset Speaker Interface)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
12		Speaker driver distortion 1ST 2ND Total Distortion	D_S		– 30 – 30 – 30		dB dB dB	– 10 dBm0 input signal, 40 ohm load across SPKR + and SPKR – ① ②
13		PCM input without clipping at the speaker μ-Law A-Law	C_{PCM}			– 3.39 – 7.39	dBm0 dBm0	40 ohm load across SPKR + and SPKR –
14		Handset driver distortion 1ST 2ND Total Distortion	D_H		– 30 – 30 – 30		dB dB dB	0 dBm0 input signal, 150 Ω load across HSPKR + and HSPKR – ① ②
15		Output offset voltage SPKR + ,SPKR – , HSPKR + and HSPKR –	V_{OS}	– 100	0	100	mV	w.r.t. V_{BIAS}
16		SPKR + and SPKR – peak power μ-Law A-Law				95	mW	40 ohm speaker
17		Envelope Delay 1000-2600 Hz Variation with 600-3000 Hz Frequency 400-3200 Hz	D_{DR}		90 170 265		μs μs μs	Input signal: 400-3200 Hz digital sinewave at 0dBm0

† Timing is over recommended temperature range & recommended power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

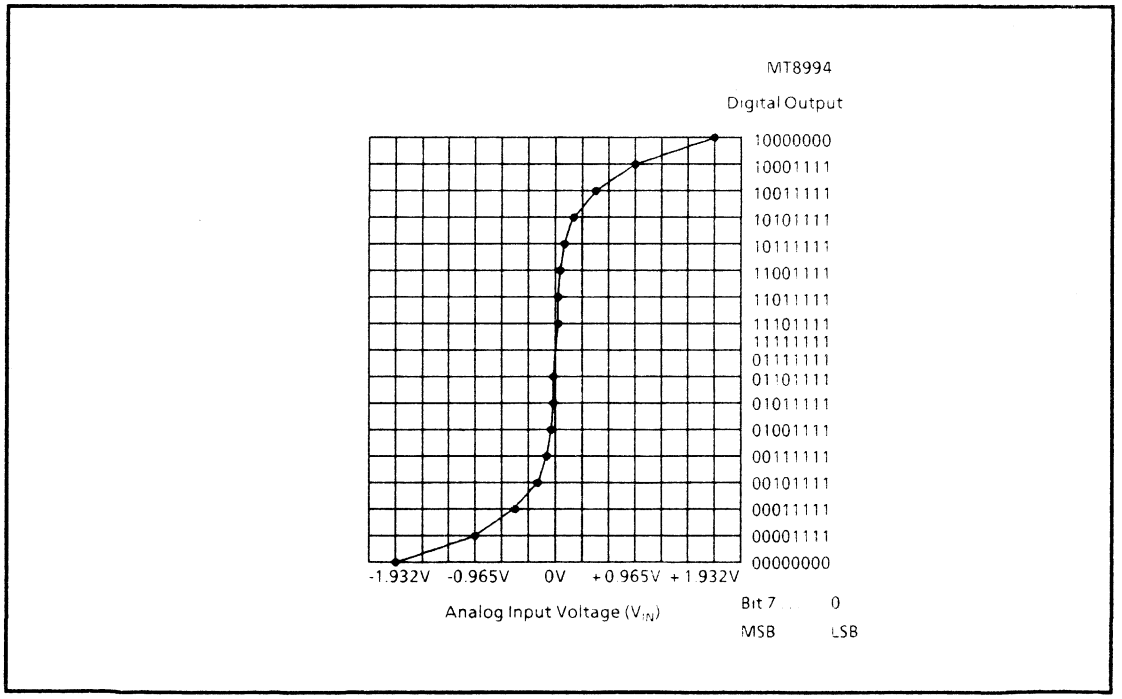


Figure 6 - μ-Law Encoder Transfer Characteristic

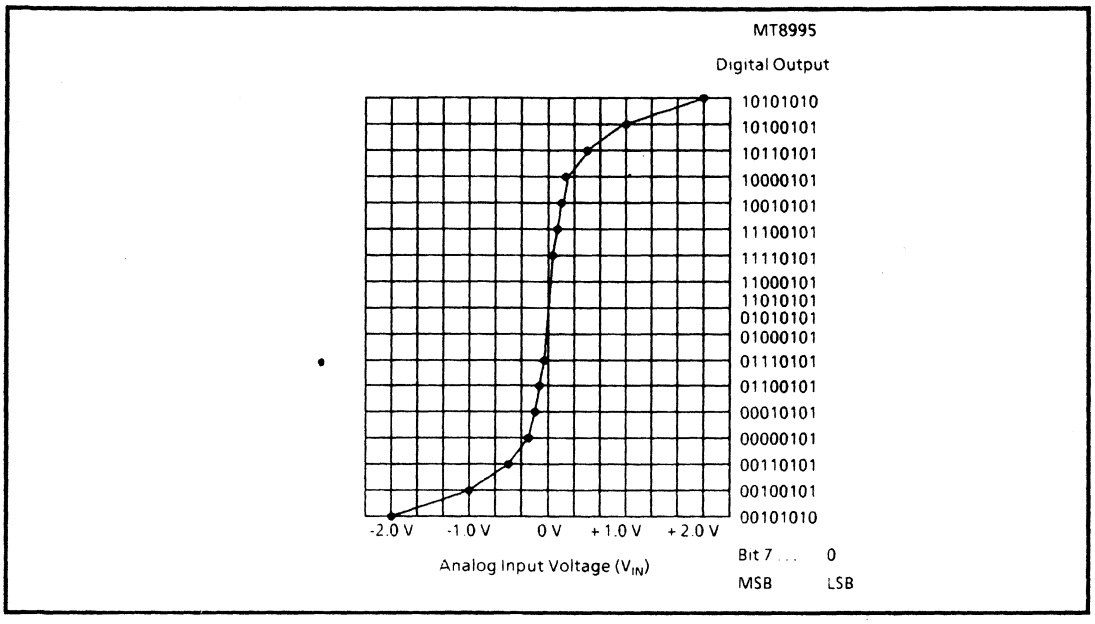


Figure 7 - A-Law Encoder Transfer Characteristic

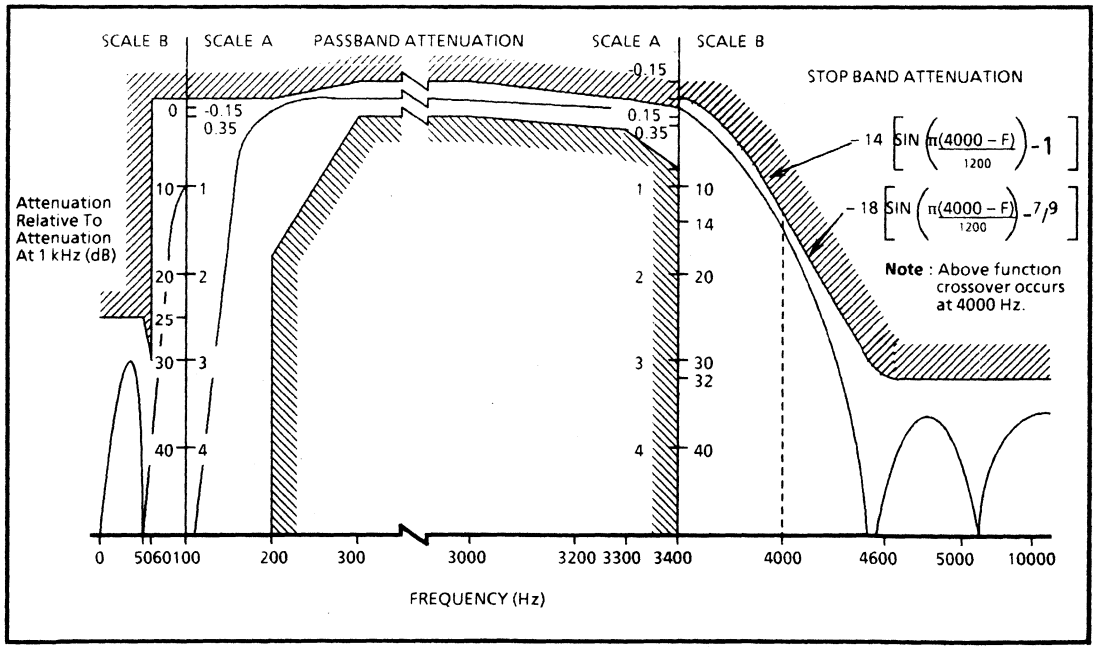


Figure 8 - Attenuation vs Frequency for Transmit Filter

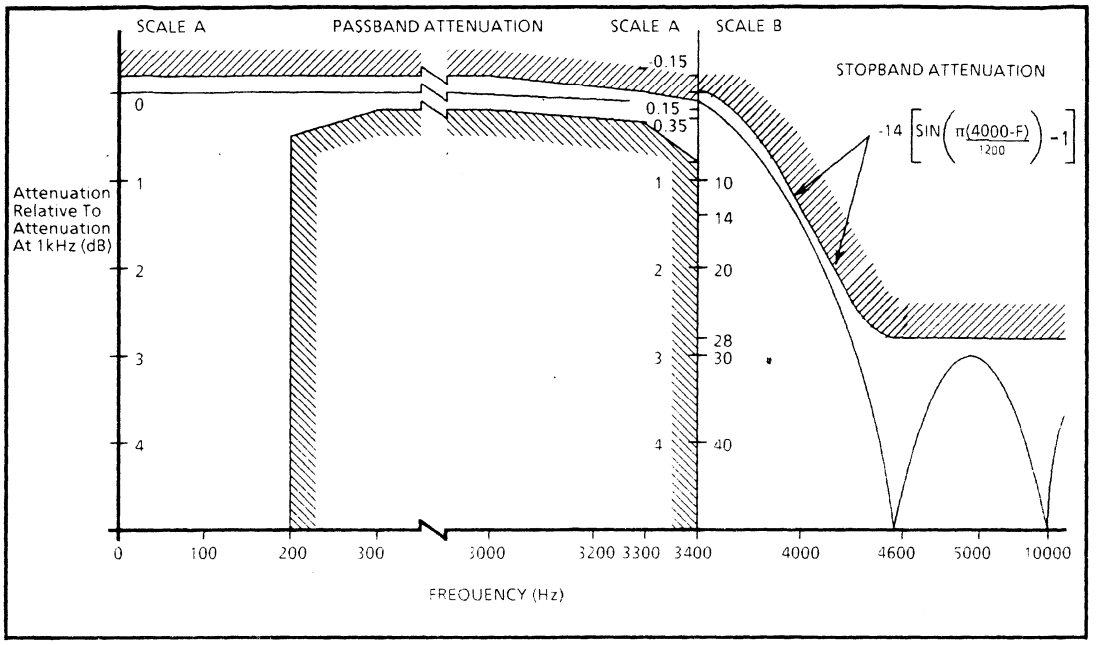


Figure 9 - Attenuation vs Frequency for Receive Filter

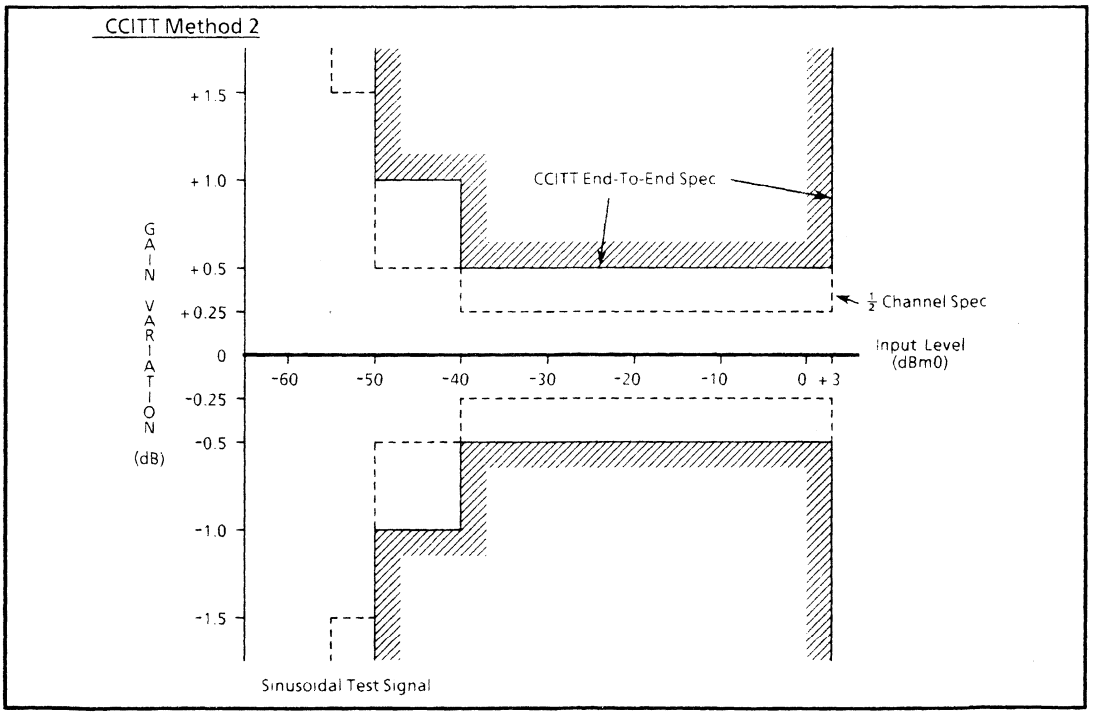


Figure 10 - Variation of Gain With Input Level (Handset Interface)

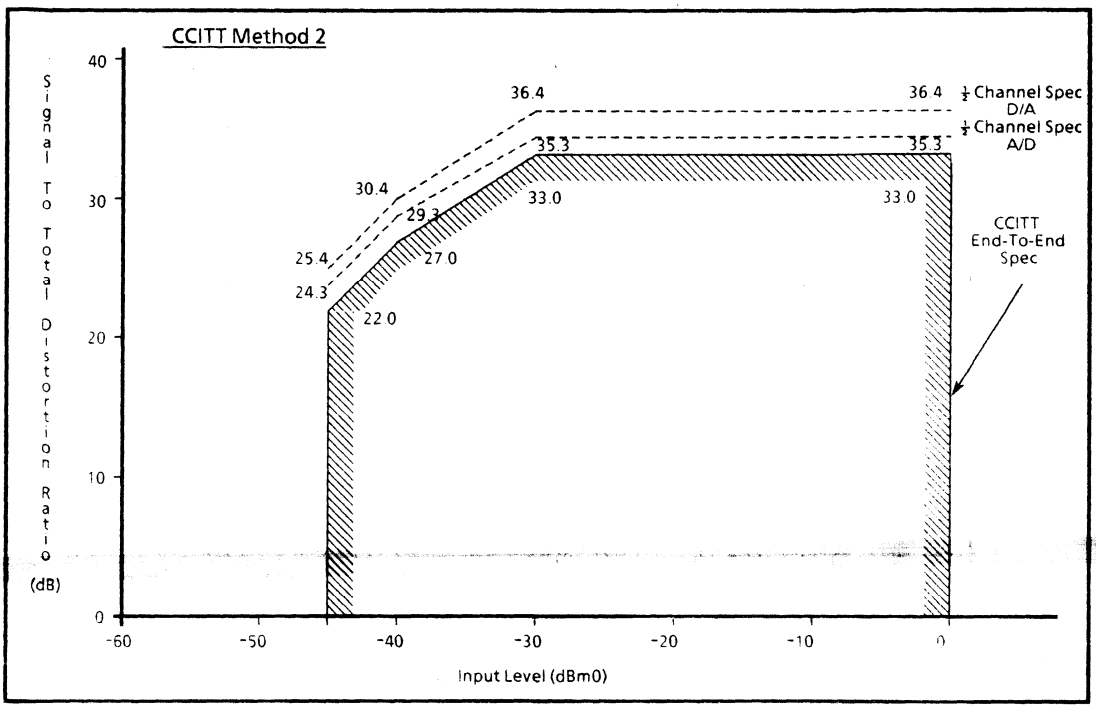


Figure 11 - Signal to Total Distortion Ratio vs Input Level (Handset Interface)

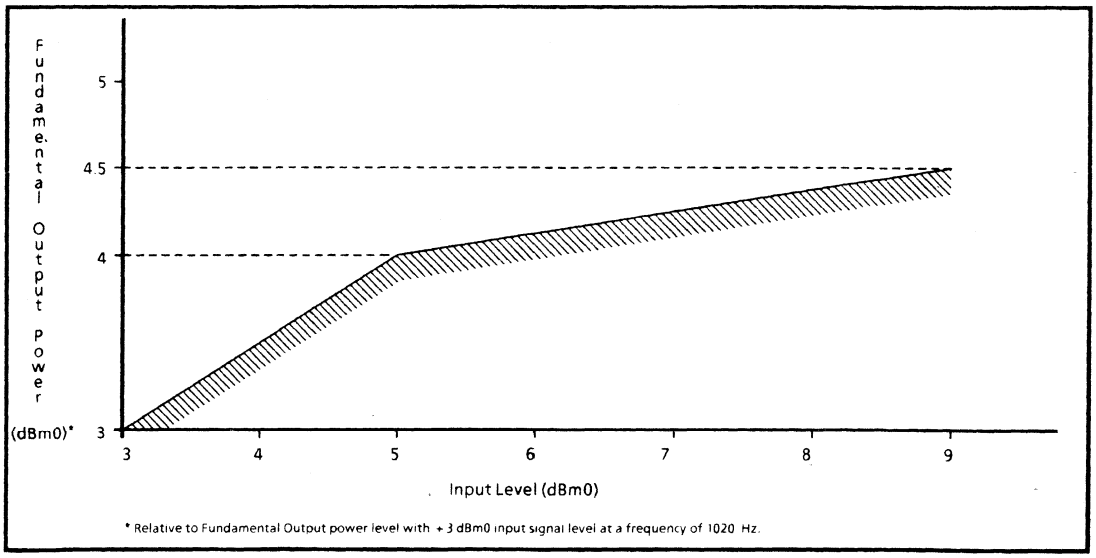


Figure 12 - Overload Distortion (End-to-End, Handset Interface)

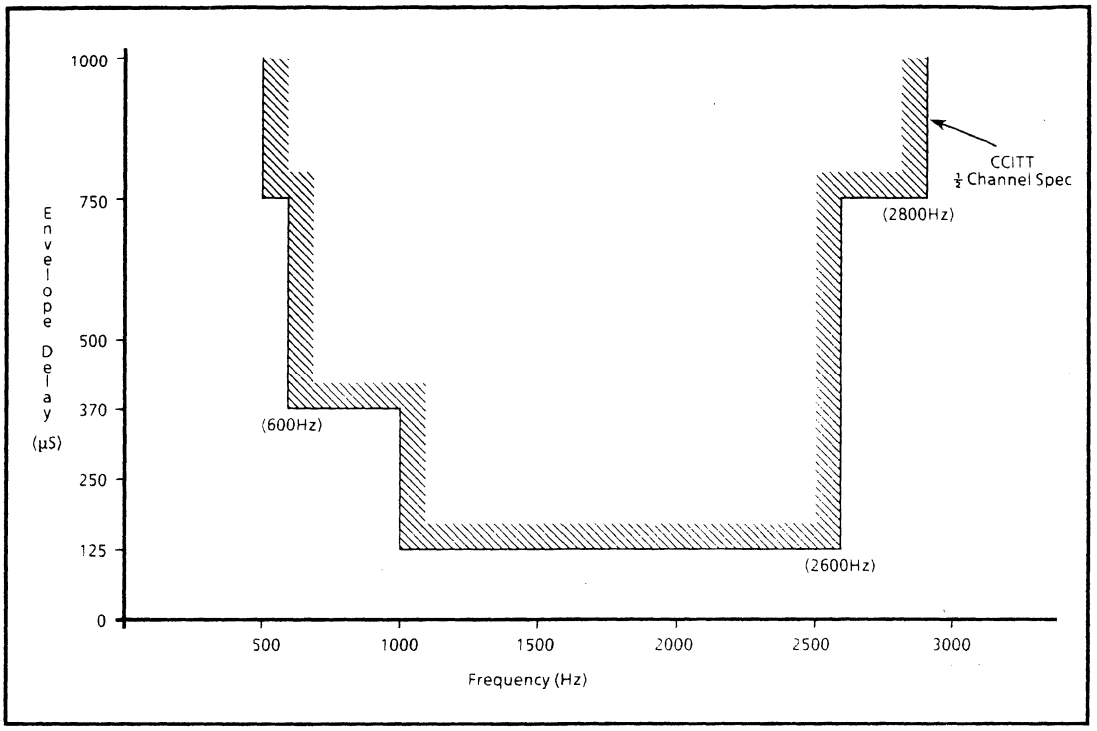


Figure 13 - Envelope Delay Variation With Frequency

Recommended Operating Conditions - Speaker-phone† (Reference section 2.3.1 and Table 5)

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1		Acoustic Separation						Receive Filter
		µ-Law		33			dB	gain = – 3.0 dB
		A-Law		40			dB	Transmit Filter
								gain = + 2.0 dB
2		Microphone Amplifier gain						Receive Filter
		µ-Law				35.6	dB	gain = – 3.0 dB
		A-Law				35.6	dB	Transmit Filter
								gain = + 2.0 dB
3		SPKR + and SPKR – capacitive load allowed per pin				2000	pF	direct speaker connection

* Parameters 1 and 2 are for design aid only and will give optimum results for Speaker-phone (hands-free) operation.

Recommended Operating Conditions - Handset Microphone

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Sensitivity	S		-40		dBV	acoustic input of 0 dBPa at 7.6 mm from lip ring at 1000 Hz
2		Output Impedance	Z_{OUT}		1		kΩ	at 1000 Hz
3		Harmonic Distortion	THD		1		%	between 300 and 3000 Hz with an input level of 0 dBPa

‡ Typical figures are at 25 °C and are for design aid only. Refer to IEEE 269 for artificial mouth calibration procedure.

Recommended Operating Conditions - Speaker-phone Microphone

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Sensitivity	S		-64		dB	(0 dB = 1 V/μbar) input of 1 μbar at 1000 Hz
2		Output Impedance	Z_{OUT}		2.2		kΩ	at 1000 Hz
3		Harmonic Distortion	THD		1		%	between 300 and 3000 Hz with an input level of 0 dBPa

‡ Typical figures are at 25 °C and are for design aid only.

Recommended Operating Conditions - Handset Speaker

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Efficiency			95.5		dBSPL	Reference frequency 1000 Hz, input signal 81.4 mV_{RMS} (open circuit) and closed loop generator impedance 150Ω
2		Impedance			150		Ω	Reference1000 Hz
3		Harmonic Distortion			1		%	between 300 and 3000 Hz

‡ Typical figures are at 25 °C and are for design aid only.

Recommended Operating Conditions - Speaker-phone Speaker

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Efficiency						
2		Impedance			40		Ω	at 1000 Hz
3		Harmonic Distortion			1		%	between 300 and 3000 Hz

‡ Typical figures are at 25 °C and are for design aid only.

AC Electrical Characteristics - Handset Speaker Driver - A-Law

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		HSPKR + and HSPKR – gain		– 7.65	– 7.30 – 13.3	– 6.95	dB dB	No load 150 ohm load (See Fig. 17)
2		HSPKR + and HSPKR – signal level				301	mV_{RMS}	Receive Filter Gain = 0 dB 150 ohm speaker with 3.14 dBm0 signal
3		HSPKR + and HSPKR – drive output				604	μW	150 ohm speaker with 3.14 dBm0 signal
4		Side-tone (from MIC input)				– 10.5 – 15.9	dB dB	with external amplifier † without external amplifier

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

† This is required to maintain speaker-phone audio loop stability. See section 2.3.1 and Table 5 for details.

AC Electrical Characteristics - Handset Speaker Driver - μ-Law

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		HSPKR + and HSPKR – gain		– 8.25	– 7.90 – 13.9	– 7.55	dB dB	No load 150 ohm load (See Fig. 17)
2		HSPKR + and HSPKR – signal level				271	mV_{RMS}	Receive Filter Gain = 0 dB 150 ohm speaker with 3.17 dBm0 signal
3		HSPKR + and HSPKR – power output				491	μW	150 ohm speaker with 3.17 dBm0 signal
4		Side-tone (from MIC input)				– 6.0 – 7.3	dB dB	with external amplifier † without external amplifier

‡Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

†This is required to maintain speaker-phone audio loop stability. See section 2.3.1 and Table 5 for details

AC Electrical Characteristics - Tone Ringer *

		Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1		Oscillator Frequency	F_O	15.7		4000	Hz	
2		Frequency Resolution	F_R	0.06		2000	Hz	
3		Frequency Shift Rate	F_S	10		16	Hz	

* Frequencies are over recommended temperature range & recommended power supply voltages

AC Electrical Characteristics - Dual Tone Genarator *

		Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1		Frequency Generated		7.8		1992	Hz	
2		Frequency Resolution		3.9			Hz	

* Frequencies are over recommended temperature range & recommended power supply voltages.

AC Electrical Characteristics - Dual Tone Multi-Frequency Signals Generation†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Low Frequency 1 Deviation	D_{LF1}		- 0.20		%	Nominal = 697 Hz
2	Low Frequency 2 Deviation	D_{LF2}		+ 0.40		%	Nominal = 770 Hz
3	Low Frequency 3 Deviation	D_{LF3}		- 0.05		%	Nominal = 852 Hz
4	Low Frequency 4 Deviation	D_{LF4}		+ 0.46		%	Nominal = 941 Hz
5	High Frequency 1 Deviation	D_{HF1}		+ 0.20		%	Nominal = 1209 Hz
6	High Frequency 2 Deviation	D_{HF2}		0.0		%	Nominal = 1336 Hz
7	High Frequency 3 Deviation	D_{HF3}		- 0.03		%	Nominal = 1477 Hz
8	High Frequency 4 Deviation	D_{HF4}		- 0.01		%	Nominal = 1633 Hz
9	Negative Twist	dBp		2.5		dB	
10	Output Amplitude Low Group High Group Low Group High Group	V_{OUT}	 – 9.0 – 6.5 – 14.5 – 12.5	 – 8.5 – 6.0 – 14.0 – 12.0	 – 8.0 – 5.5 – 13.5 – 11.5	 dBm0 dBm0 dBm0 dBm0	 μ-Law μ-Law A-Law A-Law
11	Distortion	THD		– 25		dB	

† Frequencies are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Pin Description

Pin #	Name	Description
1	SPKR +	**Non-Inverting Speaker (Output).** Output to the loudspeaker (balanced).
2	HSPKR –	**Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
3	CODECn	**CODEC Auto-null (Output).** Auto-null point for codec input. Connect 0.1 μF capacitor to V_{SS}.
4	$\overline{PWRST}$	**Power-up reset (Input).** CMOS compatible input with Scmitt trigger (active low).
5	$\overline{CS}$	**Chip Select (Input).** TTL level compatible (active low). This input signal is used to select the device.
6	AS, ALE	**Address Strobe, Address Latch Enable (Input).** TTL level compatible. The falling edge of AS or ALE causes the address to be latched within the device.
7	DS, $\overline{RD}$	**Data Strobe, Read (Input).** TTL level compatible. When used with Motorola microprocessors, DS is a positive pulse and is commonly referred to as DS (data strobe), E (enable) and Φ2 (phase 2). Functions as Intel Read signal also.
8	R/$\overline{W}$, $\overline{WR}$	**Read/Write, Write (Input).** TTL level compatible. This pin functions as a Read/Write input with Motorola microprocessors or as a Write input with Intel microprocessors.
9-16	AD0-AD7	**Multiplexed Address/Data bus (Bidirectional).** TTL level compatible.
17	NC	**No Connection.** Leave open circuit
18	$\overline{WD}$	**Watchdog (Output).** Watchdog timer output. Active Low
19	IC	**Internal Connection.** Tied to V_{SS} for normal operation.
20	V_{SS}	**Ground.** Nominally 0 V.
21-27	SD0-SD6	General purpose sense/drive points **(Bi-directional, open drain).** Input mode is TTL compatible.
28	$\overline{C4i}$	**4096 kHz clock (Input).** TTL level compatible.
29	DSTo	**ST-BUS™ Serial Stream (Output).** 2048 kbit/s output stream composed of 32 8-bit channels. The D-Phone sources digital signals during the appropriate channel, time coincident with the channels used for DSTi.
30	DSTi	**ST-BUS™ Serial Stream (Input).** 2048 kbit/s input stream composed of 32 8-bit channels; the first four of which may be used by the D-Phone for one of the following functions: 1) a transparent port 2) a PCM channel for the codec (B-channel) Input level is TTL compatible.
31	$\overline{F0i}$	**Frame Pulse (Input).** Input TTL level compatible. This input is for the frame synchronization pulse for the 2048 kbit/s ST-BUS™ stream.
32	MIC	**Microphone (Input).** Single ended input to microphone amplifier.
33	M +	**Non-Inverting Microphone (Input).** Non-inverting input to microphone amplifier from the handset microphone.
34	M –	**Inverting Microphone (Input).** Inverting input to microphone amplifier from the handset microphone.
35	V_{BIAS}	**Bias Voltage (Output).** Nominally (V_{DD}/2) volts. Used to bias the external analogue interface op-amps and the microphone input. Connect 0.1 μF capacitor to V_{SS}.
36	V_{REF}	**Reference voltage for codec (Output).** Nominally [(V_{DD}/2) – 2] volts. Used internally. Connect 0.1 μF capacitor to V_{SS}.
37	V_{SS} SPKR	**Power supply rail for speaker driver.**
38	HSPKR +	**Non-Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
39	SPKR –	**Inverting Speaker (Output).** Output to the speaker-phone speaker (balanced).
40	V_{DD}	**Positive power supply (Input).** Nominally 5 volts.

Functional Description

The trend in the digital telecommunications industry is to have digital transmission at the telephone end of the subscriber loop. Transferring voice down a digital channel requires sampling of the analog baseband voice signal at 8 kHz and producing an eight bit code from the sample. One type of encoding is called Pulse Code Modulation (PCM).

The MT8994/5 (D-Phone) is a CMOS digital telephone integrated circuit. The MT8994 conforms to the AT & T D3/D4 specification. This is the μ-Law Companding code. The MT8995 conforms to the CCITT G.712 specification. This is the A-Law Companding code. The D-Phone realizes the major functions required of a digital telephone. These functions are:

i) The conversion of analog to digital PCM and vice versa. This is the Codec function;

ii) Generation of tones. These are Dual Tone Multi-Frequency (DTMF) signals;

iii) Tone Ringer. This is intended for use as replacement for the mechanical bell in telephpone sets;

iv) Speaker-phone. This is for hands-free telephone operation;

v) The handset and the speaker-phone transducer interfaces;

vi) Sense/drive ports for keyboard scanning and display functions.

A block diagram of the D-Phone chip is shown in Figure 1. The chip is controlled via an 8-bit multiplexed address/data bus (AD0-AD7) with MOTEL circuit for bus universality. There are eleven 8-bit control registers through which the D-Phone is configured in various operating modes. Through this microprocessor port, a microprocessor has access to seven sense/drive ports (SD0-SD6) intended for keyboard scanning and display functions and a serial interface. The serial interface is the ST-BUS pins DSTi and DSTo. It provides for upto three digital PCM channels for the D-Phone telephony functions and a single transparent channel for interfacing with the external microprocessor. The digital signal processor (DSP) section executes three programs: a digital speaker-phone algorithm, a tone ringer, and a DTMF generator. The DSP operates on the digital PCM streams between the Codec and DSTi and DSTo. Both the μ-Law and the A-Law Companding codes can be accomodated. The DSP section also includes a programmable timer which is used in the generation of the ringing signals. The Filter Codec section provides the conversion interface between the voiceband analog signals of a telephone subscriber loop and the digital signals required in a digital PCM switching system. The Receive and Transmit Filters have programmable gain feature. In the transmit direction the input to the Transmit Filter is from either the handset microphone or the speaker-phone microphone while the receive signal can be routed to the handset and the speaker-phone speaker drivers. The details of operating the D-Phone is considered in the following sections:

1.0 Serial Interface

Transmitting the analog baseband voice signal down a digital channel requires a digital bandwith of 64 kbit/s. This value is derived assuming that normal voice has an upper frequency bound of 3400 Hz and that voice is translated into digital format by sampling at the rate of 8 kHz and producing an eight bit PCM sample. Because of the sampling at 8 kHz, the frame must be transmitted in a period of 125 μs. The serial interface provides for this transmission capacity of 8 bits x 8 kHz = 64

kbit/s necessary for the transmission of a telephone channel.

The serial interface is an input and an output serial data stream, running at half the $\overline{C4i}$ input rate (2048 kbit/s). This is referred to as the ST-BUS. The ST-BUS input is referred to as DSTi and the output is referred to as DSTo. See Figure14 for the format of ST-Bus Stream.

The timing for the ST-BUS is shown in Figure 2. The ST-BUS consists of 32, 8-bit channels per 125 μs frame. The frame pulse ($\overline{F0i}$) defines the frame boundaries, repeating every 125 μs. Each of the 32 channels is 3.9 μs in duration with a bit period of 488.2 ns. For more information on ST-BUS refer to ST-BUS Generic Device Specification MSAN-126.

There is an accompanying data clock ($\overline{C4i}$) which has a specified relationship with frame timing and bit timing. DSTi is sampled at the halfway point in a bit cell and DSTo is output at the start of a bit cell. Both are clocked at the falling edges of $\overline{C4i}$ one clock period apart.

The ST-BUS is connected internally to two sections of the D-Phone: the Digital Signal Processor (DSP) and the Serial-to-parallel Converter. These sections can be separately disabled to allow other devices to operate on the same ST-BUS. PCM encoded signals are routed through the DSP to the Codec.

2.1 DSTi And DSTo Channels Assignment

The D-Phone can use the last four of the first five time slots following the frame pulse ($\overline{F0i}$). The first channel (channel-0) following the frame pulse, $\overline{F0i}$, is not used. The remaining four channels may be separately enabled or disabled. The second channel is always assigned to the Serial-to-parallel converter, where it is double buffered and made accessible to the μP parallel bus. The third, fourth, or fifth channel can be assigned to the DSP. The ST-BUS output of the D-Phone, DSTo, goes to a high-impedance state during the time-slots not used or disabled.

Four serial channels utilized on ST-BUS are defined as the C-channel, B1-channel, B2-channel, and B3-channel. See Figure 15 for DSTi and DSTo channels assignment.

The C-channel is routed to the Serial-to-parallel Converter for interface to the μP bus. This channel is always in the second time-slot after the frame pulse, and contents of this channel pass transparently through the D-Phone. The D-Phone performs a serial to parallel conversion and double buffers the parallel data onto the μP data bus so that the external μP can read the C-channel. Information from the μP is double buffered into a parallel to serial register and sent out to the C-channel.

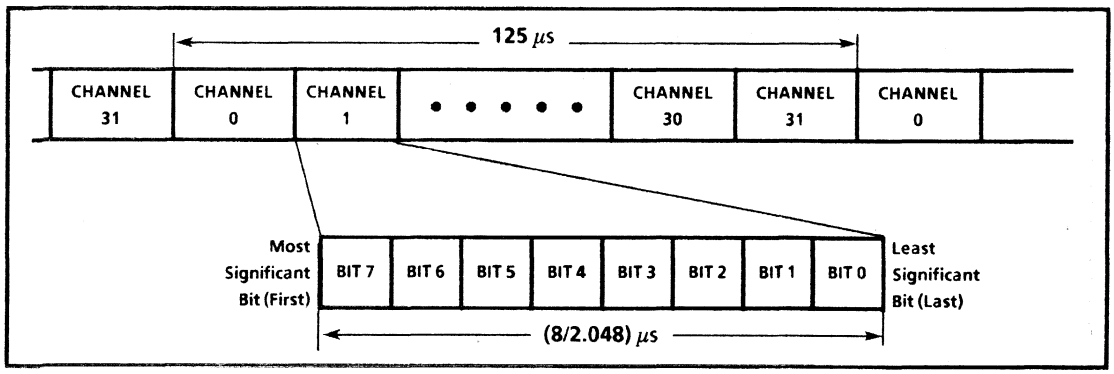


Figure 14 - Format of ST-BUS Stream

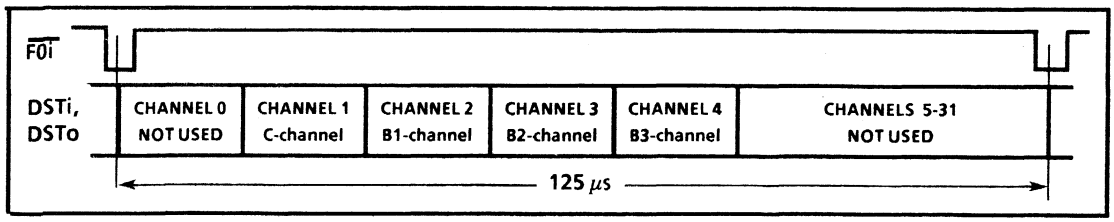


Figure 15 - DSTi and DSTo Channels Assignment

The B1-channel is usually PCM encoded voice, however, PCM encoded voice may also occur in the B2-channel or B3-channel. Any one of these three channels may be routed through the digital signal processor (DSP) to the Codec. Having the Codec enabled in more than one channel is not allowed. In this case only the first channel in which it was selected is enabled.

Time-slot assignment for the ST-BUS is achieved by the Timing Control Register, which is programmed by the external μP. The timing logic section decodes channel allocation information written into the Timing Control Register. Table1 illustrates the details of the Timing Control Register. Bit 7 (Channel 1) is used when more than one D-Phone or another ST-BUS device is connected to the same ST-BUS.

During and after power-up reset ($\overline{PWRST}$) the ST-BUS is in a high-impedance state for all channels until the Timing Control Register is programmed.

b 7	b 6	b 5	b 4	b 3	b 2	b 1	b 0
Channel 1	---	Channel 4		Channel 3		Channel 2	

bit 1	bit 0	Channel 2 selected for
0	0	High Impedence
0	1	DSP Voice Codec
1	0	High Impedence
1	1	High Impedence
bit 3	**bit 2**	**Channel 3 selected for**
0	0	High Impedence
0	1	DSP Voice Codec
1	0	High Impedence
1	1	High Impedence
bit 5	**bit 4**	**Channel 4 selected for**
0	0	High Impedence
0	1	DSP Voice Codec
1	0	High Impedence
1	1	High Impedence
bit 6	**Not Used**	
bit 7	**Channel 1 (C-channel)**	
1	Enables Channel 1	
0	Disables Channel 1	

Table 1 - Timing Control Register ‡

‡ Address = 'X5' Hex Read/Write

2.0 Digital Signal Processor (DSP)

The DSP performs the following tasks under micro-programmed control:

i) A programmable dual sinewave generator. This can provide the DTMF signals;

ii) A programmable frequency shifted square wave generator. This can provide the Tone Ringer function;

iii) A digital speaker-phone algorithm. This is for the hands-free telephone operation.

The DSP uses serial PCM from the DSTi and Codec as inputs and replaces, modifies, or leaves unaltered the PCM data to perform the above functions. PCM data to and from the Codec is delayed by one frame (125 μs).

The operation of the DSP is controlled by three registers which can be written to by the μP. The DSP function is set by the DSP Control Register. Table 2 illustrates details of the DSP Control Register. The other two registers, Tone Register 1 and Tone Register 2, are used for frequency coefficients for the tone generator programs.

2.1 Dual Tone Generator

When the DSP section is operating in the Dual Tone Generator mode a dual sinewave will be generated (digitally) and routed to the Codec and DSTo PCM channels. Either of these channels may be turned off by the DSP Control Register bit 6 (CPCMEN) and bit 5 (DPCMEN).

The Dual Tone Generator is programmed as follows:

i) Disable DSP via DSP Control Register (DSPEN, bit 0 = 0);

ii) Write frequency coefficients to the two DSP tone registers (Tone Register 1 and Tone Register 2);

iii) Select Dual Tone Generator function, enable DSP and destinations for the tones via the DSP Control Register.

The coefficients for Tone Register 1 and Tone Register 2 are calculated as follows:

Coefficient (Hex) = HEX ($10^{-3} \times 128 \times F$)
where: F is the desired frequency in Hz.
HEX( ) represents conversion to Hex.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
---	CPCMEN	DPCMEN	FS1	FS0	CADENCE	WR/ISE	DSPEN

Bit	Name	Description
7		Unused.
6	CPCMEN †	This bit when set to '1' enables the PCM channel (DSTi channel 2,3 or 4) to the Codec. When set to '0' zero is sent to the Codec.
5	DPCMEN †	This bit when set to '1' enables the PCM channel (DSTo channel 2,3 or 4 out of the DSP to DSTo. When set to '0', zero is sent to DSTo.
4	FS1	Function Select bits. FS1 FS0 0 0 No function 0 1 Dual Tone Generator 1 0 Tone Ringer 1 1 Speaker-phone algorithm
3	FS0	
2	CADENCE	This bit when set to '1' turns the Tone Ringer on. A '1' to '0' transition causes the Tone Ringer output to decay to zero with a time constant of approximately 128 ms.
1	WR/ISE	This bit controls the rate of warble when running the Tone Ringer program. When set to '1' the rate is 16 Hz and when set to '0' the rate is 10 Hz. Alternatively, this bit enables or disables the Idle state during speaker-phone operation. i.e. when ISE = 0 the speaker-phone program will switch from Full-Transmit gain to Full-Receive gain without returning to an Idle state gain level during non- speech periods.
0	DSPEN	This bit when set to '1' enables the DSP and the program execution will start on the next frame pulse.

Table 2 - DSP Control Register ‡

‡ Address = 'X9' Hex Read/Write

† The PCM words are always delayed by one frame (125 μs) in the DSP.

The highest and lowest frequencies generated are 1992 Hz and 7.8 Hz, respectively. The frequency resolution is 3.9 Hz. When Tone Register 2 is used the amplitude of the tone generated is approximately 2.5 dB above that for the tone generated by Tone Register 1. This is useful in providing the necessary negative twist for the dual tones generated. The side-tone feature is included. The level of the side-tone is controlled by the Receive Digital Gain bits 3-0 in the Receive Gain Contol Register. This provides the Dual Tone signals to the speakers.

2.1.1 DTMF Signals Generation

The Dual Tone Generator can be used to provide the DTMF signals. In this case the coefficient for Tone Register 2 is used to generate the high group DTMF signals. The Tone Register 1 coefficient is used to generate the low group DTMF signals. This provides the necessary negative twist for the high group DTMF signals. Table 3 shows the values of the coefficients in Tone Register 1 and Tone Register 2 required to generate DTMF signals.

2.2 Tone Ringer

The Tone Ringer output is a frequency shifted square wave. Values in the two frequency coefficient registers determine the frequencies of the square waves. The shift rate is set with the use of an internal timer. The resulting "frequency shifting" square wave is routed to the receive PCM speech path. The transmit PCM speech path is left unaffected when the Tone Ringer is operating.

Low-group Frequency	Tone Register 1 † Coefficient	Frequency Generated
697 Hz	59 Hex	695.3 Hz
770 Hz	63 Hex	773.4 Hz
852 Hz	6D Hex	851.6 Hz
941 Hz	79 Hex	945.3 Hz
High-group Frequency	**Tone Register 2 ‡ Coefficient**	**Frequency Generated**
1209 Hz	9B Hex	1210.9 Hz
1336 Hz	AB Hex	1335.9 Hz
1477 Hz	BD Hex	1476.6 Hz
1633 Hz	D1 Hex	1632.8 Hz

Table 3 - DTMF Signals Generation

† Tone Register 1 Address = 'X7' Hex Write Only
‡ Tone Register 2 Address = 'X8' Hex Write Only

The two frequencies are programmed in a similar way to the Dual Tone Generator, and the frequency shift is determined by setting the DSP Control Register bit 1 (WR/ISE).

The CADENCE of the Tone Ringer output is controlled by the external μP via the DSP Control Register, by setting bit 2. When bit 2 is set to '0' the square wave amplitude decays to zero with a time constant of approximately 128 ms. This cadence-off time is independent of the Tone Ringer frequencies and is not programmable. However, a sharp cut-off of the tone can be affected by setting CPCMEN bit 6 in the DSP Control Register to '0'.

The Tone Ringer is programmed as follows:

i) Disable DSP via the DSP Control Register;

ii) Write the Tone Ringer frequency coefficients into Tone Register 1 and Tone Register 2;

iii) Select the speaker volume by writing to the Receive Gain Control Register;

iv) Enable DSP and Tone Ringer via the DSP Control Register;

v) Toggle CADENCE, bit 2 in the DSP Control Register, according to the desired Tone Ringer cadence.

The 8-bit Hex coefficients are calculated as follows:

$$\text{Coefficient (Hex)} = \text{HEX}\{[1/(F \times 2.5 \times 10^{-4})] - 1\}$$

where: F is the frequency of the square wave (ringing tone) in Hz.
HEX( ) represents conversion to Hex.

The highest and the lowest frequencies generated are 4000 Hz and 15.7 Hz, respectively. The amplitude of the square wave is programmed by the Receive Digital Gain bits 3-0 in the Receive Gain Control Register.

2.3 Speaker-phone

The speaker-phone provides hands-free telephone operation. A high quality half duplex operation is achieved by soft switching the gain in the microphone and the speaker paths. This gain switching is implemented with digital gain changing in 2.5 dB steps. See Table 4. The transmit (Tx) and receive (Rx) gain sections operate in a complementary manner i.e. when the transmit signal is at its maximum the receive path has maximum attenuation and vice versa. The DSP determines which side should be given preference based upon the relative levels of the audio signals. A voice detector algorithm decides whether the audio signal is voice or background noise. If only background noise is present then the transmit and receive gains will be at mid-levels corresponding to Idle state.

The transmit and receive PCM are routed through a multiplexed digital gain section which is controlled by the DSP. This digital gain section provides 16 possible gain states. However, the speaker-phone will rest in only three of the 16 states. These three states are: Full-Transmit (Tx), Full-Receive (Rx), and Idle. During the Full-Tx state, transmit PCM is unattenuated and receive PCM has maximum attenuation. During the Full-Rx state, receive PCM is unattenuated and transmit PCM has maximum attenuation.

The speaker-phone function is programmed via the DSP Control Register as follows:

i) Disable side-tone (SIDE) and enable the speaker-phone speaker (SPSKR) and microphone (SPMIC) using the Transducer And Transmit Gain Control Register (Table 7);

ii) Program speaker gain using the Receive Gain Control Register (Table 6);

iii) Enable the DSP (DSPEN), Speaker-phone algorithm (FS1 and FS0), and PCM buffer (DSTi channel 2,3 or 4) which is CPCMEN bit via DSP Control Register.

Gain States	Transmit Gain (dB)	Receive Gain (dB)†
0 (Full-Receive)	- 37.5	+ 12
1	- 35.0	+ 9.5
2	- 32.5	+ 7.0
3	- 30.0	+ 4.5
4	- 27.5	+ 2.0
5	- 25.0	- 0.5
6	- 22.5	- 3.0
7	- 20.0	- 5.5
8 (Idle)	- 17.5	- 8.0
9	- 15.0	- 10.5
10	- 12.5	- 13.0
11	- 10.0	- 15.5
12	- 7.5	- 18.0
13	- 5.0	- 20.5
14	- 2.5	- 23.0
15 (Full-Transmit)	0.0	- 25.5

Table 4 - Speaker-phone Gain States

The speaker volume can be adjusted over the full range by setting Receive Digital Gain bits 0, 1, 2 and 3 of the Receive Gain Control Register. This then limits the Full-Receive state gain to the selected value (refer to Table 4) and will effectively move the Full-Receive state to an intermediate gain state with less transmit attenuation. For example, if the Receive Digital Gain is set at - 10.5 dB then the Full-Receive state gain will also be set to - 10.5 dB and the resulting Full-Transmit gain will be - 15.0 dB. In this case the Idle state is moved to - 10.5 dB. This feature allows the speaker-phone to operate closer to "full duplex" at lower speaker volume settings. Note that when the receive gain setting is lower than the Idle state, the Idle state is moved to the receive gain setting. When the speaker-phone microphone is operating at low volume settings additional filtering to attenuate low frequency signals present in the speaker-phone environment may be necessary. The Transmit Filter Highpass Filter is enabled in this case by setting the Receive Gain Control Register bit 7 (HPF) to '1'. This moves the low end notch from 60 Hz to 120 Hz and adds a low end roll-off with a corner frequency of 400 Hz.

2.3.1 Speaker-phone Audio Loop Stability

Proper operation of the speaker-phone requires that the audio loop stability be maintained. For this it is necessary to consider the gains involved in the speaker-phone audio loop design.

Figure 16 illustrates the gains involved in the speaker-phone audio loop. Table 5 shows the gains relating to the blocks in the speaker-phone audio loop. There are three main requirements for reliable speaker-phone operation:

i) The loop gain must be less than 0 dB at any voiceband frequency for the stability of the audio loop;

ii) Trans-hybrid loss must be less than 0 dB for the average voiceband signal power to ensure proper half duplex switching;

iii) Acoustic return signal (sum of all the blocks except Trans-hybrid Loss) must be less than 0 dB for the average voiceband signal power to ensure proper half duplex switching.

Using the configuration in Figure 16 and the gain values as shown in Table 5, the acoustic separation required in the design of the speaker-phone for a specific loss plan is determined.

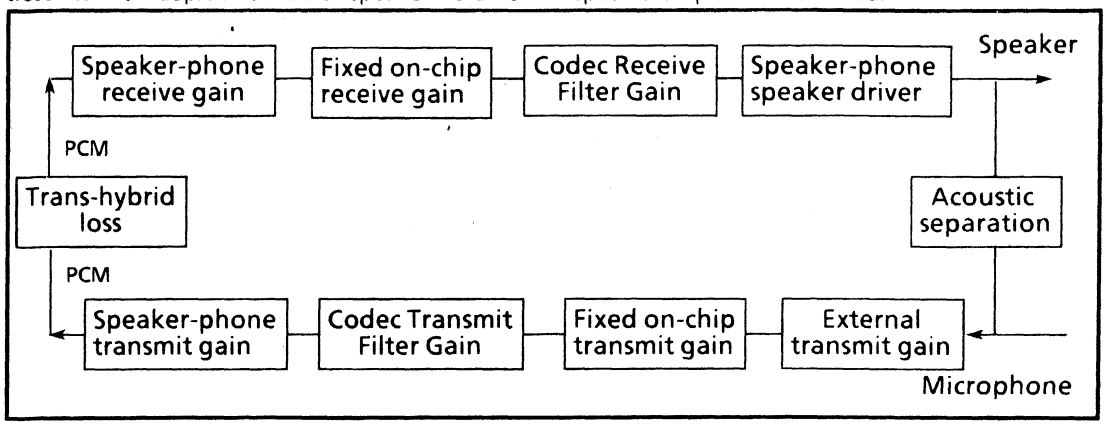


Figure 16 - Speaker-phone Audio loop

Gain Block (Reference Figure 16)	μ-Law mininum	μ- Law maximum	A-Law mininum	A-Law maximum	Reference
Trans-hybrid loss	0	0	0	0	Section 2.3.1
Speaker-phone receive/transmit gain	- 25.5	- 25.5	- 25.5	- 25.5	Table 4
Codec Receive Filter Gain	- 3.0	- 3.0	- 3.0	- 3.0	Table 6
Speaker-phone speaker driver	9.3	10.0	12.9	13.7	
External transmit gain required †	35.6	35.6	35.6	35.6	
Fixed on-chip transmit gain	13.1	13.9	16.4	17.2	Transmit path
Codec Transmit Filter Gain	2.0	2.0	2.0	2.0	Table 7
Acoustic separation required †	< - 31.5	< - 33	< - 38.4	< - 40	Section 2.3.1
Total to maintain audio loop stability	<0	<0	<0	<0	

Table 5 - Speaker-phone Audio Loop Gains (dB)

† These are suggested values only and should be tailored to accomodate the required Loss Plan

3.0 Filter Codec

The conversion interface between the voiceband analog signals of a telephone subscriber loop and the digital signals required in a digital PCM switching system is provided by the Filter Codec section. It consists of an analog to digital and a digital to analog conversion and the necessary associated filtering. The two variants of the codec function are the MT8994 and the MT8995. The difference is in the encoding law used. The MT8994 and MT8995 conform to the μ-Law and A-Law companding codes, respectively.

Analog signals in the transmit path enter at the microphone input pins (MIC and M+, M-) are filtered, sampled at 8 kHz and the samples quantized and assigned 8-bit digital values defined by the PCM encoding laws. After encoding, the digital data is made available to the DSP in the Codec ouput register. The receive digital data for the digital to analog conversion is made available in the DSP output register. After digital decoding and filtering, the analog signals leave the D-Phone at SPKR+, SPKR- and HSPKR+, HSPKR-

Separate switched capacitor filter sections are used for bandlimiting prior to digital encoding in the transmit path and after digital decoding in the receive path. The Transmit Filter is clocked at 512 kHz which is derived from the 4096 kHz master clock input.

The Receive and Transmit Filters meets the AT&T D3/D4 specifications and the CCITT G.712 recommendations. Digitally controlled gain adjust is available for the Receive and Transmit Filters.

3.1 Receive Filter

The filter is peaked to compensate for the (sin x)/x attenuation caused by the Codec's 8 kHz sampling rate. In addition, a first order lowpass filter with the corner frequency at 1 kHz is included in the Receive Filter. When this filter is enabled it reduces the high end of the filter characteristic by a maximum of 5 dB and removes the peaking. This improves the sound of the dial tone signal. The lowpass filter is enabled by setting the Transducer and Transmit Gain Control Register bit 5 (DIAL) to '1'. The gain in the Receive Filter can be varied in the range 0 to - 7 dB, in 1 dB steps. See Receive Gain Control Register Table 6.

3.1.1 Receive Gain Control

The gain in the receive direction can be controlled to an overall accuracy of 1 dB. Control is implemented in two sections of the device; the Receive Filter section, and the DSP digital gain control section.

The Receive Filter Gain can be adjusted from 0 to - 7 dB, in 1 dB steps. This Receive Filter Gain is controlled by Receive Gain Control Register bits 6, 5 and 4 as shown in Table 6.

The DSP digital gain control section provides gain in the range + 12 dB to - 25.5 dB, in 2.5 dB steps. This Receive Digital Gain is controlled by the Receive Gain Control Register bits 0, 1, 2 and 3 as shown in Table 6. Note that this gain control section is only active while the DSP is enabled (i.e. DSPEN = 1). When the DSP is disabled, (i.e. DSPEN = 0) the Receive Digital Gain is set at 0 dB

b7	b6	b5	b4	b3	b2	b1	b0
HPF	Receive Filter Gain			Receive Digital Gain			

bit 3	bit 2	bit 1	bit 0	Receive Digital Gain (dB)
0	1	1	1	+ 12.0
0	1	1	0	+ 9.5
0	1	0	1	+ 7.0
0	1	0	0	+ 4.5
0	0	1	1	+ 2.0
0	0	1	0	− 0.5
0	0	0	1	− 3.0
0	0	0	0	− 5.5
1	0	0	0	− 8.0
1	0	0	1	− 10.5
1	0	1	0	− 13.0
1	0	1	1	− 15.5
1	1	0	0	− 18
1	1	0	1	− 20.5
1	1	1	0	− 23.0
1	1	1	1	− 25.5

bit 6	bit 5	bit 4	Receive Filter Gain (dB)
0	0	0	0
0	0	1	− 1
0	1	0	− 2
0	1	1	− 3
1	0	0	− 4
1	0	1	− 5
1	1	0	− 6
1	1	1	− 7

bit 7	HPF
1	Transmit Filter Highpass Filter enabled
0	Transmit Filter Highpass Filter disabled

Table 6 - Receive Gain Control Register ‡

‡ Address = 'XB' Hex Read/Write

The Receive Gain Control Register is reset to all zeros on power-up. If the DSP remains disabled (i.e. DSPEN = 0) the resulting Receive Gain is 0 dB. If however the DSP is enabled (i.e. DSPEN = 1) the resulting Receive Gain is − 5.5 dB. This corresponds to all zeros in the Receive Gain Control Register .

3.2 Transmit Filter/Gain

Analog signals at the MIC and M+, M− inputs must be bandlimited to 512 kHz. This is to perform the necessary anti-aliasing for the following lowpass filter which is clocked at 512 kHz. A first order lowpass filter with a corner frequency of 25 kHz may be added externally. This gives an attenuation of 26 dB at 512 kHz and results in a 0.1 dB droop across the passband in the transmit path.

The gain of the Transmit Filter can be adjusted from 0 dB to 6 dB, in 2 dB steps. This Transmit Filter Gain is controlled by the Transducer And Transmit Gain Control Register bits 6 and 7 as shown in Table 7.

4.0 Transducer Interfaces

In a telephone set, interface to the handset and the speaker-phone is required. The handset and the speaker-phone transducer interfaces consists of four distinct sections. They are the handset microphone and speaker and the speaker-phone microphone and speaker. All these transducer interfaces can be powered down independently under software control via the Transducer And Transmit Gain Control Register bits 3-0 as shown in Table 7. In this case the outputs go high impedance. The output signals from the microphone(s) is routed to the Transmit Filter and input to the speaker(s) comes from the Receive Filter. In addition, a fixed side-tone is avaliable which, if enabled, routes the signals input to microphone(s) to the speakers. The side-tone is turned on /off by bit 4 (SIDE) in the Transducer And Transmit Gain Control Register.

4.1 Transducer Output Interfaces

There are two transducer output interfaces provided: telephone handset speaker and speaker-phone speaker.

4.1 .1 Telephone Handset Speaker

This is a balanced differential drive section that is capable of driving the network shown in Figure 17. The output pins are (HSPKR+ and HSPKR−). A 0.1 μF capacitor must be used to compensate the speaker driver amplifier. The pair of 75 ohm resistors and 1000 pF capacitors are required to filter external high frequency components. For more details refer to A/C Electrical Characteristic - Handset Speaker.

4.2.2 Speaker-phone Speaker Output

This is another balanced differential drive section. The output pins are (SPKR+ and SPKR−). The speaker can be connected directly to the ouput pins. For more details refer to A/C Electrical Characteristic - Speaker-phone Speaker.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TRANSMIT FILTER GAIN		DIAL	SIDE	HSMIC	SPMIC	SPSKR	HSSKR

Bit	Name	Description
7 6	TRANSMIT FILTER GAIN	Transmit Filter Gain setting. Bit 7 Bit 6 Gain (dB) 0 0 0 0 1 2 1 0 4 1 1 6
5	DIAL	This bit when set to '1' enables a first order lowpass filter in the Receive Filter with the corner frquency (3 dB point) at 1 kHz.
4	SIDE	This bit when set to '1' turns on the side-tone.
3	HSMIC	This bit when set to '1' turns on and powers up the handset microphone
2	SPMIC	This bit when set to '1' turns on and powers up the speaker-phone microphone
1	SPSKR	This bit when set to '1' turns on and powers up the speaker-phone speaker
0	HSSKR	This bit when set to '1' turns on and powers up the handset speaker

Table 7 - Transducer and Transmit Gain Control Register ‡

‡ Address = 'XA' Hex Read/Write

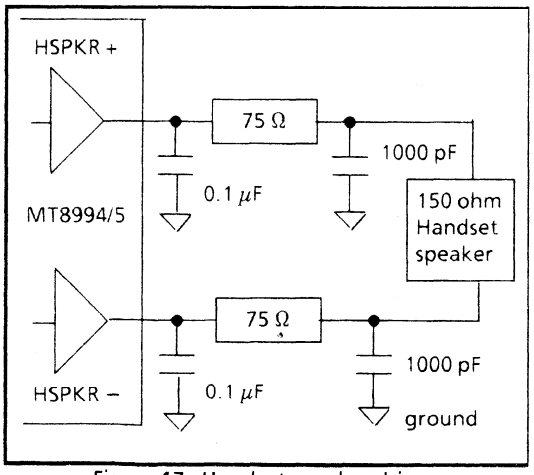


Figure 17 - Handset speaker driver

4.2 Transducer Inputs

There are two transducer input interfaces provided: a telephone handset microphone and a speaker-phone microphone. Note that both inputs need to be bandlimited to 512 kHz. Refer to section 3.2 for details.

4.2.1 Telephone Handset Microphone

The telephone handset microphone interface is a differential input circuit. The input pins are M+ and M–. The interface gain is fixed at +13.5 dB and +16.8 dB for the μ-Law and the A-Law devices, respectively. The maximum recommended common mode signal on this input is ±1 V. Figure 18 illustrates the recommended telephone handset microphone interface circuit.

4.2.2 Speaker-phone Microphone

The speaker-phone microphone interface is a single ended input (MIC). The interface gain is the same as the telephone handset microphone. Figure 19 illustrates the recommended speaker-phone microphone interface circuit.

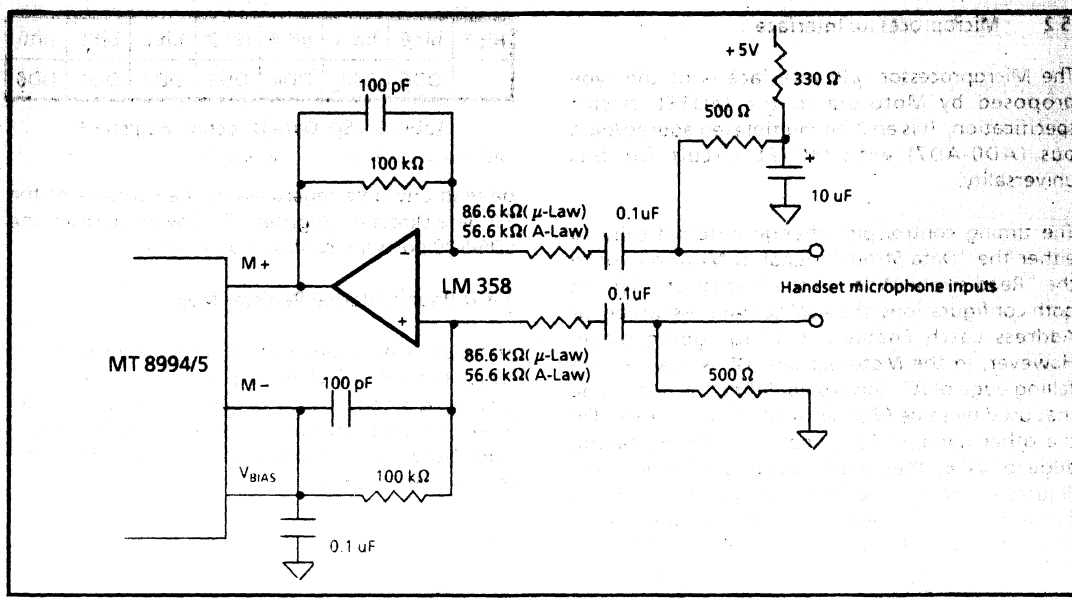


Figure 18 - Recommended Handset Microphone Interface circuit

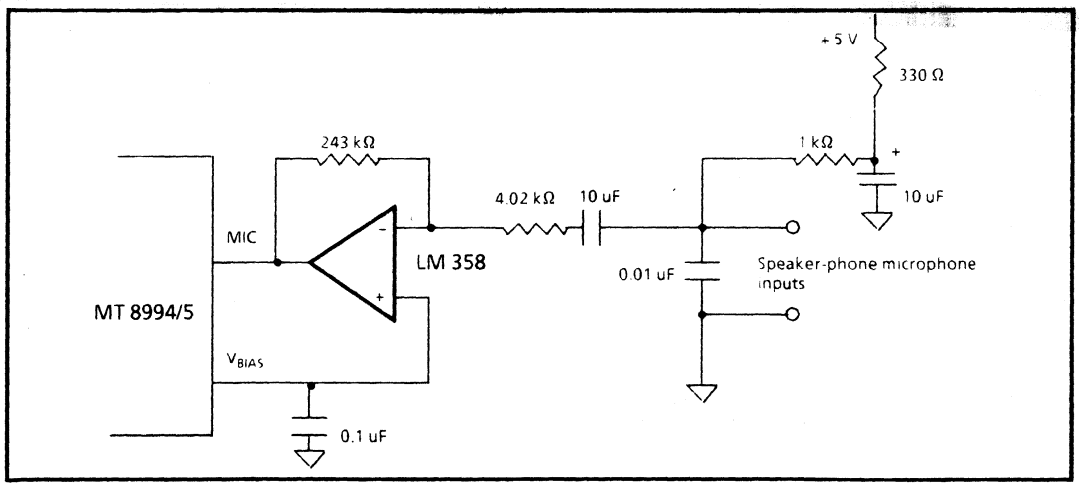


Figure 19 - Recommended Speaker-phone Microphone Interface Circuit

5.0 Microprocessor Port

The microprocessor port consists of a microprocessor interface for the external μP to provide control of the D-Phone chip, have access to the sense/drive ports and provides interface to the ST-BUS via the Serial-to-parallel Converter.

5.1 Serial-to-parallel Converter

This is a double-buffered serial-to-parallel conversion for asynchronous transfer of octets (8-bit word) from DSTi, to the internal μP bus and a parallel-to-serial double-buffer for transfer from the internal μP bus to DSTo. The Serial-to-parallel Converter buffer is enabled by setting the Timing Control Register bit 7 (Channel 1) to'1'

The Serial-to-parallel Converter is accessed by the μP at address '00' Hex. A μP read operation implements the receive function. Serial input at DSTi is avaliable as parallel output on the μP data bus. A μP write operation implements the transmit function. Parallel input on the μP data bus is available as serial output at DSTo. Note that data is transmitted least significant bit first in channel 1 (C-channel).

5.2 Microprocessor Interface

The Microprocessor (μP) interface is of the type proposed by Motorola in the MOTEL circuit specification. It is an 8-bit multiplexed address/data bus (AD0-AD7) with MOTEL circuit for bus universality.

The timing control pins change automatically to either the "Data Strobe" signal of Motorola, or to the "Read strobe/Write strobe" signal of Intel. In both configurations, the AS/ALE (Address Strobe, or Address Latch Enable), is a high-going pulse. However, in the Motorola bus, DS is low on the falling edge of AS; this would define the R/$\overline{W}$ to be that used by some 6800 series μP. See Figure 3. On the other hand, if DS is kept high on the falling edge of ALE, then Intel mode is selected. See Figures 4 and 5. The Intel bus has DS (alternate function $\overline{RD}$) high during the falling edge of ALE; this redefines the R/$\overline{W}$ line to mean "write pulse" ($\overline{WR}$). Reset places the device in the Motorola mode of operation. In Motorola mode, $\overline{CS}$ can be used to qualify data instead of DS if DS and R/$\overline{W}$ are valid.

5.3 Sense/Drive (SD) Ports

Seven TTL compatible sense/ drive ports, SD6 to SD0, are available in the D-Phone. These ports are accessed by the external μP. They are intended for keyboard scanning, display functions etc. The input/output direction is determined by the SD Data Direction Register. The port logic status is set or read via the SD Data Register.

5.3.1 SD Data Register

Table 8 describes the SD Data Register.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit
---	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Table 8 - SD Data Register ‡

‡ Address = 'XC' Hex Read/Write

The input logic status of SD6 to SD0 ports is given by a μP read. A μP write sets the required status at the SD6 to SD0 outputs if the port in the SD Data Direction Register is designated as an output.

5.3.2 SD Data Direction Register

Table 9 describes the SD Data Direction Register. The direction of the SD6 to SD0 ports is controlled by bits 6-0 in the the SD Data Direction Register. A '0' corresponds to an input mode and a '1' to an output mode. The logic status at the SD ports can be read any time regardless of the contents of the SD Data Direction Register. On Power-up reset the SD6-SD0 ports are configured as inputs.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit0
---	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Table 9 - SD Data Direction Register ‡

‡ Address = 'XD' Hex Read/Write

5.4 D-Phone Internal Register Map

There are eleven 8-bit control registers through which the D-Phone chip is configured in various operating modes. Table 10 gives a summary of the internal register map implemented in the D-Phone chip. Note that any register with unused bit(s) will read a '1' for the bit(s).

6.0 Watchdog Timer

This timer, which is not programmable, works in conjunction with the watchdog output pin ($\overline{WD}$). Writing the binary code XXX0 1010 to the address 'X6' Hex results in a reset. The $\overline{WD}$ output will go low when the D-Phone is being reset and will go high immediately after the reset is released. If, however, the timer is not written to within 2^9 cycles of the $\overline{F0i}$, then the watchdog output of the device will go low for the timeout period and the output will toggle every 2^9 $\overline{F0i}$ until the register is written to. Using 125 μs $\overline{F0i}$ this gives 7.8 Hz output. The timer is clocked on falling edge of $\overline{F0i}$.

This timer will operate even if the device is not selected and requires only $\overline{F0i}$ input.

7.0 Testing

Due to the complexity of the digital and analog circuitry, a test register has been included in the D-Phone chip. When the test modes are being exercised the contents of all the other registers are unaffected.

See Table 11 for details of setting up the Test Register. For any of the test modes to be implemented it is necessary to have TEST ENABLE bit 6 = 0 and bit 5 = 1.

Address ‡	Read	Write	Reference
X0	Serial-in to parallel-out	Parallel-in to serial-out	Section 5.1
X1	Not used	Not used	
X2	Not used	Not used	
X3	Not used	Not used	
X4	Not used	Not used	
X5	Timing control	Timing control	Table 1
X6	Not used	Watchdog Timer	Section 6.0
X7	Not used	Tone Register 1	Section 2.1
X8	Not used	Tone Register 2	Section 2.1
X9	DSP Control	DSP Control	Table 2
XA	Transducer and Transmit Gain Control	Transducer and Transmit Gain Control	Table 7
XB	Receive Gain Control	Receive Gain Control	Table 6
XC	SD Data	SD Data	Table 8
XD	Not used	SD Data Direction	Table 9
XE	Not used	Test Register	Table 11
XF	Not used	Not used	

Table 10 - D-Phone Internal Register Map

‡ In Hex. Only four least significant bits of the eight address bits are decoded by the D-Phone chip.

8.0 Applications

The MT8994/5 D-Phone chip forms part of Mitel's ISDN family of components. It is used in digital telephone sets. When combined with the MT8930 (Subscriber Network Interface Circuit-SNIC) it provides ISDN terminal equipment (TE) function. This implements interface at CCITT ISDN reference point S. The D-Phone may also be combined with the MT8952B (High level Data Link Controller-HDLC) and the MT8972 (Digital Network Interface Circuit-DNIC) to provide voice/data digital telephone set interfacing to bi-directional 2-wire digital network. See Figure 20. Low power requirements enables the circuit to be line-powered.

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	---	TEST ENABLE		---	PCMLB	DSTLB	DAC	FILTER

Bit	Name	Description
7	---	Not used
6	TEST ENABLE	This bit must be set to '0' to enable any of the test modes
5		This bit must be set to '1' to enable any of the test modes
4	---	Not used
3	PCMLB	This bit when set to '1' enables the internal PCM loopback. This loops the internal serial bus that is between the DSP and the Codec sections, providing observability of the DSP section at the DSTo pin.
2	DSTLB	This bit when set to '1' enables DST loopback. DSTo is connected to DSTi.
1	DAC ①	This bit when set to '1' enables testingof the A/D and the D/A by separating the A/D and D/A paths. The MIC input becomes the A/D input, and M – is connected to the D/A output.
0	FILTER ① ②	This bit when set to '1' enables the testing of the Transmit and the Receive Filters separately. The MIC input is connected to the Receive Filter input, and the Receive Filter output is sensed at M +. The Transmit Filter input is connected to the MIC input and the Transmit Filter output is sensed at M –

Table 11 - Test Register ‡

‡ Address = 'XE' Hex Read/Write
① For testing bit 1 = 1 and bit 0 = 1 is not a valid state
② When M + and M – are used as outputs a buffer amplifier must be provided at the pin

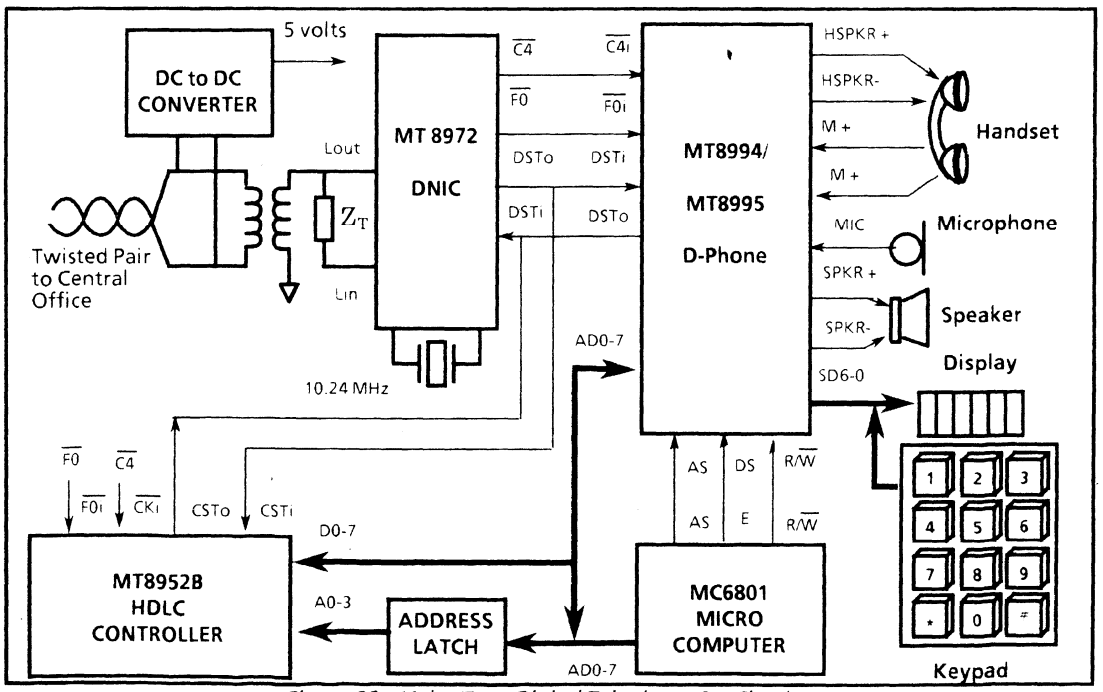


Figure 20 - Voice/Data Digital Telephone Set Circuit

Application Notes

MITEL®

ST-BUS™ FAMILY MT8980 Large Switching Arrays Using MT8980s

Application Sheet MSAS-32

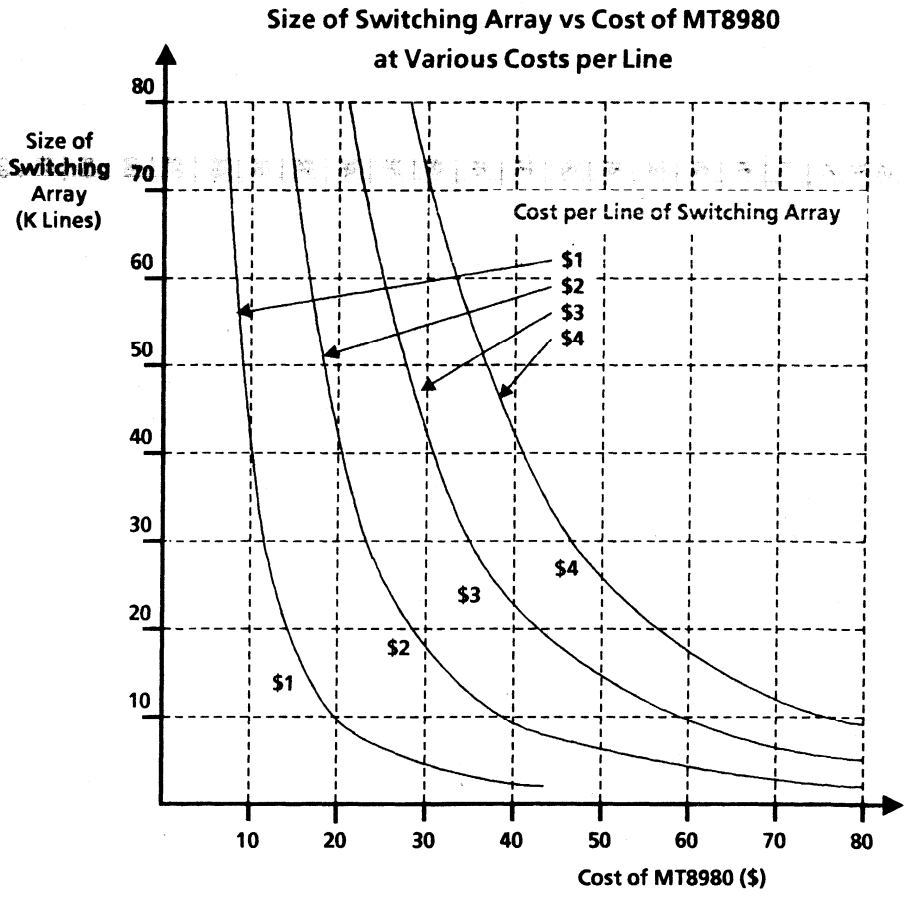
9161-001-016-NA ISSUE 2 JANUARY 1985

Large switching arrays, for tens of thousands of lines, can be built with MT8980s. The graph below shows how larger switching arrays become more economical as the cost of the MT8980 decreases.

If the design of a Central Office is economical when the cost per line for the basic switching function is $3, then a 10K line Central Office can be built if MT8980s cost $60 and an 42K line Central Office can be built if MT8980s cost $30.

The table on the next page gives the breakdown of the switching array into Input, Intermediary and Output Switches and shows the size of each and the number of MT8980s required.

Even more efficient arrays than those shown here may be built if system constraints permit it.



NB: Graph shows results for 3-Level Non-Blocking Arrays.

Large Switching Arrays using MT8980s

Structure of 3-Level Non-Blocking Switching Array

Size of Switching Array (K Lines)	Input Switches			Intermediary Switches			Output Switches			Total Number of MT8980s Used
	Number of Switches in Block	Size of Switches (ST-BUS Streams)	Number of MT8980s per Switch	Number of Switches in Block	Size of Switches (ST-BUS Streams)	Number of MT8980s per Switch	Number of Switches in Block	Size of Switches (ST-BUS Streams)	Number of MT8980s per Switch	
2	8	8 to 15	2	15	8 to 8	1	8	15 to 8	2	47
4	16	8 to 15	2	15	16 to 16	4	16	15 to 8	2	124
6	24	8 to 15	2	15	24 to 24	9	24	15 to 8	2	231
8	32	8 to 15	2	15	32 to 32	16	32	15 to 8	2	368
10	40	8 to 15	2	15	40 to 40	25	40	15 to 8	2	535
12	24	16 to 31	8	31	24 to 24	9	24	31 to 16	8	663
16	32	16 to 31	8	31	32 to 32	16	32	31 to 16	8	1,008
20	40	16 to 31	8	31	40 to 40	25	40	31 to 16	8	1,415
24	48	16 to 31	8	31	48 to 48	36	48	31 to 16	8	1,884
28	56	16 to 31	8	31	56 to 56	49	56	31 to 16	8	2,415
30	40	24 to 47	18	47	40 to 40	25	40	47 to 24	18	2,615
36	48	24 to 47	18	47	48 to 48	36	48	47 to 24	18	3,420
42	56	24 to 47	18	47	56 to 56	49	56	47 to 24	18	4,319
48	64	24 to 47	18	47	64 to 64	64	64	47 to 24	18	5,312
56	72	24 to 47	18	47	72 to 72	81	72	47 to 24	18	6,399
60	80	24 to 47	18	47	80 to 80	100	80	47 to 24	18	7,580
64	64	32 to 63	32	63	64 to 64	64	64	63 to 32	32	8,128
72	72	32 to 63	32	63	72 to 72	81	72	63 to 32	32	9,711
80	80	32 to 63	32	63	80 to 80	100	80	63 to 32	32	11,420

DNIC Questions and Answers

Application Sheet MSAS-42

9161-003-006-NA ISSUE 2 JUNE 1986

These are some of the questions that have been frequently asked regarding the DNIC and associated technological implications. The list is by no means comprehensive, and will be updated, as characterization progresses.

1. *What is the line code and transmit signal level?*

The line code used is biphase with differential encoding. The amplitude of the signal on the line is 1.2 V_{p-p} +/- 3%. Assuming a line termination of 120 ohms, this corresponds to a transmit power level of + 1.0 dBm.

2. *What does the Power Spectral Density graph of the transmitted line look like?*

The spectral density graph shows a peak response of -24dBV at 0.75fb. This would be at 120 KHz when transmitting at 160 KHz, and 60 KHz when using 80 KHz. There are zeros at 0, and 2fb. The secondary lobes have at least 36dB additional attenuation relative to the spectral peak.

3. *What is the maximum line length the DNIC can operate over?*

The maximum line length of the DNIC is a function of the type of cable that is used. Gauge as well as composition affects the loop length achievable. A more reliable means of specifying range is by using allowable dB of attenuation. In this way one value can be specified, and from this value the achievable range over the various loop configurations can be derived. The DNIC is capable of handling typically 40 dB of total attenuation. This corresponds to 34 dB of cable attenuation, and 6 dB loss in the termination impedance. From transmission theory for line attenuation, this works out to a limit in excess of 4 km on 24 AWG for 160 kHz operation.

4. *What is the limiting factor in the loop range specification?*

The maximum loop length of the DNIC is limited by the signal attenuation and noise on the line. The calculation is done by dividing the total tolerable line attenuation (in dB), by the attenuation factor for each gauge of wire and frequency. Intersymbol interference (ISI) can also be the limiting factor in certain loop configurations. Near end crosstalk (NEXT) is thought of as being the limiting factor for echo-cancelling schemes as a whole. The loop range is further limited by the characteristics of the line. Bridged taps, noise, and severe impedance mismatches can result in a shorter range.

5. *What are the associated SNR ratios and error rate figures for the listed specs?*

The SNR is a measure of the receiver tolerance. This value is also a function of the data transmission rate and loop length. At 160 kbit/s transmission on 24 AWG, the DNIC has a SNR of better than 10 dB for any loop length between 500 metres and 2 km. This is for a BER of 10^{-6}.

6. ***What does "Channel Quality" in the transmit C-channel indicate?***

The channel quality gives an indication of the relative signal to noise ratio. The 2 bits in the transmitted C-channel allow for 4 possible values of channel quality. The further the value is away from 0, the higher is the SNR. (i.e. the better the performance). The actual value cannot be directly translated into an equivalent SNR, but rather it only provides a qualitative measurement of transmission quality.

7. What does the "ATTACK" feature do?

The ATTACK feature allows for faster convergence of the echo canceller RAM when powering up. Instead of incrementing / decrementing the LSB of a particular RAM value, ATTACK disables several least significant bits, making the effective step size of the echo canceller larger.

8. ***What is the convergence time of the echo canceller without "ATTACK"? ..with "ATTACK"?***

Under normal operating conditions, the ATTACK feature is disabled except for power up. At power up ATTACK is turned on for a certain specified period of time, then it is deactivated, letting the RAM converge normally.

Convergence Times

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Attack Off at 80 kbit/s	T_{c80}		8.5	17.50	s	
2	Attack Off at 160 kbit/s	T_{c160}		4.0	8.80	s	
3	Attack On at 80 kbit/s	T_{ac80}		0.8	1.75	s	Atk. for 60ms.
4	Attack On at 160 kbit/s	T_{ac160}		0.4	.85	s	Atk. for 30ms.

9. ***Why is a 10.24 MHz crystal used as opposed to some other frequency?***

The 10.24 MHz is used because it is the lowest common multiple of the data rate clocks (80 and 160 kbit/s) and the ST-BUS clocks (2.048 and 4.096 Mbit/s).

10. ***Can the DNIC operate with a 1.544 Mhz. data stream?***

No. The internal operation of the DNIC is set up to work with a 2.048 MHz data stream such as the ST-BUS data stream. Operation with a 1.544 MHz network would only be possible if an interface was available to reformat the 1.544 MHz data into 2.048 MHz format, and a 10.24 MHz clock source was provided.

11. ***What types of packages does the DNIC come in?***

Currently the DNIC is available only in 22 pin CERDIP package.

12. ***Is the DNIC an analog or digital device?***

The DNIC is both an analog and digital device. It provides the interface between a digital system (ST-BUS) and an analog system (2 wire telephone loop plant), thus it has components internally which provide the necessary interface capabilities.

13. ***What does the PLL operate on?***

A phase-locked loop is essentially a frequency comparator with feedback. In the DNIC, the PLL uses the incoming data stream as one input frequency, and a generated 160 kHz or 80 kHz as the other. The output clock from the PLL is a 10.24 MHz. phase-locked clock. This clock is divided down to get RCK which is then compared with the incoming data stream. The 10.24 MHz output clock is then adjusted accordingly.

14. ***How can you determine whether the DNIC or system is not operating properly?***

The DNIC has special loopback testing capabilities which allows it to diagnose itself either via end-to-end testing, or via internal testing. This mode is accessed by using the received C-channel and the diagnostics register.

15. ***What are the leading causes of echos in a digital network?***

The leading causes of echos are bridged taps, cable gauge changes, and impedance mismatches.

16. What effect do bridged taps have on system performance?

The effect of the bridged taps depends largely on where in the network these bridge taps are located. If they are at the transmitter / receiver, then the effect is quite severe. The length of the bridged taps is also of concern. The most severe bridged tap is of the quarter wave length (around 250 meters). Other factors are whether the bridged tap is terminated or not, and what impedance is at the termination. Signal degradation up to 6dB per tap may be encountered.

17. ***Are the ST-BUS transmit and receive frames aligned wrt each other, or are they skewed?***

The ST-BUS transmit and receive frames are aligned wrt each other. This is achieved by double buffering the transmit data, and triple buffering the receive data. This allows transmission and reception to be activated by the same pulse.

18. ***What happens with the unused ST-BUS channels?***

Once the DNIC has finished its active channels (4 at 160 kbit/s), then the FOo pin is set. The rest of the ST-BUS channels are set to high impedance. This allows for other DNIC's to access the unused channels on the ST-BUS. By using the FOo pin connected to the FOi of the next DNIC, you could multiplex several DNIC streams onto a single ST-BUS link.

19. How is the DNIC powered?

The DNIC can be powered from the telephone line. Since it is a low power CMOS device with a typical power draw of only 50 mW, it can be continuously powered from the central office battery.

20. Is there a power down mode on the DNIC?

No. Once the DNIC loses power, the contents of the RAM are lost. On power up, the RAM must first settle before meaningful data can be transmitted.

21. With reference to the ISDN model, where does the DNIC fit it?

The DNIC corresponds to the U-Interface reference point in the ISDN model. CCITT currently does not make any recommendations for the U-Interface, leaving it to be decided on a national basis. In North America discussions are taking place under the auspicies of ANSI Technical Committee on Telecommunications (T1D1) to establish standard specifications for the U-Interface.

22. What are the advantages of Echo Cancellation over TCM (ping-pong)?

Echo cancellation is a full duplex solution in that it transmits data continuously in both directions at the same time. TCM only transmits in one direction at a time. Therefore in order to get the same effective data rate, the TCM system must transmit at over twice the required data rate. This has the effect of increasing the frequency content of the signal, making it prone to increased crosstalk, attenuation and other interference. The increased spectrum also results in a larger amount of radiated energy, which can be quite disruptive to any other transmission schemes operating in the same binder group. It seems that TCM is limited ultimately by loop delay, which is a physical limitation and is difficult to overcome. Efforts to overcome this may result in substantial degradation of customer service.

23. What are the advantages of Biphase over other line codes?

There are several advantages inherent with the Biphase line code. Since it is a two level code, it has an extra 6dB of SNR over a three level code (eg. AMI). Differential encoding makes the transmission insensitive to wiring crossover. Furthermore, the nature of the PSD graph enables the signal to be effectively bandlimited without losing the major portion of the signal content. The guaranteed zero-crossing in each baud makes data and clock extraction much more reliable and robust. Equalization for Biphase is much less complex than for other codes such as AMI and 4B3T, as these require very complex adaptive equalizers to operate properly. The adaptive equalizer adds to the cost geometry and complexity of the interface solution.

24. How long does the DNIC take to achieve synchronization after power up?

The time before valid data transmission begins is a function of the data rate, the line condition, and the initial value of the RAM. The majority of the activation time is taken up by the settling of the RAM to the appropriate line value. Synchronization is achieved concurrently with the settling of the RAM. Therefore, by the time the RAM has settled, the DNIC will have achieved synchronization.

25. Why is the data scrambled before being transmitted?

The data stream is scrambled in order to ensure orthoganality of transmission, i.e. the transmitted and received data should not be correlated in any way. Another reason for scrambling is to ensure that every RAM location is accessed and iterated down to the correct value in the initialization sequence.

26. What is the training sequence for the DNIC on power up?

The DNIC does not require a specific training sequence to achieve synchronization on power up. The scramblers in the DNIC ensure that random data is put on the line, thus guaranteeing convergence. Synchronization is achieved from the received data stream, and is independent of the actual transmitted data.

27. What kind of echo cancelling scheme does the DNIC use?

The echo cancelling scheme is referred to as "RAM based echo cancelling, using the sign bit algorithm". The process of echo cancelling is as follows. An estimate of the echo resulting from a particular transmit data sequence is stored in RAM. The value in RAM is a digital representation of the echo estimated to be reflected from the line. The RAM value is passed through a D/A converter into a summer. The summer subtracts the echo estimate from the composite signal made up of the far-end signal and actual reflected echo. An error signal, either positive or negative (i.e. sign bit), is generated which serves to either increment or decrement the value of the echo estimate stored in RAM. The next time the same data sequence is transmitted, the new value of echo estimate is used, and the process repeats itself. The RAM is active continuously and adapts to any changes in the line, characteristics, hence it is referred to as an adaptive echo cancellor.

28. What is the recommended value to use as a termination impedance?

The termination impedance (Z_t) designated by R2 C2 and C2' in Figure 18 and 19 of the datasheet, is used to match the characteristic impedance of the telephone line (Z_o). Z_t should be approximately equal to four times Z_o. This is due to the four times impedance multiplication through the 2:1 transformer. C2' has been placed in parallel to R2 to correct the phase of the signal being returned to L_{in}. Tailoring of R2, C2, and C2' can be done for specific situations such as bit rate, cable gauge, and cable characteristics. Recommended values for 160 kbit/s are: R2 = 390 ohms, C2 = 22 nF, C2' = 1.5 nF. For 80 kbit/s R2 = 390 ohms, C2 = 22 nF, C2' = 3.3 nF.

29. How does the DNIC transmit information in the Modem Mode?

The DNIC can be used as a high speed, limited distance, modem. It is capable of transmitting up to 80 KHz of NRZ data either synchronously or asynchronously. The DNIC samples the signal presented to its Di pin at the selected baud rate. This signal is converted to a biphase signal and sent onto the line. At the far end, the DNIC decodes the biphase signal, and recreates the equivalent NRZ data pattern.

30. What loopback functions does the DNIC provide?

The DNIC has three loopback options which are activated via the C-channel and the diagnostics register. The first loopback loops DSTi to DSTo at the local end for system diagnostics. The second loopback loops back L_{out} to L_{in} at the local end for system and DNIC diagnostics. The third loopback loops back DSTo to DSTi at the remote end to provide full end to end diagnostics. In the DSTi to DSTo and DSTo to DSTi cases, it's only the B channels which are looped back. With the L_{out} to L_{in} loopback, the entire Biphase output stream is looped back.

31. What are the major applications of the DNIC?

The DNIC is essentially a digital transmission device. It can easily be used in voice and data transmission systems. The DNIC is an excellent PBX device, allowing flexible digital line card and terminal design using 2 wire transmission. ISDN type services can be carried by the DNIC over the U-Interface. The DNIC can provide a high speed data stream for multiplexed lower rate data, such as RS-232C. The DNIC can also be used as a SLC-96, or D4 channel bank interface, allowing easy multiplexing into a T1 stream.

32. What further information is available on the DNIC?

The DNIC is supported by a team of highly skilled applications engineers providing practical information to potential users in order to facilitate the design-in of the DNIC. There is a DNIC Application Note (MSAN-124) available which highlights some of the many potential applications of the DNIC. Reprints of several DNIC related published papers are also available.

33. What is in the future for the DNIC?

Work is currently going on to increase the performance of the DNIC. An application circuit is available which can be used to increase the performance of the DNIC. MSAS-46 describes the extender circuit configuration as well as specifying values for 80 and 160 kbit/s operation. With the extender circuit, performance in the range of 42 dB of cable attenuation can be achieved. This corresponds to over 6 km on standard 24 AWG telephone cable for 80 kbit/s and 5 km for 160 kbit/s.

34. What other devices does Mitel have for ISDN?

Mitel makes a complete family of devices for ISDN. Devices used in CPE applications include the MT896X series of PCM filter codecs and the MT8950 data codec, which converts lower speed data (up to 19.2 kbps async) into 64 kbit/s channels. An S-Interface transceiver (MT8930) is currently in development and is expected to be available in late 1986. T1 (MT8975) and CEPT (MT8978) interface families are currently available for the Primary Access Rates (S1 and S2). The MT8952 HDLC Protocol Controller is designed to provide D-channel layer two X.25 formatted information. Further to these ISDN devices, Mitel has other ST-BUS devices which facilitate circuit design. These include the MT8980 Digital Crosspoint Switch, and the MT8940 Dual Digital Phase-Locked Loop For the pre-ISDN environment, Mitel has a family of analog line interfaces (C.O., ONS, OPS) which provide transformerless conversion between analog and digital lines.

MITEL®

Application Sheet **MSAS-46**

Loop Extender Circuit for the MT8972 DNIC

9161-001-033 NA ISSUE 1 APRIL 1986

The circuit shown in Figure 1 may be used to extend the line length over which the MT8972 can operate. The configuration of the circuit is the same for both 80 kb* and 160 kb. The component values for each baud rate are listed in Table 1. Operation has been achieved with up to 40dB of line attenuation (measured at 60 kHz for 80 kb and 120 kHz for 160 kb). The transmission performance of the loop extender circuit for a bit error rate of 10^{-6} is summarized in Tables 2 and 3.

The MT8972 L_{OUT} (Pin #1) signal is pre-equalized and amplified. It is then passed through the line termination impedance (CL, RL, RLL) and through the transformer to the line. The transmitted power on the line is limited to 10 dBm/120Ω and can be altered by varying the value of the resistor R2.

* kb - kilo bits per second

The MT8972 expects to receive a composite signal on L_{IN} (Pin #21) which should be one-half of V_{LOUT}, plus the sum of the far-end signal, noise and echoes. The passive circuit (C2, C3, C4, R6, R7 and R8) supplies one half of the V_{LOUT} with the proper phase to optimize the internal pre-cancellation. The differencing circuit of OP2 forms the external hybrid.

The circuit shown in Figure 2 illustrates a typical application of the loop extender circuit. Jumpers allow the reçonfiguration of the circuit from MT8972 alone to MT8972 with loop extender. This switchable configuration allows the MT8972 and loop extender circuit to operate on loops with attenuation less than 7dB.

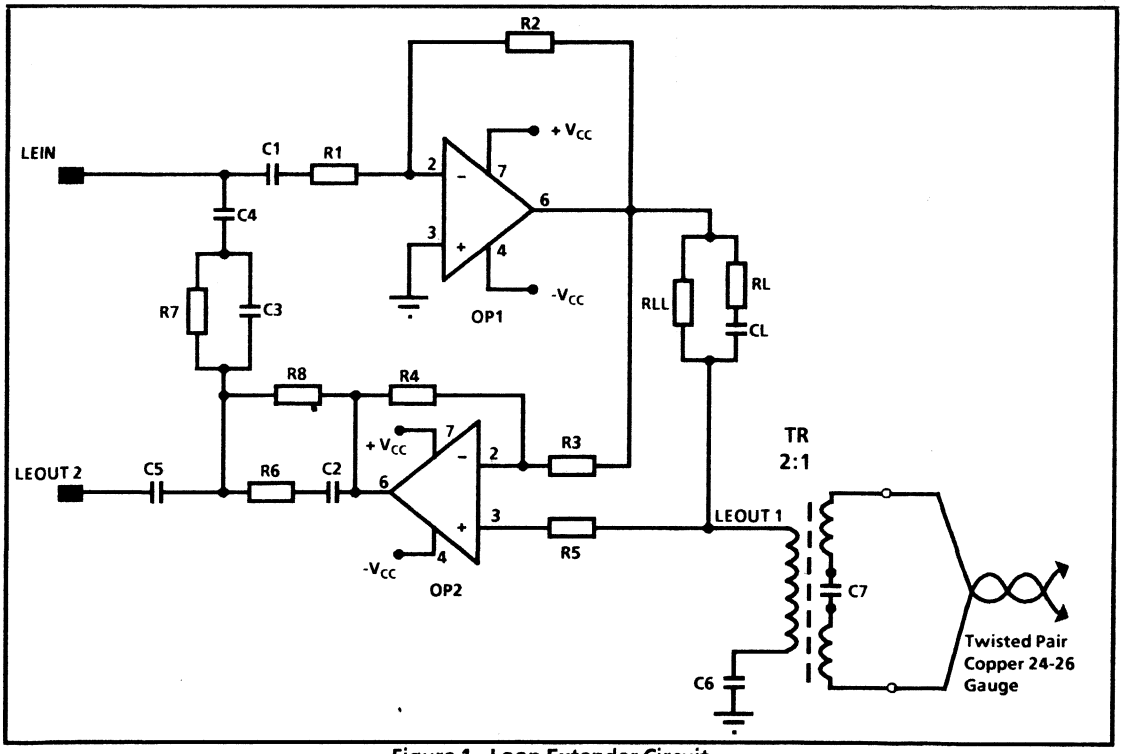


Figure 1 - Loop Extender Circuit

				80 kb		160kb	
R1	24k	5%					
R2	75k	5%					
R3	20k	1%					
R4	20k	1%	C1	560pF	5%	330pF	5%
R5	10k	10%	C2	5.6nF	5%	3.3nF	5%
R6	360Ω	2%	C3	6.2nF	5%	3.6nF	5%
R7	470Ω	2%	C4	10nF	5%	5.6nF	5%
R8	2.7k	5%	CL	12nF	5%	15nF	5%
RL	430Ω	2%	RLL	3k	5%	3.9k	5%
OP1,OP2 (Note 1)	LF411	(National Semiconductor)					
C5	47nF	10%	Note: V_{CC} = ± 10 to ± 15V				
C6	100nF	10%					
C7	1µF	10%					

TR Transformer
1. Turns ratio 2:1 (split secondary)
2. Frequency response - flat passband (+ /- 3 dB) 10kHz to 500kHz
3. Primary inductance - 50mH
4. DC capability - max. 100mA without transformer saturation

Table 1 - Component Values

80 kb		
CONFIGURATION \ CABLE	24 AWG (6.9 dB/km at 60kHz)(Note 2)	26 AWG (10.0 dB/km at 60kHz)
DNIC to DNIC	0.0 to 5.2 km	0.0 to 3.4 km
DNIC with LEC* to DNIC and LEC	0.9 to 6.5 km	0.65 to 4.1 km

Table 2 - Transmission Performance at 80kb (BER = 10^{-6})

160 kb		
CONFIGURATION \ CABLE	24 AWG (8.0 dB/km at 120kHz)	26 AWG (11.5 dB/km at 120kHz)
DNIC to DNIC	0.0 to 4.1 km	0.0 to 3.0 km
DNIC with LEC to DNIC with LEC	0.65 to 5.1 km	0.5 to 3.6 km

Table 3 - Transmission Performance at 160kb (BER = 10^{-6})

*LEC = Loop Extender Circuit

Note 1 : The selection criteria for operational amplifier:
-Slew rate SR ≥ 10V/µs
-Output Voltage Swing = 20Vpp for R_L = 700Ω
The specified op-amp LF411 can be replaced by LF353 with supply voltage of ± 15V + /- 10%.

Note 2: The attenuation of the cable as specified by Bell System Technical Reference PUB 62411

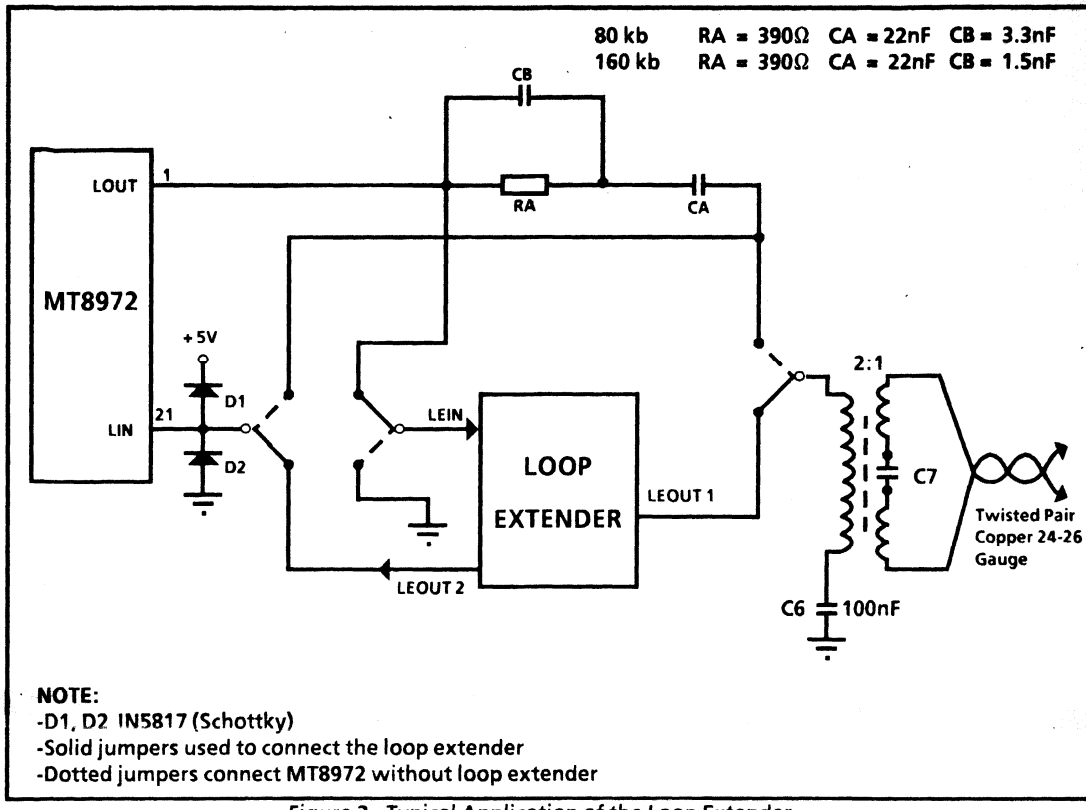


Figure 2 - Typical Application of the Loop Extender

Notes:

MITEL

Application Note **MSAN-101**
Applications of the MT8804A 8 × 4 Analog Switch Array

AUG. 1982

Contents

- The MT8804 in detail
- Modular line interface circuit
- DTMF Receiver tester control circuit
- Test equipment switching system
- 4-Channel 4-bit D/A convertor
- Programmable attenuator
- Multi output programmable frequency divider
- MT8804 status indicator

Introduction

The constant trend in electronic design is towards circuits which minimize power and space requirements while improving on the performance characteristics of their predecessors. The field of analog switching is no exception to this design strategy. The Mitel MT8804A CMOS 8 × 4 Analog Switch Array is a micropower device which replaces several CMOS MSI packages and meets the stringent specifications required in analog switching systems. The 8 × 4 array configuration and minimal interchannel crosstalk make the MT8804A ideal for crosspoint switching applications. This application note provides both functional and parametric details of the device that would normally be required in designing the MT8804A into such systems. A series of application circuits and descriptions is presented to further illustrate the use and versatility of the MT8804A in communications and other more general areas.

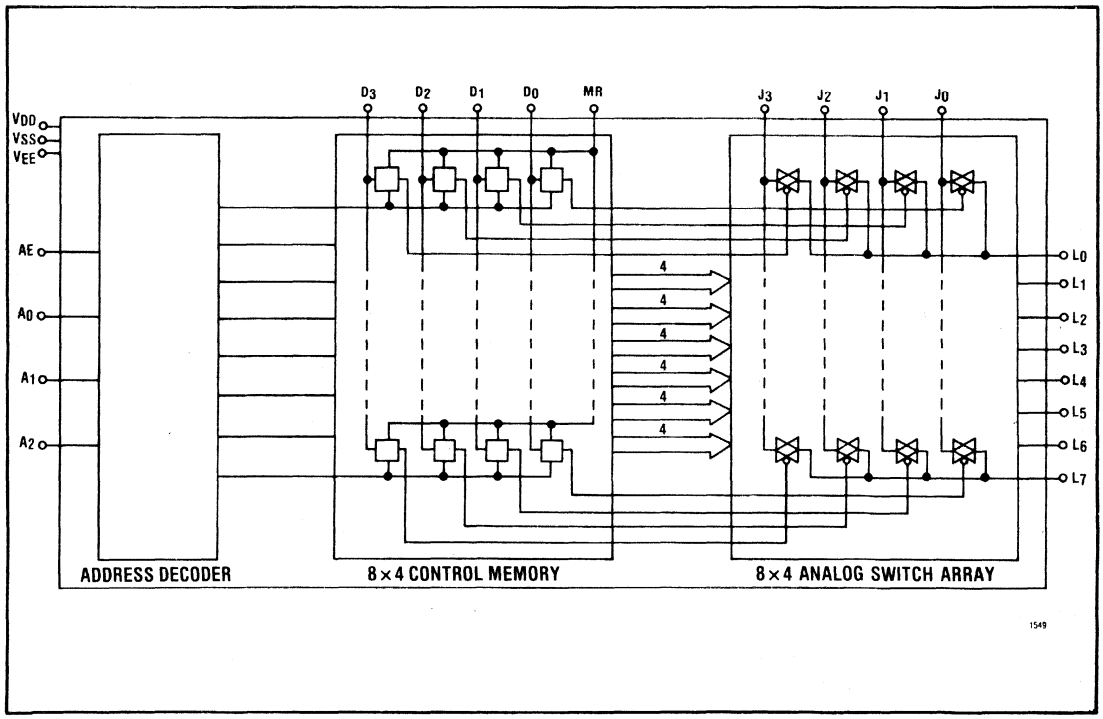


Fig. 1 Functional Block Diagram

The MT8804A in Detail

Configuration and Control

The 32 analog switches in the MT8804A are configured in an 8 × 4 array as shown in Figure 1. The eight switches in each column are connected to an input/output Junctor (J_0 - J_3), and similarly, the four switches of each row are connected to an input/output Line (L_0 - L_7). Each crosspoint switch provides either isolation or transmission between its associated line and junctor. The states of the switches are controlled by a set of 32 latches arranged in an 8 × 4 array corresponding to the analog switch matrix. A logical HIGH stored in a latch turns the corresponding switch ON, while a LOW level turns the switch OFF. Data is asynchronously written into the control latches whenever the Address Enable (AE) input is HIGH. The latch outputs are directly connected to the control inputs of the analog switches. This direct interconnection results in a "continuous read" of the control memory (latches) by the analog switches.

Writing data into the control memory is done the same as in a standard random access memory. However, since no read control signals are required, the control store can uniquely be treated as a write-only-memory. The eight rows are selected by the three Address (A_0 - A_2) inputs. The signals on these lines are decoded to a one-of-eight active high format. The Address Enable (AE) input gates the active output from the decoder to the enable inputs of the latches in the addressed row. Levels present on the Data (D_0 - D_3) inputs are asynchronously latched when the AE input is high. The data corresponds directly to the states of the switches in the addressed row; i.e. D_0 to J_0, D_1 to J_1, etc. For example, if junctor J_1 was to be connected to L_4, the control inputs would be set up as follows: $D_3\ D_2\ D_1\ D_0 = 0010$, and $A_2\ A_1\ A_0 = 100$. Pulsing the AE input HIGH would complete the connection. If instead, both J_1 and J_3 were to be connected to L_4 then the data inputs would be set to $D_3\ D_2\ D_1\ D_0 = 1010$ and all else would remain the same. Similar connections can be programmed for each of the eight lines (L_0 - L_7). All of the latches in the control memory are asynchronously reset whenever the Master Reset (MR) input is HIGH. This results in all analog switches being turned OFF, isolating all junctors from all lines.

Power Supply Considerations

The MT8804A is equipped with on-chip logic level converters to simplify the interface to logic circuits in an analog switching system. The control inputs of the device are driven from signals between V_{DD} and V_{SS}. All of the control inputs are active HIGH with V_{DD} being a logical HIGH level and V_{SS} a logical LOW. The analog or digital signals switched through the array are allowed to swing between V_{DD} and V_{EE}.

The power supply input voltages are defined as follows:

$5V \leq V_{DD} - V_{SS} \leq 13V$ Digital
$5V \leq V_{DD} - V_{EE} \leq 13V$ Analog
$0V \leq V_{SS} - V_{EE} \leq 8V$ Level Convertors

These voltages define the operating power supply ranges of the digital and analog inputs and the logic level converters. While the analog and digital power supplies have identical limits the levels may be different in a given application. For example, a valid power supply configuration is as follows:

$V_{DD} = +5V$, $V_{SS} = 0V$ and $V_{EE} = -6V$. The control inputs are thus driven from a 5V CMOS logic system while the signals on the lines and junctors can swing from $+5V$ to $-6V$. Caution must be used to meet all three power supply constraints when deciding upon a power supply configuration. The following is an example of invalid power supply voltages: $V_{DD} = +5V$, $V_{SS} = 0V$, and $V_{EE} = -12V$. In this case, $V_{DD} - V_{EE} = 17V$ which exceeds the analog power supply range.

Analog Switch Characteristics

Like all monolithic analog switches, the MT8804A exhibits a resistive characteristic when turned on. This 'ON' resistance has two components, the actual resistance of the channels of the MOS transistors and the interconnect resistance between switches. The potential variation of the total resistance with temperature, power supply voltage and input signal voltage is illustrated in Figure 2 and 3. Most applications will not be adversely affected by the ON resistance or its variations with these parameters. However in some systems and applications with more stringent specifications, special considerations may be required. In cases such as driving through the MT8804A into low impedance loads, or using the device in a gain control circuit, it becomes necessary to consider the switch resistance in design equations.

Timing Measurements

Timing measurements such as propagation delays, set up and hold times, etc. on the control inputs of the MT8804A cannot be made directly as

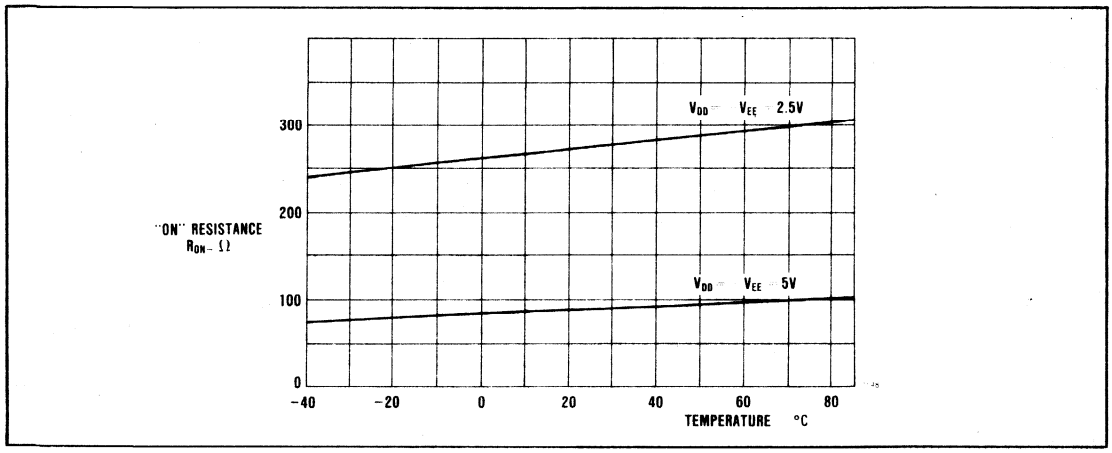


Fig. 2 On Resistance VS Temperature (Input Signal Voltage = Supply Voltage/2)

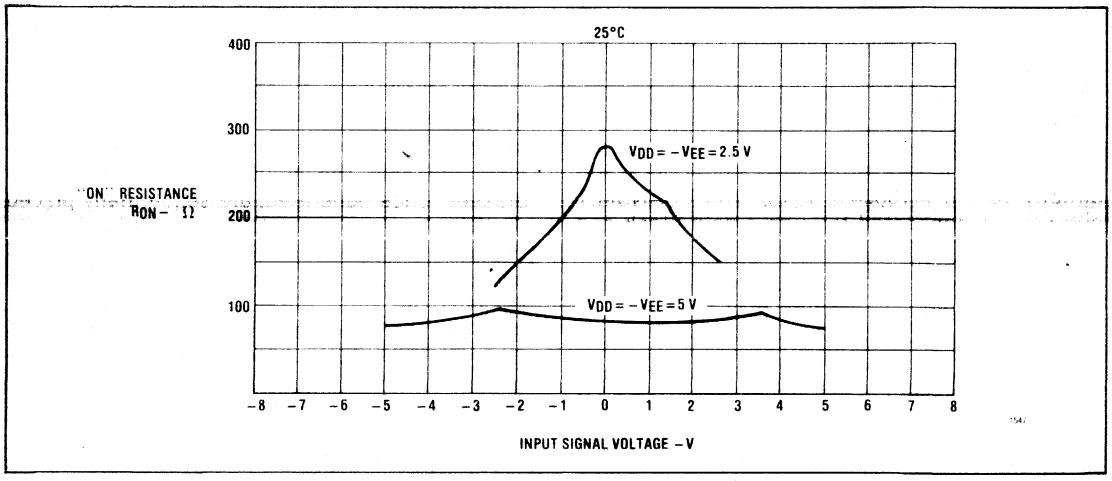


Fig. 3 On Resistance VS Input Signal Voltage

digital outputs are not available. For this reason, these measurements are made indirectly by observing the effects of changes in the control memory on the states of the analog switches. For example, to measure t_{PAE}, the propagation delay from the address enable (AE) input to the signal output, the following steps are taken. A load circuit (50pF in parallel with 10K) is connected from a given junctor to ground (V_{SS}). One of the lines (L_0 - L_7) is connected to V_{DD}. With all switches initially OFF, the control inputs are set up to connect the load circuit to V_{DD} through the appropriate switch. The AE input is pulsed HIGH and the propagation delay time is measured from the 50% voltage point of the resulting signal across the load. In both cases, time is measured from the leading edge of the signal. The actual time measured has three components.

1) The write time into the control latch
2) The turn on time of the analog switch
3) The propagation time through the channel of the switch

In digital switching applications of the MT8804A, it is this total time that is of concern. In general, however, the minimum time needed to write data into the latches is required. This is represented by the first of the three components listed above and is by far, the longest of the three. Therefore, basing system design on the actual measurements of total time will add a small safety margin without sacrificing significant device performance.

A special note is made in regards to the minimum address set up time (t_s). Due to internal capacitive loading on the AE input, the MT8804A requires more time to enable the control latches than is needed to enable and decode the address lines. For this reason, it is not necessary to provide any time for the address lines to settle prior to applying a pulse to the AE input. In other words, address changes are allowable up to and including the leading edge of the AE pulse.

Modular Line Interface Circuit

The MT8804A is shown in an eight channel line interface switching application in the circuit diagram of Figure 4. The ITT North 3081/3082 Subscriber Line Interface Circuit (SLIC) isolates the MT8804A's from the telephone lines. The main function of the SLIC is to provide a 2-wire to 4-wire conversion between the balanced TIP and RING lines and the single ended TRANSMIT and RECEIVE lines. Incoming signals accepted on the RECEIVE input of the SLIC are converted to differential form and fed onto the Tip and Ring pair. Likewise, signals are accepted from the Tip and Ring lines and appear on the TRANSMIT ouput. The RECEIVE inputs of the SLIC's are connected directly to the MT8804's (L_0-L_7). The TRANSMIT outputs are connected through a gain block and then onto the MT8804A's.

This gain block is required to compensate for approximately 17dB of insertion loss from the TIP and RING inputs to the TRANSMIT output of the SLIC. The gain block shown provides the gain required to fully recover the signal loss. However, when phones are on-hook, an audio frequency oscillation may occur. An analog switch, controlled by the Switchhook Detection output of the SLIC, reduces the ac gain to unity preventing this oscillation. A small capacitor placed around the feed back loop eliminates spurious high frequency oscillation.

Network Control

In general, to complete a telephone call with this system, it is necessary to connect the TRANSMIT output of a calling party to the RECEIVE input of a called party and vice versa. Thus, for each telephone conversation, two speech paths are required. In the configuration shown in Figure 4, four simultaneous conversations are possible. With all of the MT8804A's reset, the junctors (J_0 - J_3) are floating and not assigned to any particular telephone line. Thus, the junctor can be completely controlled by software in a microprocessor system, independent of the particular telephone line being switched. The software must maintain a record of which junctors are in use and which are free for completing calls. To better illustrate these points, all the steps required to complete a connection between two parties will be outlined.

The signal paths connecting the junctors of MT8804A's have been arbitrarily named S_0 to S_7 for reference. To connect a call from a given source party to a destination party, it is necessary to interconnect the respective TRANSMIT and RECEIVE leads. To accomplish this, addresses for the source and destination lines of the call must first be generated. The source address is derived from the off-hook conditions which are either encoded or scanned. The destination address is generated by reception of dial pulses or DTMF signals. Once these addresses have been established, the software can implement a control sequence to close the appropriate switches. This sequence is not unique as the order in which switches in the MT8804A are closed is not critical. The example which follows illustrates a possible control sequence that could be used.

If it is assumed that all of the signal paths (S_0 - S_7) are free, then S_0 and S_1 would be used to complete the call. The source and destination addresses, once generated, are sequentially placed on the microprocessor data bus and hence onto the address inputs of the MT8804A's. Since S_0 and S_1 are being used, the data inputs (D_3 D_2 D_1 D_0) must be alternatively set to 0001 and 0010. With the source address on the address lines and D_3 D_2 D_1 D_0 = 0001, the ADDRESS ENABLE (AE) of chip 'A' is taken HIGH. The data lines are next set to D_3 D_2 D_1 D_0 = 0010 and the AE input of chip 'C' is taken HIGH. This completes the connections of the TRANSMIT and RECEIVE leads of the source party to S_0 and S_1 respectively. It remains only to connect the destination TRANSMIT lead to S_1 and RECEIVE lead to S_0 to complete the 2-way interconnection. To do this, the destination address is set on the address inputs of the MT8804A's. the data lines are again set to D_3 D_2 D_1 D_0 = 0010 and the AE input of chip 'A' is taken HIGH.

Lastly, with D_3 D_2 D_1 D_0 = 0001, the AE input of chip 'C' is pulsed high. This connects the TRANSMIT and RECEIVE leads of the destination line to S_1 and S_0 respectively as required. All necessary interconnections are thus complete and the processor become free to service other calls.

To disconnect a telephone call, the following steps are taken. Once a change in off-hook condition is detected, the address from the scanning circuitry is put onto the address lines and the data

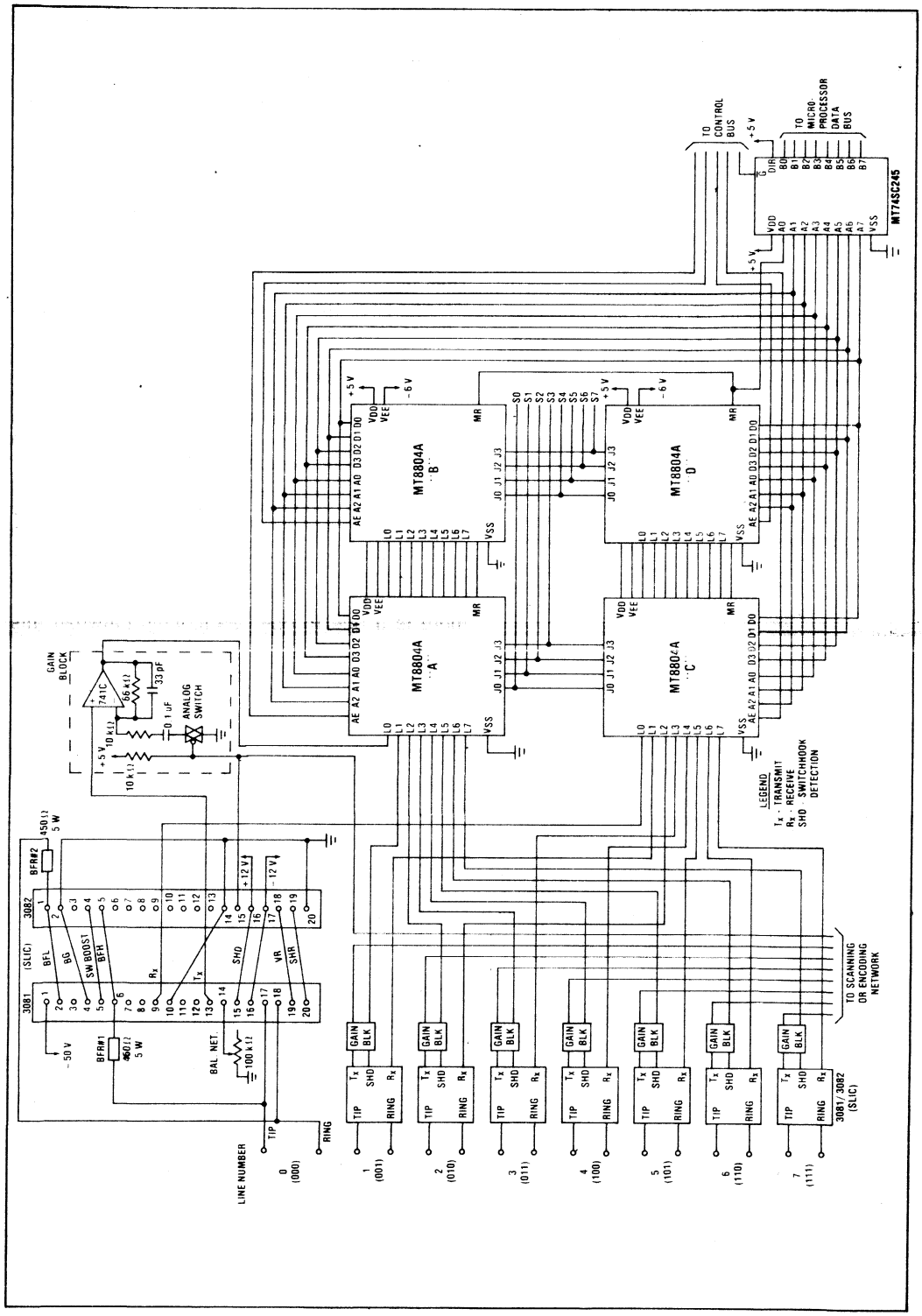


Fig. 4 Line Interface Switching Circuit (8 - Port Module)

lines are all set to zero. The appropriate Address Enable pulses are applied to implement the disconnection. Once both parties have been scanned, the signal paths used for the conversation are freed and added to the list of available signal paths. The MASTER RESET, when taken high, will disconnect all interconnections, freeing all signal paths. This is useful for system initialization or testing.

Switching Network Modularity and Expansion

The 8 port line interface switching module shown in Figure 4 would typically be used as the basis for larger systems such as a PBX. Expansion to a larger switching network involves two independent steps. The first involves increasing the maximum number of simultaneous conversations that can be conducted. This is referred to as traffic handling capacity, and is increased by adding MT8804A's in pairs to the basic module as shown in Figure 5. The lines (L_0 - L_7) are extended and connected to those of the new devices. The junctors (J_0 - J_3) of the two aditional MT8804's are connected together to provide 4 additional signal paths. The network as shown has 12 signal paths and hence can carry 6 simultaneous telephone conversations.

The second expansion step is to increase the number of 8 port modules. Figure 6 shows the interconnection between two basic modules of Figure 4. The signal paths (S_0 - S_7) are extended to show how the two modules are connected. The control lines of each module (not shown) would be connected to the system data bus and appropriate enabling signals would have to be generated. That is, each module would also have a unique address. Combining both expansion steps is exemplified by a network comprised of two expanded switching modules of Figure 5. This would result in a system with 16 ports (telephone lines) capable of handling 6 simultaneous conversations.

The normal sequence in designing a switching network involves first establishing the maximum traffic handling capacity of the system. With this in hand, the 8 port modules can be designed with the appropriate number of MT8804A's. Modular system expansion would then only involve adding the required number of such modules. The number of MT8804A's required per module and total is shown in Table 1 as functions of the number of ports to the network and traffic handling capacity. From the table it can be seen that there is a one to one relationship between this traffic handling capacity and the number of

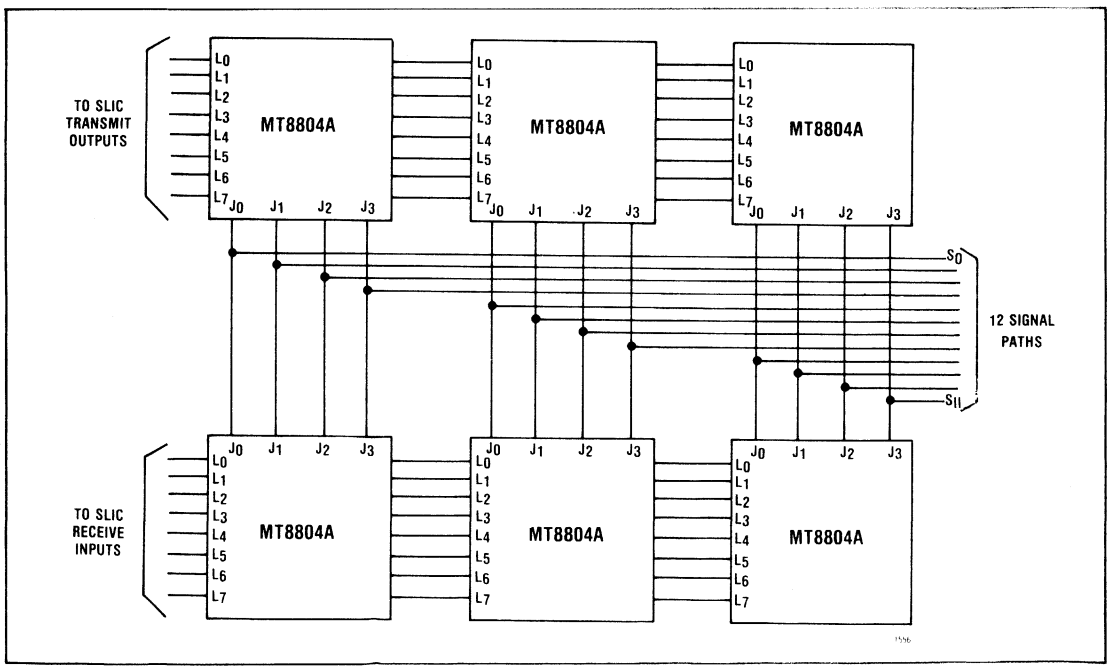


Fig. 5 Expanded Switching Module

MT8804A's required in the corresponding module. This can be used as a design aid in determining the amount of circuitry required to implement various sized systems. This information is expanded in the table of Table 2. Here, is shown the variation in the number of MT8804A's required as a function of traffic handling capacity only in a fixed 256 port system.

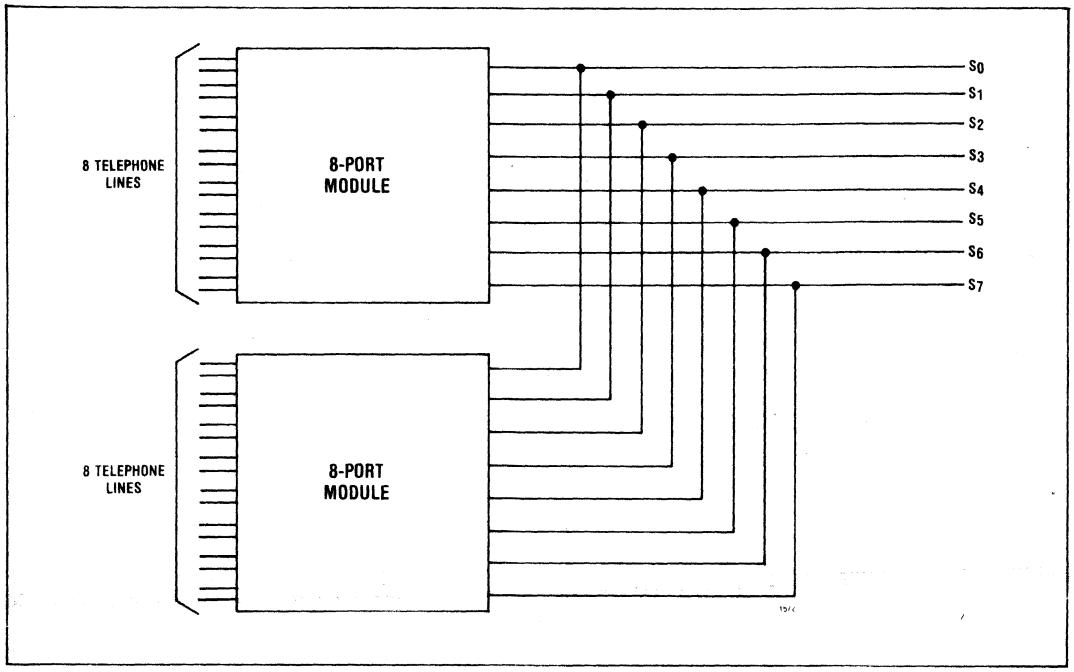


Fig. 6 Expanded Switching Network

TABLE 1
NUMBER OF MT8804A'S AS A FUNCTION OF SYSTEM SIZE

NUMBER OF PORTS TO NETWORK	8	16	32	64	128	256
NUMBER OF 8 PORT MODULES	1	2	4	8	16	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL	4	16	64	256	1024	4096

Table 2
Number of MT8804A's as a Function of Traffic Density for a 256 Port Network

NUMBER OF PORTS TO NETWORK	256	256	256	256	256	256
NUMBER OF 8 PORT MODULES	32	32	32	32	32	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL	128	256	512	1024	2048	4096

1535

Summary

Using the MT8804A in line interface switching systems offers many advantages over conventional circuit elements. Replacing relays or smaller analog switch packages with this device results in great reductions in size and power consumption. Simultaneoulsy, a low level of interchannel crosstalk is maintained. The on-chip control memory with microprocessor compatible inputs provides ease of control and minimizes external circuit requirements. The 8 × 4 analog switch matrix configuration provides great flexibility in modular switching network design. All of these factors combine to make the MT8804A an ideal basis for PBX and key system networks.

Dual Tone Multifrequency Receiver Tester Control Circuit

The versatility of the MT8804A is shown in the Dual Tone Multifrequency (DTMF) receiver tester control circuit of Figure 7. The high and low tones may be mixed or a composite DTMF signal may be fed directly to the receiver under test. By mixing either f_L or f_H through the 200K resistor, plus or minus 6dB of twist may be added to the resulting DTMF signal. The amount of twist may be varied by adjusting resistor values. Dial tone rejection can be tested by switching in the CM7065, Mitel Corporation's Precise Dial Tone Generator. The series resistor (R_S) and potentiometer are chosen to limit the voltage to the MT8804A to the supply limits. Sensitivity to 60Hz can be similarly tested. If the receiver under test has the facility to accept dial pulses, these may be generated by switching the power supplies in and out at the required rates. A single pole double throw relay R1, is added to provide a switchable output impedance to simulate long line conditions. The relay drive is also switched by the MT8804A. The control of the MT8804A is provided by a stored test program in a microprocessor system or a hardwired controller which dictates the sequence of input signals presented to the receiver under test.

Test Equipment Switching System Functional Description

The MT8804A is used as an analog coupling circuit in this test equipment switching system application. Various signal sources, voltmeters, a 2-channel oscilloscope and a frequency counter are connected to the multiplexer. (This selection of course is arbitrary). The test points of the circuit under test can be connected to the multiplexer via banana plugs and jacks, aligator clips or any appropriate means of interconnection. This circuit can be very useful in analyzing prototype circuits which require various measurements at multiple test points.

The test instruments are connected to the test points of the circuit under test through the MT8804A's as shown in Fig. 8. The individual instruments are selected by keys on the keypad as is the particular test point to which this equip-

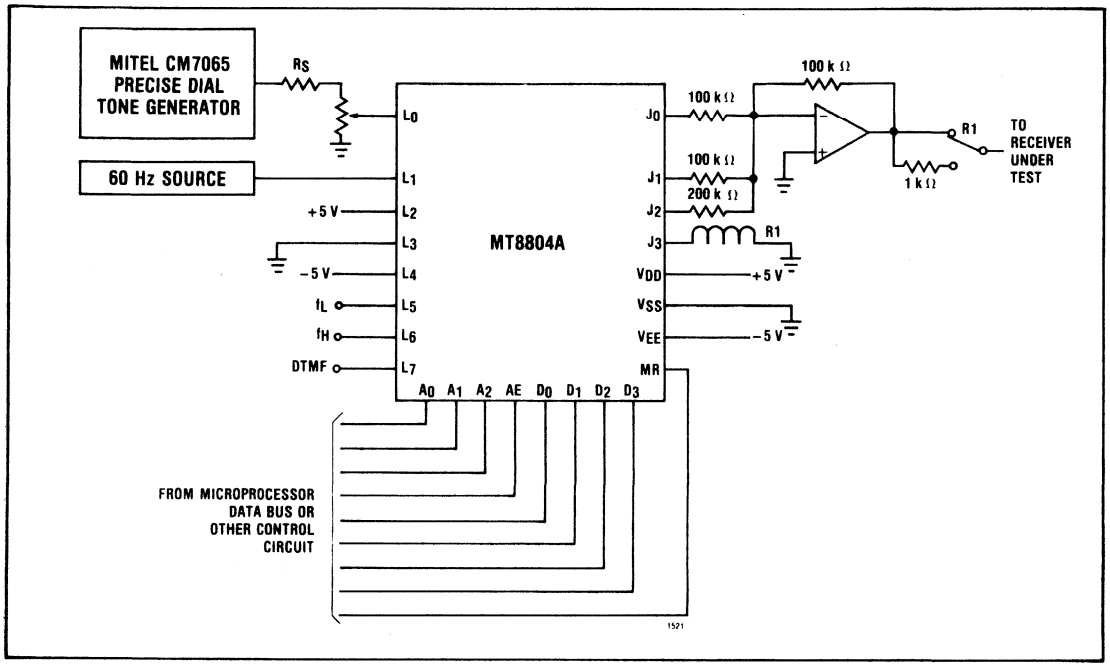


Fig. 7 DTMF Receiver Tester Control Circuit

ment is connected. The system is operated as follows. First the 'TEST POINT' switch is pressed, followed by one of the numbered keys on the keypad. These correspond to the test points. Next, a sequence of keys designated the same as the test equipment is pressed. Finally the 'CONNECT' button is pressed. This completes the connection of the test equipment keyed in to the selected test point. This procedure can be repeated until each test point has been connected or all of the test instruments assigned. The signal sources may be simultaneously connected to more than one test point.

It is a simple matter to disconnect all of the test instruments from a given test point. This is accompolished by again pressing the 'TEST POINT' switch, keying in the number corresponding to the appropriate test point and then pressing the 'DISCONNECT' button. Pressing the 'MASTER RESET' switch at any time disconnects all test instruments from all test points.

Circuit Operation

The two MT8804A's are the heart of this analog switching circuit, coupling combinations of test instruments to the eight test points of the circuit under test. Using all CMOS components and asynchronous operation results in ultra-low operating power consumption.

The allowable voltage swing from the signal sources is from +5V to −5V as determined by the MT8804A power supplies. The control inputs swing from +5V to 0V. User control of the circuit is via a standard 16 switch keypad and four additional momentary pushbutton switches. The keypad consists of 16 SPST switches with one common terminal which is connected to V_{DD} = +5V. The eight switches, marked '1' through '8' are connected to an 8 line to 3 bit binary encoder (4532). The remaining keys are connected to NOR R-S latches (4043) directly. All sixteen switches are pulled to ground through resistors.

Pressing the 'TEST POINT' switch clears all the latches, setting up the circuit for new data. The address (A_0, A_1, A_2) of the MT8804A from the '4532' encoder is asynchronously latched. This address is decoded by the MT8804A to select the line (L_0 - L_7) and hence the test point corresponding to the numbered key pressed. The Group Select (GS) output of the '4532' goes high whenever one of its eight data inputs goes high. This signal is also latched and used to gate the AE pulse to the MT8804A. This ensures that a test point number has been entered and hence prevents unwanted or accidental connections. A series of designated test equipment keys is pressed setting corresponding latches which are connected to the data inputs (D_0 - D_3) of the MT8804A's. These data inputs in turn correspond

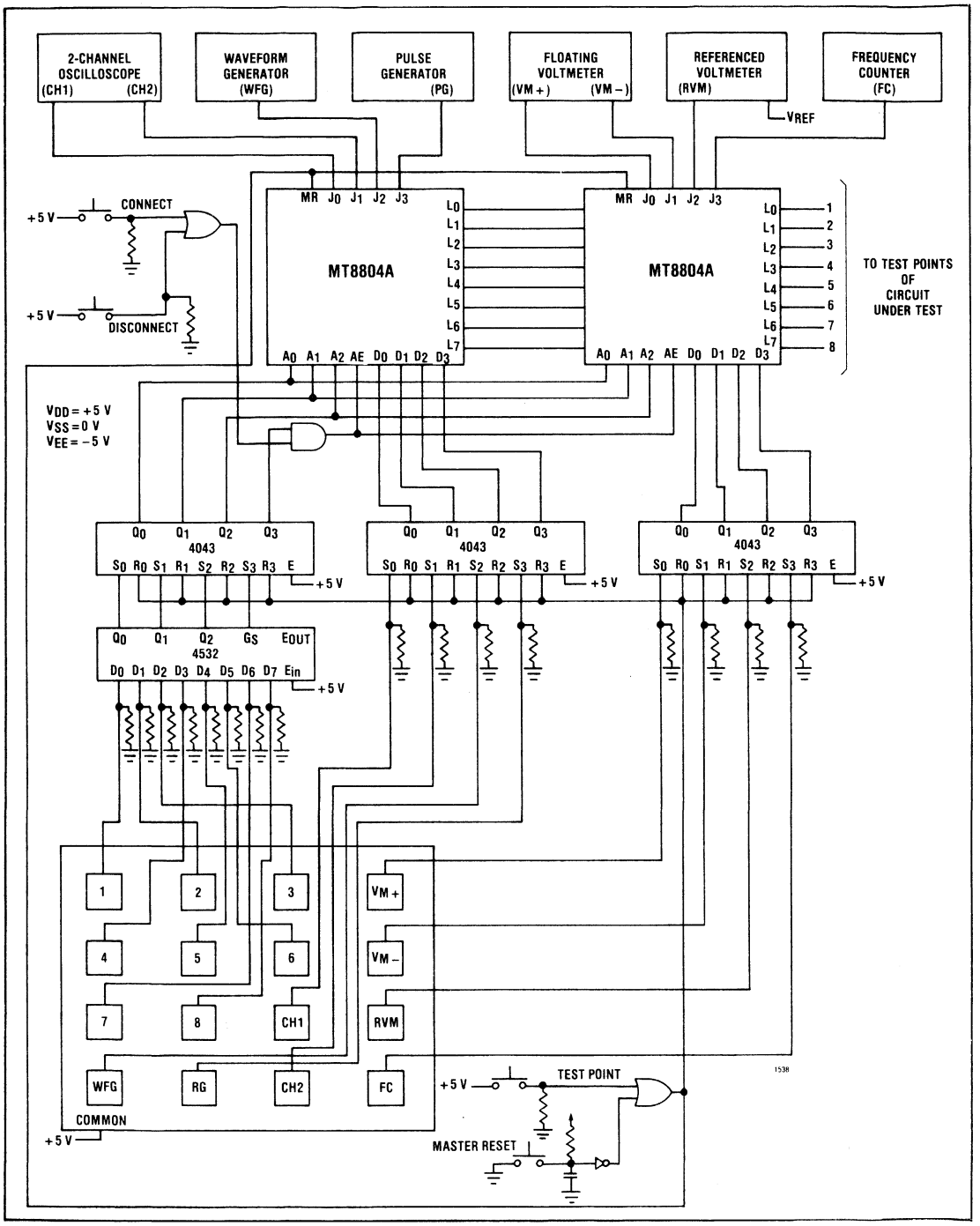


Fig. 8 Test Equipment Switching System

to the junctors (J_0 - J_3) to which the test equipment is connnected. Pushing the 'CONNECT' button pulses the AE inputs of the two MT8804A's, completing the desired connection.

During a disconnect sequence, the latches are cleared by the 'TEST POINT' switch. The numbered key pressed sets up the address of the test point to be disconnected. Pressing the 'DISCONNECT' button next pulses the AE inputs. However, this time, all data inputs are at logical 0's so that all switches to the addressed test point are opened. The 'MASTER RESET' when activated opens all switches in the MT8804A disconnecting all test equipment from all test points. A power-up reset is provided by the resistor, capacitor and inverter in the master reset line. This prevents unwanted connections on power-up. Any convenient values of resistance and capacitance are appropriate provided that the power-up time is short in comparison to the time constant. It is necessary, at all times, to supply power to the switching circuit prior to energizing signal sources.

4-Channel 4-Bit D/A Converter

The circuit of Figure 9 can be used to implement a low resolution (4-Bit), multichannel D/A converter. The digital signals are input on the address lines (A_0, - A_1, AE) and the analog signals are switched from the resistive divider to the lines of the MT8804A (L_0 - L_7) and onto the junctors as selected by the data inputs. Any voltage profile can be programmed be it linear, logarithmic etc. by selecting the appropriate resistors for the divider network. The linearity and monotonicity of the converter are determined by the matching of resistors used. The temperature stability of the converter is dependent upon the relative tracking of the resistors in the network with temperature. The resistor network is shown with one end connected to V_{DD} and the other to V_{SS} or V_{EE}. By setting $V_{EE} = -V_{DD}$, the convertor outputs will swing from V_{DD} to V_{SS} = 0V in one mode and symetrically about 0V from $\pm V_{DD}$ in the other. The op amp buffers are used to reduce the effects of the ON resistance of the MT8804A.

The four analog outputs can simultaneously provide four independent voltages or any combination of outputs may be at the same voltage. The converter can be expanded to more digital inputs by extending the resistive ladder and adding MT8804's.

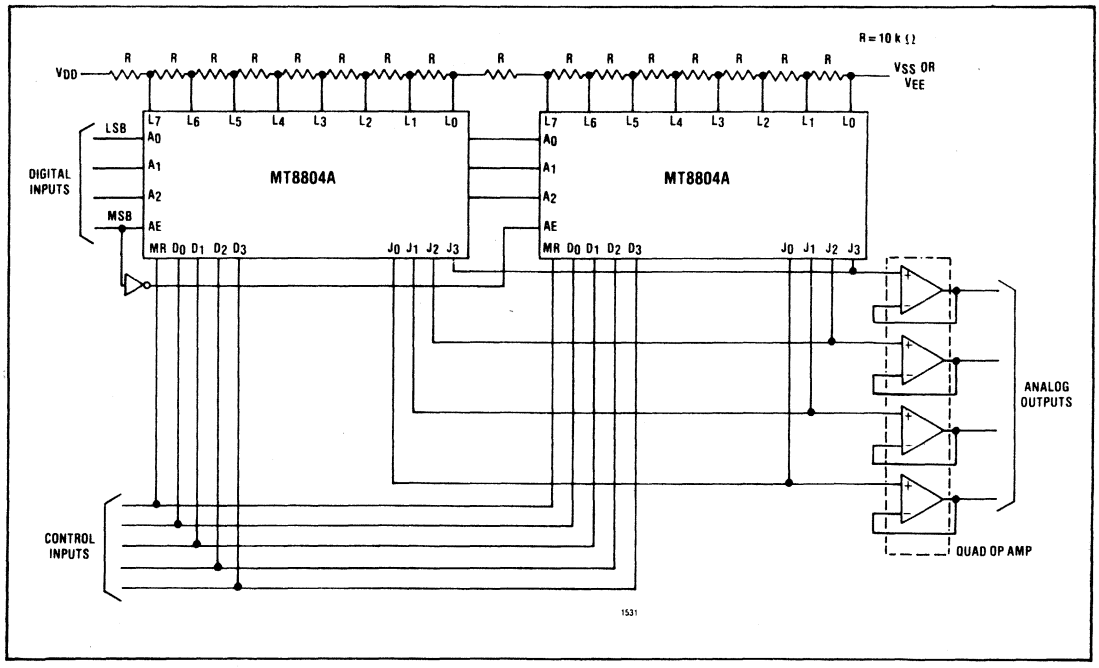


Fig. 9 4-Channel 4-Bit D/A Converter

Programmable Attenuator

The programmable attenuator shown in Figure 10 is capable of providing up to 61dB of attenuation or 20dB of gain. Selecting the input attenuation is accomplished via the address inputs (A_0, A_1, A_2) and can be chosen in 3dB steps. The range is selected in 20dB steps by gating an attenuated input signal onto the appropriate junctor (J_0 - J_3) via the data inputs (D_0 - D_3). The attenuated input signal is buffered after passing through the MT8804A to provide constant input impedance to the attenuator circuit. The resistor multipliers shown provide a logarithmic profile of attenuation, calibrated in dB. A linear profile for use in control system applications is accomplished easily by appropriate choice of resistors. The attenuation accuracy is purely a function of resistor tolerances. The circuit attenuation can be expressed as follows:

FOR ADDRESS $(A_0\ A_1\ A_2)_2 = N_{10}$

$A_{dB} = -(V_o/V_i)\,dB = (3 \times N_{10} + A_R)\,dB$

Where $(A_2\ A_1\ A_0)_2$ — Address expressed as binary number

A_R — Attenuation in dB of range attenuator

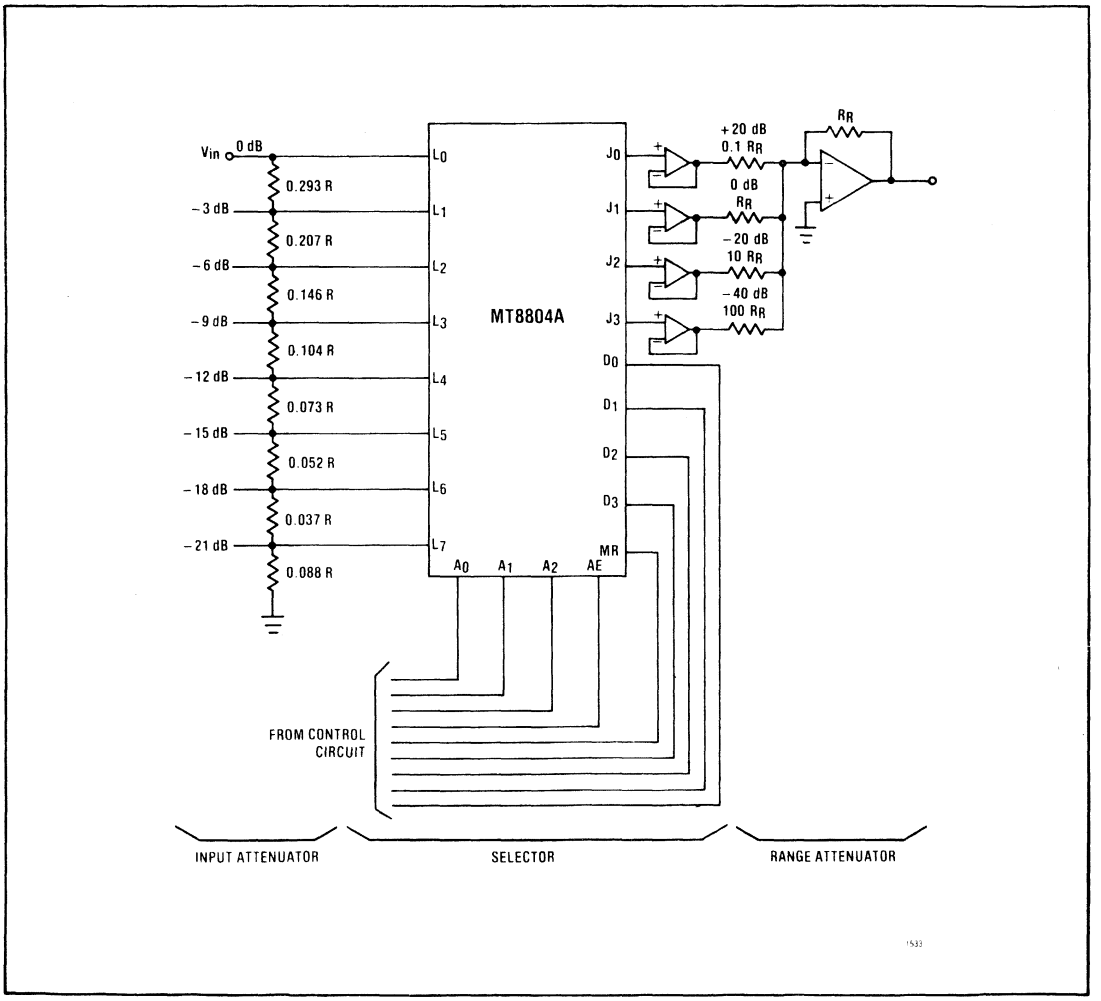


Fig. 10 Programmable Alternator

Multi-Output 2^n Programmable Frequency Divider

The circuit of Figure 11 provides up to 4 independent output frequencies each of which is a binary weighted multiple of a given input frequency. The frequency division factor is represented by the binary coded number on the address inputs of the MT8804A. The division range for the circuit shown is from 2^0 to 2^7. This range can be increased by adding counters for frequency division and MT8804A's to do the switching. The four data inputs (D_0 to D_3) control which output line or lines are switched to a particular frequency. The master reset (MR) when taken high turns all switches off.

MT8804A Status Indicator

In applications where the MT8804A is controlled by a hardwired control circuit as opposed to a microprocessor system, it may be necessary or desirable to have a record of line-junctor interconnections. Since outputs of the control latches are not available, a duplicate memory map is required. An 8 × 4 array of light emitting diodes is used to provide visual output of the information. (See Fig. 12) Control data written into the MT8804A is copied into a Random Access Memory. The RAM shown, the Fairchild 4710BX, is a CMOS device organized as 16 four bit words. As such, 2 MT8804A's could be mapped with one device. The RAM outputs can be used for control purposes as well as visual outputs as shown in the diagram.

A scanning oscillator and counter (negative edge triggered) are used to continuously read data out of the RAM and refresh the LED matrix. The address provided by this binary counter is decoded to a one of eight active low output format by the MD74SC138. Drive current is provided by two 74367 hex 3-state TTL buffers. A variable duty cycle waveform may be applied to the output enables to provide intensity modulation. When data is written into the MT8804A and RAM, the address is provided by the control circuit. This address is isolated from the scanning counter by the octal three state buffer, MD74SC241.

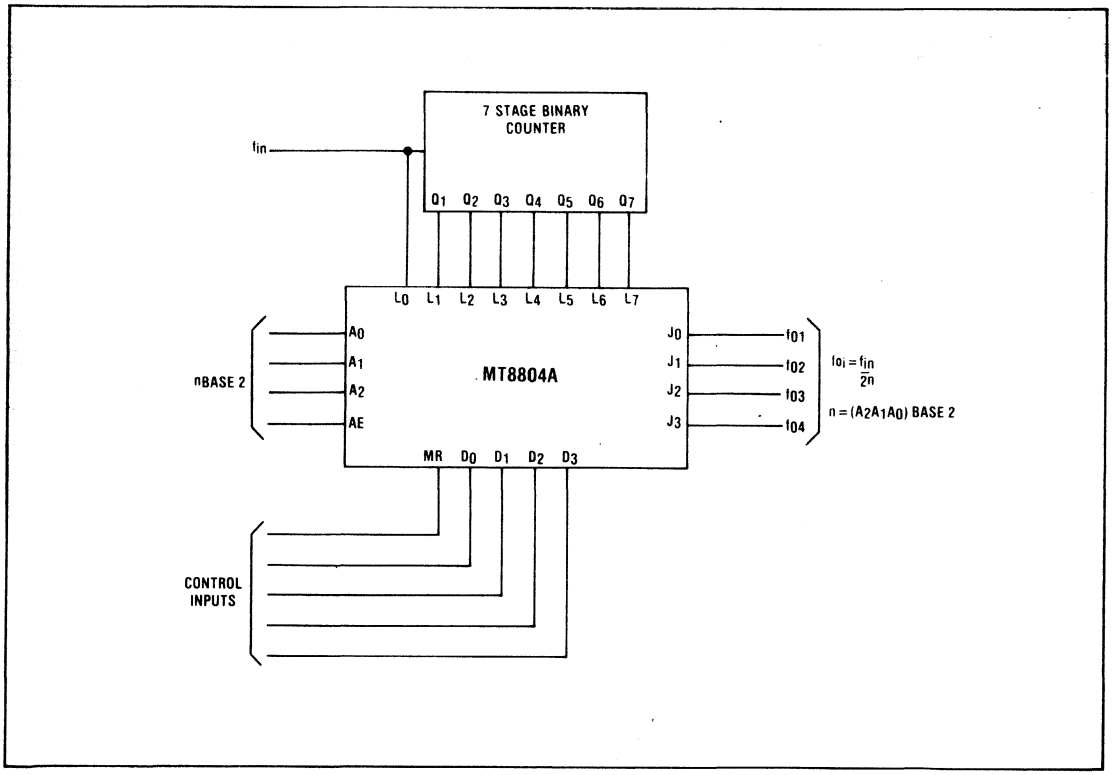


Fig. 11 Digital Application

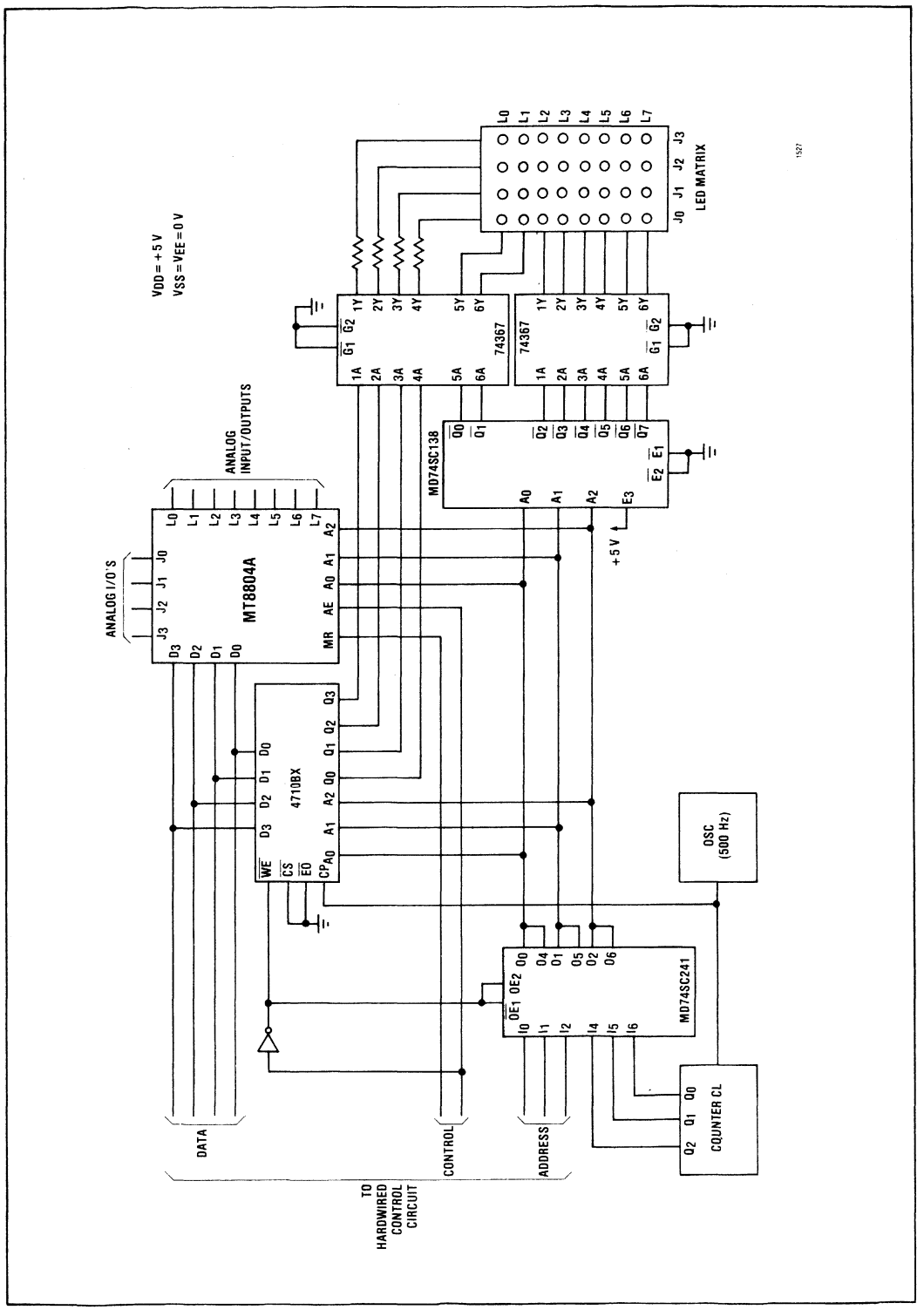


Fig. 12 Memory Map and Visual Indication of MT8804A Control Memory Status

MITEL®

Application Note MSAN-102
Glossary of Digital Telecommunications Terms

August 1986

The following is a list of terms, and their definitions, commonly encountered in the telecommunications industry in relation to digital switching and transmission of speech signals. Where possible, definitions have been based on the international recommendation of CCITT. The terms have been sorted into the following categories:

- •SIGNAL PROCESSING
- •DIGITAL SIGNALS
- •PCM MULTIPLEXING
- •TIMING
- •SIGNALLING
- •CODES
- •DIGITAL SYSTEMS
- •PARAMETERS & UNITS

SIGNAL PROCESSING

A-Law
Companding/encoding law commonly used in Europe (see Companding Law).

A/D (Analog to Digital) Converter
Converts an analog signal sample to a digital representation suitable for digital processing and switching.

Aliasing Noise
A distortion component which will be created if a sampled signal bandwidth is effectively greater than 1/2 the sample rate.

Anti-Aliasing Filter
A filter (normally low pass) which band limits the input signal before sampling to less than half the sampling rate, to prevent aliasing noise.

Codec (PCM)
An assembly comprising an encoder and a decoder in the same equipment, usually operating at a sample rate of 8kHz to accommodate a 300Hz to 3.4kHz bandwidth input signal.

Companding
The processes of dynamic range compression of a signal and subsequent expansion in accordance with a given non-linear transfer characteristic (companding law) which is usually logarithmic. The purpose of companding is to allow transmission of the signal via a channel incapable of carrying the uncompressed dynamic range of the signal. In terms of digital transmission this involves a reduction in the number of bits per sample and consequently the transmission bit rate compared to a linear coding law being used. The tradeoff for this effective increase in the dynamic range handling capacity of the channel is a degradation in signal to noise performed at high signal levels compared with an uncompanded (linear) systems.

Companding Law (CCITT Encoding Law)
Mathematically defined non-linear transfer characteristic used for companding. This may be a smooth continuous function or a piecewise (commonly linear) approximation to a continuous function (CCITT segmented encoding law). The two commonly used laws in telecommunications are μ-Law (North America), A-Law (Europe).

Compression
Reduction of a signal's dynamic range in such a way that small signal characteristics are maintained. Usually a logarithmatic type conversion is used (see Companding).

D/A (Digital to Analog) Converter
Converts a digital word to an analog value.

Decision Value
A reference value defining the boundary between adjacent intervals in quantizing or encoding.

Decoder (PCM Receiver)
A device which performs repeated D/A conversion, expansion and the sample-and-hold function necessary to convert a serial stream of PCM samples to a sample-and-hold equivalent of the originally encoded analog signal (see Codec and Decoding).

Decoding
A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delta Modulation (Simple)
A single bit per sample iterative coding technique for converting an analog signal to a digital bit stream which can be decoded simply by integrating the digital bit stream and lowpass filtering. To obtain telephony quality transmission requires a sample rate of approximately 8kHz.

Delta-Sigma Modulation (Simple)
A single bit per sample iterative coding technique for converting an analog signal to a digital bit stream. The resulting bit stream is a pulse density function of the original analog signal which can be recovered simply by low pass filtering the bit stream. To obtain telephony quality transmission requires a sample rate of approximately 8kHz.

Dynamic Range
The dynamic range of a converter is a measure of its ability to handle a wide range of input amplitude and is defined as the ratio of the largest resolvable signal to the smallest signal that can be handled.

Encoder (PCM)
A device which performs repeated sampling, compression and A/D conversion to convert an analog signal to a serial stream of PCM samples representing the analog signal (see Codec and Encoding).

Encoding
Coding
The generation of digital character signals to represent quantized analog samples.

Encoding Law (see Companding Law)
The law defining the relative values of the quantum steps used in quantizing and encoding.

Error Ratio
A measure for the distortion of a digital signal is the error ratio which is defined as number of wrongly received bits divided by the total number of received bits.

Expansion
Expansion of a compressed signal back to its original dynamic range (see Companding).

HIDM (High Information Delta Modulation)
One of many companded delta modulation schemes. Operates at lower sample rates than simple delta modulation for equivalent performance.

Instantaneously Companded Delta-Sigma Modulation
As its name implies - an equivalent scheme in delta-sigma modulation to the HIDM scheme.

Linear Quantizing
Quantizing in which all the intervals are equal, i.e. linear A/D converter.

Non-Linear Quantizing
Quantizing in which the intervals are not all equal. This keeps the quantizing distortion as low as possible.

Pulse Code Modulation (PCM)
A process in which an analog signal is sampled, and the magnitude of each sample with respect to a fixed reference is quantized and converted by coding to a digital signal. This is the prevalent technique for digital transmission in communications systems.

Quantizing
A process in which samples are classified into a number of adjacent intervals (amplitude steps) each interval step being represented by a single value called the quantized value.

Quantizing Distortion
Due to the restriction of a finite number of produced amplitude steps, a difference inevitably occurs between the information which can be transmitted and the original information. This difference is called quantizing distortion.

S&H (Sample and Hold)
A circuit which samples a signal and holds the sample value until the next sample is taken. In A/D conversion, S/H is usually an analog function. In D/A conversion, the S/H may be performed digitally, making continuous use of the D/A convertor or the D/A convertor may be shared by other functions and its output signal held by an analog sample and hold circuit.

Sample
The value of a particular characteristic of a signal at a chosen instant.

Sampled Data System
A system that operates on samples of the analog input signals. Can be either analog (e.g. switched capacitor filter) or digital (speech coding/digital filter) processing or both.

Sampling
The process of taking samples, usually at equal time intervals.

Sampling Rate
The number of samples per unit time.

Segmented Encoding Law
An encoding law which an approximation to a smooth law is obtained by a number of linear segments.

Single Channel Codec
Codec which is designated to operate on a single signal source and *not* in a multiplexed mode performing the codec functions for more than one signal source.

Single Chip Codec
A single integrated circuit capable of performing all codec functions and in some cases providing an auxiliary signalling interface. It may be either single channel or multiplexable.

Smoothing (Decode or Reconstruction) Filter
Usually low pass. Restores the desired analog signal at the S&H, D/A or decoder output by blocking high frequency components produced by sampling.

Working Range
The permitted range of values of an analogue signal over which a transmission or other processing equipment can operate.

Virtual Decision Value
Two hypothetical decision values, used in quantizing or encoding. Located at the ends of the working range used, and obtained by extrapolation from the real decision values. Effectively specify the maximum input signal amplitude.

μ-Law
Companding/encoding law commonly used in North America (see Companding Law).

DIGITAL SIGNALS

ADI
Alternate digit inversion. Used with A-Law to ensure sufficient 1-0/0-1 transitions for clock extraction (timing recovery) in PCM multiplex transmission equipment.

Asynchronous Transmission
A mode of communication characterized by start/stop transmissions with undefined time intervals between transmissions.

Binary Digit
A member selected from a binary set, e.g. 1,0; V+, V-; H,L.

Note: Bit is in abbreviation for binary digit.

Character Signal
A set of signal elements representing a character, or in PCM representing the quantizing value of a sample.

Note: In PCM, the term "PCM word" may be used in this sense.

Digit
A member selected from a finite set.

Note 1: In digital transmission, a digit may be represented by a signal element, being characterized by the dynamic nature, discrete condition and discrete timing of the element, e.g. it may be represented as a pulse of specified amplitude and duration.

Note 2: In equipment used in digital transmission, a digit may be represented by a stored condition being characterized by a special physical condition, e.g. it may be represented as a binary magnetic condition of a ferrite core or voltage condition in a semiconductor memory cell.

Note 3: The context of the use of the term should be as such as to indicate the radix of notation. (The meaning of "digit" in Notes 1, 2, and 3 translates into French as "élément numerique".)

Note 4: In telephone subscriber numbering, a digit is any of the numbers 1, 2, 3...9 or 0 forming the elements of a telephone number (Recommendation Q.10). (This meaning of "digit" translates into French as "chiffre".)

Digital Signal
A signal constrained to have a discontinuous characteristic in time and a set of permitted discrete values.

Equivalent Bit Rate
In a line coded signal, the number of binary digits that can be transmitted in a unit of time.

Note: The point which the equivalent bit rate is referred may be either real or hypothetical.

Intersymbol Interference
Interference in a digital (or any Time Division) transmission system caused by a symbol in one signalling interval being spread out and overlapping the sample time of a symbol in another signal interval.

Jitter
Short-term variations of the significant instants of a digital signal from their ideal positions in time.

Regardless of the stability of clocks at both ends of a digital transmission system, certain amounts of instability occur in the received signal because of external electrical disturbances and changing physical parameters of the transmission link. The resulting instability in the line clock is referred as "jitter"

Regeneration
The process of recognizing and reconstructing a digital signal so that the amplitude, waveform and timing are constrained within stated limits.

Synchronous Transmission
A mode of digital transmission in which discrete signal elements (symbols) are transmitted at a fixed and continuous rate.

PCM MULTIPLEXING

Channel Bank
Terminal equipment for a transmission system used to multiplex individual channels using FDM or TDM techniques.

Digital Multiplex Equipment
Equipment for combining, by time division multiplexing (multiplexer) a defined integral number of digital input signals into a single digital signal at a defined digit rate and also for carrying out the inverse function (demultiplexer).

Frame
A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Highway
A common path or a set of parallel paths over which signals from a number of channels pass with separation achieved by time division.

Justification (Pulse Stuffing)
A process of changing the rate of a digital signal in a controlled manner so that it can accord with a rate different from its own inherent rate, usually without loss of information.

Multiframe
A set of consecutive frames in which the position of each frame can be identified by reference to a multiframe alignment signal. The multiframe signal does not necessarily occur, in whole or in part, in each multiframe.

Multiplexing
The process of combining the multiple signals into a single channel for transmission over common facilities.

PCM Multiplex Equipment
Equipment for deriving a single digital signal at a defined digit rate from two or more analogue channels by a combination of pulse code modulation and time division multiplexing (multiplexer) and also for carrying out the inverse function (demultiplexer). The description should be preceded by the relevant equivalent binary digit rate, e.g. 2048 kbit/s PCM multiplex equipment.

Primary Block
(American: Digroup)
A basic group of PCM channels assembled by time division multiplexing.

Note: The following conventions could be useful:

Primary block μ- a basic group of channels derived from 1544 kbit/s PCM multiplex equipment.

Primary block A- a basic group of PCM channels derived from 2048 kbit/s PCM multiplex equipment.

Time Division Multiplexing
Several information channels are multiplexed (time shared) over a single communication circuit by sampling each channel periodically and allocating each sample an assigned time slot in the circuit.

T1 Carrier System (North America)
PCM multiplex equipment using 8 digit μ-Law, 24 channels (time slot).

30 Channel Mux (U.K. & Europe)
CCITT recommended form PCM multiplex equipment. 8 digit A Law, 30 speech channels + 2 utility channels (32 time slots in all) transmission rate 2,048 kbit/s.

Transmultiplexer
An equipment which transforms signals derived from frequency division multiplex equipment to time division multiplexed signals having the same structure as those derived from PCM multiplex equipment and vice versa.

24 Channel Mux (U.K.)
Early PCM multiplex equipment: 7 digit A-Law, 1 signalling bit associated with each time slot, 24 channels (time slots), transmission rate 1536 kbit/s.

TIMING

Channel Time Slot
A time slot starting at a particular phase in a frame and allocated to a channel for transmitting a character signal and possibly in-slot signalling or other information.

Digit Time Slot
A time slot allocated to a single digit.

Frame Alignment
The state in which the frame of the receiving equipment is correctly phased with respect to that of the received signal.

Frame Alignment Signal
The distinctive signal used to enable frame alignment to be secured.

Frame Alignment Time Slot
A time slot starting at a particular phase in each frame and allocated to the transmission of a frame alignment signal.

Master Clock
A clock which generates accurate timing signals for the control of other clocks and possibly other equipments.

Mesochronous
Two signals are mesochronous if their corresponding significant instants occur at the same average rate.

Non-Synchronous Network
(Asynchronous Network)
A network in which the clocks need not be synchronous or mesochronous.

Signalling Time Slot
A time slot starting at a particular phase in each frame and allocated to the transmission of signalling.

Synchronous
Two signals are synchronous if their corresponding significant instants have a desired phase relationship.

Synchronous Network
A network in which the clocks are controlled so as to run, ideally, at identical rates, or at the same mean rate with limited relative phase displacement.

Time Slot
Any cyclic time interval which can be recognized and defined uniquely.

Timing Recovery
(Timing Extraction)
The derivation of a timing signal from a received signal.

Timing Signal
A cyclic signal used to control the timing of operations.

SIGNALLING

CCIS
Common channel interoffice signalling.

Common Channel Signalling
A signalling method using a link common to a number of channels for the transmission of signals necessary for the traffic via these channels.

Signalling
The exchange of electrical information (other than by speech) specifically concerned with establishment and control of connections, and management, in a communication network. May be transmitted by independent link, designed time slots, designation bit positions in a time slot or by "bit stealing" specific speech bit positions in the PCM codeword. In a transmission, system signalling may carry equipment status, routing, billing and testing data.

When referred to the line card of a digital switch, signalling includes-on hook/off hook status, ring trip, applying ringing, dialed digit information, test signals. Where ON CARD time slot assignment is performed, signalling also includes time slot identification.

Speech Digit Signalling
(sometimes called Bit Stealing)
Signalling in which digit time slots primarily used for the transmission of encoded speech are periodically used for signalling.

CODES

A-Law/or μ-Law Companded
8 bit PCM Binary code. The codes almost universally used for PCM digital switching and transmission. When a reference is made to PCM, it is almost invariably these codes which are being referred to (A-Law version in Europe and μ-Law version in North America).

Alternate-Mark Inversion Signal (AMI) (Bipolar Signal)
A pseudo-ternary signal, conveying binary digits, in which successive "marks" are normally of alternate, positive and negative, polarity but equal in amplitude and in which "space" is of zero amplitude.

HDB-3 Code - High Density Bipolar 3 Code
Here two consecutive ones of the same polarity are permitted (interrupting a zero sequence which is too long).These violation bits, moreover, are arranged to form an AMI sequence in itself. (See modified AMI).

Line Code
A code chosen to suit the transmission medium and giving the equivalence between a set of digits generated in a terminal of other processing equipment and the pulses chosen to represent that set of digits for the line transmission.

Modified Alternate Mark Inversion
An AMI signal which does not strictly conform with alternate mark inversion but includes violations in accordance with a defined set of rules.

PCM Binary Code
A pulse code in which the quantized values are identified by binary numbers taken in order.

Note: This term should not be used for line transmission.

Pulse Code
A code giving the equivalence between the quantized value of a sample and the corresponding character signal.

DIGITAL SYSTEMS

'Blocking' System
There are more telephones than through connection paths so dynamic channel allocation is needed on a demand basis. If all channels are busy, new calls are are blocked from completion or are delayed until a channel becomes available.

Connection
The circuits and equipment which together provide a communication path between two subscriber stations.

Digital Switching
A process in which analog signals are converted to digital signals and connections are established by operations on the digital signals. Alternatively, digitally transmitted signals are routed by operating on the digital signals directly without converting to analog.

'Non-Blocking' System
Each telephone has a guaranteed through connection when needed. This may be in the form of dedicated channels (fixed channel asignment) which guarantees any phone the same communication channel at any time.

STS Switch
Space Time Space Switch - large switch consisting of a time switch block between two space switch blocks.

Space Division
Use of different physical paths to transmit two or more channels (N.B. 'space division multiplex' is a contradiction in terms).

Space Switch (Abbrev.) Space Division Switch
Multiport switch in which ports are interconnected by use of different physical paths.

TST Switch
Time Space Time Switch - large switch consisting of a space block between two time switch blocks.

Time Switch (Abbrev.) Time Division Multiplex Switch
Multiport switch in which all ports have access to the same physical path on which transmitted data from individual ports are allocated unique time slots. Send and receive paths are connected by both accessing the same time slot. The path may be a serial data or parallel data highway.

PARAMETERS & UNITS

dB
Decibel - unit of measure of relative power level defined as $10\log_{10}(P_1/P_2)$ assunming R1 = R2 where P_1 and P_2 are the power levels.

dBm
Power in dB relative to 1 mW.

dBm0
dBm referred to or measured at a point of zero transmission level.

dBmp
dBm psophometrically weighed. Unit of power in dBm measured with psophometric weighting. Conversion is as follows:

$dBmp = 10\log_{10}pWp - 90$
$= dBa - 84$
$= dBm - 2.5$ (for flat noise 300-3400 Hz)

dBm0p
Circuit noise in dBm0 measured on a line with a noise measuring set having psophometric weighting.

dBr
dB relative to point of zero transmission level.

dBrn
(decibels above reference noise). Weighted circuit noise power in dB referred to 1 picowatt (−90 dBm) which is defined as 0dBrn. Type of weighting is indicated by next letter (see dBrnc).
Note: With 'C' message weighting, a 1mW 1 kHz tone will read +90 dBrn, but the same power with the noise randomly distributed over a 3 kHz band (300-3400 cps) will read +88dBrn.

dBrnc
Weighted circuit noise power in dBrn, measured on a line by noise measuring set with 'C' message weighting.

dBrnc0
Noise measured in dBrnc referred to zero transmission level point (0TLP).

$$dBrnc0 = dBrnc - 20 \log_{10} R_{LOAD}/600$$

Gain Level Linearity (U.K.)
See Gain Tracking Error.

Gain Tracking Error (N.A)
Gain Level Linearity
A measurement of the dependence of a device gain on signal level. The output signal is compared to the input signal (assuming unity gain) over a range of input signals. The variation of gain from a constant gain (determined at 0dBm input level) is the gain tracking error.

Idle Channel Noise
The total signal energy measured at the output of the device when the input of the device is grounded. Unless otherwise specified, this is a wideband noise measurement.

Load Capacity
(Overload Point)
In PCM, the level expressed in dBm0, of a sinusoidal signal the positive and negative peaks of which coincide with the positive and negative virtual decision values of the encoder.

Peak Limiting
In PCM, the effect caused by the application to an encoder of an input signal whose value exceeds the virtual decision values of the encoder.

Quantizing Distortion
The distortion resulting from the process of quantizing.

Quantizing Distortion Power
The power of the distortion component of the output signal resulting from the process of quantizing.

Signal to Distortion Ratio (S/D)
The ratio between the input signal level, and the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (by filtering for example).

Weighting Filters
Several different filters have been used to represent the transmission passband characteristics of different communication networks. The two most frequently used are C-message (N.A) and Psophometric (Europe) weighting filters.

MITEL

Application Note **MSAN-106**

An Introduction to Mitel DTMF Receivers

NOV. 1981

Dual-tone multi-frequency (DTMF) receivers have been built using various filtering techniques. The most recent relies on MOS/LSI for higher quality and reduced cost. LSI DTMF detection relies on algorithms developed both empirically and analytically. New generations of receivers are just emerging: miniature hybrid receivers are already available in volume production. General acceptance in the marketplace has resulted in an acceleration of the innovation and the pricing trends made possible by the latest advances in LSI technology.

DTMF Signalling

Introduced over 25 years ago, DTMF signaling (also known as Touch-Tone*, Tel-Touch, etc.) has been steadily gaining ground at the expense of dial-pulse signalling. Not only is a Touch-Tone telephone more convenient and more efficient to use, but it offers a higher reliability in the transmission of signals. As a result, signaling is no longer confined to telephony but has seen its domain expanded to various fields such as answering machines, radio communications, data transmissions and remote control.

The telephone handset generates a composite audio signal made of the superposition of two tones selected by line-and-column addressing of a keyboard. This scheme is shown in Figure 1.

These frequencies were chosen in such a way that neither their harmonics nor their intermodulation products fall in one of the tone bands. Separation between tones is typically 10%.

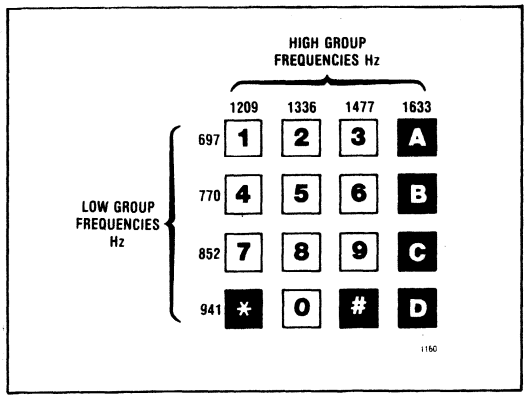


Fig. 1 DTMF Keypad Encoding

The fourth column of buttons (1633 Hz tone) is not usually present in today's telephone sets. However, it is available for future use. A 4 × 4 matrix of buttons is presently used in some military phones and is suitable for implementation in telephone sets intended for multiple functions such as financial transaction terminals, credit checking machines and some PBX or CBX systems.

The dual-tone signal is heard in the ear-piece and is sent over the telephone lines to the private branch exchange (PBX) or directly to the central office, where it must be decoded into the digit that it represents. The decoder circuitry — or receiver — will convert the DTMF signal to a binary format or to a 2-of-8 format. For the traditional dial-pulse equipment, a further conversion is needed to achieve a complete Touch-Tone to dial-pulse interface, allowing telephone companies to offer subscribers Touch-Tone service in areas where the equipment is not compatible. Such an application is termed a tone-to-pulse converter.

Before 1974, a number of techniques were used to achieve DTMF detection. Passive filters, using LC networks for each frequency, can still be found in some installations. When integrated operational amplifiers became more readily available, the designers switched to active filters using IC's and RC networks. With the advent of the phase-lock-loop in IC form, new designs were introduced embodying this approach.

Every solution outlined so far had technical or cost-related disadvantages. Advances in MOS/LSI technology have made it possible to solve the problem of DTMF decoding at considerable cost savings.

Digital DTMF Detection

The basic method of discriminating various frequencies from each other using digital logic is to relate the number of cycles of some reference clock signal to each period of the unknown frequency. Typically, the DTMF signal is sent first through a band-splitting filter which separates the high- and low-band frequencies (Figure 2). Each frequency is then square-shaped and processed separately. The problem consists of establishing whether a frequency is recognizable as a DTMF tone, considering that it is within a certain fre-

*Touch-Tone is a registered service mark of AT&T.

quency tolerance, or that it is a mere simulation of a true DTMF tone, such as produced by speech. As a result, the designer is faced by a dilemma: if the "accept" criteria are too relaxed, DTMF tone-pairs are quickly recognized as valid, and so are speech segments which simulate a real DTMF signal. This is referred to as "talk-off". Now, if the "accept" criteria are too strict, detection time is inordinately stretched and the receiver is no longer in compliance with timing requirements. In other words, if detection time is fixed this becomes a compromise between:

A. Tolerance to received-tone imperfections and noise.

B. Immunity to tones simulated by speech (talk-off).

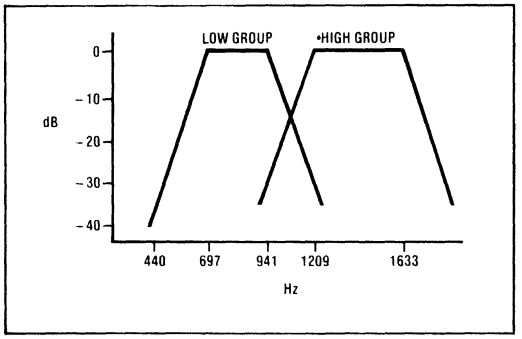


Fig. 2 Idealized Bandsplit Characteristic

Modern receiver design can successfully deal with this problem by optimizing both the front-end filtering and the digital detection algorithm. Such a product — the MH88305 — has been developed by Mitel to serve the most exacting requirements of DTMF reception, as seen in central office applications. The MH88305 is a self-contained hybrid DTMF receiver measuring 1.5 x 2.5 x 0.25 inch (3.8 x 6.3 x 0.63 cm). No external components are needed to operate this receiver (even the time-base crystal is enclosed), although the addition in each case of a single resistor or capacitor allows the designer to modify three of the device parameters: detect time (time to detect the presence of a valid tone-pair); sensitivity (minimum acceptable signal level); and twist acceptance (degree of mismatch between the amplitudes of the two tones of a pair). The unit connects directly to the telephone line. Talk-off immunity is excellent: less than five "hits" on the Mitel test tape CM7291. Error rate is typically better than 1 error in 100,000 applied tones and third-tone tolerance meets the CEPT recommendation of (A-16) dBm for a swept in-band tone applied simultaneously with undeviated signal frequencies. Power consumption at 5 V is a mere 50 mW and input sensitivity can be adjusted down to −42 dBm giving a maximum dynamic range of 55 dB as illustrated in Figure 4.

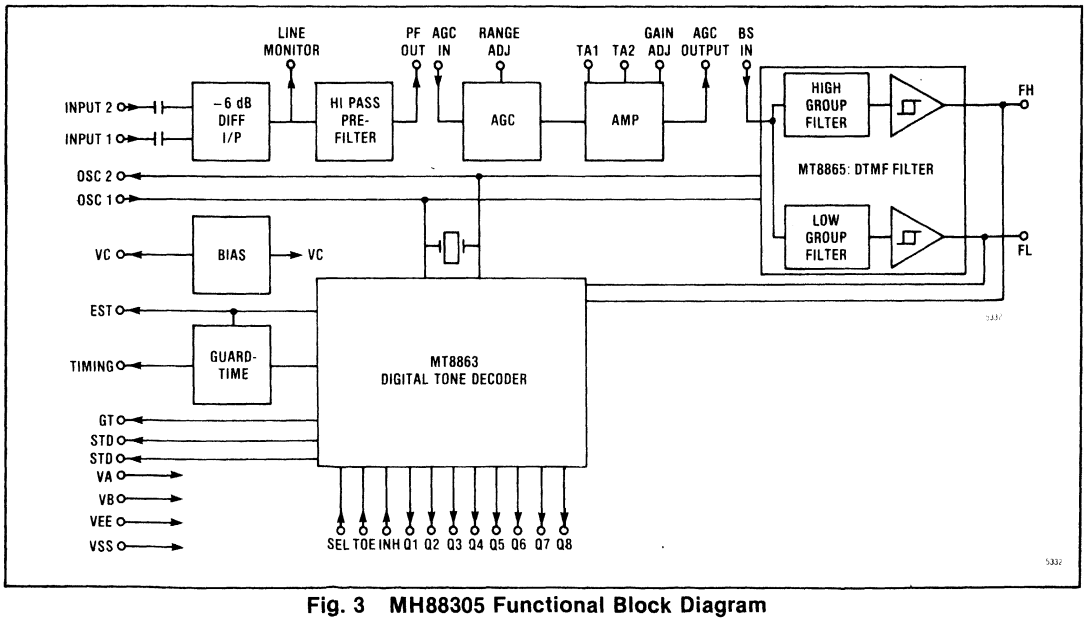


Fig. 3 MH88305 Functional Block Diagram

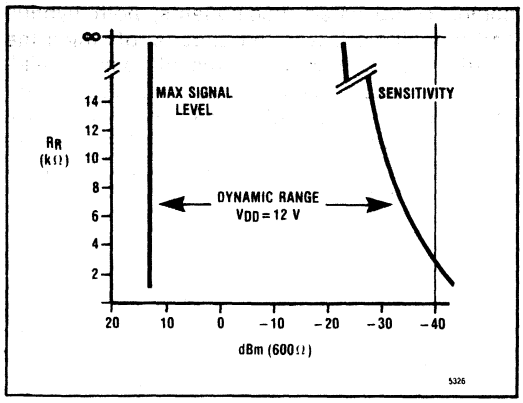


Fig. 4 MH88305 Input Signal Characteristics

DTMF Receiver Specifications

The worst case specifications of a DTMF receiver are typical of Central Office requirements:

Input Dynamic range	: – 26 dBm to + 6 dBm
Twist (V_{FH}/V_{FL})	: – 8 dB to + 4 dB
Dial Tone	: 350 Hz mixed with 440 Hz
Tone Burst (min.)	: 40 ms ON, 40 ms OFF
Repetition rate (max.)	: 12 pps
Valid tone accept	: ± 1.5%
Invalid tone reject	: ± 3.5%
Signal-to-noise ratio	: 16 dB
Silence gap bridging	: 15 ms

For other applications, such as keyphone systems, the specifications are less stringent. No dial tone is used. Little twist exists on the line. In this case, some circuitry — such as the dial tone rejection filter — can be omitted.

Digital Detection Algorithm

There are several MOS/LSI devices on the market which perform DTMF digital detection. Some are even proprietary to companies involved in the manufacture of complete DTMF receivers, and thus are not sold as chips. All these devices have a basic tenet in common: digital period-counting relying on a zero-crossing detector. Little difference exists in the choice of tone bandwidths. The main divergences lie in the choice of criteria leading to accept or reject a tone-pair. It is instructive to discuss one of the more general techniques.

In order to reduce the overall system cost, the designer tries to shift the design complexity to the contents of the LSI device rather than the front-end filtering which is typically costlier. Thus, when the band-splitting filters have less-than-ideal attenuation, the separated tones will carry a residue from the other band. This, in addition to random noise, results in jitter of the zero crossings (Figure 5).

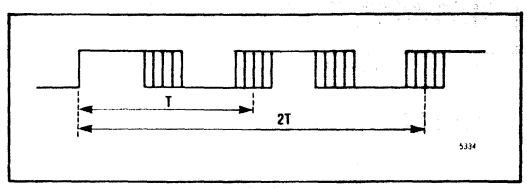


Fig. 5 Zero-Crossing Jitter

Averaging several pulses eliminates most of the jitter effects. However, it also allows easier speech simulation of tone-pairs. In order to improve speech rejection, single-period counting is made to concur with the counting of several periods. Such a technique is used in the Mitel MT8860 decoder and its variants, the MT8862 and MT8863. The Mitel MH88305, which uses the MT8863 digital decoder, also uses an LSI bandsplit filter, the MT8865. This device uses switched-capacitor filters implemented in Mitel's double-poly ISO²-CMOS™ technology.

The MT8860/8865 chip pair integrates an entire functional receiver, the external circuitry required being dependent on the user's system environment and specification. Typical enhancements might be a differential input amplifier for line interfacing; prefiltering for extra dial-tone rejection; agc circuitry for extended dynamic range. All of these enhancements are incorporated into the MH88305 hybrid.

In addition to the digital detection algorithm, Mitel tone receivers incorporate a further validation check during a period termed the guard-time. This time is user-accessible since it is set by an external RC time constant and it offers the designer further flexibility in optimizing receiver performance while complying with his particular system timing requirements. Use of the guard-time feature is fully described in the data sheets of the devices referenced here; Figure 6 tabulates the four main system timing parameters which may be adjusted.

TONE-PAIR RECOGNITION	TIMING CONDITION*
SHALL EXIST MAY EXIST SHALL NOT EXIST	$T_P > t_{REC}$ $\overline{t_{REC}} \leq T_P \leq t_{REC}$ $T_P < \overline{t_{REC}}$
SHALL CEASE MAY CEASE SHALL NOT CEASE	$T_A > t_{ID}$ $t_{DO} \leq T_A \leq t_{ID}$ $T_A < t_{DO}$

TYPICAL VALUES OF SYSTEM PARAMETERS	
t_{REC}	< 38 ms
$\overline{t_{REC}}$	> 20 ms
t_{ID}	< 38 ms
t_{DO}	> 20 ms

*T_P = THE CONTINUOUS PRESENCE OF A VALID TONE-PAIR.
T_A = THE CONTINUOUS ABSENCE OF A VALID TONE-PAIR.

Fig. 6 Typical System Timing Constraints

Future LSI Receivers

Work is being conducted at Mitel to develop still smaller and more cost-effective receivers. The first of the new generation monolithic receivers now under development is the MT8870, which combines the filter and decoder functions in one chip contained in a compact 18-pin package. Gains in performance as well as reductions in cost and size are expected from this ISO²-CMOS device, making possible the use of DTMF receiver technology in many new application areas.

The analog functions implemented in today's hybrids (e.g. differential front end with sensitivity control; agc for wide dynamic range) are also susceptible to integration using the analog capabilities of the ISO²-CMOS technology. Future developments will therefore be able to place more and more of this analog circuitry onto the chip, for an even more compact receiver solution.

This development constitutes the last of five DTMF receiver generations:

I. LC, PLL and active filter receivers.

II. MOS/LSI detector chip receivers.

III. Hybrid self-contained receivers.

IV. Two-chip CMOS receivers.

V. Single-chip CMOS receivers.

The dividends of this progression are well-known today:

— better performance;

— higher reliability;

— smaller system size;

— lower system cost.

While the single-chip receiver may be said to complete in a sense the evolution of the DTMF receiver, this marks the starting point for even more complex subsystem components, both hybrids and monolithic integrated circuits, of which the DTMF receiver function represents only a building-block. Such components, in common with other areas in which VLSI is used to its limits, will necessarily be highly specialized to the intended application (e.g. mobile radio, remote control receivers, data receivers, etc.).

Pricing Trends

The telephone operating companies have accelerated the conversion of their equipment to tone dialing. The reason for this is that, apart from the added reliability and convenience of DTMF signalling, the cost of DTMF installation is quickly amortized by the additional revenue available on a DTMF line. Advances in design and the adoption of MOS/LSI has driven the price lower every year. Actual numbers have been used to generate the price curve shown in Figure 7. Future pricing is predicated on advances in technology and pricing trends in both the telecommunications and the semiconductor industries.

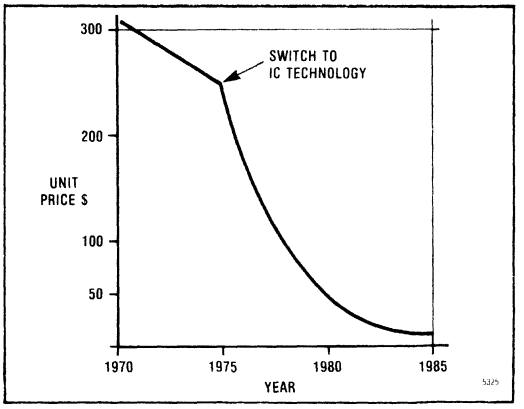


Fig. 7 DTMF Receiver Pricing Trends

According to this curve, a sub-$10 receiver is already projected for 1985, even though inflation is working in the opposite direction. And to stress the point, we are referring to a finished and testing product in a single compact package.

Four main factors account for this phenomenon:

1. Increase in competition between DTMF receiver manufacturers.
2. Switch to MOS/LSI technology, thus taking advantage of semiconductor pricing curves.
3. Acceptance by the telephone companies of newer technologies and reduction of the procurement cycle.

4. Emergence of new applications for DTMF signalling.

An Alternative to Modems?

The emerging new application areas for DTMF signalling deserve some special consideration, as it is these applications which are today being stimulated by the cost-effectiveness of the DTMF approach, and which will in turn benefit as growing volume pushes receivers further down the pricing curve.

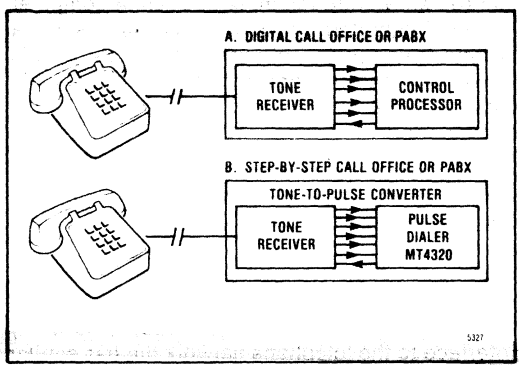


Fig. 8 Conventional DTMF Receiver Applications

Today, DTMF receivers are found primarily in central office and PABX equipment, where the two primary applications are in the receiver proper and in tone-to-pulse converters (Figure 8). Diminishing costs are now permitting the use of receivers at the subscriber end of the installation, transforming the standard voice channel into an economical means of data transmission. The attractiveness of this approach lies in the fact that data may be entered through any standard (DTMF) telephone keypad, eliminating the need for modems, acoustic couplers and other specialized interfacing equipment. Without specialized subscriber equipment, DTMF data transmission is one-way only, and has limited transmission speed and character-set compared to modem solutions, but many applications exist where these shortcomings do not impose a limitation on system performance. Such applications would be characterized as requiring only numeric data (plus possibly the 2 to 6 extra codes embodied in the DTMF specification); as requiring only a moderate data rate (e.g. when data entry speed is limited by speed of operator input); and as being either 'one-way' or else susceptible to some alternative means of data reception (such as achieved by voice synthesis). Many applications of this sort are emerging in fields extending well beyond the telecommunications industry itself.

New DTMF Receiver Applications

DTMF technology lends itself to a variety of remote-control applications, in the home (control of heating, appliances, pay-television, etc.) and in industry (control of remotely located installations such as data-loggers, radio transmitters, pumping stations, etc.). The only added expense is at the

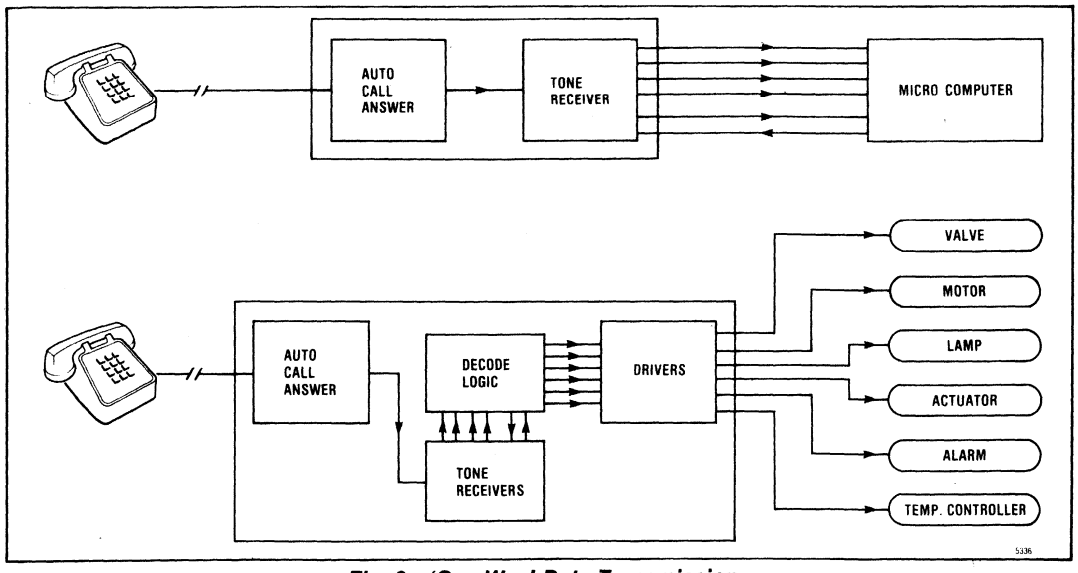


Fig. 9 'One-Way' Data Transmission

controlled location (auto-answer, receiver, security logic and controller); the controlling location may be any DTMF telephone, including call-boxes and radiotelephones. Certain of these remote-control applications also benefit from the low power consumption of CMOS technology.

Remote data-entry is an application which benefits from the concept of data input through any telephone. For example, a salesman on the road may enter his orders directly into a central computer from any remote location without specialized portable equipment, eliminating equipment and maintenance costs and enhancing user convenience. All that is required is a DTMF receiver installation at the central computer, with the appropriate interface software. A similar application might allow an individual to order goods via his telephone keypad.

Remote-control and data-entry are both applications requiring essentially 'one-way' data transmission (Figure 9), although some audible response would normally be implemented to confirm to the user that correct data has been entered. A more sophisticated approach (Figure 10) must be taken where the called location is required to give a more detailed response. This concept is typified by an application such as credit-card verification, where a central computer must provide a confirmation number in response to a keyed-in card number. The obvious solution is voice-synthesis, which maintains the cost and convenience advantage of eliminating specialized equipment at the point of sale. This technology may also bring some of the functions of today's 'electronic bank tellers' directly into the home, again without adding subscriber equipment.

One of the installations which may conveniently be controlled from a remote telephone is the answering machine. The user may command replay of messages and update his own recorded message at will. The machine may also be programmed to store messages intended for specific callers only and activated by a pre-arranged code keyed in by the caller. An economical all-solid-state answering machine may follow the concept of storing a 'follow-me' telephone number updated remotely through DTMF signalling and played back to callers via voice synthesis.

One of the more exciting of domestic applications is the home communications system, which brings together telephones, intercom, appliance control, answering machine and home computer in one integrated network. Accessing such a system from any remote telephone clearly adds flexibility to the concept, and might even be applicable to two-way communication between home-computers.

Although some of the major benefits of DTMF signalling stem from an extension of the utility of existing telephone installations, its proven reliability and low cost allow it to be used in any multiple-location signalling network (Figure 11) such as might be found in industrial control systems. The system does not necessarily have any interface to the telephone network but has similar requirements in that it must operate reliably over long distances in the presence of noise and other disturbances. In such an off-line network, the designer has the flexibility to adjust signalling parameters such as tone durations and amplitudes, to conform to his specific application needs.

DTMF signalling is also being extended into mobile-radiotelephone applications (Figure 12). This allows the radio link to 'plug-in' transparently to the telephone network, simplifying the interface, and the same DTMF encoding may be used to transmit channel and other information to and from the mobile installation. Noise and talk-off

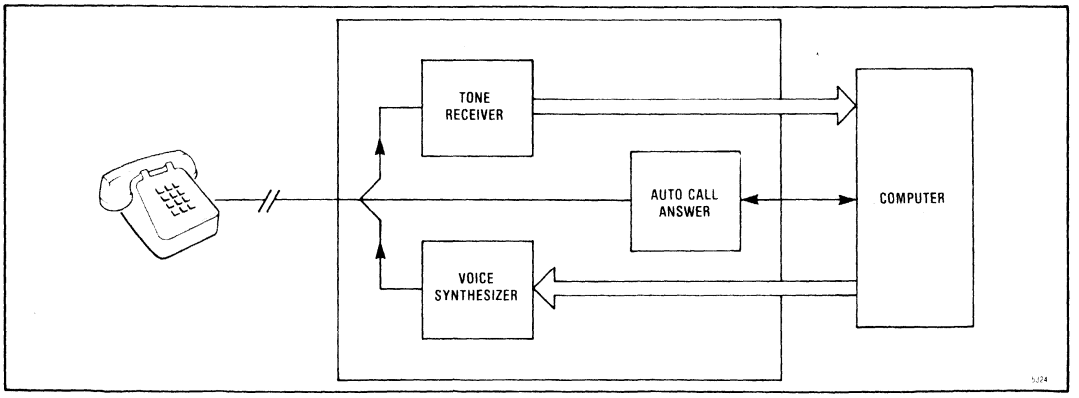


Fig. 10 'Two-Way' Data Transmission

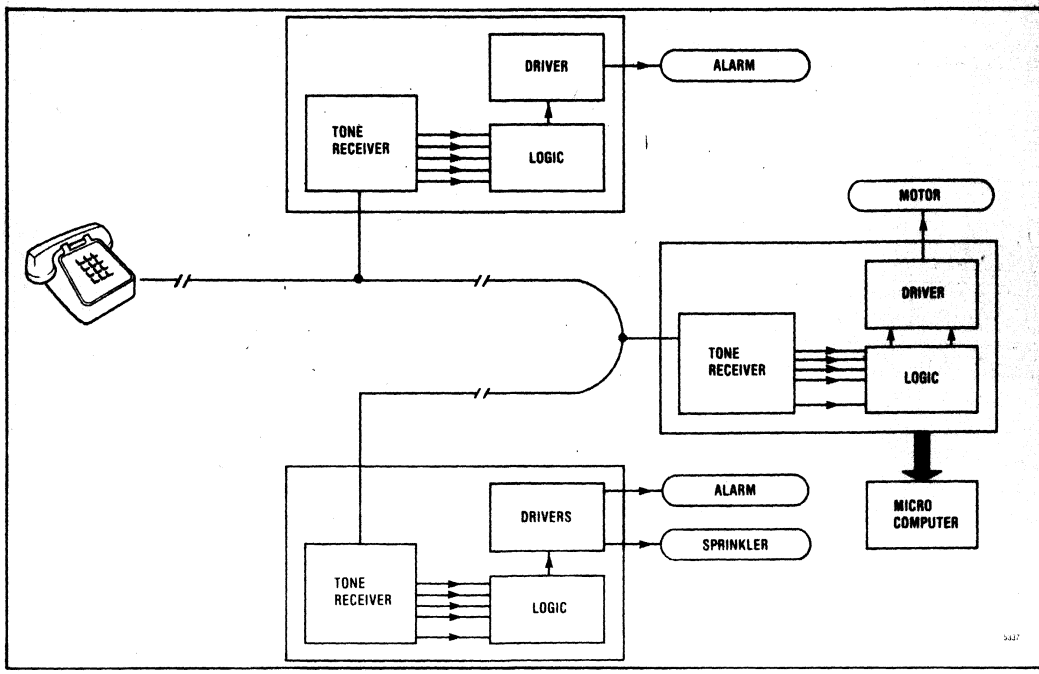


Fig. 11 Single Line Multiple Location Control

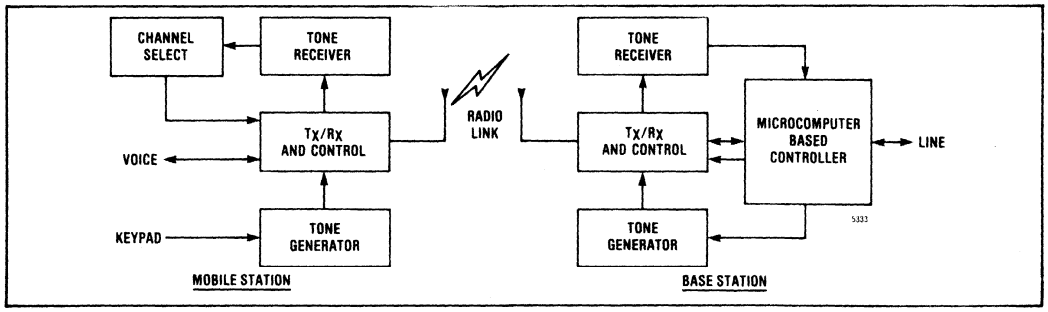


Fig. 12 Mobile Radiotelephone Applications

considerations are rather different in radiotelephone networks, and adjustment of timing parameters can be made to optimize performance in this environment.

Conclusion

A description of the DTMF signalling medium has illustrated its main features both for conventional dialing applications and for certain data transmission and remote control applications. An overview of the "state-of-the-art" as illustrated by the Mitel DTMF receivers has shown the benefits of performance, cost and size which are now available.

Usage of DTMF signalling is enjoying an explosive growth driven primarily by three interacting factors:

1. Increased cost-effectiveness due to LSI implementation.
2. General availability of an input medium (the subscribers telephone).
3. Existence of complementary technologies (such as voice-synthesis).

It remains to be seen what other new applications will be stimulated by the availability of the DTMF signalling medium.

MITEL

Application Note MSAN-107
Understanding and Eliminating Latch-Up in CMOS Applications

PM AUGUST 1982

Contents

Introduction

The purpose of this Application Note is to assist both those designers who are familiar with the use of CMOS devices as well as those considering CMOS designs for the first time.

Attracted by the many advantages offered by CMOS devices, designers using them for the first time are often unaware of, or are overly sensitive to the phenomenom of latch-up. Understanding a few facts will resolve both of these situations. Basically speaking, any analog or digital device fabricated in one of the many CMOS processes available, can be made to latch-up if stressed severely enough. However, when properly applied, CMOS devices are quite insensitive to actual conditions that exist in most systems. Further, if a few simple precautions are taken at the design stage, then latch-up can be completely avoided.

Latch-up is defined as the creation of a low impedance path between the power supply rails by the triggering of parasitic, four-layer bipolar structures (SCR's) inherent in CMOS input and output circuitry. In this note, details of these SCR structures are examined in the context of Mitel's ISO-CMOS technology. By developing an understanding of the aspects of circuit and system design related to the triggering of these SCR's, design methods and guidelines can be acquired to greatly reduce the probability of latch-up occurrence. By implementing the suggested techniques and circuitry, the designer can gain the advantages of CMOS circuitry without major concern about latch-up related problems.

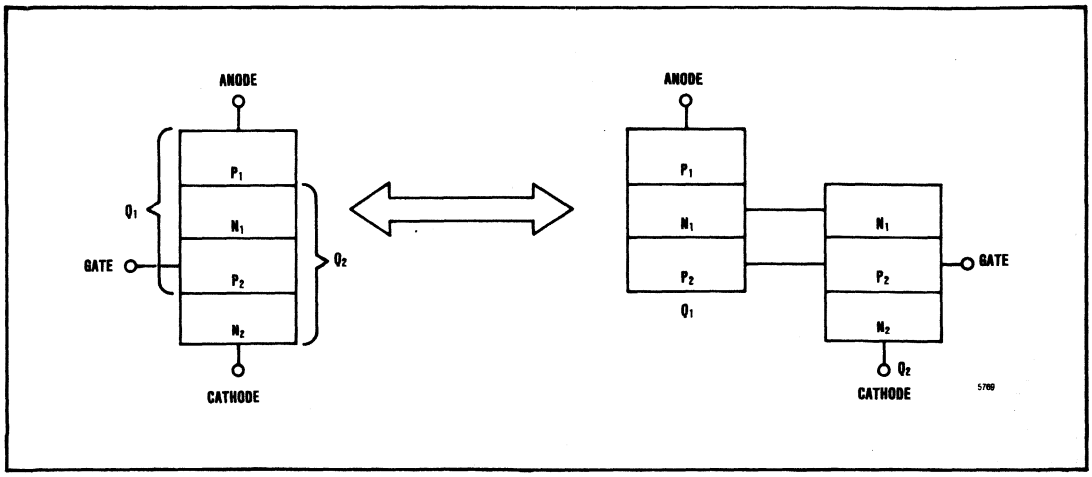


Fig. 1 Four-Layer SCR Structure

Semiconductor Device Considerations

Background on SCR's

Prior to discussing latch-up in CMOS devices, it is advantageous to briefly review the basic theory of SCR operation. This will be helpful in developing an understanding of the relationships between external circuit and system conditions and the resultant triggering of latch-up in CMOS devices. The basic SCR structure is that of a four-layer device as shown in Fig. 1. The device has three terminals: Anode, Cathode and Gate. Fig. 2 shows how the SCR can be modelled with two bipolar transistors, one NPN and one PNP. In the normal mode of operation, the SCR is turned on by injecting sufficient current into the base of Q_2 to turn this transistor on. When this is done, Q_2 begins to draw collector current via the base-emitter junction of Q_1. As a result Q_1 also turns on, injecting additional current into Q_2's base. This in turn causes Q_2 to turn on harder, supplying more base current to Q_1. This positive feedback arrangement sustains conduction, and ensures that the SCR continues to conduct even if the gate current is interrupted.

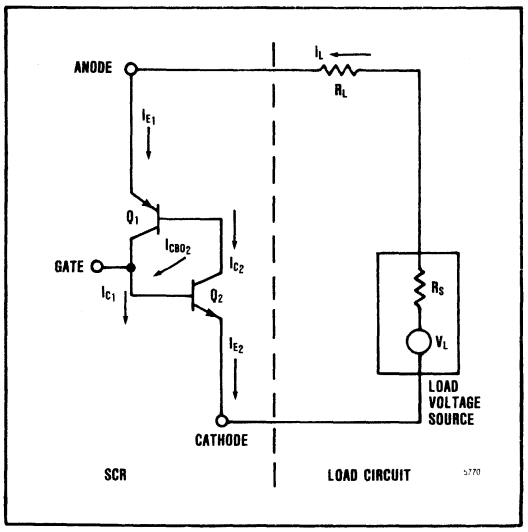


Fig. 2 Bipolar Model of an SCR

The device will remain in this latched state indefinitely. To turn the SCR off, one of two things can be done. If the voltage applied across the SCR is reduced to the point where Q_1's base-emitter junction turns off (V_{Sus}), then Q_2 will be starved of base current and the SCR will turn off. Alternatively, if the current through the SCR is reduced below its holding current then it will also turn off. The holding current is the minimum current required to sustain conduction and is a function of the physical dimensions of the device and the transistor gains (Fig. 3). As mentioned, this is the way that the SCR is controlled in normal applications. There are various other ways that an SCR may be triggered. These must be examined as they are directly related to latch-up problems.

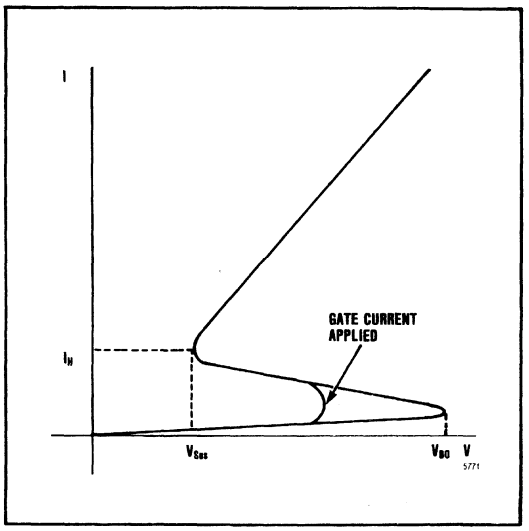


Fig. 3 SCR Current-Voltage Characteristic

Looking at Fig. 2, it can be seen that the load current and the two emitter currents of Q_1 and Q_2 are all equal. Also the load current is equal to the sums of the two collector currents and a leakage current from Q_2's collector to its base (I_{CBO_2}). It can be shown (refer to Appendix) that:

$$I_L = I_{CBO_2} \left[\frac{(1 + \beta_1)(1 + \beta_2)}{(1 - \beta_1 \beta_2)} \right] \quad (1)$$

Where β_1 and β_2 are the current gains of Q_1 and Q_2 respectively.

Normally, with no base current supplied to Q_2, the load current will be small since the leakage I_{CBO_2} is small, as are the current gains (β_1, β_2) at this low value of collector current. If, however, the current gains increase to the point where the product, $\beta_1\beta_2$, approaches unity, then the load current will become very large, limited only by the load impedance, the series impedance of the SCR, and source impedance of the power supply. There are various applied conditions that will cause this to happen. Increasing the load voltage beyond the

breakover voltage, V_{BO}, will have this effect. As the anode-cathode voltage across the SCR increases, the collector-emitter voltages of Q_1 and Q_2 also increase. This corresponds to increases in the collector-base reverse biases. The collector-base junctions of the two transistors are physically the same area, the N_1-P_2 junction (Fig. 1). As the reverse bias increases, the energy of the minority carriers increases causing more carriers to be dislodged, which in turn pick up energy. This continues until the junction undergoes an avalanche breakdown resulting in an increase in the collector currents of Q_1 and Q_2. The resulting increase in β_1 and β_2 cause the SCR to latch on.

A very rapid change in the anode to cathode voltage of an SCR can also cause it to trigger. This is known as the "dV/dt" effect. The N_1-P_2 junction, being reversed biased, exhibits a capacitance. This capacitance varies with the reverse bias voltage applied across the junction. Hence the current through the capacitor is described by:

$$\frac{d(C_j V_{AK})}{dt} \quad (2)$$

$$= \frac{C_j\, dV_{AK}}{dt} + \frac{V_{AK}\, dC_j}{dt} \quad (3)$$

The junction capacitance, C_j decreases with increasing reverse bias and hence the second term of equation (3) is negative. If, however, the rate of change of applied voltage is large enough, the first term of equation (3) will dominate and the current through the SCR will increase. If the current increases sufficiently to cause the $\beta_1\beta_2$ product to approach unity, then the SCR will latch on.

The effects of temperature must also be noted at this point. Increasing temperature will cause an increase in both the leakage current through the SCR and in the current gains β_1, β_2 of the two bipolar transistors. As such, the magnitude of the driving force required to turn the SCR on will decrease with increasing temperature. In other words, the SCR will be more easily triggered as temperature increases for any of the triggering mechanisms described.

Corollaries exist between each of the three methods of turning an SCR on as described, and the ways in which the parasitic SCR structures of CMOS devices are triggered. The normal mode of triggering an SCR is by injecting current into its gate terminal. This corresponds to forcing current into the inputs or outputs of a CMOS device by applying voltages that go outside of the power supply rails. This is by far the most common form of latch-up triggering. The avalanche breakdown mechanism described also applies directly to CMOS devices, although its occurrence is far less prevelant. Excessive voltage on the power supply pins, whether continuous or transient, may result in latch-up occurrence. It is also theoretically possible to trigger parasitic SCR devices by the dV/dt method as a result of high speed transients on the supply rails. However, this will rarely happen in a real application. Each of these triggering methods will be examined in the next section in the context of the ISO-CMOS topology for both the output and input structures.

Parasitic Bipolar Structures in the ISO-CMOS Topology

As with any CMOS technology, ISO-CMOS contains certain parasitic bipolar structures associated with its output devices and input protection circuitry. These parasitic transistors are interconnected in such a way as to form four-layer devices. As such, SCR devices are present at both the inputs and outputs of ISO-CMOS circuits. These devices are normally in their off state and will remain off as long as the absolute maximum ratings of the devices are not exceeded.

Output SCR Structures

A typical ISO-CMOS output driver contains one N-channel MOSFET with its source tied to V_{SS} and one P-channel MOSFET with its source tied to V_{DD}. The drains of the two transistors are connected together to form the output and the gates are commoned to form the input (Fig. 4). The fabrication of these transistors in close proximity results in the formation of a parasitic SCR connected directly across the power supply rails. When triggered, this SCR presents a low impedance to the power supply causing excessive current to flow.

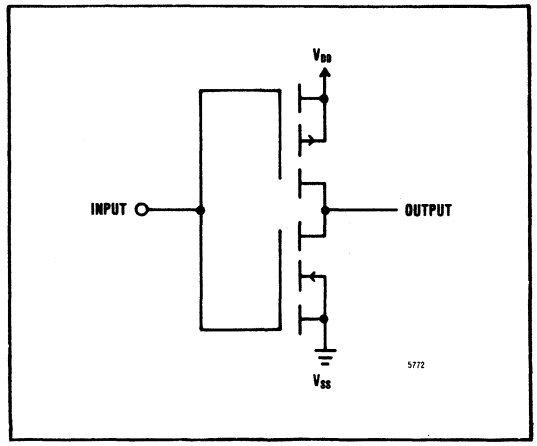


Fig. 4 Typical Output Circuit

This situation is potentially destructive, resulting in damage to bond wires or metal supply tracks on the die due to localized overheating. The SCR is formed as follows. A vertical NPN transistor results from the fabrication of the N-channel device. The N− substrate serves as the collector and is biased at V_{DD}. The P− well acts as the base and the source and drain N− diffusions are the emitters of the transistor. One emitter is tied to V_{SS} and the other to the output. A wide base lateral PNP transistor is formed when a P-channel device is located close to an N-channel transistor. The P-channel source and drain diffusions are two emitters of the transistor: one tied to V_{DD} and the other to the output. The N− substrate acts as the base and hence, is in common with the collector of the vertical NPN. The P− well is the collector of the PNP which is also base of the NPN. Due to the shared diffusions, the vertical NPN and lateral PNP transistors are effectively connected as an SCR (Fig. 5). This parasitic SCR is connected directly across the supply rails. Hence, when triggered, it can cause excessive current to flow. The SCR is normally turned off for nominal operating supply voltages and with all output voltages within the power supply limits. This SCR may be externally triggered causing the output structure to latch-up. The triggering mechanism can be any one of those mentioned in the previous section.

Output voltages being forced outside of the power supply limits is the most common cause of output latch-up. Two parameters are defined at this point for use in subsequent discussions. These are I_{LU} and V_{LU}. I_{LU} is the current which must flow through the output structure to cause latch-up to occur. V_{LU} is the voltage excursion outside of the power supply rails at the output pin that results in I_{LU} flowing through the output structure. In other words, I_{LU} and V_{LU} are the conditions at the output pin that will result in latch-up triggering. These same parameters also apply to input latch-up (see next section). Consider first an output voltage which goes below V_{SS} by more than V_{LU}. This causes the P− well to output base-emitter junction of the vertical NPN transistor to become forward biased. Since this acts as the SCR gate, triggering occurs. Current is pulled from V_{DD} through the lateral PNP and is injected into the P− well, causing a localized drop across this diffusion. This voltage drop will forward bias the base-emitter junction of the NPN which is referenced to V_{SS}. Once this occurs, latch-up will be sustained and a low impedance path is created from V_{DD} to V_{SS}.

A note must be taken here in regard to the amount of over-voltage required to trigger latch-up. In the above paragraph, it was mentioned that voltages exceeding the supply rails by more than V_{LU} will cause a current I_{LU} to flow and hence trigger latch-up. The guaranteed values quoted in the data sheet are 0.3V and 10mA respectively for these parameters. These limits are used in production testing and hence, appear in the Absolute Maximum Ratings for MITEL devices. In practice, it is more likely to require from 0.6V to 2V of over-voltage and from 50 to several hundred milliamps of current to cause output latch-up to occur. For input latch-up to occur, it can take several volts of over-voltage and similar currents to induce latch-up due to the series resistance of the input protection circuitry (Fig. 6).

When the V_{DD} supply rail is exceeded by a voltage greater than V_{LU}, a similar set of events occurs. In this case, the output to substrate base-emitter junction of the lateral PNP becomes forward biased. Collector current from this transistor

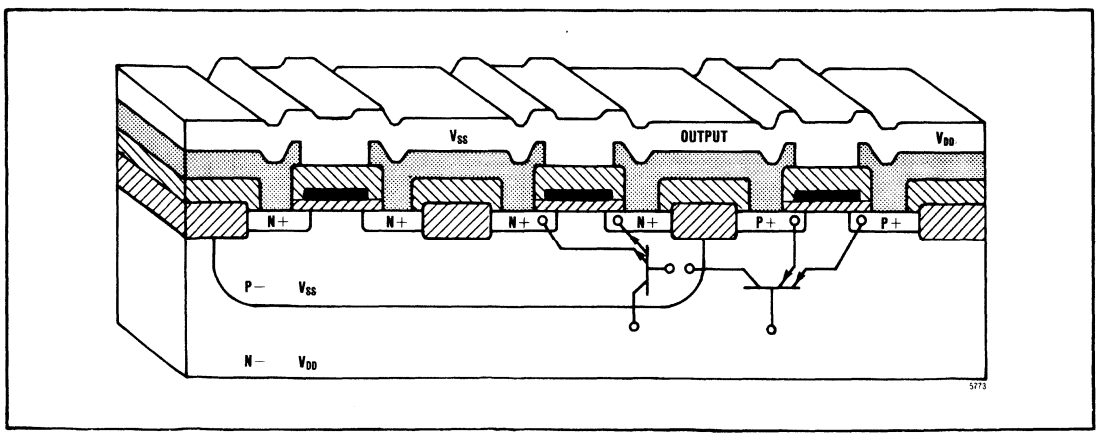


Fig. 5 Output SCR Structures

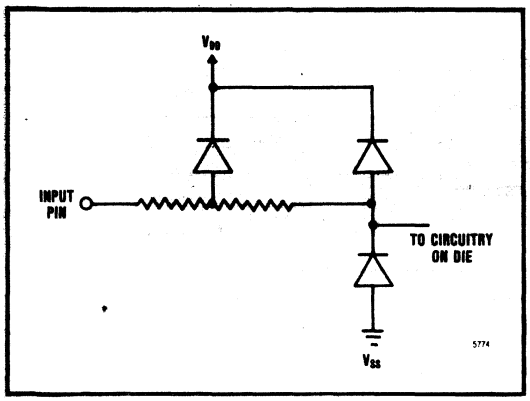


Fig. 6 Input Protection Circuit Schematic

is injected into the P− well, again causing a lateral voltage drop. This voltage drop causes the P− well to V_{SS} referenced base-emitter junction of the NPN to become forward biased. This transistor's collector current, pulled from the substrate, causes a lateral voltage drop across the substrate. This voltage drop, in turn, will forward bias the V_{DD} to substrate base-emitter junction of the PNP. Thus, latch-up will be sustained even if the output overvoltage condition is removed and a low impedance path again exists between V_{DD} and V_{SS}.

There are two other causes of output latch-up that are less likely to occur, but nonetheless must be noted. The first of these is the result of overvoltages on the power supply pins. Excessive voltage between V_{DD} and V_{SS} (i.e. greater than the absolute maximum rating) can cause an avalanche breakdown of the reverse biased substrate to P− well collector base junction of the bipolar transistors. This will cause the SCR to trigger as outlined in the previous section. The second triggering mechanism will be apparent in very few systems. Very fast voltage spikes on the power supply rails can induce a "dV/dt" triggering of the SCR, also as outlined earlier. This can potentially result in circuit damage by transients which in themselves would not have sufficient energy to cause damage due to localized power dissipation. Once triggered, the SCR may remain latched on until the supply voltage is reduced below its sustaining voltage or if the current is reduced below its holding current.

Input SCR Structures

Parasitic SCR structures can also result due to the fabrication of CMOS input protection circuitry. The ISO-CMOS input protection circuit schematic is shown in Fig. 6. As shown, there is a distributed diode connected to V_{DD} and another diode to V_{SS}. The series resistor is primarily intended for static protection, but also provides latch-up protection. The diodes are connected together at the input node. An SCR structure results when the V_{DD} referenced diode is fabricated in close proximity to an N-channel transistor (Fig. 7) or when the V_{SS} referenced diode is located close to a P-channel device (Fig. 8).

It is important to note here the difference between input and output SCR structures. The output SCR was connected directly between V_{DD} and V_{SS}, and hence, is more likely to be destructive once triggered. The input SCR structure is connected from the input node to one of the supply rails. Thus, for an input to remain latched, the circuitry driving the input must be capable of supplying the sustaining current of the SCR. For this latch-up to be destructive, the input driver must be capable of supplying large amounts of current. A potentially more dangerous situation occurs when a complimentary transistor, to the one forming the SCR, is located nearby. A secondary SCR structure results from this and it is connected across the supply rails (Figs. 7 and 8).

Consider the V_{SS} referenced diode situation first. The source and drain diffusions of the P-channel

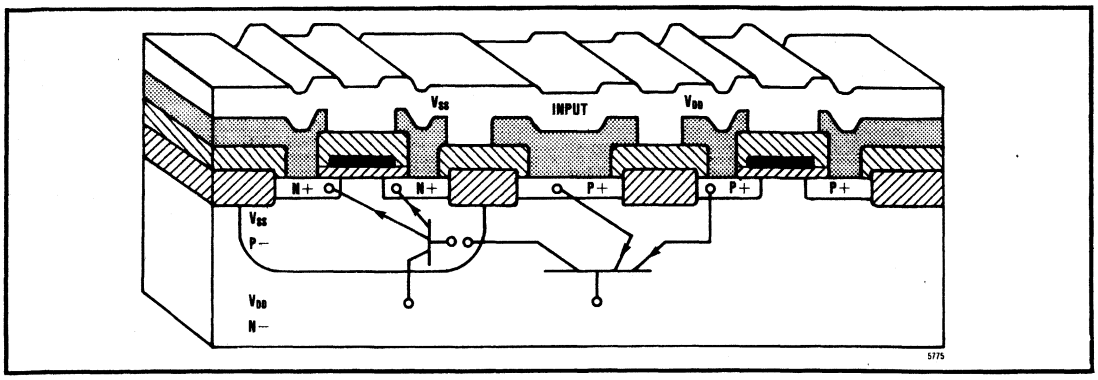


Fig. 7 Input SCR Structure with V_{DD} Diode

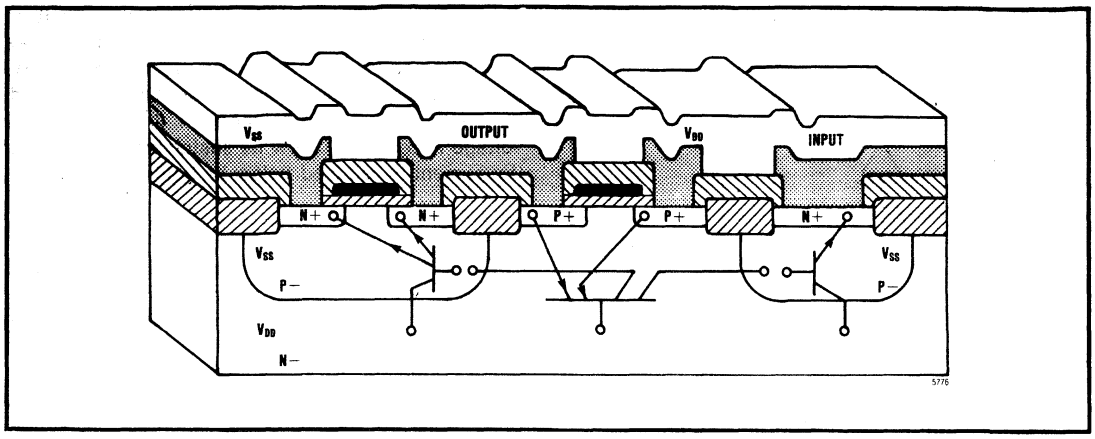


Fig. 8 Input SCR Structure with V_{SS} Diode

TABLE 1
MD74SC540AC Latch-Up Inducing Voltages and Currents

Forced I/O Condition	Latch-Up Inducing Conditions	
	V_{LU} (Volts)	I_{LU} (mA)
Outputs above V_{DD}	1.9	200
Outputs below V_{SS}	1.0	90
Inputs above V_{DD}	1.9	80
Inputs below V_{SS}	25.0	25

transistor form the emitters of a lateral PNP transistor. The substrate acts as the base and the P− diffusion of the diode is the collector. This diode, with the substrate, forms a vertical NPN transistor. The two transistors are interconnected as an SCR due to common diffusion areas. If an applied input voltage is below V_{SS} by more than V_{LU}, then the gate-cathode junction of the SCR will become forward biased and turn the SCR on. This latch-up condition will continue as long as this input condition persists or if the input circuitry can supply the minimum holding current. As mentioned, a potentially more hazardous situation can develop if an N-channel transistor is also located nearby. The P− well of this transistor serves as a second collector of the lateral PNP transistor. When the input voltage goes negative, the gate of the SCR is turned on as mentioned. However, this second collector now injects current into the P− well causing a second SCR structure to latch on. This device is connected across the power supply rails and hence, can be destructive. This same situation can result with the V_{DD} referenced protection diode. In this case, the SCR structures will be triggered by voltages which exceed V_{DD} by more than V_{LU}.

As was mentioned earlier, the actual values of V_{LU} and I_{LU} are typically much greater than the 0.3V and 10mA limits on the data sheets. Table 1 shows some of the numbers pertaining to the current production version of the MD74SC540AC, one of MITEL's Octal Interface devices. As can be seen it requires voltages from 1.0V to 1.9V and currents from 90 to 200mA to trigger output latch-up. On the input side, it requires 1.9V for V_{LU} and 80mA for I_{LU} in the V_{DD} case. For the V_{SS} case, I_{LU} is only 25 mA, but V_{LU} is 25V and hence this situation would virtually never exist in a system. It has been empirically determined that if a device exhibits values of I_{LU} exceeding 50mA or V_{LU} exceeding a few volts, then this device will be extremely insensitive to latch-up in the majority of circuits and systems. A severe system fault would be required to induce latch-up in such devices.

System and Circuit Considerations

In the majority of systems and circuits using CMOS devices, latch-up should not be a major cause for concern. Being aware of the sources of latch-up problems will aid the designer in even further reducing the probability of latch-up damage to his circuits. Implementing some of the precautionary measures suggested in the following sections will ensure a trouble-free system.

The aspects of system and circuit design that can result in latch-up occurrence will be examined in the context of a "worst case" system example. In other words, systems containing combinations of the attributes of the example system will be more

likely to experience latch-up problems. The relationships between these systems aspects and the resultant latch-up triggering mechanisms will be described. Suggestions will be made intent upon reducing the risk of triggering the parasitic SCR's through careful design techniques. The protection circuits, which will be illustrated, should help in preventing circuit damage in case latch-up occurs. It should be noted at this point, that in systems where the input and output pins of the CMOS devices never go outside of the power supply rails either during power-up or in continuous operation, latch-up is not likely to ever occur. The first step, then, is to define a system which contains various components that qualify it for a "worst case" rating in a latch-up sense.

A "Worst Case" System

A circuit or system which has all of the following attributes and/or capabilities is more likely to experience latch-up problems. This is not to say that latch-up is inevitable in systems containing many of these attributes, only that the designer must be aware of potential problems and take steps at the design stage to avoid them. The following list summarizes the system aspects most likely to be associated with latch-up problems:

1) System operation/maintenance procedures allow insertion or removal of printed circuit cards with system power applied.
2) The system is powered by multiple supply voltages (e.g. +12V, +5V, and Gnd) or has a multi-supply at same voltage (e.g. +5V regulated, +5V unregulated).
3) Circuits utilize complex capacitive decoupling techniques particularly associated with multiple power supply voltages.
4) Integrated circuits on one system PCB drive other devices on different PCB's via a backplane, ribbon cable, etc.
5) Devices drive high capacitive loads such as long data or address buses.
6) System contains high speed address and/or data buses of sufficient length to cause their inductive properties to become significant at the frequencies in question (ribbon cables are a prime example).
7) System has electronic inputs that are directly accessible by the end user of the system.
8) Digital devices are driven from analog devices powered from higher supply voltages, utilizing input diodes for clamping.

Each of the above entries will now be examined in terms of its potential for triggering latch-up. The first four items are very interdependent. While each of these will be given consideration in separate sections, cross referencing will be extensive. The remaining items are relatively independent and thus, will be looked at in relative isolation.

Insertion/Removal of System PCB's "Live"

Inserting or removing printed circuit cards from a powered-up system can trigger latch-up in several different ways if certain precautions are not taken. One potential hazard that can occur is for an input or output edge terminal to make contact before the power supply pins are connected. If driven by a device on another circuit card, this input/output pin could have a voltage applied to it with no supply voltage to the device. Even if this situation exists for only a short period of time, then latch-up may be triggered when the power supply pin is connected. It is important to note that three-state outputs are also vulnerable in this situation. Such output drivers only present a high impedance to voltages within the device supply rails. Voltages on these outputs exceeding the supply can indeed trigger latch-up.

One solution to this problem is to slightly extend the power supply terminals with respect to the remaining edge terminals on the PCB (Fig. 9). This will ensure that power supply connections are the first made and last broken on insertion and removal of the PCB respectively.

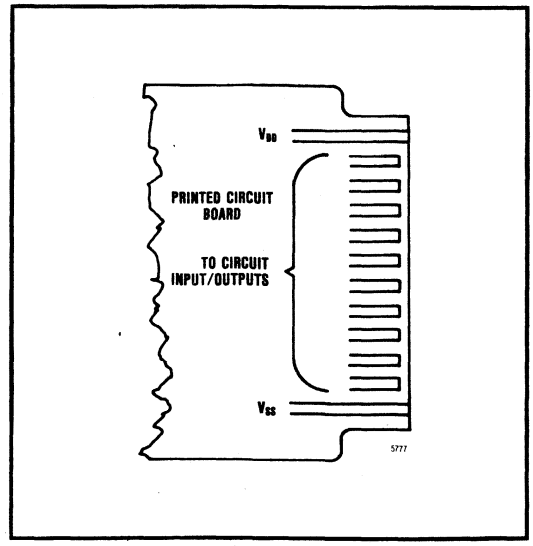


Fig. 9 PCB with Inset I/O Edge Terminals

Plugging a circuit card live into a system with multi-power supply voltages can result in the application of power supply over-voltages to certain devices. Consider the local decoupling scheme shown in Fig. 10. If a PCB containing such decoupling was plugged into a system live, then the following situation could result. Assume that all capacitors are discharged and that C_1 is much greater than C_2. It is possible that when the PCB is inserted, the +12V terminal makes connection first, then the ground, and lastly the +5V connection is made. In this situation, C_1 and C_2 are momentarily connected in series. The +12 volts applied to C_1 causes the voltage at the ground point to increase in accordance with the charge sharing between C_1 and C_2. This voltage could approach 12 volts since $C_1 \gg C_2$. When the ground terminal makes connection, the voltage at the nominal 5V rail will jump up by the amount of voltage initially present at the ground point (i.e. almost 12V). This results in an over-voltage condition being applied to the devices supplied by the 5V rail. If the applied voltage exceeds the absolute maximum rating for these devices then latch-up may be triggered by the avalanche breakdown mechanism described in an earlier section. This problem is more likely to be evident in systems with power supplies differing greatly in magnitude since potential over-voltages can become quite large. A prime example is a telephone switching system which would typically contain a −48V supply as well as +5V and other supply voltages.

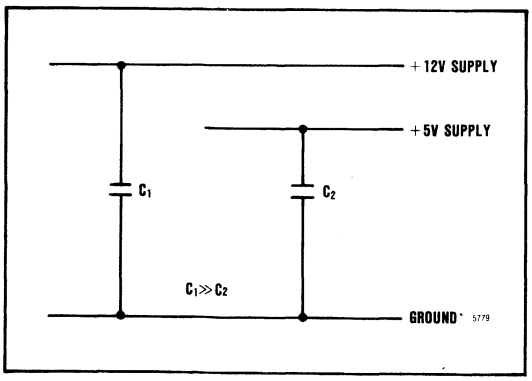


Fig. 10 Local Decoupling Scheme in Multi-Supply System

This problem can also be overcome by indenting the edge terminals on PCB's. In this case, there must be more than one level of indentation to ensure that the power supply connections are made in a sequence that will alleviate this problem. The safest way to accomplish this is to have power supply connections made in the order of ascending voltage magnitude (Fig. 11). For example, in a system with a +5V supply and +12V supplies, the ground line should make connection first, the +5V supply next and finally, the +12V and −12V supplies at the same time. This ascending order of magnitudes ensures that no over-voltages occur even if one of the power supplies pulls the other through the decoupling capacitors. The ground line should always make connection first to ensure that a positive supply does not pull a negative one or vice versa. Connecting opposing power supplies (e.g. +12V) at the same time will ensure cancellation of the effects of their connection.

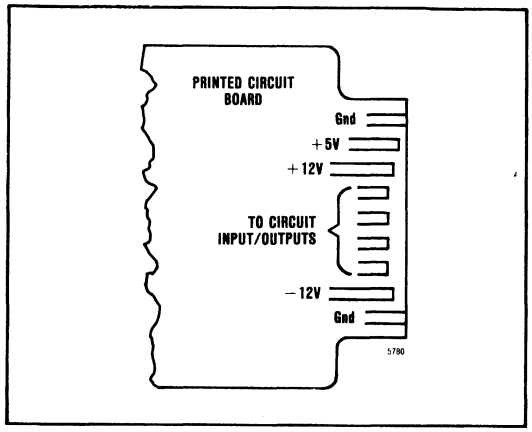


Fig. 11
Multi-Level Indentations of I/O Edge Terminals

In systems which have a large number of power supplies to contend with, it may not be feasible to provide the required number of indentations on the PCB. In this case, a careful analysis of the decoupling used must be done to establish potential problem areas. Where possible, decoupling capacitors on different supplies should be of equal magnitude. This will tend to minimize over-voltages due to equal charge sharing between the capacitors. If, after all possible precautions have been taken, there is still a possibility of power supply over-voltages occurring, then it may be necessary to provide some form of current limiting or local regulation to prevent circuit damage.

The simplest form of protection is to connect a resistor in series with the power supply (V_{DD} or V_{SS}) pin of the devices in question (Fig. 12a). The size of this resistor can be chosen to either prevent latch-up from occurring or to prevent circuit damage when latch-up does occur. If latch-up is to be prevented then the minimum resistor value is chosen as follows:

$$R = \frac{V_{Supply} - V_{DDMax}}{I_{DDMax}}$$

where V_{Supply} = Maximum Supply Voltage Generated

$V_{DD_{Max}}$ = Absolute Maximum Rating for V_{DD}

$I_{DD_{Max}}$ = Supply Current at $V_{DD_{Max}}$

This will ensure that $V_{DD_{Max}}$ is never exceeded at the device.

There is one last potential hazard that can develop due to "live" insertion of PCB's. On boards with little local decoupling, plugging the card in can result in an extremely fast transient on the power supply leads of devices on the board. These transients could theoretically result in triggering latch-up due to the dV/dt effect described earlier. This problem can be avoided by decoupling the power

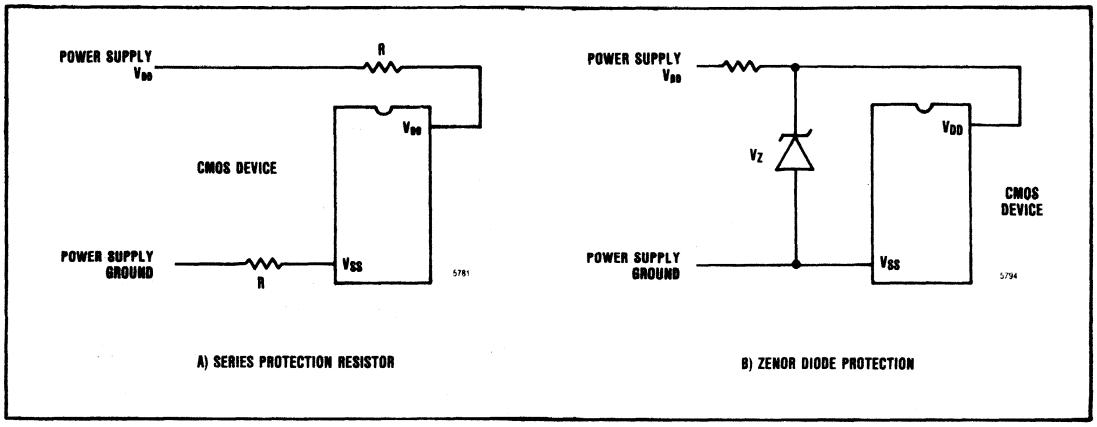


Fig. 12 Power Supply Over-Voltage Protection

To simply prevent damage due to latch-up, the resistor is chosen to limit the supply current to a few hundred milliamps at the maximum applied voltage. There are a few factors which must be taken into consideration when the maximum value for this resistor is selected. The source impedance of the power supply will be increased by the amount of the added resistance. This will result in a decrease in the current sourcing or sinking capacity of the device, depending on whether the resistor is in the V_{DD} or V_{SS} line respectively. There is also a corresponding increase in the output propagation delay, proportional to product of the protection resistor and the load capacitance. Finally there is a decrease in the noise immunity of the device proportional to the product of this resistor and the total instantaneous supply current (including the output currents). For devices such as the MD74SCXXX, it is recommended that this resistor be placed in the V_{DD} line as there is more available noise immunity for high level outputs (when driving TTL or other MD74SCXXX devices).

If a current-limiting resistor cannot be used due to constraints on output drive, speed or noise immunity, then the alternative is to connect a zener diode between V_{DD} and V_{SS} to prevent over-voltages across the device (Fig. 12b). A current-limiting resistor may still be necessary, but its value can be very small, limited only by the power-handling capacity of the zener diode.

supply on the board with sufficiently large capacitors to slow down the power supply ramp up when the board is plugged in. These capacitors must be chosen to be compatible with the overall decoupling scheme to prevent the over-voltage problem just described.

Similar transients on the power supply can be generated due to switching of high speed, high current devices such as ECL and Schottky TTL circuits driving heavy DC current loads. Also, back EMF generated by opening of inductive loads such as relays can induce nasty voltage spikes. Adequate high frequency decoupling will usually remedy the problem. A 0.01 to 0.1μF ceramic capacitor connected as close to the device as possible across the power supply pins will shunt most of this high frequency energy to ground (Fig. 13). Connection of flyback diodes around inductive loads is also recommended to limit back EMF surges.

Problems Associated with Multi-Power Supply Voltages and Associated Decoupling Circuitry

In systems that have more than one independent power supply, care must be taken to ensure correct sequencing during power-up and power-down cycles. This is required to prevent input and output over-voltage conditions from developing. Consider, for example, a device powered from a +5V supply that has its outputs connected to a device powered

from a +7V supply. Under steady state conditions, the output levels from the 5V devices would lie well within the supply voltage of the 7V device. However, if during power-up the 5V supply was to exceed the 7V supply, then the output voltage of the 5V device could exceed the instantaneous supply voltage of the 7V device (Fig. 14). This over-voltage could cause the 7V device to latch-up. A similar situation can occur between two devices powered by separate supplies of equal magnitude such as 5V regulated and 5V unregulated supplies. In this case there is the added concern when three-state outputs are tied together. These outputs are also subject to over-voltage triggering of latch-up. Such outputs present a high impedance only to signals lying within the power supply voltages. It must be stressed that these over-voltage conditions need only exist for a very brief period of time to trigger latch-up. Thus, even transient over-voltages during power-up may pose a problem.

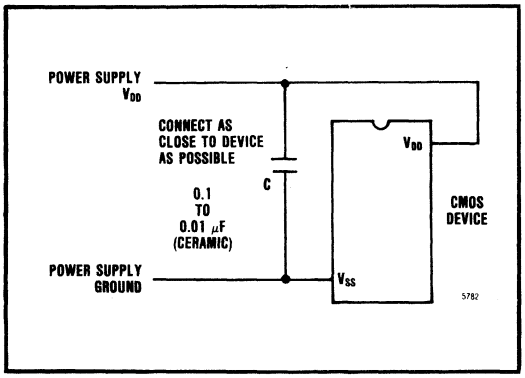


Fig. 13 High Frequency Power Supply Decoupling

To ensure proper power supply sequencing, careful attention must be paid to the selection of decoupling components both at the initial design stage and when design revisions are done. This applies to both main power supply decoupling as well as local board decoupling. While proper sequencing may be evident at main distribution points, local sequencing can be altered by large capacitors on individual boards. Boards which have a large DC power requirement are likely to have such decoupling and hence, must be looked at carefully.

One way of ensuring that power supplies track when turning on or off is to connect a diode from the lower supply voltage to the higher one in the case of unequal supplies (Fig. 15). This will cause the supplies to track within one diode drop until they attain proper levels. In the case of two equal supplies, two diodes can be connected back to back, forcing supplies to track, independent of which supply comes up first.

Devices Driving Others on Separate PCB's

When integrated circuits in a system drive other devices on separate PCB's (via a backplane for example), then the considerations given in the previous two sections must be applied globally to the system. This was already mentioned in the section on plugging in PCB's "live". That is, when a PCB is plugged into a backplane with the system power applied, there is the danger that an input or output pin will contact an active line on the backplane before the power supply connection is made. The solution to this problem, as mentioned, lies in indenting the I/O edge terminations with respect to power supply terminals on the PCB.

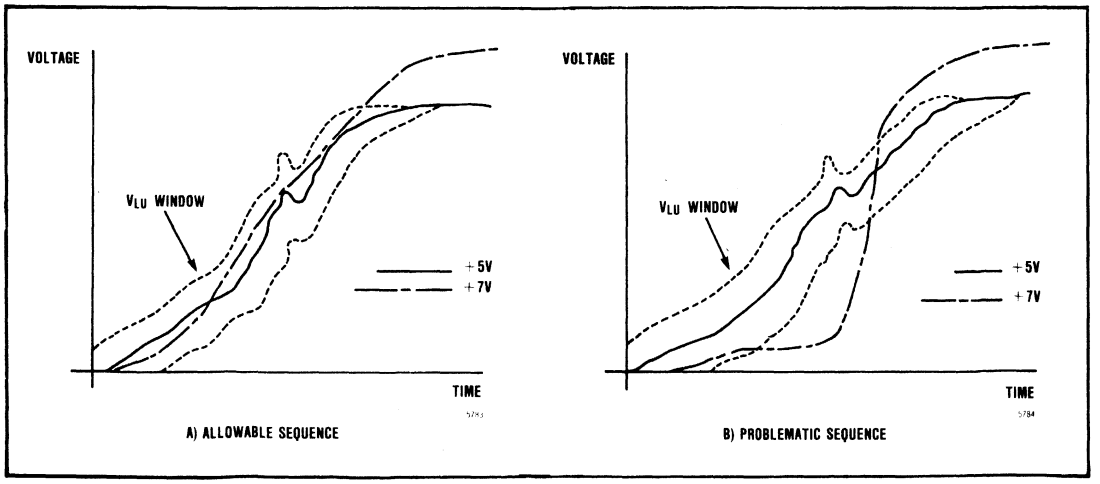


Fig. 14 Power Supply Sequencing

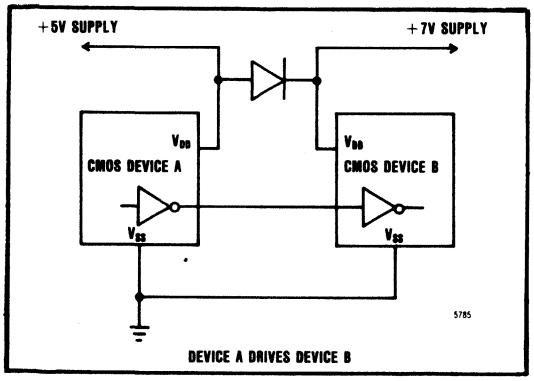


Fig. 15 Forced Power Supply Tracking with Clamping Diode

Power supply sequencing should be given special attention in systems with devices that drive off-board. The same criteria applies here as was described for multi-supply systems. However, care must also be taken in single supply systems. In this case, large amounts of local decoupling can cause the supply voltages on some boards in the system to ramp up slower than on others. Devices on boards whose power supply ramps up quickly, can impress an over-voltage on devices on other boards. If this over-voltage is large enough, then latch-up may be triggered.

Whenever possible, local decoupling should be equalized on all boards within the system to minimize these effects. In systems where all off-board drivers are three-state devices, a simple solution exists. All outputs should be kept in a high impedance state during power-up and power-down. Thus, no current will be available to trigger latch-up even if differential supply voltages develop from board to board. Alternatively, current limiting resistors can be connected in series with any inputs or outputs that may be subjected to over-voltages. These resistors are sized to limit current to less than 10mA:

$$R = \frac{(V_{Diff} - 0.3V)}{10mA}$$

where V_{Diff} = maximum instantaneous voltage differential between power supplies

The side effects of connecting these resistors are the same as mentioned previously for power supply over-voltage protection. There will be reductions in current drive from outputs, in speed, and in noise immunity on outputs driving DC loads through these resistors.

Devices Driving Long Address or Data Buses

Long address and data buses can exhibit quite large capacitances. Devices which drive such buses or have their inputs tied to one, can be subjected to over-voltage conditions. This is especially true if large DC current loads are switched on the same PCB (e.g. a group of LED's during a lamp test). Over-voltages can develop as follows. The change in the power supply current causes a localized voltage drop on the supply pins of the devices near to the device drawing the load current. This is a result of the finite resistance of the power supply tracks and contact resistance of any connectors. At the same time, the bus capacitance tends to hold the voltage on the inputs and outputs connected to the bus at the full supply voltage. If a sufficient voltage differential develops between the bus and the local power supply, then the bus capacitance will discharge via the input and output structures. This current can attain a magnitude of tens of milliamps and hence trigger latch-up (Fig. 16).

Various precautions can be taken to reduce the chances of this problem occurring. Reducing the power supply resistance and bus capacitances can be done at the time of initial design. Wide power supply tracks and low contact resistance connectors should be used whenever possible. Buses should be kept as short as possible and have the largest possible spacings between the lines. If this problem still results due to system restraints on PCB layout, then the connection of a decoupling capacitor across the power supply pins of the devices latching-up should help (Fig. 17). The size of the capacitor depends upon the magnitude of the local current and the local resistance of the power supply. Normally a 10μF capacitor will clear up such problems and should not interfere with the local power supply sequencing on most PCB's.

There is one other way in which an input/output over-voltage can occur on long buses. There exists, on such buses, intertrack capacitance as well as capacitance to ground. When two adjacent tracks are at opposite logic levels (one at 5V, the other at ground), this capacitance charges to the full supply voltage. When the track initially at ground potential suddenly goes high, the signal is coupled through the capacitor to the other track. The voltage on this track increases from its initial value of 5V, impressing over-voltages on any devices connected to this track.

Minimizing intertrack capacitance by interleaving signal and ground tracks should be done wherever board space permits. Alternatively, external clamping diodes can be connected on tracks exhibiting these voltage excursions. The diodes may need be Schottky diodes if regular ones do not clamp soon enough to prevent current flow through I/O structures. Regular silicon diodes may still be used if they are referenced to voltages inset by 0.7V from

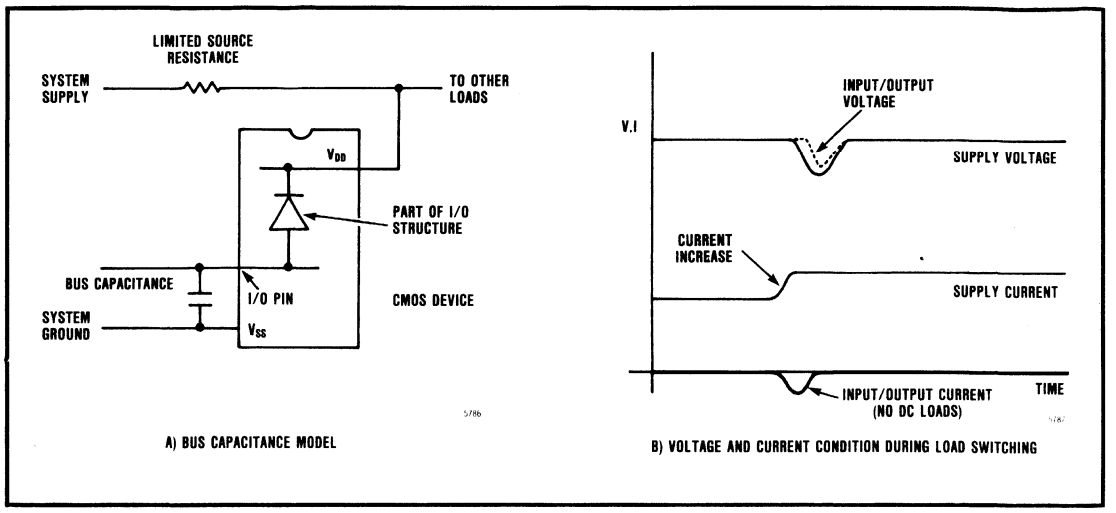


Fig. 16 Effects of Switching DC Loads Combined with Large Bus Capacitors

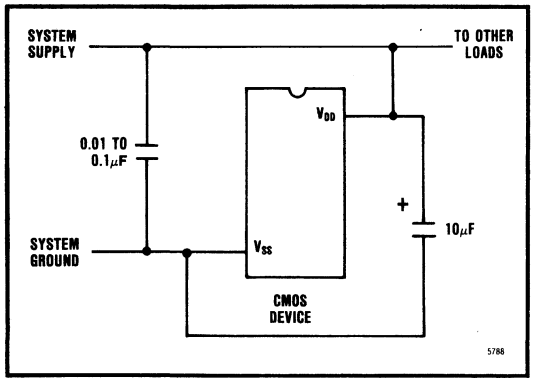


Fig. 17 Local Decoupling to Offset Load Switching Effects

the supply rails. The clamping circuit shown in Fig. 18 should be quite effective, but as can be seen, this circuit will dissipate power. This may or may not be a problem depending on the overall system requirements. The decoupling capacitors help to absorb the high frequency energy. The resistor values shown are selected for a 5V supply and should be scaled for other supply voltages.

Ribbon Cables – A Special Case

A ribbon cable is a special case of long bus structure. The problems mentioned in the previous section also apply here. However, if the ribbon cable is of sufficient length, then its inductive properties become significant. The distributed inductance and capacitance form a second order circuit which can "ring" when driven by fast, digital signals. The result is the generation of damped oscillations centered about the positive and negative supply rails (Fig. 19). The positive and negative excursions outside of the supply rails impress overvoltages on inputs and outputs connected to the ribbon cable. If of sufficient amplitude, these overvoltages may trigger latch-up.

Solving the problem can be as simple as terminating each end of such cables with resistors to reduce the ringing voltages. However, these resistors will dissipate extra power. An alternative is to connect external protection diodes as shown in Fig. 20. These diodes will clamp any generated over-voltages. If the problem persists, it may be necessary to use Schottky diodes to ensure that the external diodes conduct before the input/output structures do.

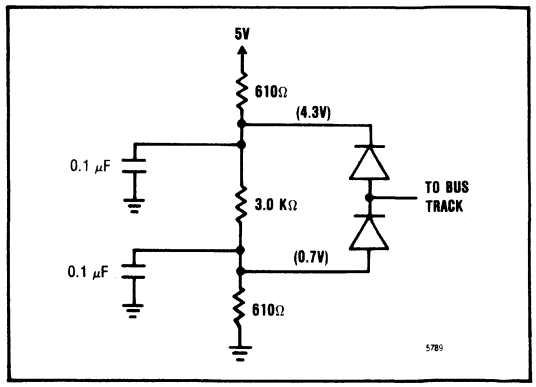


Fig. 18 Clamping Circuit for Long Buses

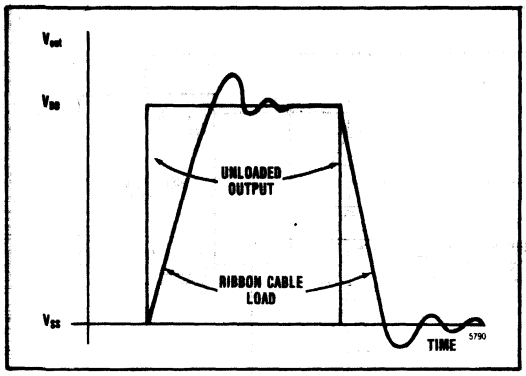


Fig. 19
Ringing Effect Due to Driving Ribbon Cable

Systems with End-User Accessible Inputs/Outputs

An extreme condition of input/output over-voltage can develop in systems which have end-user accessible I/O ports. The user may apply signals to these ports when the system power supply is not turned on. Devices in the system connected to these ports are likely to latch-up when the power is turned on due to the current flowing through the I/O structures. Resistors can be connected in series with these I/O's to limit the current during these periods. As mentioned, these resistors will have direct effect on the speed and noise performance of these ports.

Latch-up may also be triggered if the end user applies voltages to the I/O ports which exceed the system power supply voltages. The protection resistors suggested above may provide adequate protection against this hazard as well. However, performance constraints on the port may be such that the current-limiting resistors chosen are too small to protect against severe faults such as accidental connection of the AC mains supply. Protection against such faults can be provided by connection of external clamping diodes in the manner outlined for ribbon cables. Again, Schottky diodes may be required.

If fault conditions are likely to be very severe, it may be necessary to reference external clamping diodes to voltages inset by 0.7V from the power supply (Fig. 21). These diodes will conduct before the input/output structures of the device on the port whenever an over-voltage condition exists. Thus, no current will flow to trigger latch-up. The reference voltages are inset by 0.7V to allow the use of regular, low-cost diodes. Due to the potentially large currents flowing through the protection diodes, a clamping circuit similar to the one in Fig. 18 is not feasible. The output resistance in this case needs to be substantially lower.

Digital and Analog Devices in Same System

In systems which have digital and analog devices powered by different supply voltages, there is the potential hazard of over-voltage conditions developing. Consider, for example, the case of an

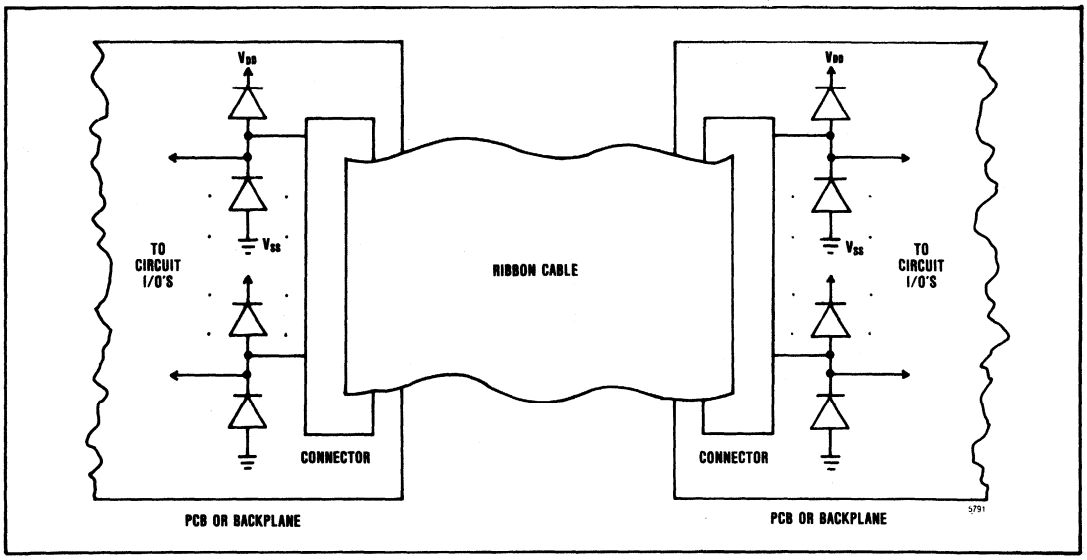


Fig. 20 External Clamping Diodes

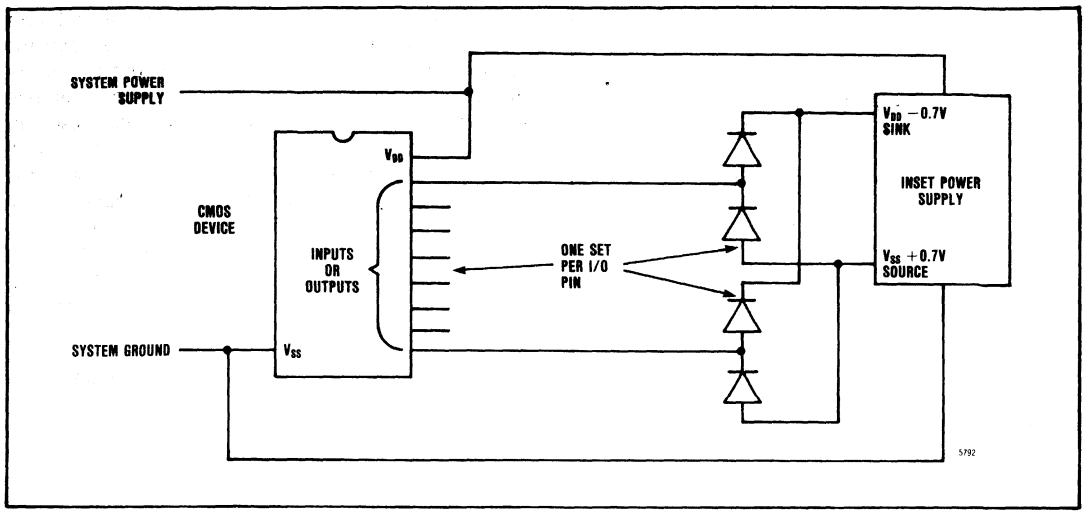


Fig. 21 Inset Supply Voltages for External Clamping

analog comparator powered from +10V driving a digital device powered from a +10V supply. When the comparator output goes low, it will approach −10V and pull the digital input below V_{SS} (0V). If the comparator can pull enough current, then latch-up may be triggered. Putting a resistor in series with the input will limit the current and prevent latch-up. However, it is not a recommended procedure to use the input diodes as clamping circuits. A more advisable solution is to use a resistive divider as shown in Fig. 22. When the comparator output goes low, the divider will have 20V across it. Half of this voltage will be dropped across each resistor so that the digital input sits at 0V. When the comparator output goes high, no current flows through the divider so that the digital input sits at V_{DD}. Since the CMOS input has an extremely high input impedance, the value of these resistors can be very large (>100K) to minimize power consumption.

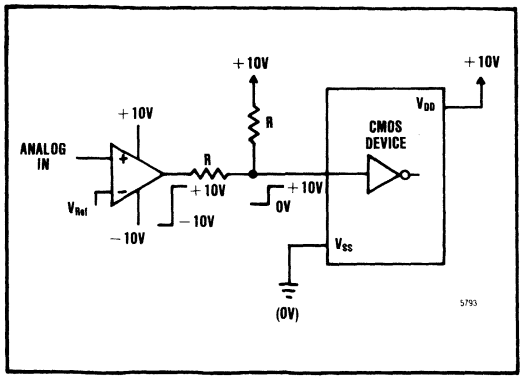


Fig. 22 Voltage Divider to Limit Voltage Swing on CMOS Input

Conclusion

In the vast majority of circuits and systems employing CMOS devices, latch-up will not be a major concern. When simply applied according to manufacturers' recommendations, CMOS devices are not overly sensitive to the normal circuit conditions that exist within a system. What has been attempted in this application note is to develop an understanding of the latch-up phenomenon and its causes to assist designers in avoiding potential pitfalls caused by a simple lack of knowledge.

Having briefly reviewed the basic theory of SCR operation in general, and as it applies to CMOS input and output structures, an understanding of the mechanism of latch-up was developed. Taking a close look at various aspects of system and circuit design has revealed that various precautionary measures taken at the design stage can greatly reduce the risk of latch-up occurrences. In cases where system performance or features create potentially hazardous situations beyond the designer's control, the implementation of simple protection circuitry will again minimize problems.

Through the use of careful design practices, augmented by protection circuitry when needed, the designer can use CMOS analog and digital integrated circuits extensively. System and circuit reliability will no longer be a function of latch-up related problems.

Reference

1. S.B. Dewan and A. Straughen, "Power Semiconductor Circuits", pp. 77-84, John Wiley and Sons, 1975.

Appendix

The following is a derivation of equation (1) of the main text. Fig. 2 is referenced for this purpose.

The collector and emitter currents of Q_1 and Q_2 are related by:

$$i_{C_1} = \alpha_1 i_{E_1} \qquad i_{C_2} = \alpha_2 i_{E_2}$$

Looking at Fig. 2, it can be seen that the load current and the emitter currents of Q_1 and Q_2 are all equal. Also the load current is equal to the sums of the two collector currents and a leakage current from Q_2's collector to its base (I_{CBO_2}). Therefore:

$$\begin{aligned} I_L &= i_{C_1} + i_{C_2} + I_{CBO_2} \\ &= \alpha_1 i_{E_1} + \alpha_2 i_{E_2} + I_{CBO_2} \\ &= (\alpha_1 + \alpha_2) I_L + I_{CBO_2} \\ &= \frac{I_{CBO_2}}{1 - (\alpha_1 + \alpha_2)} \end{aligned}$$

The collector-emitter current gains (α_1,α_2) can be expressed in terms of the collector-base current gains (β_1,β_2) as:

$$\alpha_1 = \frac{\beta_1}{1 + \beta_1} \qquad \alpha_2 = \frac{\beta_2}{1 + \beta_2}$$

Substituting these into the equation above yields:

$$I_L = \frac{I_{CBO_2}}{1 - \left(\frac{\beta_1}{1 + \beta_1} + \frac{\beta_2}{1 + \beta_2}\right)}$$

$$I_L = I_{CBO_2}\left[\frac{(1 + \beta_1)(1 + \beta_2)}{1 - \beta_1 \beta_2}\right]$$

MITEL®

Application Note **MSAN-108**

Applications Of The MT8870 Integrated DTMF Receiver

RBW 9161-001-002-NA ISSUE 1 JUNE 1983

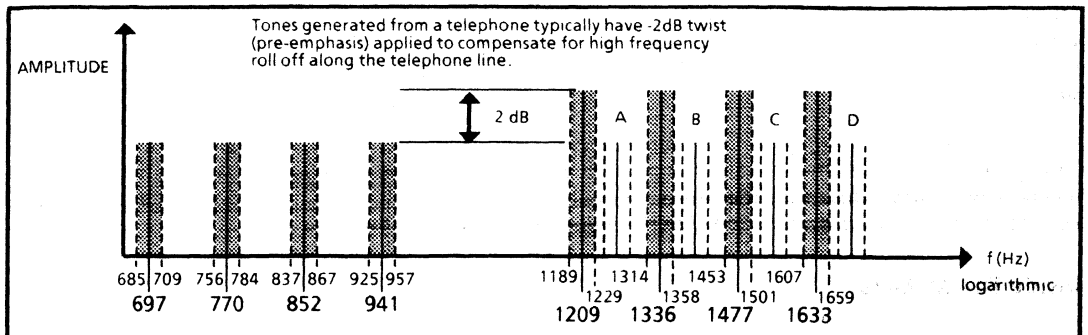
Contents

Introduction

The purpose of this Application Note is to provide information on the operation and application of DTMF Receivers. The MT8870 Integrated DTMF Receiver will be discussed in detail and its use illustrated in the application examples which follow.

More than 25 years ago the need for an improved method for transferring dialling information through the telephone network was recognized. The traditional method, dial pulse signalling, was not only slow, suffering severe distortion over long wire loops, but required a DC path through the communications channel. A signalling scheme was developed utilizing voice frequency tones and implemented as a very reliable alternative to pulse dialling. This scheme is known as DTMF (Dual Tone Multi-Frequency), Touch-Tone™ or simply, tone dialling. As its acronym suggests, a valid DTMF signal is the sum of two tones, one from a low group (697-941Hz) and one from a high group (1209-1633Hz) with each group containing four individual tones. The tone frequencies were carefully chosen such that they are not harmonically related and that their intermodulation products result in minimal signalling impairment (Fig. 1a). This scheme allows for **16 unique combinations. Ten of these codes represent the numerals zero through nine, the remaining six** (*,#,A,B,C,D) being reserved for special signalling. Most telephone keypads contain ten numeric push buttons plus the asterisk (*) and octothorp (#). The buttons are arranged in a matrix, each selecting its low group tone from its respective row and its high group tone from its respective column (Fig. 1b).

The DTMF coding scheme ensures that each signal contains one and only one component from each of the high and low groups. This significantly simplifies decoding because the composite DTMF signal may be separated with bandpass filters, into its two single frequency components each of which may be handled individually. As a result DTMF coding has proven to provide a flexible signalling scheme of excellent reliability, hence motivating innovative and competitive decoder design.



Standard DTMF frequency spectrum ±(1.5% + 2 Hz). Second harmonics of the low group (possibly created due to a non-linear channel) fall within the passband of the high group (indicated by A,B,C,D). This is a potential source of interference.

Fig. 1a The Dual Tone Multifrequency (DTMF) Spectrum

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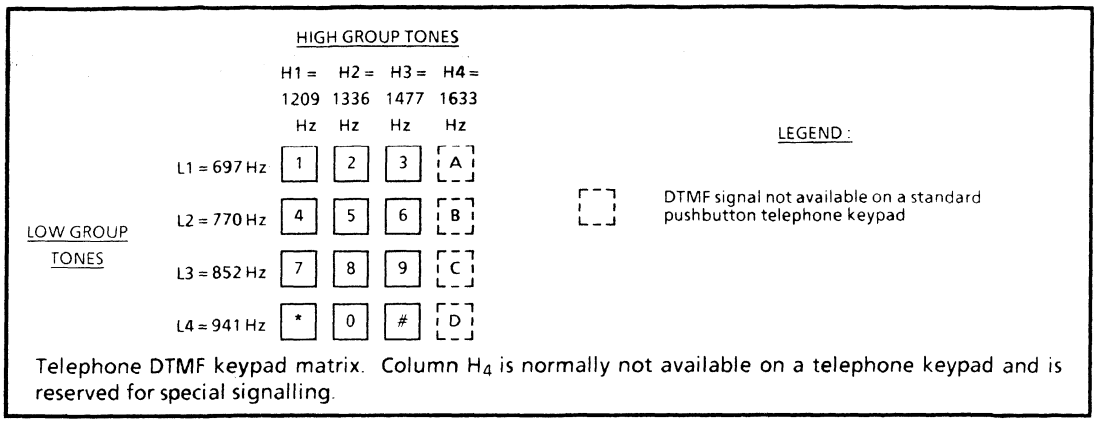


Telephone DTMF keypad matrix. Column H_4 is normally not available on a telephone keypad and is reserved for special signalling.

Fig. 1b The Dual Tone Multifrequency (DTMF) Keypad

Development

Early DTMF decoders (receivers) utilized banks of bandpass filters making them somewhat cumbersome and expensive to implement. This generally restricted their application to central offices (telephone exchanges).

The first generation receiver typically used LC filters, active filters and/or phase locked loop techniques to receive and decode DTMF tones. Initial functions were, commonly, phone number decoders and toll call restrictors. A DTMF receiver is also frequently used as a building block in a tone-to-pulse converter which allows Touch-Tone™ dialling access to mechanical step-by-step and crossbar exchanges (Fig. 2).

The introduction of MOS/LSI digital techniques brought about the second generation of tone receiver development. These devices were used to digitally decode the two discrete tones that result from decomposition of the composite signal. Two analog bandpass filters were used to perform the decomposition.

Totally self-contained receivers implemented in thick film hybrid technology depicted the start of third generation devices. Typically, they also used analog active filters to bandsplit the composite signal and MOS digital devices to decode the tones.

The development of silicon-implemented switched capacitor sampled filters marked the birth of the fourth and current generation of DTMF receiver technology. Initially single chip bandpass filters were combined with currently available decoders enabling a two chip receiver design. A further advance in integration has merged both functions onto a single chip allowing DTMF receivers to be realized in minimal space at a low cost.

The second and third generation technologies saw a tendency to shift complexity away from the analog circuitry towards the digital LSI circuitry in order to reduce the complexity of analog filters and their inherent problems. Now that the filters themselves can be implemented in silicon, the distribution of complexity becomes more a function of performance and silicon real estate.

Inside The MT8870

The MT8870 is a state of the art single chip DTMF receiver incorporating switched capacitor filter technology and an advanced digital counting/averaging algorithm for period measurement. The block diagram (Fig. 3) illustrates the internal workings of this device.

To aid design flexibility, the DTMF input signal is first buffered by an input op-amp which allows

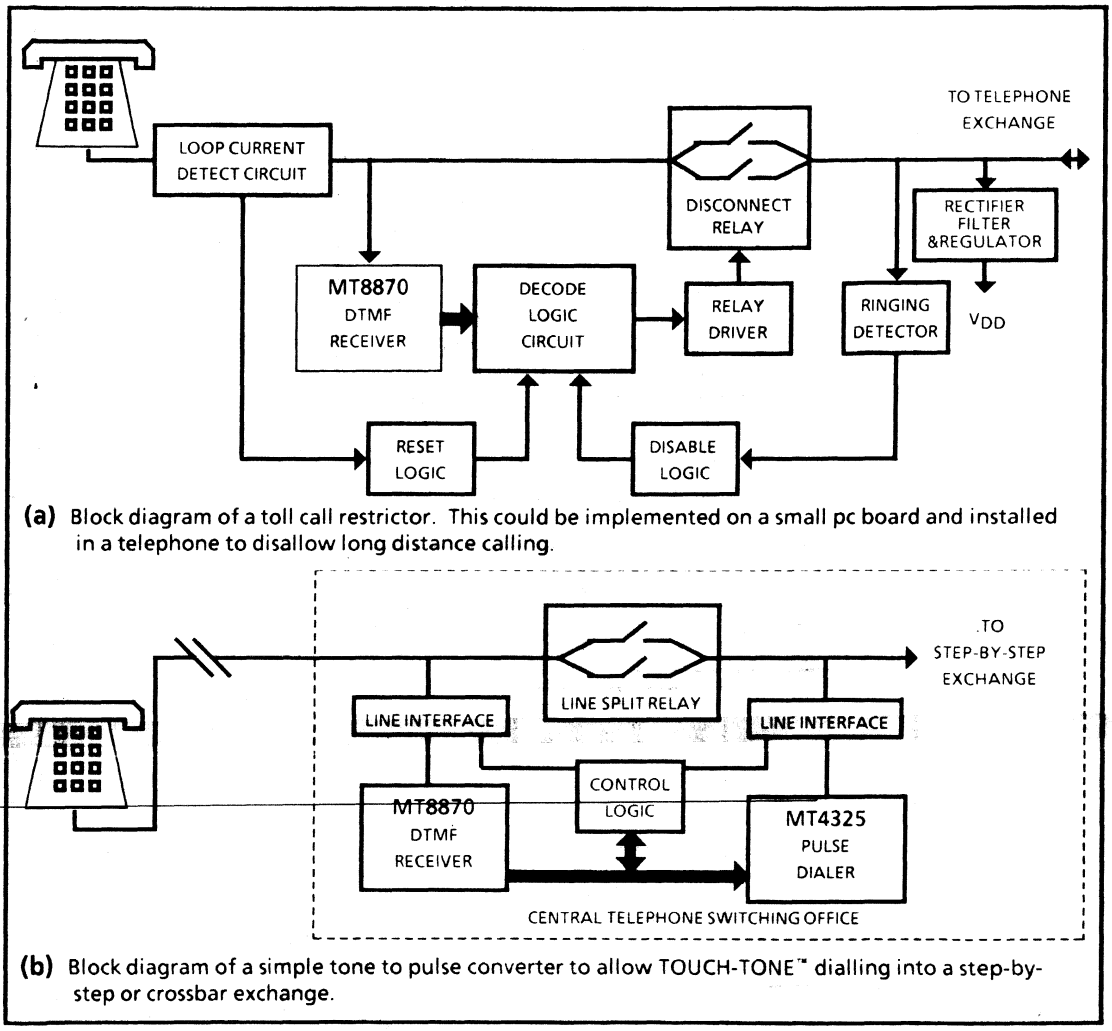
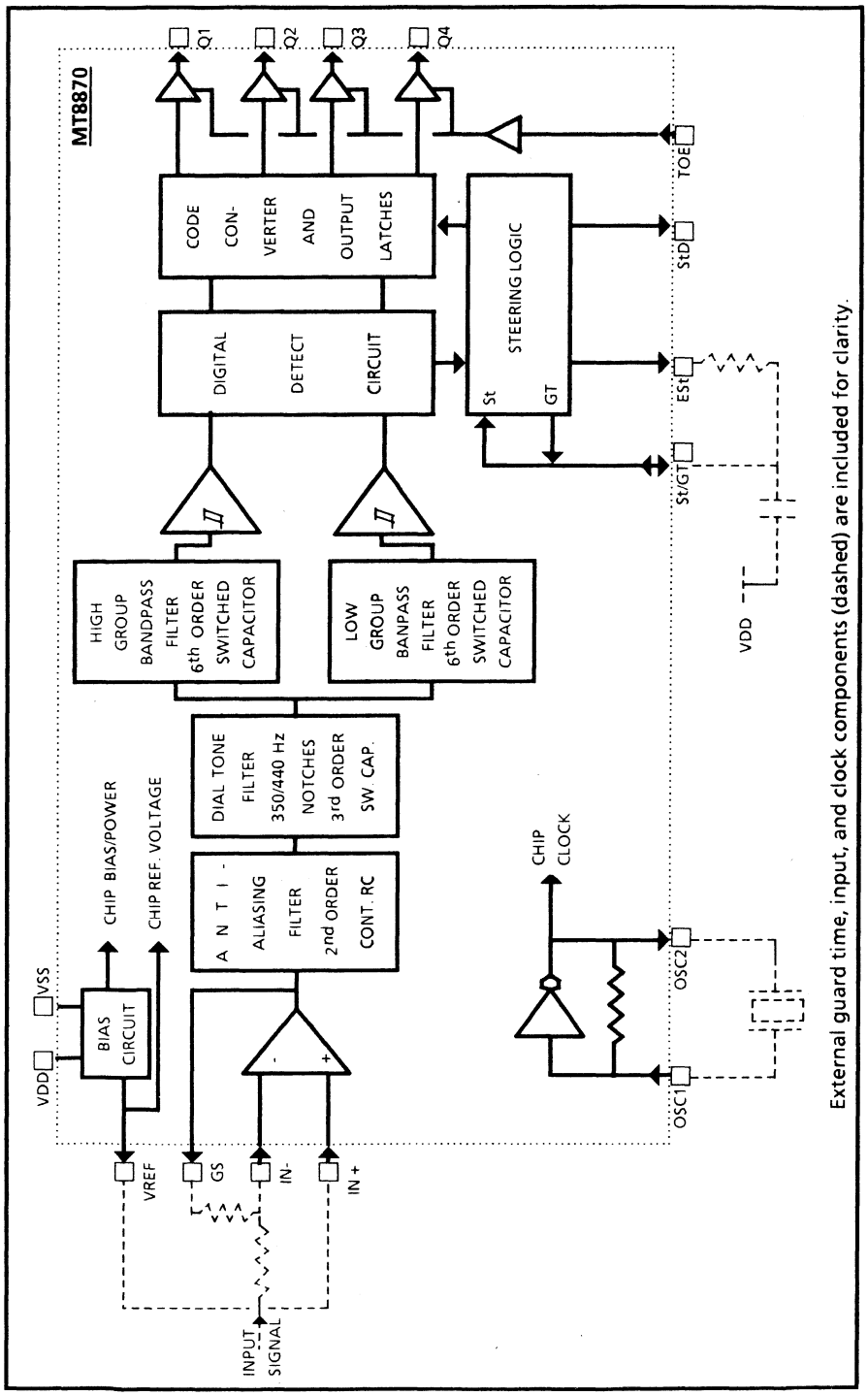


Fig .2 Typical DTMF Receiver Applications.

adjustment of gain and choice of input configuration. The input stage is followed by a low pass continuous RC active filter which performs an anti-aliasing function. Dial tone at 350 and 440Hz is then rejected by a third order switched capacitor notch filter. The signal, still in its composite form, is then split into its individual high and low frequency components by two sixth order switched capacitor bandpass filters. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator.

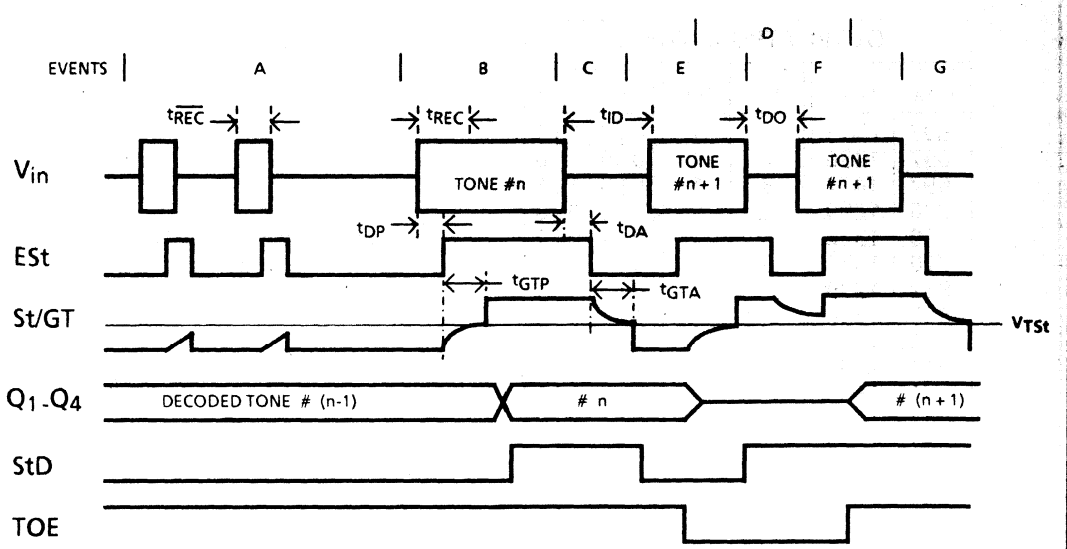
The two resulting rectangular waves are applied to digital circuitry where a counting algorithm measures and averages their periods. An accurate reference clock is derived from an inexpensive external 3.58MHz colourburst crystal.

The timing diagram (Fig. 4) illustrates the sequence of events which follow digital detection of a DTMF tone pair. Upon recognition of a valid frequency from each tone group the Early Steering (ESt) output is raised. The time required to detect the presence of two valid tones, t_{DP}, is a function of the decode algorithm, the tone frequency and the previous state of the decode logic. ESt indicates that two tones of proper frequency have been detected and initiates an RC timing circuit. If both tones are present for the



External guard time, input, and clock components (dashed) are included for clarity.

Fig.3 MT8870 Functional Block Diagram



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE
E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE)
F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED
G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DECTECTION OF CORRECT TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4	4-BIT DECODED TONE OUTPUT
StD	DELAYED STEERING OUTPUT. INDICTES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTES A VALID SIGNAL.
TOE	TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
$t_{\overline{REC}}$	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Fig. 4 MT8870 Timing Diagram

OUTPUT TRUTH TABLE

f_{LOW}	f_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1209	0	1	1	0	1	0
941	1336	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0
-	-	ANY	0	Z	Z	Z	Z

0 = LOGIC LOW 1 = LOGIC HIGH
Z = HIGH IMPEDANCE

Output truth table. Note that key "0" is output as "1010_2 (ie: 10_{10})" corresponding to standard telephony coding.

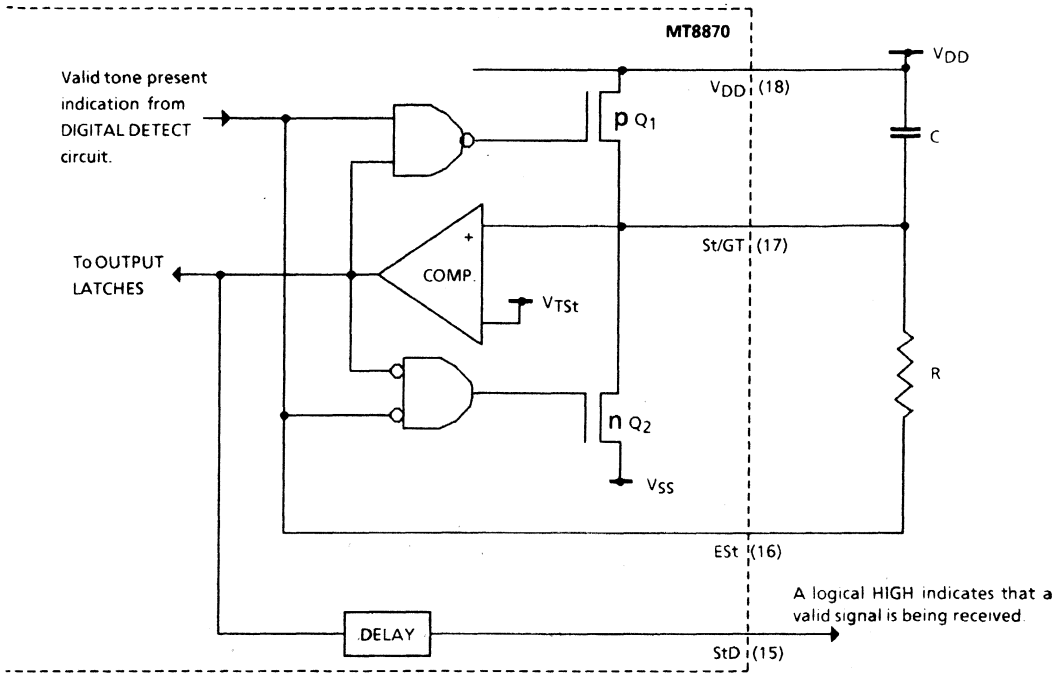
Fig. 5 MT8870 Output Truth Table.

minimum guard time, t_{GTP}, which is determined by the external RC network, the DTMF signal is decoded and the resulting data (Fig.5) is latched in the output register. The Delayed Steering (StD) output is raised and indicates that new data is available. The time required to receive a valid DTMF signal, t_{REC}, is equal to the sum of t_{DP} and t_{GTP}.

A simplified circuit diagram (Fig. 6) illustrates how the chip's steering circuit drives the external RC network to generate guard times. Pin 17, St/GT (Steering/Guard Time), is a bidirectional signal pin which controls StD, the output latches, and resets the timing circuit. When St/GT is in its input mode (St function) both Q_1 and Q_2 are turned off and the voltage level at St/GT is compared to the steering threshold voltage V_{TSt}. A transition from below to above V_{TSt} will switch the comparator's output from low to high strobing new data into the output latches, and raising the StD output. As long as an input level above V_{TSt} is maintained StD will remain high indicating the presence of a valid DTMF signal.

Initially, when no valid tone-pairs are present, capacitor C is fully charged applying a low voltage to St/GT. This causes a low at the comparator's output and since ESt is also low, Q_2 turns on ensuring that C is completely charged. In this condition St/GT is in its output mode (GT function). When a valid tone-pair is received ESt is raised turning off Q_2 which puts St/GT in its high impedance input mode and allows C to discharge through R. If this condition persists for the tone-present guard time, t_{GTP}, the voltage at St/GT rises above V_{TSt} raising StD which indicates reception of a valid DTMF signal. If the tone pair drops out before the duration of t_{GTP}, ESt is lowered turning on Q_2 which charges C resetting the tone-present guard time.

Once a DTMF signal is recognized as valid both ESt and the comparator output are high. This turns on Q_1 which discharges C and initializes the tone-absent guard time, t_{GTA}. After the DTMF signal is removed, ESt is lowered, Q_1 turns off placing St/GT in its input mode and C begins to charge through R. If the same valid tone-pair does not reappear before t_{GTA} then the voltage at St/GT falls below V_{TSt} which resets the timing circuit via Q_2 and prepares the device to receive another signal. If the same valid tone-pair reappears before t_{GTA}, ESt is raised turning on Q_1 and discharging C which resets t_{GTA}. In this case StD remains high and the tone dropout is disregarded as noise.



Simplified steering circuit. Initially ESt is low, C is fully charged applying 0V to St/GT and Q_2 is on. Upon reception of a valid tone pair ESt is raised turning off Q_2 and allowing C to discharge through R which increases the voltage at St/GT. When V_{TSt} is reached the comparator output goes high indicating a valid signal, latches the outputs and turns on Q_1 which discharges C. When the tone pair is lost ESt goes low Q_1 turns off and C charges through R decreasing the voltage at St/GT. When V_{TSt} is reached StD goes low and Q_2 turns on resetting the timing circuit.

STEERING TRUTH TABLE

ESt	St(/GT)	(St/)GT	StD
0	$<V_{TSt}$	0	0
0	$>V_{TSt}$	Z	1
1	$<V_{TSt}$	Z	0
1	$>V_{TSt}$	1	1

0 = LOGIC LOW
1 = LOGIC HIGH
Z = HIGH IMPEDENCE
V_{TSt} = Threshold Voltage (typically 1/2 V_{DD})

Steering circuit truth table. Note that pin 17 (St/GT) acts as both an input and an output depending on the relative states of ESt and the comparator output.

Fig. 6 MT8870 Steering And Guard Time Circuit Operation

To provide good reliability in a typical telephony environment, a DTMF receiver should be designed to recognize a valid tone-pair greater than 40mS in duration and, to accept as successive digits, tone-pairs that are greater than 40mS apart. However in other environments, such as two-way radio, the optimum tone duration and intra-digit times may differ due to noise considerations.

By adding an extra resistor and steering diode (Fig. 7b, 7c) t_{GTP} and t_{GTA} can be set to different values. Guard time adjustment allows tailoring of noise immunity and talk-off performance to meet specific system needs.

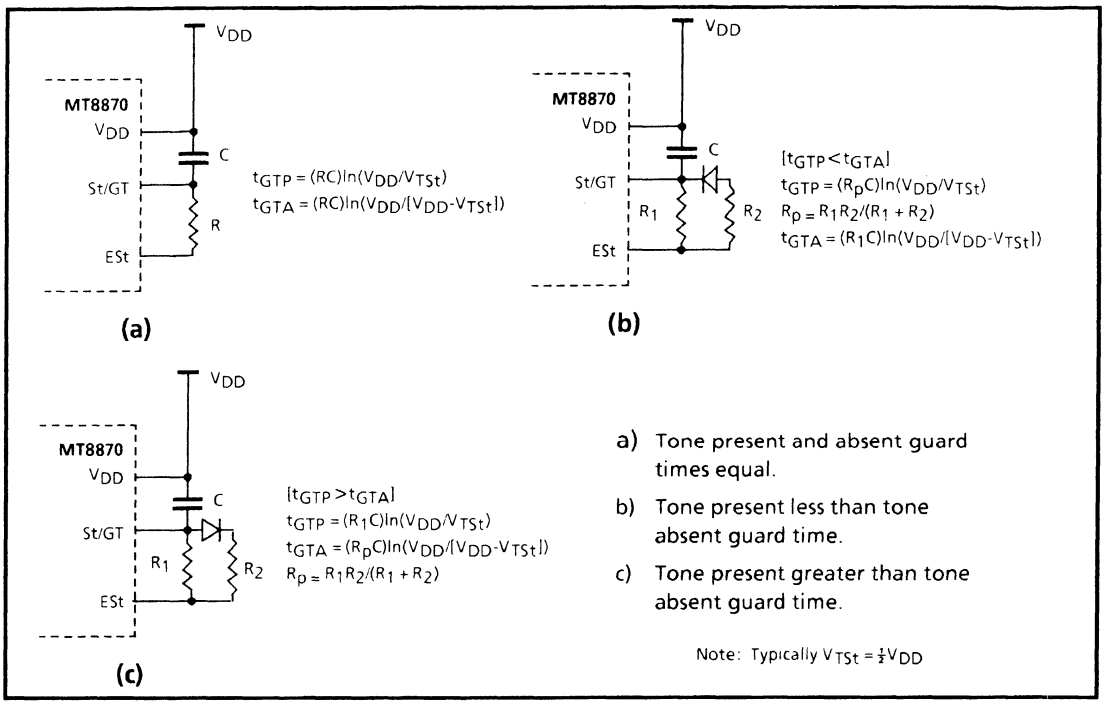


Fig. 7 Guard Time Circuits.

Talk-off is a measure of errors that occur when the receiver falsely detects a tone pair due to speech or background noise simulating a DTMF signal. Increasing t_{GTP} improves talk off performance since it reduces the probability that speech will maintain DTMF simulation long enough to be considered valid. The trade-off here is decreased noise immunity because dropout (longer than t_{DA}) due to noise pulses will restart t_{GTP}. Therefore, for noisy environments, t_{GTP} should be decreased. The signal absent guard time, t_{GTA}, determines the minimum time allowed between successive DTMF signals. A dropout shorter than t_{GTA} will be considered noise and will not register as a successive valid tone detection. This guards against multiple reception of a single character. Therefore, lengthening t_{GTA} will increase noise immunity and tolerance to the presence of an unwanted third tone at the expense of decreasing the maximum signalling rate.

The intricacies of the digital detection algorithm have a significant impact on the overall receiver performance. It is here that the initial decision is made to accept the signal as valid or reject it as speech or noise.

Trade-offs must be made between eliminating talk off errors and eliminating the effects of unwanted third tone signals and noise. These are mutually conflicting events. On one hand valid DTMF signals present in noise must be recognized which requires relaxation of the detection criteria. On the other hand, relaxing the detection criteria increases the probability of receiving "hits" due to talk off errors.

Many considerations must be taken into account in evaluating criteria for noise rejection. In the telephony environment two sources of noise are predominant. These are, third tone interference, which generally comes from dial tone harmonics, and band-limited white noise . In the MT8870 a complex digital averaging algorithm provides excellent immunity to voice, third tone and noise signals which prevail in a typical voice bandwidth channel.

The algorithm used in the MT8870 combines the best features from two previous generations of Mitel digital decoders with improvements resulting from years of practical use within the telephone environment. The algorithm has evolved through a combination of statistical calculations and empirical "tweaks" to result in the realization of an extremely reliable decoder.

Applications

The proven reliability of DTMF signalling has created a vast spectrum of possible applications. Until recently, many of these applications were rendered ineffective due to cost or size considerations. Now that a complete DTMF receiver can be designed with merely a single chip and a few external passive components one can take full advantage of a highly developed signalling scheme as a small, cost-effective signalling solution.

The design of a DTMF receiving system can generally be broken down into three functional blocks (Fig. 8). The first consideration is the interface to the transmission medium. This may be as simple as a few passive components to adequately configure the MT8870's input stage or as complex as some form of demodulation, multiplexing or analog switching system. The second functional block is the DTMF receiver itself. This is where the receiving system's parameters can be optimized for the specific signal conditions delivered from the "front end" interface. The third, and perhaps most widely varying function, is the output control logic. This may be as simple as a 4 to 16 line decoder, controlling a specific function for each DTMF code, or as complex as a full blown computer handling system protocols and adaptively varying the tone receiver's parameters to adjust for changing signal conditions. Several currently applied and conceptually designed applications are described subsequently but first let's consider the design of a typical input stage.

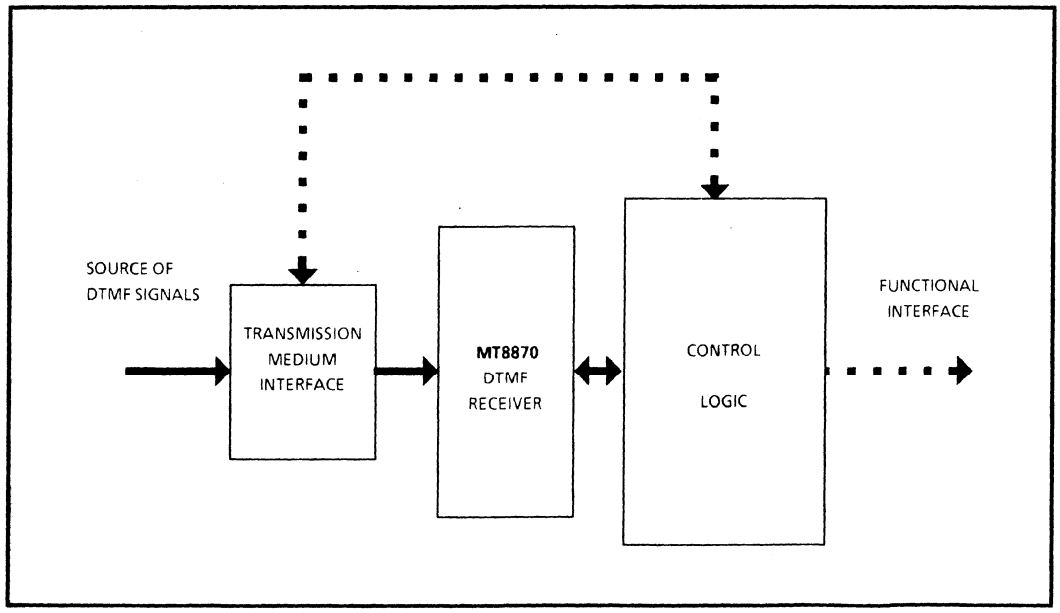


Fig. 8 Modular Approach To DTMF Receiver Systems

The input arrangement of the MT8870 provides a differential input op amp as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail. The output of this op amp is available to provide feedback for gain adjustment.

A typical single ended input configuration having unity gain is shown in Figure 9. For balanced line

applications good common mode rejection is offered by the differential configuration (Fig. 10). In both cases, the inputs are biased to 1/2 V_{DD} by V_{Ref}.

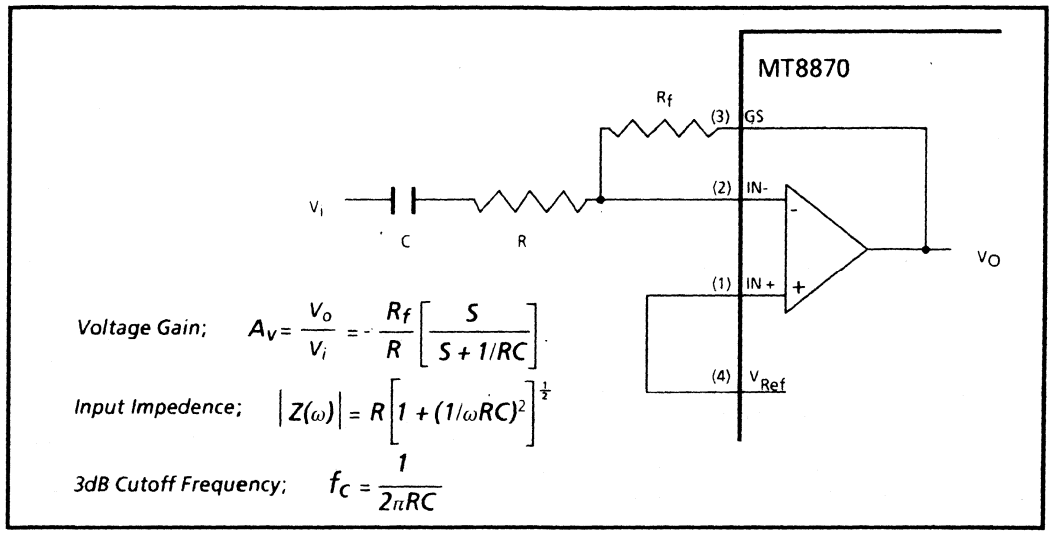


Fig. 9 Single Ended Input Configuration

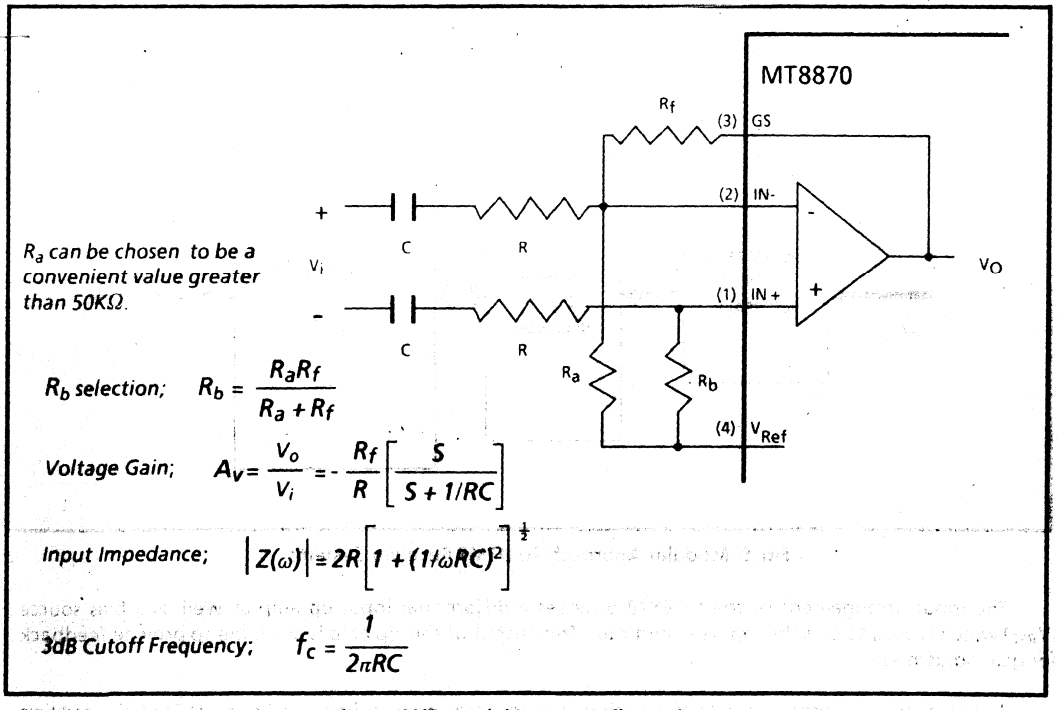


Fig. 10 Differential Input Configuration

Consider an input stage which will interface to a 600Ω balanced line. To reject common mode noise signals, a balanced differential amplifier input provides the solution.

With the input configured for unity gain the MT8870 will accept maximum signal levels of + 1 dBm (into 600Ω). The lowest DTMF frequency that must be detected is approximately 685Hz. Allowing 0.1dB of attenuation at 685Hz, the required input time constant may be derived from;

$$M(\omega)_{dB} = 20log_{10}\frac{R_f}{R} + 20log_{10}\frac{\omega\tau}{\left\{(\omega\tau)^2+1\right\}^{\frac{1}{2}}} \qquad where\ M(\omega)_{dB}\ is\ the\ amplifier\ gain\ in\ decibels$$

ω *is the radian frequency*

τ *is the input time constant*

$$Therefore \quad -0.1 = 20log_{10}\frac{(2\pi)685\tau}{\left\{\left[(2\pi)685\tau\right]^2+1\right\}^{\frac{1}{2}}}$$

$$or\ \tau = 1.52mS$$

Now, choosing R = 220K gives a high input impedance (440K in the passband) and C = τ/R = 6.9nF (use a standard value of 10 nF). For unity gain in the passband we choose $R_f = R$. R_a and R_b are biasing resistors. The choice of R_a is not critical and could be set at, say... 68K. Bias resistor R_a adds a zero to the non-inverting path through the differential amplifier but has no affect on the inverting path. This zero can be exactly cancelled by the added pole due to R_b if R_b is chosen as;

$$R_b = \frac{R_a R_f}{R_a + R_f}$$

With appropriate input transient protection, this circuit will provide an excellent bridging interface across a properly terminated telephone line for end-to-end or key system applications. Transient protection may be achieved by splitting the input resistors and inserting zener diodes to achieve voltage clamping (Fig. 11). This allows the transient energy to be dissipated in the resistors and diodes and limits the maximum voltage that may appear at the op-amp inputs.

It is important to consider the amount of shunt capacitance introduced by the protection devices. In this case the parasitic capacitances of the zener diodes are in series which reduces their effect. Relatively large shunt capacitances will attenuate the high group frequencies causing the input signal to "twist" which degrades receiver performance.

"Twist" is known as the difference in amplitude between the low and high group tones. It is specified in dB as:

$$TWIST = 20 log_{10} \frac{V_L}{V_H} \quad where\ V_L\ is\ the\ amplitude\ of\ the\ low\ frequency\ tone$$

$$and\ V_H\ is\ the\ amplitude\ of\ the\ high\ frequency\ tone.$$

Twist is usually caused by the frequency response characteristic of the communication channel. Along a telephone line higher frequencies tend to roll off faster than the lower ones so the line response is usually compensated for by applying pre-emphasis (negative twist) to the originating DTMF signal. In extreme cases the receiver may require compensation. This could be realized with a filter arrangement utilizing the input op amp.

Any communication path that can pass the human voice spectrum is eligible for DTMF signalling. Therefore a variety of "front-end" interfaces may be applicable in a given control system. More commonly used media are copper wire and RF channels. An optical fibre could carry a light beam modulated by DTMF. Although this would incur a large overhead in terms of bandwidth utilization, optical fibres do offer isolation from external electro-magnetic interference. For example, if control or data signals must be sent near a high power transmission line environment, strong electric and magnetic fields could have a devastating effect on signals transmitted over wires. DTMF over fibre-optics could easily be employed as a highly reliable communications method in a harsh interference infested environment.

In modern digital switching equipment the MT8870 can easily be interfaced to a digital PCM line by using a codec as an input interface (Fig. 12). Actually, all that is required for the interface is a PCM decoder. In fact, the output filter that normally is associated with PCM decoders is not required since the high group DTMF bandpass filter has an upper cutoff frequency low enough to meet the required roll-off of the PCM filter.

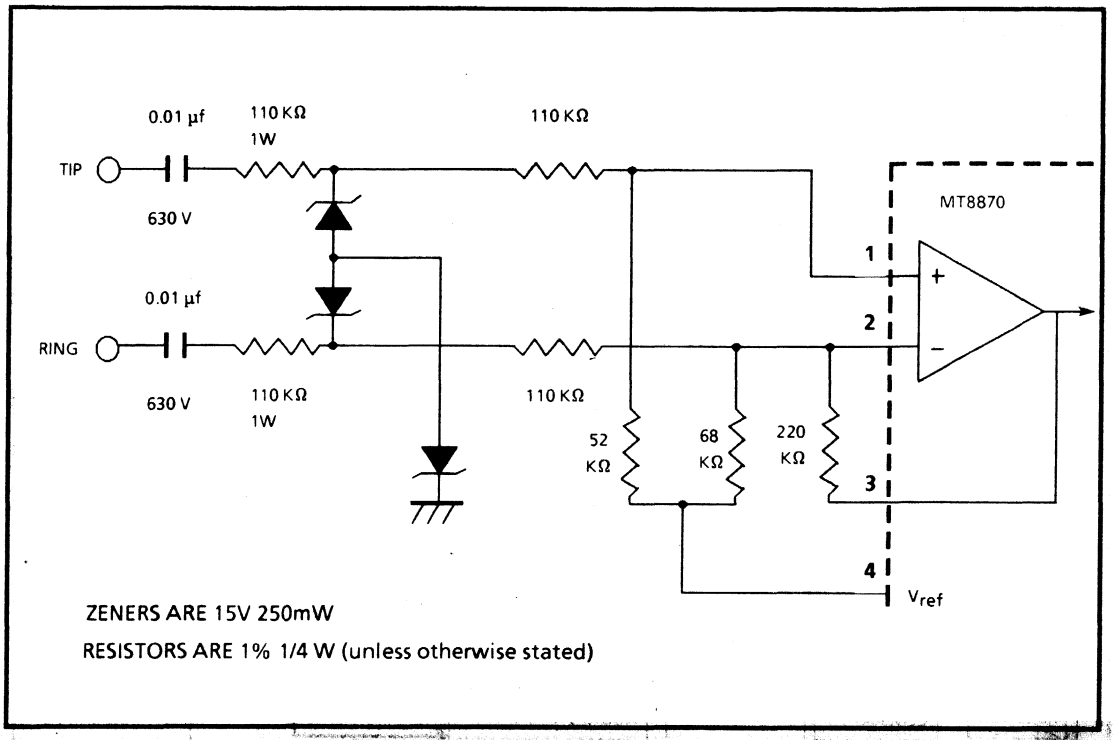


Fig. 11 MT8870 Front End Protection Circuit

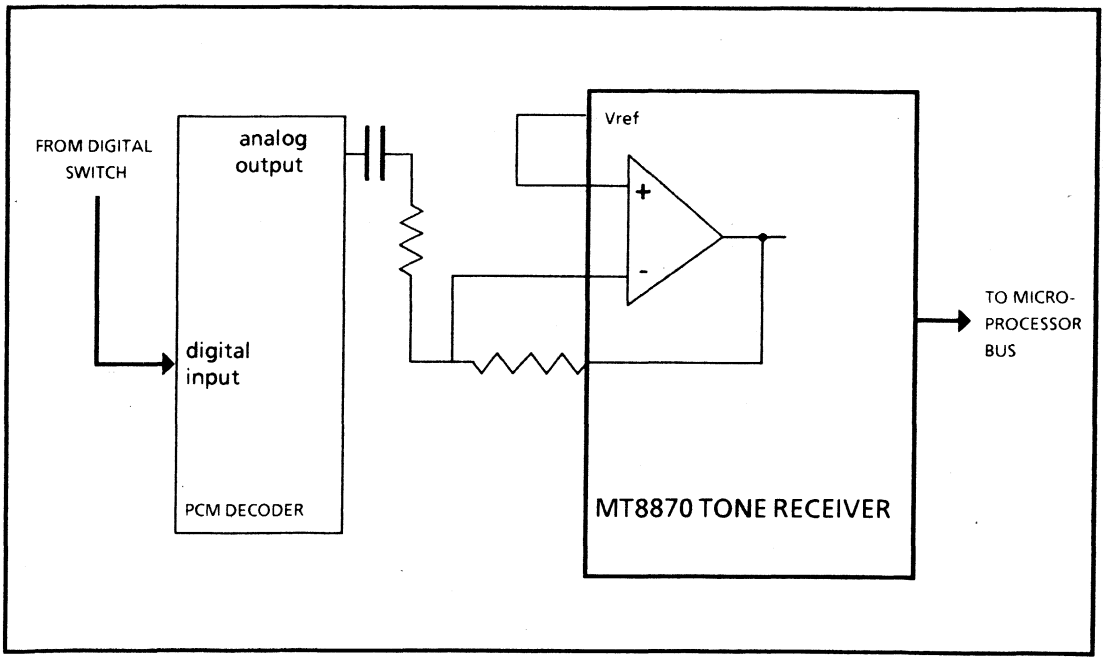


Fig. 12 Interfacing The MT8870 To A Digital PABX Or Central Office

DTMF In Mobile Radio Applications

DTMF signalling plays an important role in distributed communications systems, such as multi-user mobile radio (Fig. 13). It is a "natural" in the two-way radio environment since it slips neatly into the center of the voice spectrum, has excellent noise immunity and highly integrated methods of implementation are currently available. It is also directly compatible with telephone signalling, simplifying automatic phone patch systems.

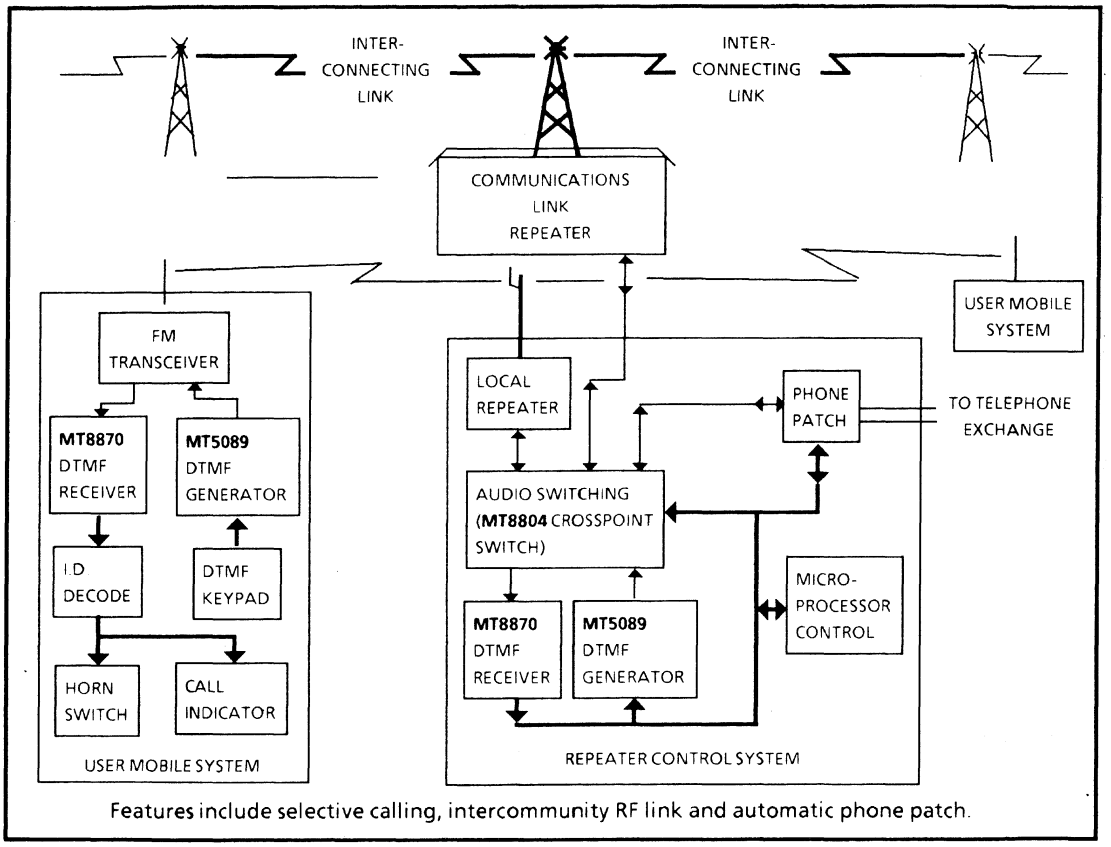


Fig. 13 DTMF Controlled Radio Repeater

Several emergency medical service networks currently use DTMF signals to control radio repeaters. Functions are, typically, mobile identification, selection of appropriate repeater links, selection of repeater frequencies, reading of repeater status, and for completing automatic phone patch links.

If available in a system of this type, audio from a long distance communications link (microwave, satellite, etc.) could be switched, via commands from the user's DTMF keypad, into the local repeater. This would offer the mobile user a variety of paths for communication without the assistance of a human operator.

A multi-channel repeater system serving a multitude of user groups may be found to achieve its most effective performance in the "trunked" mode. In this case, one RF channel is reserved for system signalling. System operation could be achieved as follows.

Each mobile plus the repeater system contain a DTMF receiver, DTMF generator and appropriate

control logic. Mobiles are assigned individual DTMF I.D. codes and always monitor the signalling channel when idle. An originating mobile automatically sends a DTMF sequence containing its own I.D. and the I.D. of the called party. This is recognized by the repeater control which retransmits the called party's I.D. The answering mobile returns a DTMF handshake indicating to the repeater control that it is available to accept a call. At this time the repeater control sends a DTMF command sequence to both the originating and answering mobiles which instructs their logic circuits to switch to a specific, available channel. If all channels are busy the repeater control could send DTMF sequences to put both mobiles on "hold" and add their I.D.'s to a "channel-request" queue. This arrangement would allow users to access any available frequency and converse privately instead of being restricted to one assigned channel which is shared among several user groups.

As well as an individual I.D., each mobile belonging to a particular organization could also have a common group I.D. This would allow dispatch messages to be sent to all company mobiles simultaneously. Since mobiles would be under DTMF control, messages could be sent to an unattended vehicle and, at the user's convenience, displayed on a readout.

Each radio link either established or attempted would result in DTMF I.D. codes being sent to the repeater control. These occurrences could easily be collected by a computer for statistical analysis or billing information. Customers who have defaulted on rental payments could be denied access to the system.

Simplified block diagrams of the control systems for both the repeater and mobiles are shown in Figures 14 and 15 respectively.

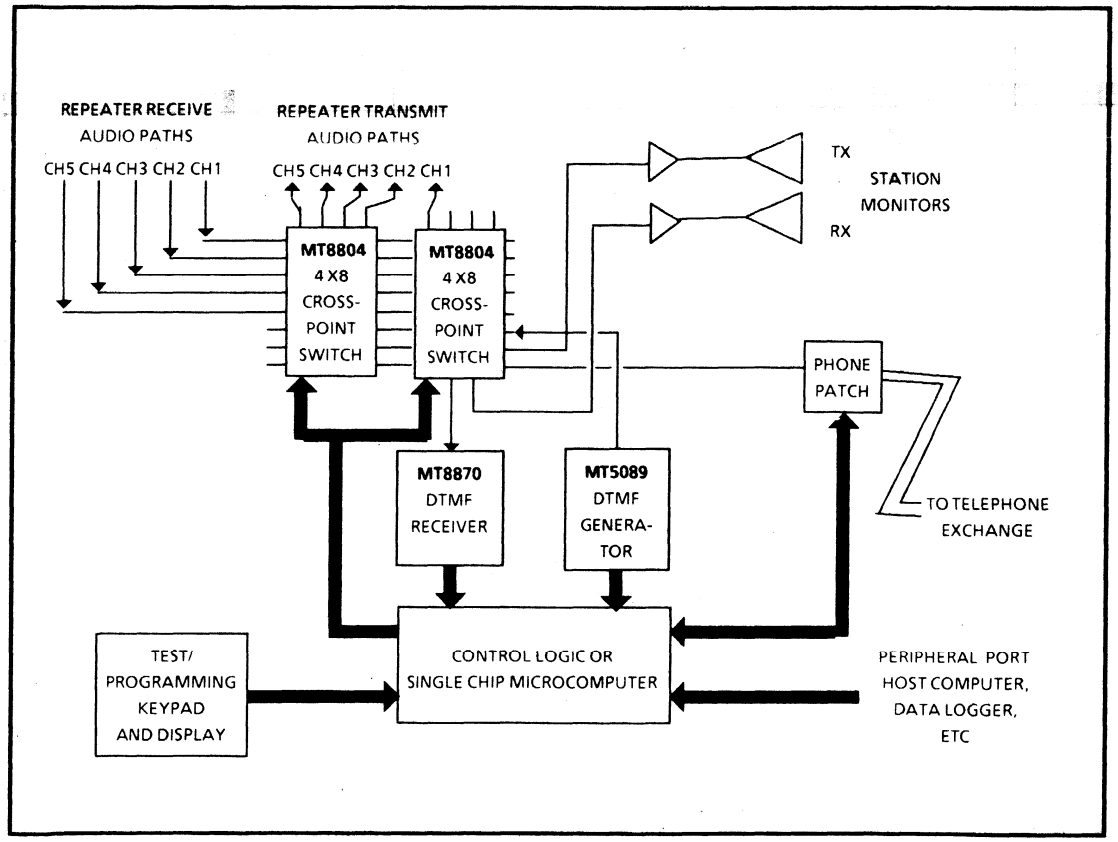


Fig. 14 Block Diagram Of Control For "Trunked" Repeater System

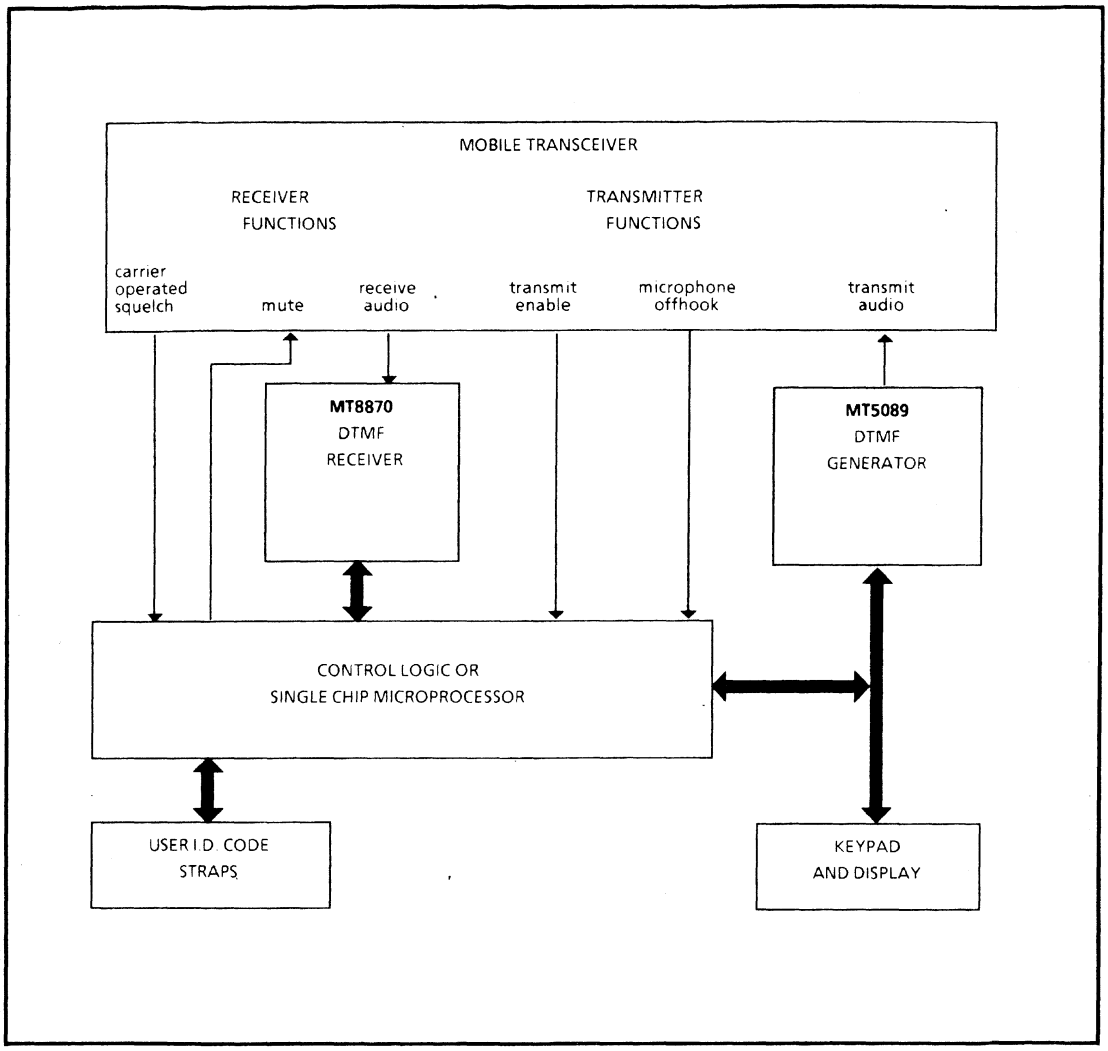


Fig.15 Block Diagram Of Mobile Radio Control System

Distributed Control Systems

There are many other applications which also fall into the distributed communications/control class. That is, several devices being controlled via a common communications medium whether it be RF, copper wire or optical fibres, etc.

Consider, for example, an existing pair of wires circulating throughout a plant. By connecting DTMF receivers at strategic points along this path one could conceivably control the whole plant from a single DTMF transmitter (Fig. 16). Each DTMF receiver would monitor the common line until its specific I.D. was received, at which time it would transfer data to its functional control logic.

With some simple logic a circuit can be devised to recognize a sequence of programmed DTMF code. Figure 17 illustrates a method of detecting a DTMF code sequence of arbitrary length, N. The object is to

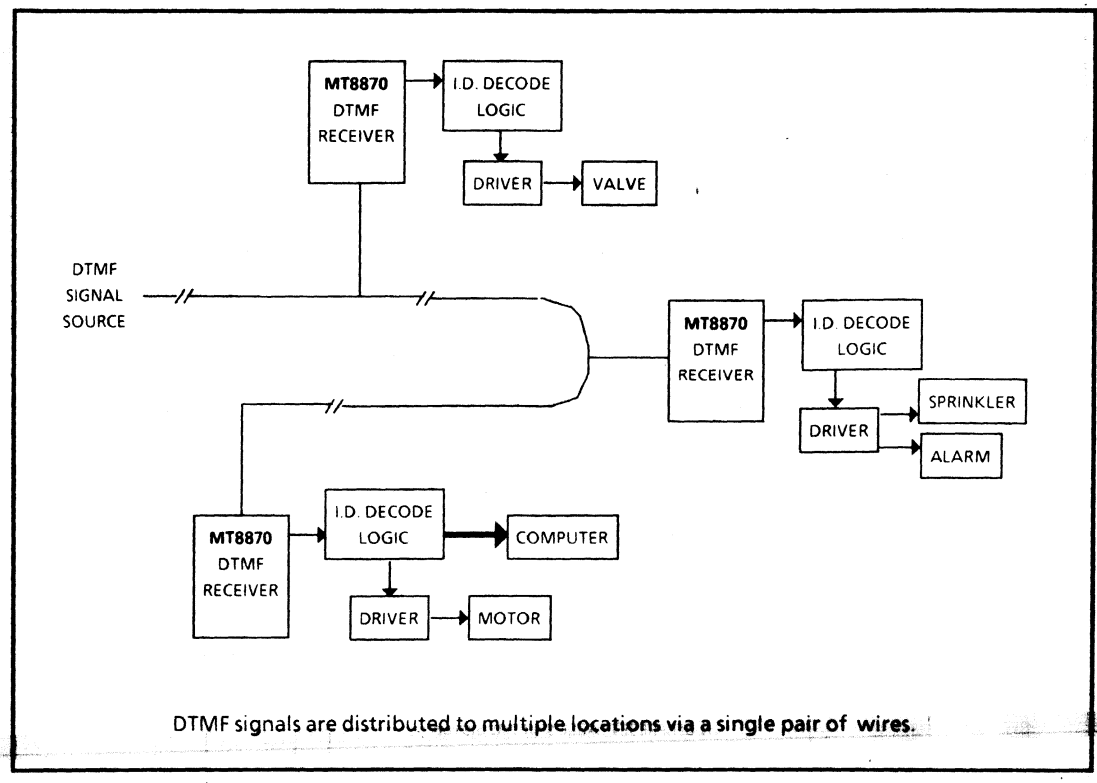
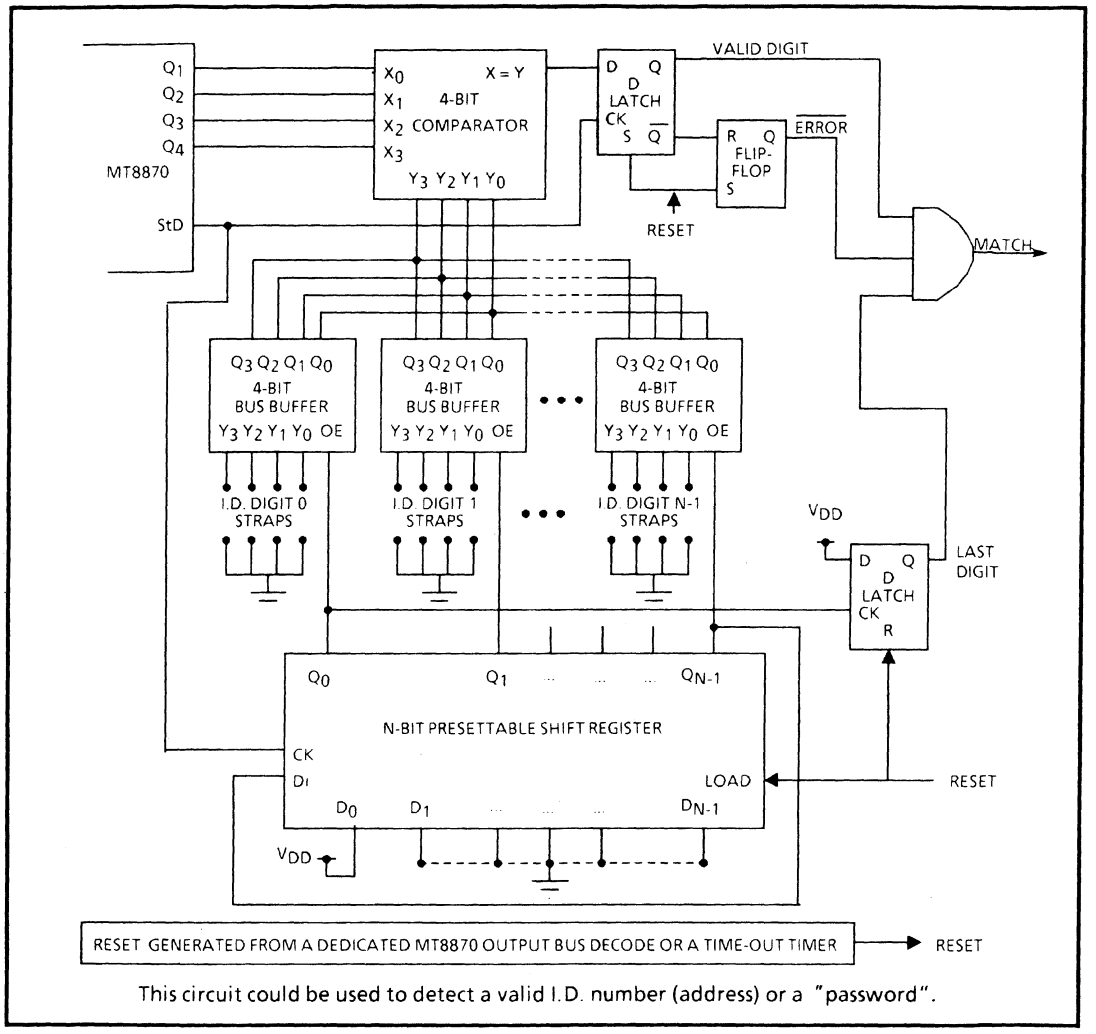


Fig.16 Distributed Control System

compare N sequential 4-bit DTMF data words to N preprogrammed 4-bit I.D. words. Programming the I.D. code is accomplished by applying the desired logic levels to the inputs of N 4-bit bus buffers. This may be achieved with straps as shown, dipswitches or thumbwheels. Pull-up resistors should be applied to the buffer inputs. Initially, after a RESET has occurred, Q_0 of the presettable shift register is set logically high, the remaining outputs are reset. This activates the first bus buffer which applies its outputs to the Y inputs of a 4-bit comparator. The "LAST DIGIT" latch is reset, the "ERROR-" flip-flop and "VALID DIGIT" latch are set. These three signals are ANDed indicating a "no-match" condition. When a valid DTMF signal is received its data appears at the comparators "X" inputs, a comparison occurs and the result appears at the "X = Y" output. After 3.4 µS (typical) Std rises indicating that the MT8870 output data is valid and strobes "X = Y" into the "VALID DIGIT" latch. The shift register advances one position which enables the next bus buffer. If the result of the comparison was true then the "VALID DIGIT" output is high. If all digits of the sequence match then the high output from the shift register "wraps around" from Q_{N-1} to Q_0, which strobes the "LAST DIGIT" latch high. This activates the three input AND gate indicating a "match" condition. If non-matching data is received any time during the detection sequence the "ERROR-" flip-flop is reset which disables the AND gate until a system "RESET" occurs. "RESET" may be generated in a variety of ways depending on the system design objective. If one DTMF code is reserved exclusively for the "RESET" function then the MT8870 outputs can be decoded directly. This requires that the controller send a "RESET" command prior to sending an I.D. sequence. Alternatively a "time-out" timer, triggered by StD, could serve to generate a system reset if a certain time lapse occurs between received signals. This method places time constraints on the system but eliminates the need to consume a DTMF command for the "RESET" function.

The concept of using a common transmission medium for control signalling applies to several possible situations. Plant process control, remote measurement control, selective intercom call systems, institutional intercom systems, two way radio control, pocket pagers and model car or boat remote control, just to mention a few.



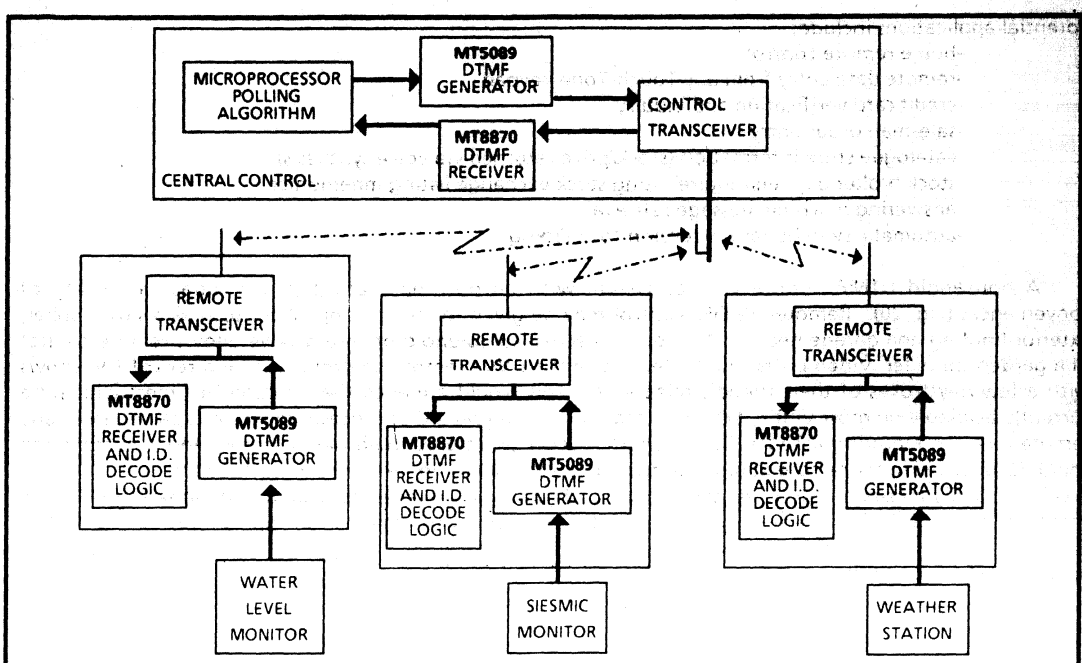
This circuit could be used to detect a valid I.D. number (address) or a "password".

Fig. 17 N- Character Sequence Identifier

Conversely, data could be collected from distributed sources. Implemented on a circulating wire or an RF channel, as illustrated in Figure 18, information could be collected by a central unit which individually polls each monitor to ask for data. Alternatively, the system could be interrupt driven (Fig.19). In this case each monitor, when ready to send data, generates an interrupt request by sending a DTMF I.D. sequence followed by a data stream. Interrupt masking or prioritizing could be achieved from the the central control end by applying DC levels across a wire pair or sending a pilot tone in an RF system. Remote data collection units would monitor this signal to detect when a higher priority interrupt is being handled or the communications channel is busy.

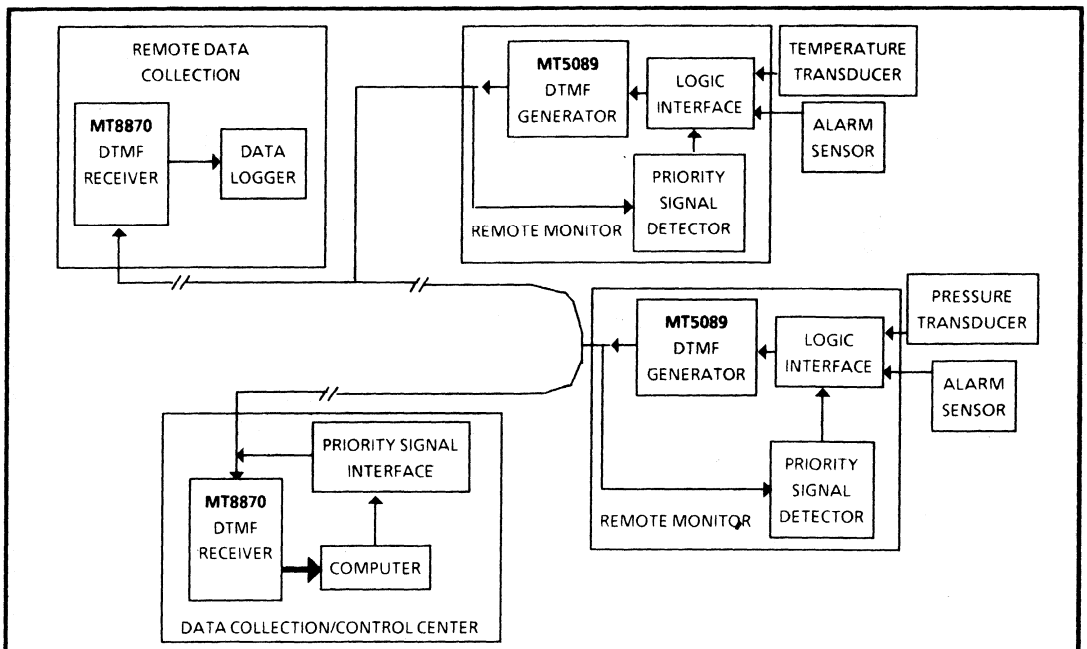
Data Communication Using DTMF

There is a vast array of potential applications for DTMF signalling using the existing telephone network. Considering that there are millions of ready-made data sets installed in convenient locations (i.e. the Touch Tone™ telephone) remote control and data entry may be performed by users without requiring them to carry around bulky data modems.



Polling system for multiple location remote data collection.

Fig. 18 DTMF Controlled Data Collection



Remote monitors send data while the interconnecting pair of wires is clear of other interrupts.

Fig. 19 Interrupt Driven Data Collection System

Potential applications include:

-home remote control
-remote data entry from any Touch-Tone keypad
-credit card verification and inquiry
-salesman order entry
-catalogue store information (stock/price returned via voice synthesis)
-stock broker buy/sell/inquire -using stock exchange listing mnemonics
-answering machine message retrieval
-automatic switchboard extension forwarding

A household DTMF remote control system with an optional data port can boast a variety of conveniences (Fig. 20). Remote ON/OFF control may be given to electric appliances such as a slow cooker, exterior lighting and garage heater. An electro-mechanical solenoid operated valve allows remote control of a garden sprinkler. Video buffs could interface to their VCR remote control inputs and record T.V. shows with a few keystrokes of their friend's telephone. This would enhance the function of timers which are currently available on most VCR's. Schedule changes or unexpected broadcasts could be captured from any remote location featuring a Touch-Tone™ phone. Security systems could be controlled and a microphone could be switched in for remote audio monitoring. Interfacing a home computer to the data port makes an excellent family message center. At the remote end messages are entered from a telephone keypad. The computer responds with voice messages generated by a speech synthesizer. In the home, messages to be left are entered via the computer keyboard. Messages to be read may be displayed on the computer monitor or "played back" through the speech synthesizer.

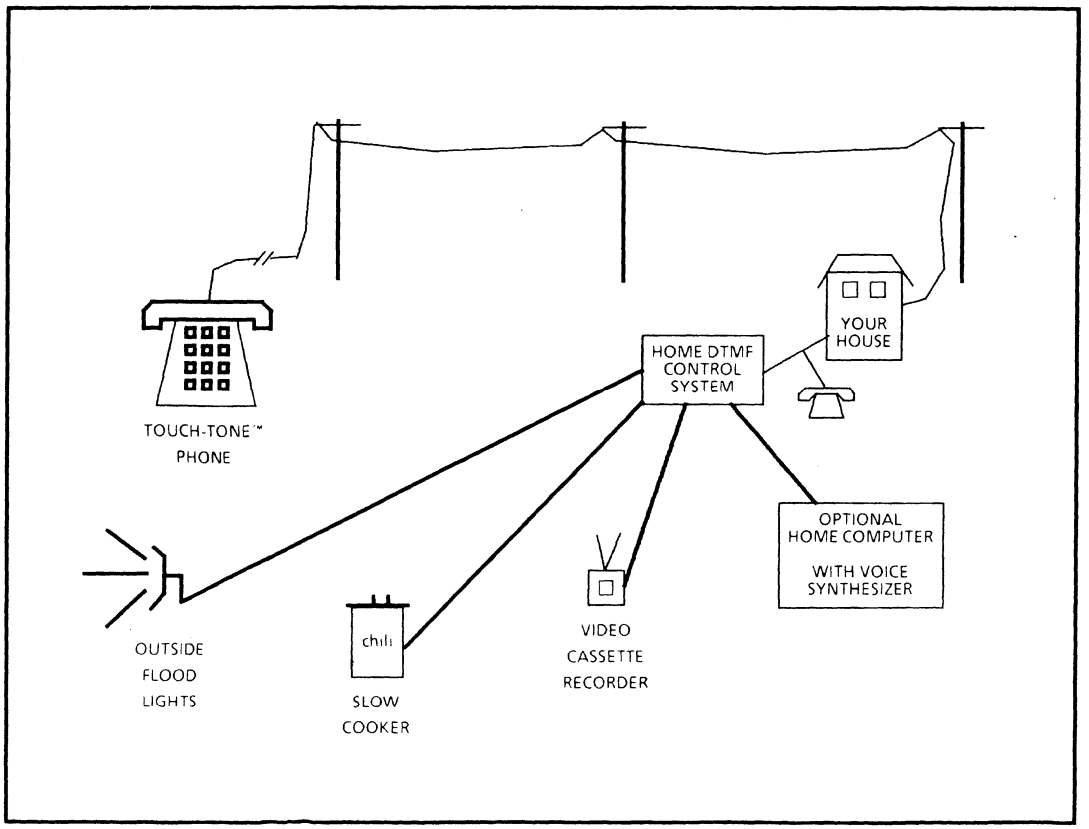
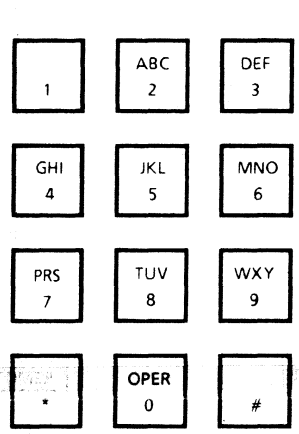
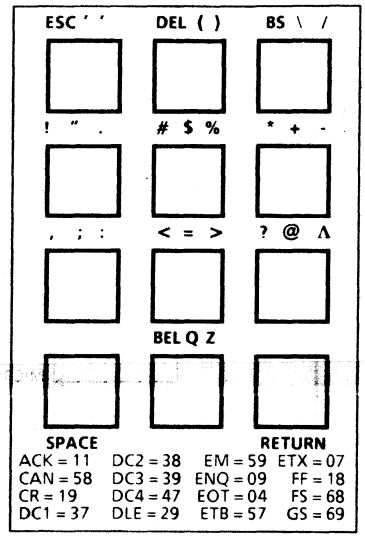


Fig. 20 Home DTMF Remote Control System

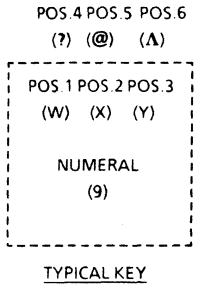
A scheme for coding ASCII characters using one and two digit DTMF signals is outlined in the appendix. Notice that on a telephone keypad keys 2 through 9 are represented by three alpha-characters as well as a numeral. To send an alpha-character, using this scheme, first press the key on which the character appears then press the key corresponding to the position in which the character appears on its key (1, 2 or 3). Numerals are sent by touching the desired number followed by a zero. The asterisk (*) and octothorp (#) have been reserved for "space" and "return" respectively. A plastic overlay the size of a credit card expands the number of useable "positions" on each button (Fig. 21). This serves as a guide for sending other ASCII codes and fits snug into a credit card wallet. ASCII control characters that are not commonly used could be listed at the bottom of the card. This user-friendly algorithm eliminates the need to memorize conversion codes and allows significant functionality even without the overlay reference.



(a)



(b)



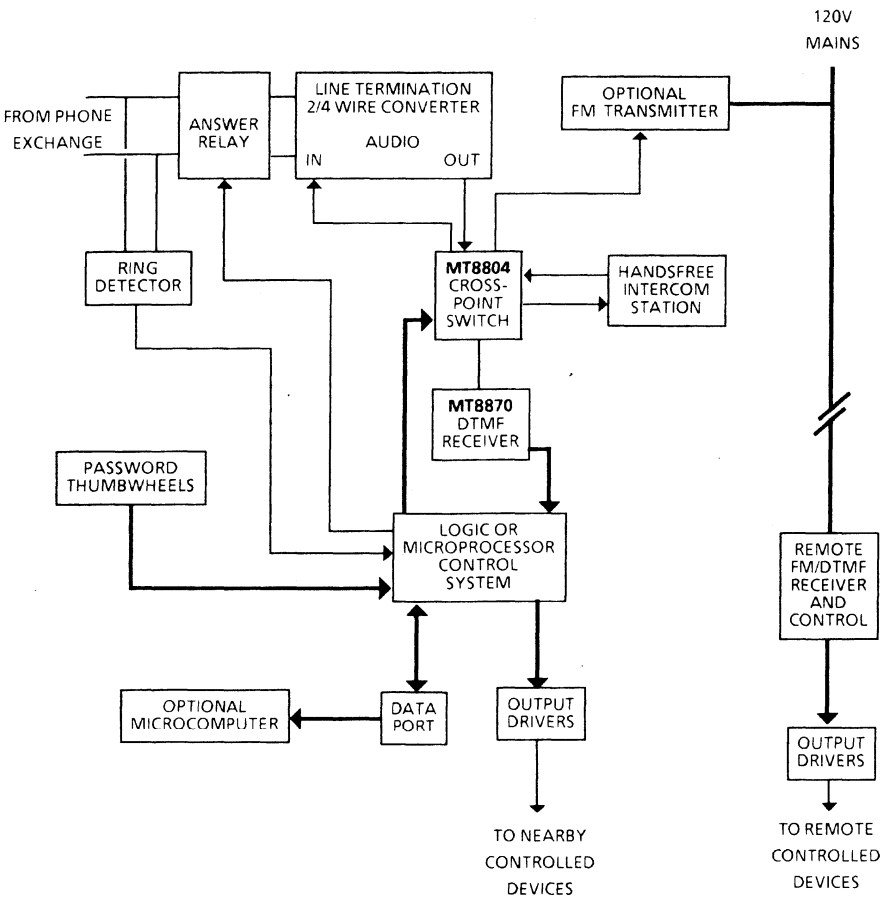
TYPICAL KEY

KEYS "2" THROUGH "9" EACH REPRESENT THREE ALPHABETIC CHARACTERS HENCE HAVE THREE INHERENT "POSITIONS" (POS.1,POS.2, AND POS.3) A PLASTIC OVERLAY CARD ADDS THREE MORE POSITIONS (POS.4,POS.5,AND POS.6) TO KEYS "1" THROUGH "0". * AND # ARE RESERVED EXCLUSIVELY FOR THE SPACE AND RETURN FUNCTIONS.

a) Layout of a standard telephone keypad showing inherent character positions for coding purposes.
b) Credit card size overlay expands each keys function by adding three more character positions.
The * and # are reserved to send "SPACE" and "RETURN" as single key operations. Each other ASCII code requires two keystrokes. To send a character simply push the button on or over which it appears, then push the numeral corresponding to its position . For example, to send a "T" push '8' followed by '1', to send "%" push '5' followed by '6'.

Fig. 21 Using A Pushbutton Phone As A Data Terminal

A simple block diagram shows how this scheme may be implemented for a home DTMF control system (Fig. 22). A ringing voltage detector signals the microprocessor of an incoming call. The microprocessor, after the prescribed number of rings, closes the answer relay engaging the proper terminating impedance. A two-to-four wire converter splits bidirectional audio from the balanced telephone line into separate single ended transmit and receive paths.



An FM transmitter could be used to couple control signals for distribution over existing power lines. This would eliminate the need for installing wires between the DTMF control unit and remote controlled devices.

Fig. 22 Block Diagram Of Home DTMF Remote Control System

Receive audio is then switched to the DTMF receiver through the crosspoint switch. Upon receiving a valid DTMF signal, the microprocessor is alerted by the rising edge of StD. The microprocessor then checks for a valid password sequence and decodes subsequent commands. A command can be entered to put the system into remote-control mode. In this case the crosspoint switch is configured to route DTMF signals into the FM-over-mains transmitter as well as the system tone receiver. Forwarding of control signals is accomplished by applying an FM carrier to the power line. This eliminates the need to string control wires haphazardly about the house. The appropriate device is selected by its unique DTMF I.D. code. The microcomputer keeps track of all device locations and their I.D. codes since it must decide when to supply function outputs to the "nearby" devices and when to let the "remote" receivers handle the data.

Subsequent data is transmitted to a selected device until a 'reset' command is entered.

Upon receiving any DTMF signal, answer back tones are returned by the microprocessor to acknowledge valid or invalid operations and to indicate the state of an interrogated device. For example, a low to high tone transition could indicate that a particular device is on, a high to low transition indicating the off state. A command could be entered to put the system in an 'external' mode which would allow communications through the data port. A host computer could be connected to this port to broaden the scope of the system.

The resident microprocessor unit contains the software and hardware to control ringing verification, password and command decoding, answer back tone generation, audio routing, output function latches and an optional data port. Output drivers buffer the latches and switch relays or SCRs to control peripheral devices.

An infinite variety of devices could be controlled by such a system, the spectrum of which is limited only by the ability to provide appropriate interfacing. This system could also be the heart of a DTMF intercom system allowing intercommunication, "phone-patching", and remote control from varied household locations. This type of system concept is, of course, anything but limited to home use. Many applications can provide conveniences to consumers, salsepeople and executives.

For example, a merchant could verify credit card accounts quickly utilizing only a telephone keypad for data entry (Fig. 23). Each credit card company could reserve one or more telephone lines to provide this function, reducing the human effort required. The receiving end system would be required to answer the call, provide a short answer back tone or message, receive and decode the credit card account number, verify it, verify the owner's name and give a go/no-go authorization. This return data could easily be provided with the aid of a voice synthesizer. An auto-dialler containing appropriate phone numbers could be installed at the merchant end as an added time saver.

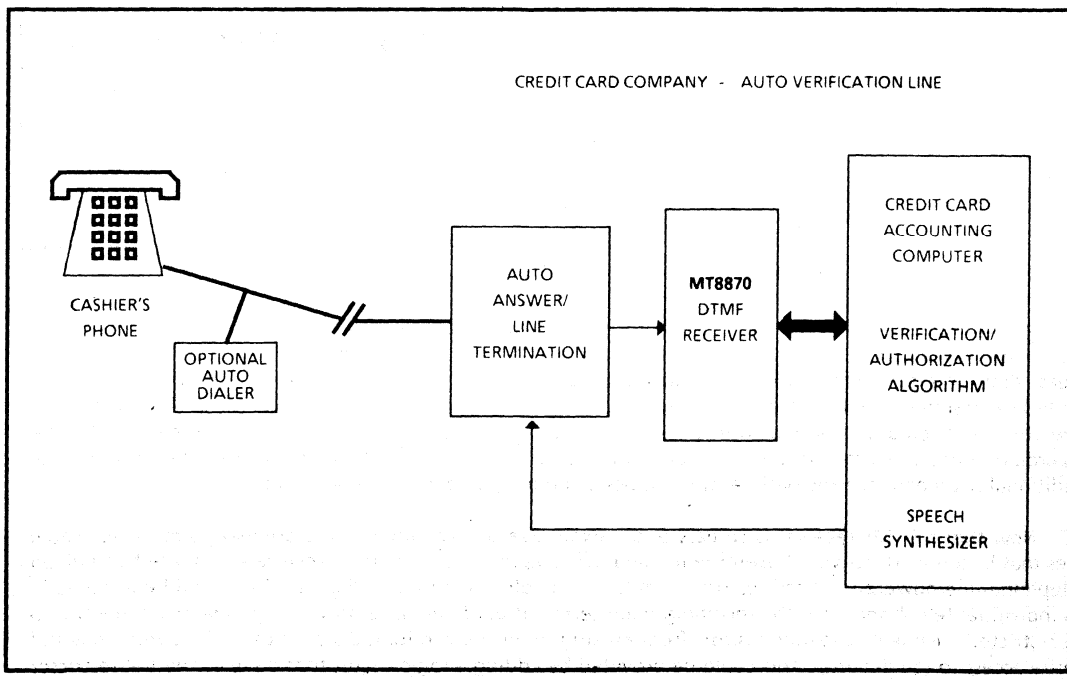


Fig. 23 DTMF Data Communications For An Auto Verification Line

With a similar arrangement, a travelling salesman could access price, delivery and customer status, enter or delete merchandise orders and retrieve messages all from the comfort of the customer's office (Fig. 24a). A department store could provide shop-by-phone service to its customers using telephone keypad data entry (Fig. 24b). Brokerage firms, utilizing the stock exchange mnemonic listings could provide trading price information and buy/sell service via telephone keypad entry. A voice synthesizer could provide opening and current trading price, volume of transactions and other pertinent data. A telephone answering system manufacturer could apply this technique, allowing users to access and change outgoing and incoming messages from a Touch-Tone™ phone.

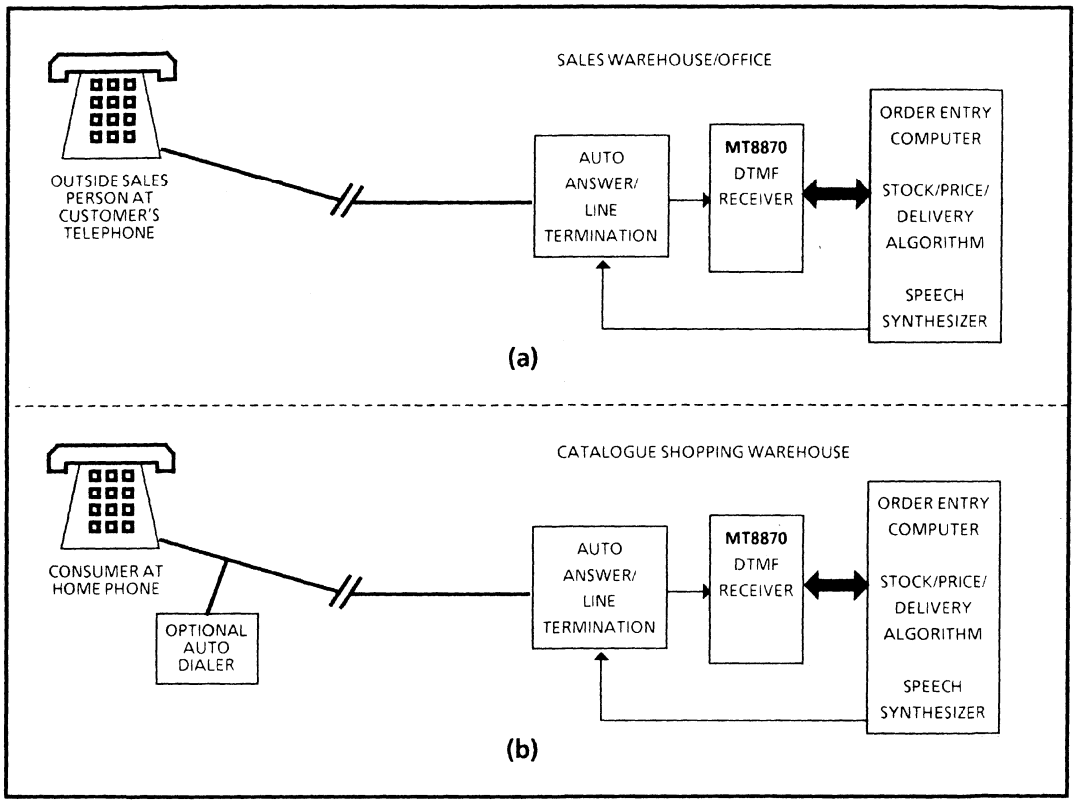


Fig. 24 Two Applications Of DTMF Data Communications

A PBX manufacturer could offer a feature that relieves the switchboard attendant from unneccesary interaction. A call could be answered automatically and a recording may reply "Thank you for calling XYZ. Please dial the extension you wish to contact or zero for the switchboard". If the caller knows the called party's extension in advance it is not neccesary to wait for the switchboard attendant to forward the call. The attendant could be notified to intervene if there is no action by the caller say, ten seconds after the recording ends. This provides a similar function to a "Direct Inward Dialling" (DID) trunk but without the additional overhead incurred with renting a block of phone numbers as in the DID case.

Now that a DTMF receiver is so easy and inexpensive to implement there are many simple dedicated uses that become attractive. A useful home and office application for DTMF receivers is in a self-contained telephone-line-powered toll call restrictor similar to the block diagram in Fig. 2a. This could be installed in an individual telephone or at the incoming main termination depending on which phone or phones are to be restricted. While disallowing visitors from making unauthorized long distance calls, the owner may still desire access to toll dialling. This could be provided by adding a logic circuit that disables the toll restrictor upon receiving a predetermined sequence of DTMF characters (Fig. 17). In this case, the user must enter his

password before dialling a long distance number.

Conclusion

The applications for DTMF signalling are tremendous and due to innovative technological advances its use is increasingly widespread. DTMF offers highly reliable, cost effective signalling solutions which require no development effort on the user's part. The advent of single chip receivers has allowed many products that were previously not cost-effective to be manufactured in production quantities.

DTMF signalling was originally designed for telephony signalling over voice quality telephone lines. This signalling technique has been applied to a multitude of control and data communications systems. All that is required is a voice quality communication channel with appropriate interfacing. The applications are limited only by one's imagination.

Appendix

ASCII TO DTMF CONVERSION

Partial ASCII coding and conversion to 2 sequential DTMF signals

ASCII	HEX	DTMF	ASCII	HEX	DTMF	ASCII	HEX	DTMF
ACK	06	1 1	!	21	4 4	A	41	2 1
BEL	07	0 1	"	22	4 5	B	42	2 2
BS	08	3 4	#	23	5 4	C	43	2 3
CAN	18	5 8	$	24	5 5	D	44	3 1
CR	0D	1 9	%	25	5 6	E	45	3 2
DC1	11	3 7	&	26	7 9	F	46	3 3
DC2	12	3 8	'	27	1 6	G	47	4 1
DC3	13	3 9	(	28	2 5	H	48	4 2
DC4	14	4 7	)	29	2 6	I	49	4 3
DEL	7F	2 4	*	2A	6 4	J	4A	5 1
DLE	10	2 9	+	2B	6 5	K	4B	5 2
EM	19	5 9	'	2C	7 4	L	4C	5 3
ENQ	05	0 9	-	2D	6 6	M	4D	6 1
EOT	04	0 8	.	2E	4 6	N	4E	6 2
ESC	1B	1 4	/	2F	3 6	O	4F	6 3
ETB	17	5 7	0	30	0 0	P	50	7 1
ETX	03	0 7	1	31	1 0	Q	51	0 2
FF	0C	1 8	2	32	2 0	R	52	7 2
FS	1C	6 8	3	33	3 0	S	53	7 3
GS	1D	6 9	4	34	4 0	T	54	8 1
HT	09	1 2	5	35	5 0	U	55	8 2
LF	0A	1 3	6	36	6 0	V	56	8 3
NAK	15	4 8	7	37	7 0	W	57	9 1
NUL	00	0 4	8	38	8 0	X	58	9 2
RS	1E	7 7	9	39	9 0	Y	59	9 3
S0	0E	2 7	:	3A	7 6	Z	5A	0 3
S1	0F	2 8	;	3B	7 5	[	5B	8 7
SOH	01	0 5	<	3C	8 4	\	5C	3 5
SP	20	*	=	3D	8 5	]	5D	8 8
STX	02	0 6	>	3E	8 6	^	5E	9 6
SUB	1A	6 7	?	3F	9 4	_	5F	8 9
SYN	16	4 9	@	40	9 5	`	60	1 5
US	1F	7 8				DEL	7F	2 4
VT	0B	1 7						

Application Note MSAN-112
T1/DS1 Digital Trunk Interface Solutions Using The MT8975/MH89750

9161-001-031 NA ISSUE 1 April 1986

TABLE OF CONTENTS

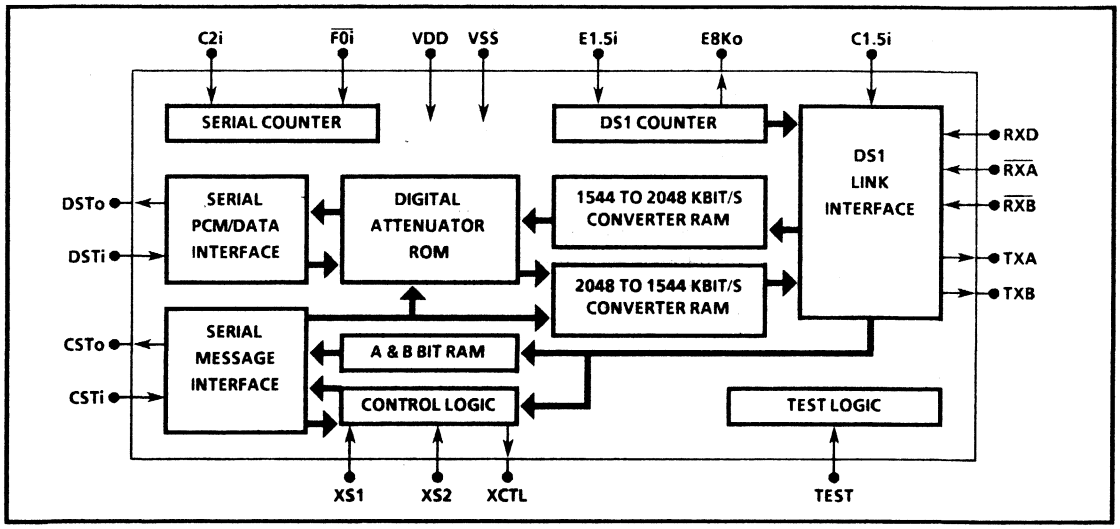
Introduction

Since the deregulation of the telephone industry the demand for more and better services has been on the rise. Many of the new services are being carried to subscribers via high speed digital transmission links. The use of T1/DS1 technology leads the way in providing these services. Mitel manufactures three different T1 trunk solutions to satisfy the needs of the T1 user, the MT8975, the MH89750 and the MH89756. These devices are used in a wide variety of telecom applications such as PBX's, Channel Banks, and Digital Central Offices. T1 interfaces are also becoming widely used in the data transmission market, and they will also be a major digital carrier in the ISDN scheme.

This application note will deal with the first two components, the MT8975 and the MH89750. The MT8975 and the MH89750 are designed to interface an asynchronous digital transmission line to a synchronous serial bussing system, operating at 2.048 MHz. The digital transmission line is a D3/D4 format T1 digital trunk. The 2.048 MHz serial bussing system is known as the ST-BUS or Serial Telecom Bus. These devices contain all of the required sections to interface to a digital trunk, as well as all of the buffering and reformatting required to interface to the ST-BUS system.

The MT8975 is a CMOS I.C. available in a 20 pin ceramic DIP or a 24 pin LCC package. The MH89750 is a 40 pin ceramic hybrid that contains the MT8975 plus additional interface circuitry.

Sections 1 through 4 of this document describe the detailed operation of the MT8975. Sections 5 and 6 describe those additional features incorporated in the MH89750.



Functional Block Diagram MT8975

TABLE OF CONTENTS

1.0 Detailed Functional Description, MT8975

The MT8975 is a single chip solution of a T1 interface. It contains both transmitter and receiver circuits as well as the received elastic buffer. All of the formatting and rate adaptation between the ST-BUS and T1 line is done internally.

1.1 Transmitter Section

The MT8975 assembles the data and control information received on the ST-BUS into the 24 channels plus an S bit used in D3/D4 format. The transmitter inserts the A and B bits into the proper frame, performs zero code suppression, enables or disables the yellow alarm, and outputs the steering signals used to generate the Alternate Mark Inversion (AMI) line code.

1.1.1 D4 Format

D3/D4 format is made up of 24 8 bit channels and a single bit, the S bit, that is used to define the frame and superframe boundaries. Figure 1 illustrates the D3/D4 format. Figure 2 shows the two patterns that are multiplexed into the S bit. The Terminal Framing pattern is used to define the frame boundaries, and the Signalling Framing pattern defines the 12 frame multiframe. The S bit pattern is generated internally and inserted into the transmitted signal to create a D3/D4 format output stream.

1.1.2 A, B, Bit Insertion/Common Channel Signalling

When to insert the signalling bits into the T1 bit stream is determined by the Signalling Framing portion of the S bit pattern. A '0' to '1' transition in

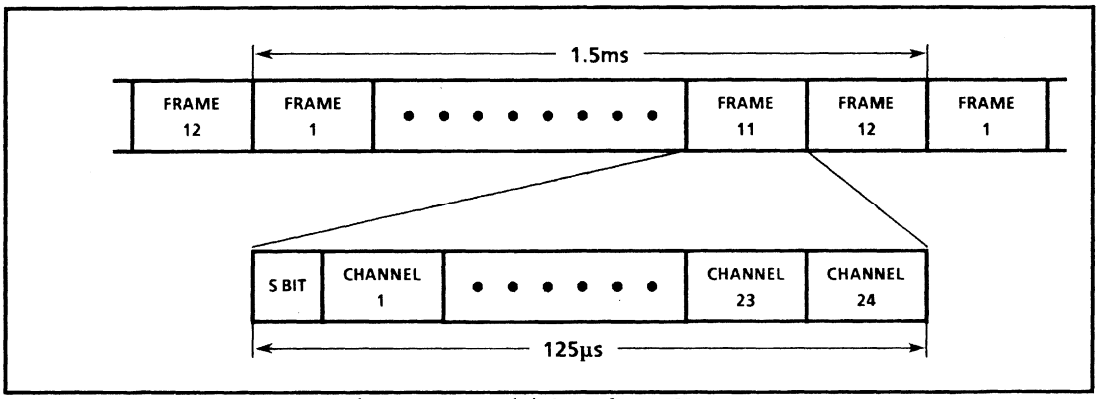


Figure 1 - DS1 Link Superframe Format

FRAME NUMBER	SBIT		BIT NUMBERS IN CHANNELS		SIGNALLING CHANNEL
	Terminal Frame Pattern	Multi. Frame Pattern	Character Bits	Signalling Bit	
1	1		1-8		
2		0	1-8		
3	0		1-8		
4		0	1-8		
5	1		1-8		
6		1	1-7	8	A
7	0		1-8		
8		1	1-8		
9	1		1-8		
10		1	1-8		
11	0		1-8		
12		0	1-7	8	B

Figure 2 - S Bit Framing Pattern

the F_s pattern indicates that the least significant bit of every channel in the following frame contains the A bit, and a '1' to '0' transition indicates that least significant bit of every channel in the following frame contains the B bit. The A and B signalling bits, for each of the 24 channels, are input through the Control ST-BUS interface and inserted into the proper frame by the MT8975.

Robbed bit signalling, or A, B bit signalling, can be disabled to allow the use of common channel signalling. In a common channel signalling environment the information is input via the ST-BUS interface in one of the standard channels. The most likely situation is that channel 24 would be used to send a packet type of protocol such as CCITT Q.931. This would increase the flexibility of the network greatly over the four state robbed bit signalling that is used at the present.

See Section 3.0 for more information on the ST-BUS interface.

1.1.3 Alarm Transmission

The MT8975 has the ability to enable or disable the transmission of the yellow, or remote alarm. When the yellow alarm is active bit 2 of all output channels is transmitted as a '0' until the yellow alarm is disabled. The transmit yellow alarm is activated when the system detects loss of frame synchronization for a period of two to three seconds. The system software must time the frame synchronization signal externally. The transmit yellow alarm indicates to the far end that the near end is unable to synchronize to the signal that it is receiving.

1.1.4 Zero Code Suppression, B8ZS

There are two line code options available in the MT8975, Alternate Mark Inversion (AMI), and Bipolar 8 Zero Substitution (B8ZS). In AMI, a 1 (one) is transmitted as a pulse and a 0 (zero) is transmitted as no pulse. Alternate 1's are sent as pulses of opposite polarity. If a channel contains all 0's then bit 2 of that channel is jammed to a '1'.

For B8ZS the output code is still AMI except that any block of eight 0's is replace by a sequence of marks and spaces with bipolar violations inserted in predetermined locations. For example, a string of eight 0's would be replaced by the following sequence: 000VB0VB where V stands for a violation and B stands for a valid pulse. A violation is the occurrence of two pulses of the same polarity in a row. The block of eight 0's is not confined by frame or channel boundaries as it is for standard AMI line code. Figure 3 illustrates the two possible output codes that are produced by B8ZS.

1.2 Receiver

The receiver searches for and monitors the frame synchronization, signalling bits and yellow alarm. It also contains a 2 frame elastic buffer to perform slips, and accommodate received bit jitter.

1.2.1 Frame Synchronization

The receive section of the MT8975 searches the incoming bit stream to find the S bit pattern that will define the frame and superframe boundaries. The receiver performs an integration of the terminal framing portion of the S bit pattern to establish synchronization. The algorithm has an out-of-frame slope that is four times greater than the in-frame slope. This enables the circuitry to withstand errors within the F_t portion of the S bit pattern. The MT8975 is guaranteed out-of-frame for two out of four, to two out of five errors. The worst case average reframe time is approximately 14 msec. Worst case average reframe time is defined as the time required to reframe when the maximum number of bits must be examined, in the absence of errors.

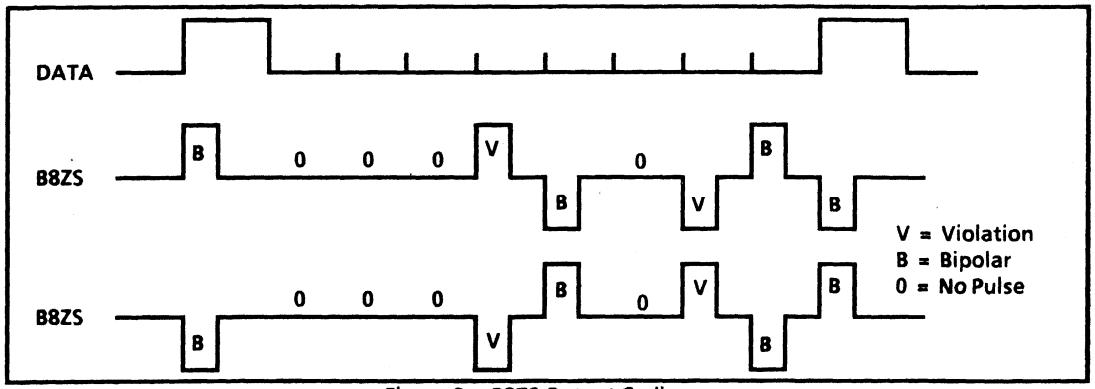


Figure 3 - B8ZS Output Coding

1.2.2 A, B Bit Detection

The A and B signalling bits are extracted from the received data once the chip is synchronized. When the chip is in sync the 6th and 12th frames can be identified by the signalling framing pattern that is present in the F_s portion of the S bit position. The receiver extracts the A and B signalling bits by monitoring the F_s portion of the S bit pattern by looking for the '0' to '1' and '1' to '0' transition in the same manner as the transmitter does when inserting the signalling bits.

1.2.3 A, B Bit Debounce

The A and B bits are debounced and stored in the signalling RAM. They are debounced for five superframes, or 7.5 to 9.0 msec. This eliminates the need for an external debounce circuit, but still detects a pulse width of 10 msec. Signalling bit debouncing is active at all times. If a valid set of signalling bits must be retained when the interface loses synchronization then a software image of the signalling bits should be kept in system RAM. The image should only be updated after checking the frame synchronization. The debounce time ensures that the new A and B bits are valid if all 24 channels are read within 7.5 msec.

1.2.4 Received Alarm

Bit position 2 of each channel is continually monitored for consecutive 0's. If bit 2 of every channel has been 0 for 596 msec the received alarm is activated. The detection algorithm uses an integrator so that the detection circuitry is resistant to errors in bit position 2. The 596 msec detect time leaves the software ample time to meet the 300 to 1000 msec detect time for the system. The alarm signal releases in 200 msec.

1.2.5 Bipolar Violations, B8ZS

Bipolar violations are counted by an internal 8 bit counter, and reported every time the counter reaches 256. The minimum sample period used by the bipolar violation counter is 96 msec. This restricts the maximum error rate that can be calculated from this information. Any violations that are caused by B8ZS code are not included in this count.

1.2.6 Elastic Buffer

1.2.6.1 Slip Buffer

Once the received data has been processed the channels are passed through the 2 frame elastic buffer. This elastic buffer allows the chip to do a controlled slip. That is, if the received data is arriving at an average speed that is greater than the speed that the ST-BUS is removing the data then the elastic buffer will eventually overflow or slip. In this case, one complete frame of received data will be lost. In other words, it will not be output on the ST-BUS. If the received data is arriving slower than ST-BUS is removing data then the elastic buffer will repeat one complete frame of information when it slips. The elastic buffer is 2 frames long, but the maximum throughput delay is restricted to 1.3 frames. The size of the buffer restricts the slip rate of a free running system to a reasonable limit, but still keeps the throughput delay acceptable.

1.2.6.2 Jitter Buffer

Incorporated within the elastic buffer there is also a jitter buffer. The guaranteed size of the jitter buffer is 31.25 µsec. The receiver will, therefore, accept 31.25 µsec peak to peak jitter. Jitter is the short term variations in the received data rate or the variation in the pulse position. The primary cause is variations in the repeater thresholds over the length of the transmission line. The elastic buffer absorbs these small variations in the received data rate so that the received data can be output on the system side of the MT8975 at a fixed rate.

2.0 Digital Line Interface

The MT8975 provides a unipolar digital interface and as such it can not interface directly to the T1 transmission line. In order to do this a Digital Line Interface is required. This line interface must convert the unipolar outputs that swings from 0 to +5V into the bipolar AMI signal on the transmission line that swings from approximately +3V to -3V.

2.1 Transmitter

2.1.1 TxA, TxB Steering Signals

In order to generate the AMI signal with a minimum number of external components the transmitter provides the user with two bipolar steering circuits. These two outputs, TxA and TxB, correspond to the required positive and negative pulses on the transmission line. Figure 4 illustrates how TxA and TxB relate to the AMI pulses on the line.

2.1.2 External Output Drivers and Transformers

TxA and TxB are the signals used to drive the bipolar transistors which in turn drive the line coupling transformer. Figure 5 shows a

recommended output circuit for TxA and TxB. The transistors are driven into saturation when they are turned on, which applies a step function to the transformer. The step input to the transformer produces a very nearly constant di/dt before the current reaches steady state. By operating in the transient portion of the inductance response the secondary of the transformer produces an almost square pulse. The base terminal of the transistors is AC coupled to the MT8975 so that there is no DC path from the 12 volt supply to ground. The detailed transformer specification is in Appendix A.

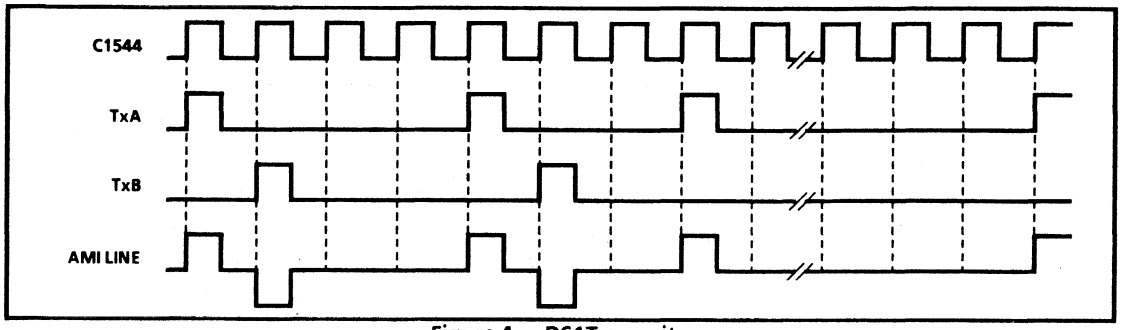


Figure 4 - DS1Transmit

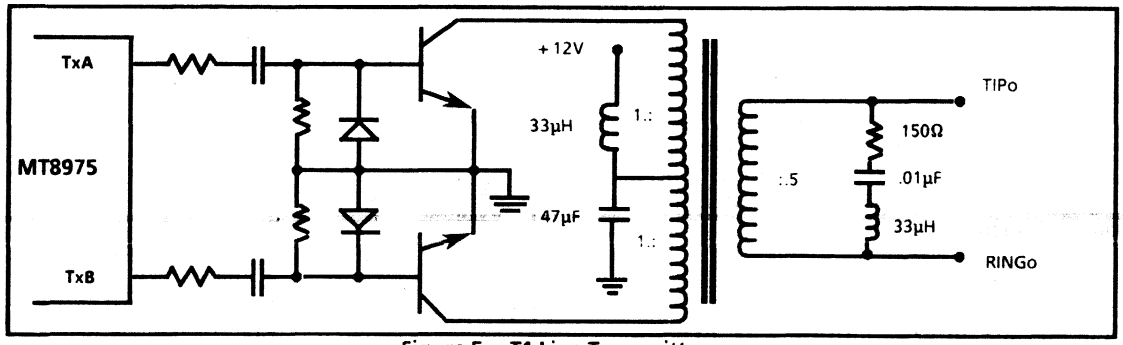
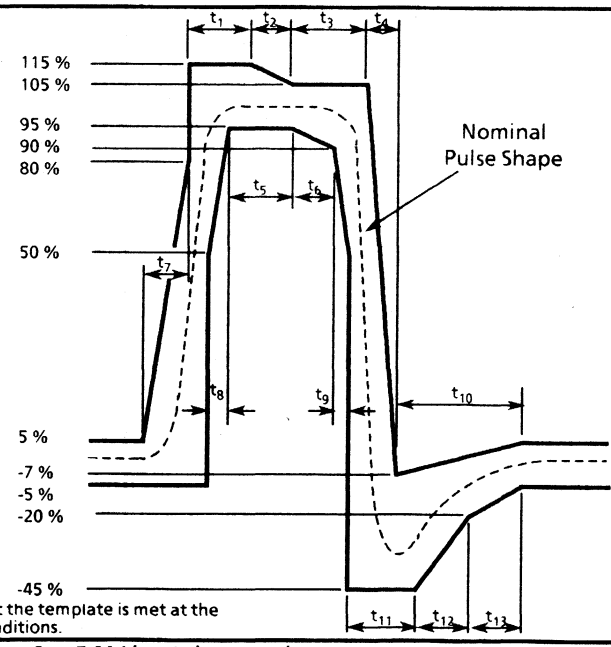


Figure 5 - T1 Line Transmitter

SYMBOL	TIME
t_1	100 ns
t_2	75 ns
t_3	175 ns
t_4	50 ns
t_5	100 ns
t_6	100 ns
t_7	75 ns
t_8	50 ns
t_9	50 ns
t_{10}	375 ns
t_{11}	150 ns
t_{12}	175 ns
t_{13}	175 ns



Note 1: Template is not to scale
Note 2: The equalization network will assure that the template is met at the crossconnect for the three line length conditions.

Figure 6 - DS1 Line Pulse Template

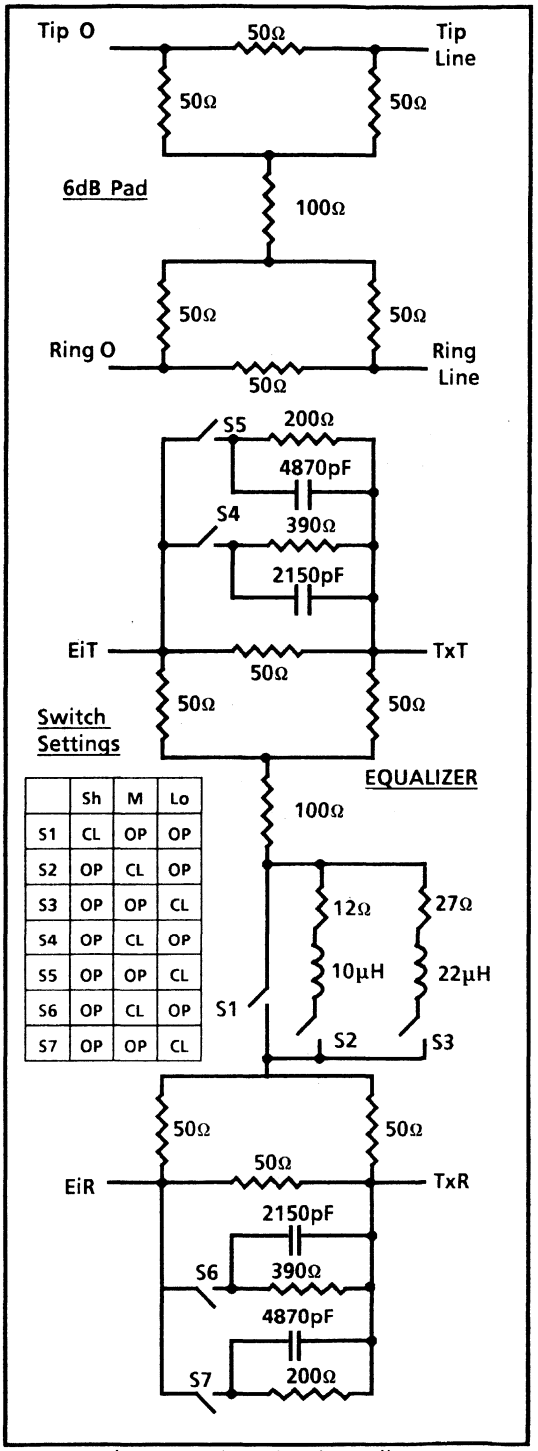
2.1.3 Output Pulse Shaping, RLC Network

In order to meet the pulse shape requirements of AT&T Technical Advisory # 34 for crossconnect compatible equipment, the output pulse from the transformer must be shaped by an external RLC circuit. The RLC shown in Figure 5 provides the undershoot that is shown in the pulse template in Figure 6. The impulse response of this network is critically damped so that it produces a single ringing cycle to create the undershoot.

2.1.4 Line Impedance Matching and Pre-equalization

The size of the pulse produced by the circuit in Figure 5 is double that of the template in Figure 6. In order to reduce the pulse height to approximately three volts it is passed through a 6dB pad. This is a balance pad with 100 ohms input and output impedance. As well as reducing the height of the pulse, the 6dB pad also provides a matched impedance to the 100 ohm twisted pair transmission line. If the transmission medium is not 100 ohm twisted pair then the characteristics of the pad can be changed to produce the required pulse height and output impedance. The top portion of Figure 7 shows a 6 dB pad with 100 ohm input and output impedance.

The other function that is incorporated into the 6dB pad is the pre-equalizer. This is used to enable the interface to drive up to 655 ft. of 22 AWG twisted pair. By applying L and C components to the 6dB pad the frequency response can be altered. Twisted pair cable attenuates high frequencies more than the low frequencies, which tends to round off square pulses as they travel down the cable. If the 6dB pad attenuates the low frequencies by 5 to 6dB and the high frequencies by 0dB then the pulses will tend to retain more of their original shape after travelling down a length of cable. By switching in selected L and C components the frequency response of the 6dB pad can be tailored to pre-equalize the signal so that the pulse shape conforms to the template shown in Figure 6 for several lengths of cable. The configuration shown in Figure 7 has three settings for use on a 100 ohm balanced line of 22 AWG twisted pair. Figure 8 show the frequency response of the three setting equalizer.



	Sh	M	Lo
S1	CL	OP	OP
S2	OP	CL	OP
S3	OP	OP	CL
S4	OP	CL	OP
S5	OP	OP	CL
S6	OP	CL	OP
S7	OP	OP	CL

Figure 7 - 6dB Pad and Equalizer

2.2 Receiver

2.2.1 $\overline{RxA}$ and $\overline{RxB}$ Input Steering Signals

The received AMI signal must first be decoded into two bipolar steering signals that are similar to TxA and TxB in the transmitter. Figure 9 illustrates how the AMI line must be decoded into its two component signals, $\overline{RxA}$ and $\overline{RxB}$. The receiver uses

these two signals to count the number of bipolar violations in the received data stream, and to detect the violations that are a part of B8ZS pattern. Violations that are contained in B8ZS code are not counted as received bipolar violations. Every time the receiver detects 256 violations it reports this in the master status word. This eliminates the need for external hardware and simplifies the system software that is required to calculate the T1 error rate. However, there is one restriction placed on the BPV counter. The minimum sample time for the BPV counter is 96 msec. Effectively this places an upper limit on the bit error rate that can be calculated with this device, but it turns out to be approximately 300 x 10**-3, well above any realistic operating conditions. The advantage of limiting the sample time is that the system can pole the BPV bit, in the Master Control Word, at 50 msec intervals and is guaranteed to detect all changes in the BPV bit.

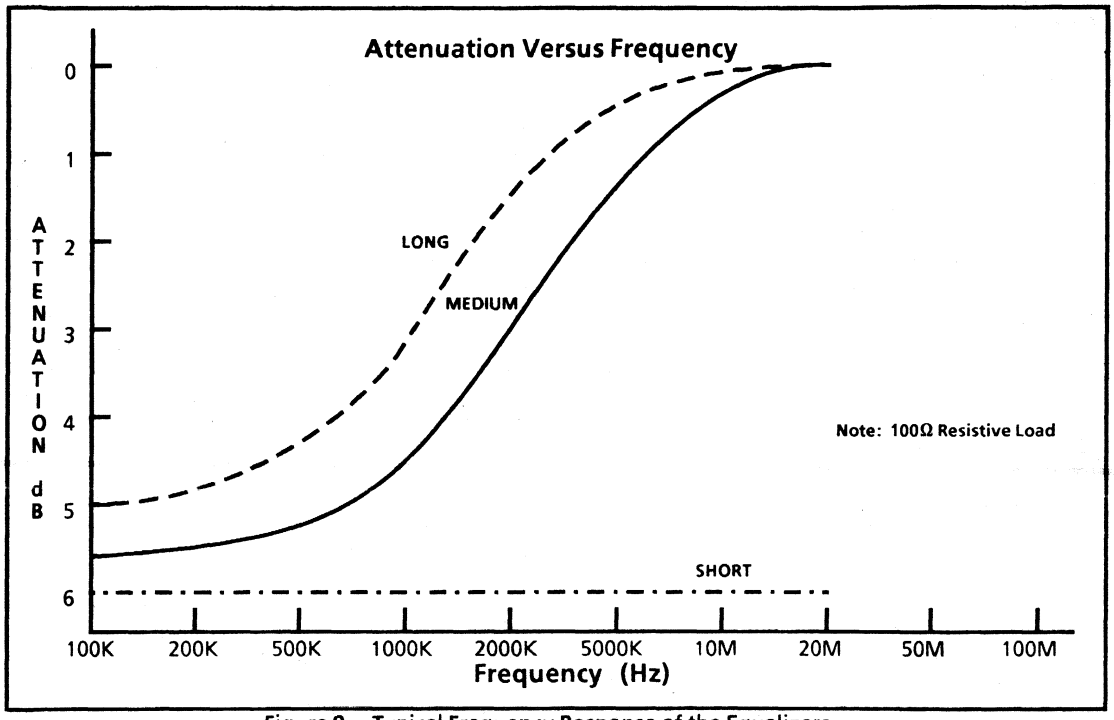


Figure 8 - Typical Frequency Response of the Equalizers

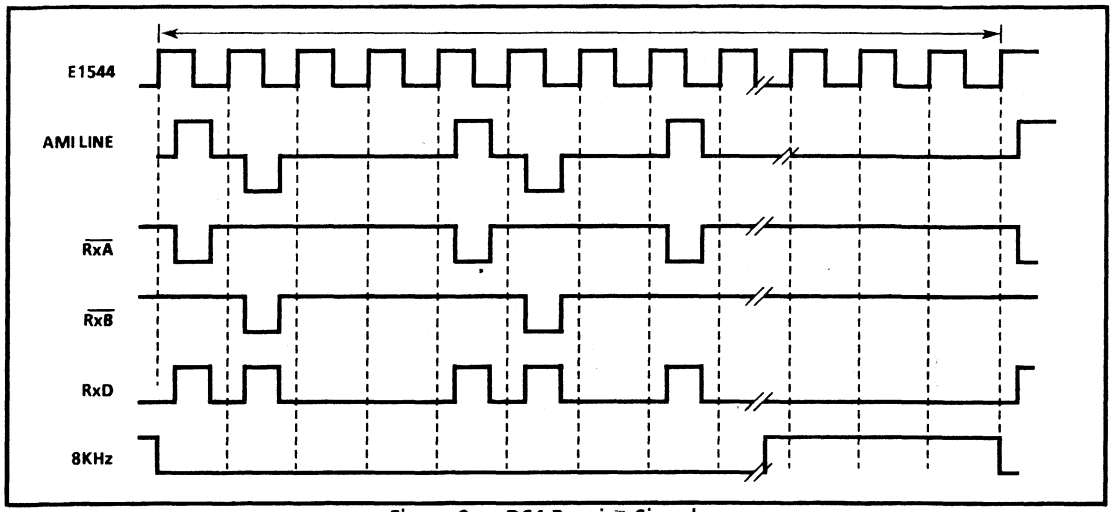


Figure 9 - DS1 Receive Signals

2.2.2 External Input Circuit

The received line interface circuit shown in Figure 10 will decode the AMI line into its two bipolar steering signals. This circuit creates the $\overline{RxA}$ and $\overline{RxB}$ inputs. The bipolar transistors in this circuit are designed to fire at approximately 1.5 volts. Since there is no equalization of the signal before it is decoded, this restricts this circuit to being used in a crossconnect type of environment. If the input to the receiver is intended to be directly from a repeatered line then the repeater function must be implemented before the AMI signal is decoded into $\overline{RxA}$ and $\overline{RxB}$.

2.2.3 Line Impedance Matching and Transformer

The 400 ohm resistor across the secondary of the transformer in Figure 10 matches the characteristic impedance of the transmission line when it is reflected through to the primary side of the transformer. If a non-standard transmission line is used then this resistor can be changed to match the desired characteristic impedance. The detailed transformer specification can be found in Section 5.3

2.2.4 Received Data Input

The received data is input to the receiver in a unipolar return-to-zero format. This is done by combining $\overline{RxA}$, and $\overline{RxB}$ with an external NAND gate. The Received Data, RxD, is clocked into the receiver by the falling edge of the extracted 1.544 MHz clock, see Figure 9. See Section 3.2.5 for details of the clock extractor. An external NAND gate is used so that the delays into the chip are equal for RxD, and E1.5i. The position of $\overline{RxA}$ and $\overline{RxB}$ with respect to E1.5i and RxD will only be skewed by the delay through the NAND gate. This leaves an equal amount of buffer around the falling edge of E1.5i for jitter on RxD. The slightly smaller jitter tolerance of $\overline{RxA}$ and $\overline{RxB}$ is considered acceptable since they are only used to count bipolar violations.

2.2.5 Clock Extraction

The only information that the receiver gets from the line is the data rate. In order to clock the data into the chip it needs to have a clock which is synchronized to the received data rate. This type of a clock is known as an extracted clock. This clock must be able span the gaps between pulses on RxD in order to clock in the logical '0' and the logical '1' bits.

Two of the most commonly used types of clock extractors are the pulsed tank circuit, and the current injection oscillator. The first one is simply an LC tank circuit that has been set to oscillate at 1.544 MHz. Figure 11 is an example of this type of circuit. Each pulse on RxD will cause the circuit to oscillate. The Q of this circuit is selected so that it will oscillate for a period of approximately 15 bits. A high gain amplifier is put on the output of this circuit to square up the oscillation so that it can be used as the received clock. There is a practical limit to how high a Q this type of circuit can have, which in turn is why the pulse density on the T1 line is so important. If there are not enough pulses in the RxD then the extracted clock will shut down.

The other most commonly used clock extractor is the current injection oscillator. This type of extractor oscillates on its own, without any input from RxD. Figure 12 illustrates this type of a clock extractor. The free running frequency of the oscillator is set to 1.544 MHz. Each pulse that is received is differentiated to cause a current spike to be injected into the feedback path. This causes the frequency of the oscillator to follow the frequency of the received data. Both of these extractors follow the data rate when there are pulses on RxD and both of them tend to return to their natural frequency when there are no pulses on RxD.

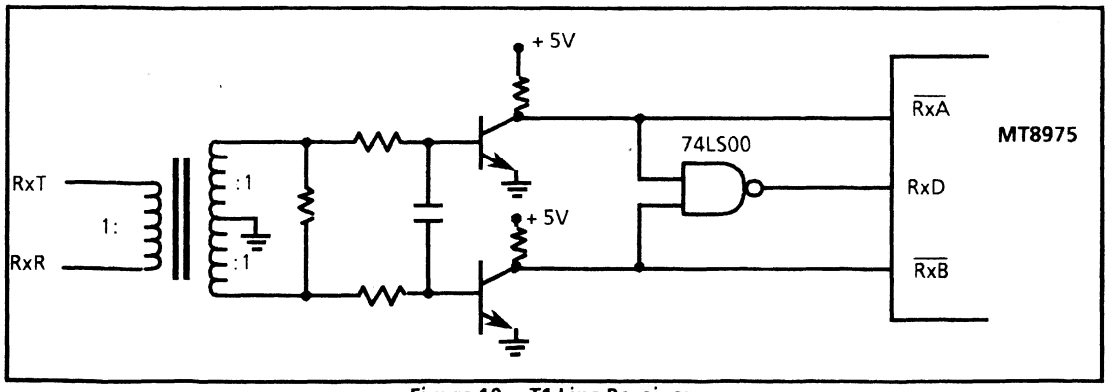


Figure 10 - T1 Line Receiver

To aid the system in synchronizing its clocks to the T1 received data rate the MT8975 divides the extracted 1.544 MHz clock by 193 to generate E8Ko. This output clock is nominally 8KHz and is used by the system to generate clocks that are phase-locked to the average received T1 data rate.

3.0 ST-BUS Interface

The ST-BUS is the system interface to the MT8975. It is a 2.048 MHz serial stream that is divided into 32 8 bit channels, see Figure 13. Frame boundaries are marked by an external frame pulse, F0i-. The MT8975 uses DSTi and DSTo for the 24 T1 information channels, and CSTi and CSTo for the control information. The CSTi stream contains 24 8 bit control words and a Master Status Word. All of the selectable features are controlled through these 24 Control Words. The CSTo stream contains 24 8 bit status words and a Master Status Word. All of the status information is reported in the ST-BUS through these 24 Status Words.

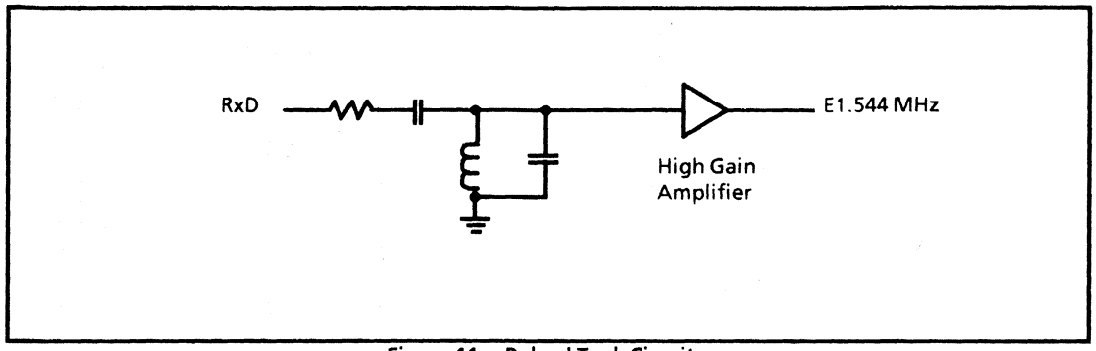


Figure 11 - Pulsed Tank Circuit

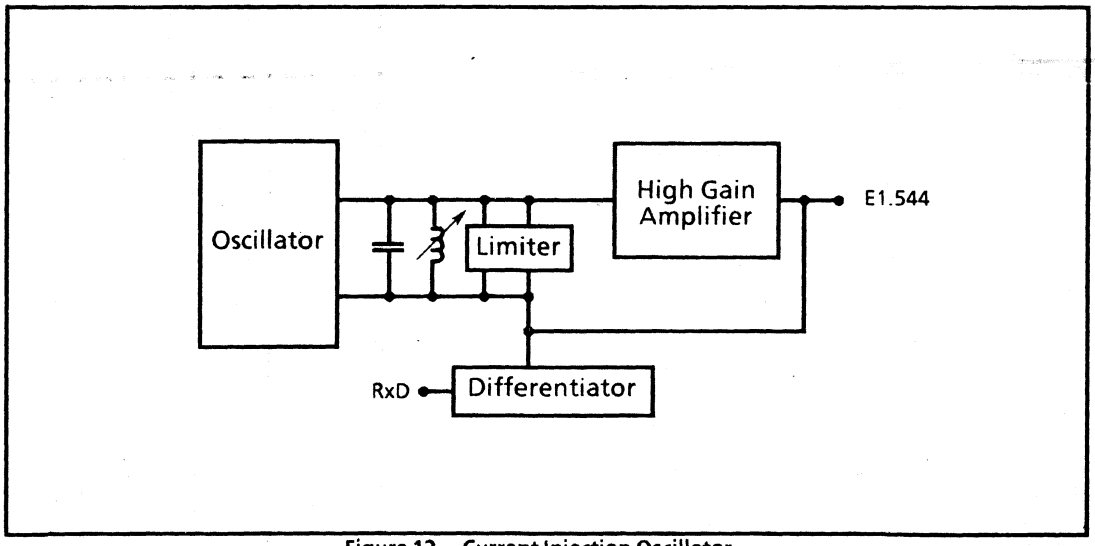


Figure 12 - Current Injection Oscillator

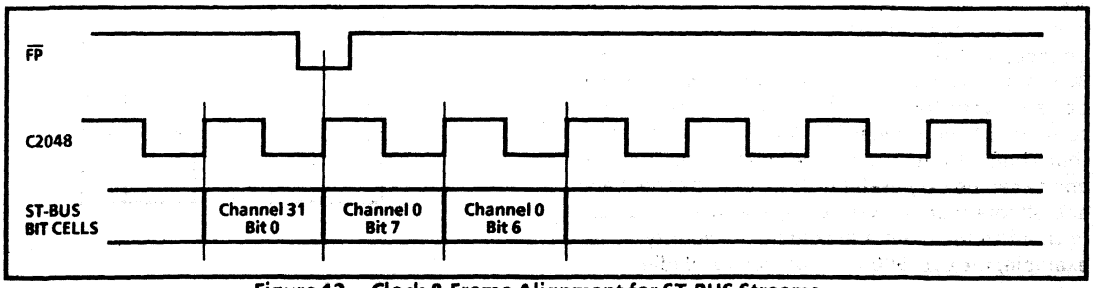


Figure 13 - Clock & Frame Alignment for ST-BUS Streams

3.1 Data ST-BUS Interface

Since there are only 24 channels in a D4 format T1 stream 8 of the ST-BUS channels have been left blank. One out of every four channels is not used beginning with channel 0. Figure 14 shows the position of the valid channels within the ST-BUS frame. These are the only channels that will be transmitted by the MT8975.

3.1.1 Rate Conversion 2.048MHz - 1.544 MHz

Seeing that the ST-BUS and the T1 have different clock rates, the MT8975 transmitter must do a rate adaptation from 2.048 MHz to 1.544 MHz. In order to accomplish the rate adaptation without any loss of information the ST-BUS clock, C2i, and the T1 transmit clock, C1.5i, must be phase locked together by an external phase-locked loop. By positioning the T1 channels as shown in Figure 14 the rate adaption circuit in the transmitter is greatly simplified. The required phase-locked loop will be discussed in greater detail in Section 4.0.

4.1.2 Sourcing Data in Serial or Parallel Format

Figure 15 illustrates a typical configuration where the input and output data is sourced in a serial fashion. The 24 codecs are assigned consecutive channels on STi0 and STo0. The MT8980, operating in normal mode is programmed to switch those 24 consecutive channels from the codecs to the DSTi and DSTo format shown in Figure 14. For example: STo1 channel 1 is sourced from STi0 channel 0, and STo0 channel 0 is sourced by STi1 channel 1. The MT8980 will very easily reposition the data to meet the format requirements of DSTi and DSTo.

Data that is to be transmitted on the T1 line can also be supplied in a parallel format by the MT8980. The mechanism used is called message mode. Using the example of Figure 15, any of the 24 T1 channels can be sourced through the microprocessor port by placing that individual channel into message mode. To place a given channel into message mode the bit called Message Channel in the associated byte of the Connection Memory High must be set to a '1'. After this has been done the contents of the corresponding Connection Memory Low will be output on the ST-BUS in the associated timeslot. This information will be sent every frame until the system changes the contents of the Connection Memory Low or takes that channel out of message mode. This type of ability can be very useful if this was a channel bank and all idle channel were to have a specific pattern in them to maintain a maximum 1's density. If for example, the byte $00 were written to all idle

DSTi	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	X				X				X				X				X				X				X				X			
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

Figure 14 - Relationship Between Input DSTi Channels and Transmitted DS1 Channels
-X Denotes Unused Channels

DSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	X				X				X				X				X				X				X				X			
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

Figure 14a - Relationship Between Received DS1 Channels and Output DSTo Channels
-X Denotes Unused Channels

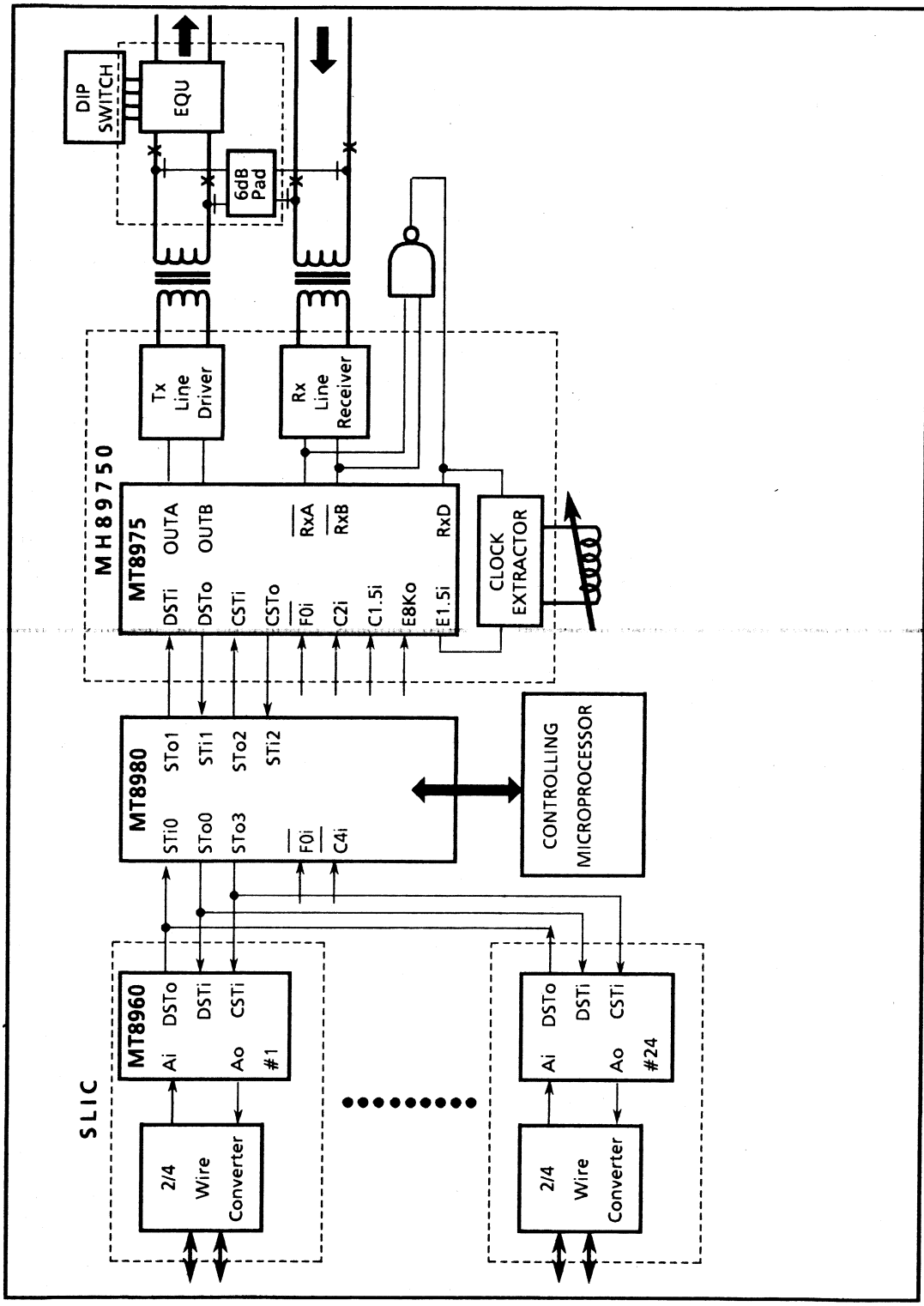


Figure 15 - Typical Configuration

channels, by using message mode, the output pattern on the T1 link would be all 1's. The output pattern is all 1's because the transmitter inverts the data between DSTi and TxA and TxB.

3.2 Control ST-BUS Interface

All of the control and status information for the MT8975 is supplied to the chip in serial format. The chip uses one ST-BUS link as a Control ST-BUS input, CSTi, and one ST-BUS link as Control ST-BUS output. Per channel control/status information occupies 24 channels and master control/status occupies 1 channel. Using a serial format may seem inconvenient at first glance, but the MT8980 provides a simple and easy to use means of sending and receiving these ST-BUS signals. By using this type of serial control stream the bulky parallel address and data buses are eliminated from the architecture. This will then free up a lot of real estate on the system backplane and the line cards.

3.2.1 Sourcing Control Information in Parallel Format

There are two options for sourcing information in a parallel format. The first one is to use the option contained in the Connection Memory High. This is the same procedure that is explained in Section 3.1.2 for sourcing data in a parallel format. This would be used when there is a single MT8980 that is connected to DSTi/o and CSTi/o. The second method of entering message mode in the MT8980 is to use the control register. This method can be used when a single MT8980 is dedicated to operating the Control Interface of several T1 trunks at the same time. By setting bit 6 of the control register to 1, all channels of all links are placed into message mode. It is now a simple matter of writing the required byte into the appropriate Connection Memory Low address to set up the 24 Per Channel Control Words and the Master Control Word. This also has the added advantage of reducing the set up procedure to one operation, compared to approximately one operation per channel when the Connection Memory High is used.

To monitor the information received from CSTo, of the MT8975, memory select bits in the Control Register are set for the data memory ($01). This configures the MT8980 so that all reads of channels are from the data memory, which is the data received by a STi pin. Now the system can read a Per Channel Status Word or a Master Status Word by reading the appropriate byte in the Data Memory associated with the proper input stream. Since the MT8980 stores the received information in its own memory the system can read status information at any time during the frame, and not only when it is output from the MT8975. Another useful technique that can be used to source and monitor control and status information is Split Memory mode. Split Memory mode causes all reads to be from the Data Memory, and all writes to be from the Connection Memory Low. When used in conjunction with either one of the message mode options the control and status information for a given channel can be manipulated without changing the memory select bits, in the control register, from the Connection Memory Low to the Data Memory. This reduces the number of operations required by the system to operate the interface.

3.2.2 Control Channels and Master Control Channel Format

The format of information on CSTi is shown in Figure 16. The 24 Per Channel Control Words are input one channel early, when compared to the format of DSTi and DSTo. Inserting the control information one channel before the channel it is intended to control facilitates the timely application of this information by the MT8975. The Master Control Word occupies one of ST-BUS channels that would normally be left blank. This word contains information that pertains to the overall operation of the chip and not a particular channel. Features such as zero code suppression and alarms can be activated by the Master Control Word. All of the unused channels of CSTi should be set to $00 for normal operating conditions. Tables 1 and 2 show the Per Channel Control Word format and the Master Control Word format.

The digital attenuation feature is provided to allow the user the ability to meet the variety of loss and level plans that are required for different types of calls and different telephone authorities. When used in conjunction with the digital attenuation features of Mitel's MT8960 series of codecs almost any loss and level plan can be accommodated.

3.2.3 Status Channels and Master Status Channel Format

The format of the data on CSTo is shown in Figure 16. The 24 Per Channel Status Words are output one channel early when compared to the received channels that they represent. The format of the Per channel Status Words and the Master Status word is shown in Tables 3 and 4. All of status information can be read by the system with an MT8980 in split memory mode or by reading the Data Memory directly. The A and B signalling bits presented to the system in the Per Channel Status Words are

CSTi	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
				X				X				X				MC				X				X				X				X
DSTi	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	0

Figure 16 - Relationship Between Input CSTi Channels and Controlled DSTi Channels
-X Denotes Unused Channels, -MC Denotes Master Control Word

CSTo	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
				X				X				X				MS				X				X				X				X
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

Figure 16a - Relationship Between Received DS1 Channels and Output CSTo Channels
-X Denotes Unused Channels, -MS Denotes Master Control Word

only valid when the MT8975 is in synchronization. It is recommended that the system keep a software image of the A and B bits and that the sync. bit in the Master Status Word is checked before updating the signalling bits.

3.2.4 External Status and Control

There are three uncommitted pins on the MT8975. They are labelled XCtl, XS1, and XS2. These three pins do not relate to the T1 line format or specification in any way. They are included to enhance the flexibility of the devices ST-BUS interface. External Control, XCtl, is controlled by bit 3 of the Master Control Word, and therefore is updated once per frame or every 125 µsec. The two External Status pins, XS1 and XS2, are sampled once per frame and the result is multiplexed into bits 4 and 5 of the Master Status Word. These two functions allow the system to control and monitor external circuits that are related to the T1 line card. For example: one of the external status pins could be used to monitor the output of an all ones detector. This function is not included in the MT8975, but the external status bit would allow the system to monitor this circuit with the Master Status Word used in the MT8975. The external control pin could be used to activate an external loopback relay like the one shown in Figure 15. As in the external status pin this would allow the system to control the loopback in the same Master Control Word used to control the MT8975.

4.0 Clock Generation and Synchronization

The MT8975 has two sets of clocks, the ST-BUS clocks and the T1 clocks. The ST-BUS clocks are used for DSTi/o and CSTi/o and the T1 clocks are used for TxA, TxB, $\overline{RxA}$, $\overline{RxB}$, and RxD. In certain situations the T1 clocks are also used to synchronize the system, or ST-BUS clocks to the received data rate.

4.1 ST-BUS Clocks C4, C2, and F0i

The ST-BUS is a synchronous system that uses an external clock and synchronization signal. The frame pulse, $\overline{F0i}$, marks the boundary between channels 31 and 0. The MT8975 uses a 2.048 MHz clock called C2i and the 8KHz frame pulse called $\overline{F0i}$. The required alignment of the two is shown in Figure 13. The MT8980 uses a 4.096 MHz clock that is called $\overline{C4i}$, and the same $\overline{F0i}$ frame pulse. The alignment of $\overline{C4i}$ with respect to C2i and $\overline{F0i}$ is also shown in Figure 13. A simple clock generation circuit in Figure 17 shows how $\overline{C4i}$, C2i, and $\overline{F0i}$ can be generated by using the Mitel MT8940 DPLL.

BIT	NAME	DESCRIPTION
7	(unused)	
6	B8ZS	If 0 then Bit 7 of the DS1 carrier (the second last bit transmitted, corresponding to Bit 1 in the DSTI ST-BUS™) is jammed to 1 if all other bits of the channel on the DS1 carrier are 0. If 1 then all sequences of 8 zeros on data routed to the DS1 carrier are replaced by B8ZS code irrespective of channel boundaries or the presence of the S-bit in the 8 zeros. B8ZS code received from the DS1 carrier is always replaced by 8 zeros.
5	(unused)	
4	8kHzSEL	If 1 then the 8kHz pin is low for received DS1 channels 1 to 15 and high for channel 16 to the S-bit. If 0 then the 8kHz pin is high impedance.
3	XCTL	The information at this location is output directly onto the XCTL pin once per frame.
2	(unused)	Test bit.
1	CCS	If 1 then bit stealing by A & B signalling bits is prevented. Valid PCM or data is transmitted on every channel of the DS1 carrier for all frames. This option is used when common channel signalling is used. If 0 then the A & B signalling bits which are input on PCM bits 1 & 0 of the appropriate CSTI channels are sampled during frames 6 and 12 replace PCM bit 0 of the DSTI channels for these frames.
0	ALARM	If 1 then bit 2 of every channel transmitted on the DS1 carrier is jammed to zero. If 0 then bit 2 of the DS1 carrier behaves normally.

Table 1 - Data Format on CSTI Channel 15 - Master Control

BIT	NAME	DESCRIPTION
7,6	RXPAD2, 1	Per channel receive attenuation control bits RXPAD2 RXPAD1 Attenuation(dB) 0 0 0 0 1 -5 1 0 -3 1 1 -6
5,4,3	TXPAD4, 2,1	Per channel transmit attenuation control bits TXPAD4 TXPAD2 TXPAD1 Attenuation (dB) 0 0 0 0 0 0 1 -4 0 1 0 -5 0 1 1 -1 1 0 0 -3 1 0 1 -2 1 1 0 -6 1 1 1 1
2	LOOP	Per channel transmit attenuation control bits TXPAD4 TXPAD2 TXPAD1 Attenuation (dB) 0 0 0 0 0 0 1 -4 0 1 0 -5 0 1 1 -1 1 0 0 -3 1 0 1 -2 1 1 0 -6 1 1 1 .1
1	TX A-BIT	This bit is sampled and output instead of bit 0 of the corresponding DSTI channel during frame 6 unless the CCS bit (bit 1 on CSTI channel 15) is 1.
0	TX B-BIT	This bit is sampled and output instead of bit 0 of the corresponding DSTI channel during frame 12 unless the CCS bit (bit 1 on CSTI channel 15) is 1.

Table 2 - Data Format on CSTI Channels used for Controlling Channels on the DS1 Link

BIT	NAME	DESCRIPTION
7-5	(unused)	
4	XS1	This bit contains the data sampled at the XS1 pin once per frame.
3	RX0	This bit goes to 1 when the alarm condition is detected on the received DS1 link (i.e. bit 2 of every received channel is zero) and returns to 0 after the alarm condition is removed.
2	BPV	This bit changes state after 256 bipolar violations other than B8ZS code has been detected on the received DS1 link.
1	SLIP	This bit changes state after a slip between the received DS1 link and the CSOUT stream has been detected.
0	SYN	This bit goes to 1 when synchronization to the received DS1 link is lost and returns to 0 once synchronization is regained.

Table 3 - Data Format on CSTo Channel 15 - Master Status

BIT	NAME	DESCRIPTION
7-2	(unused)	
1	RX A-BIT	This bit is the A signalling bit from the DS1 carrier after it has been debounced for 7.5 ms to 9 ms.
0	RX B-BIT	This bit is the B signalling bit from the DS1 carrier after it has been debounced for 7.5 ms to 9 ms.

Table 4 - Data Format on CSTo Channels used for Monitoring Channels on the DS1 Link

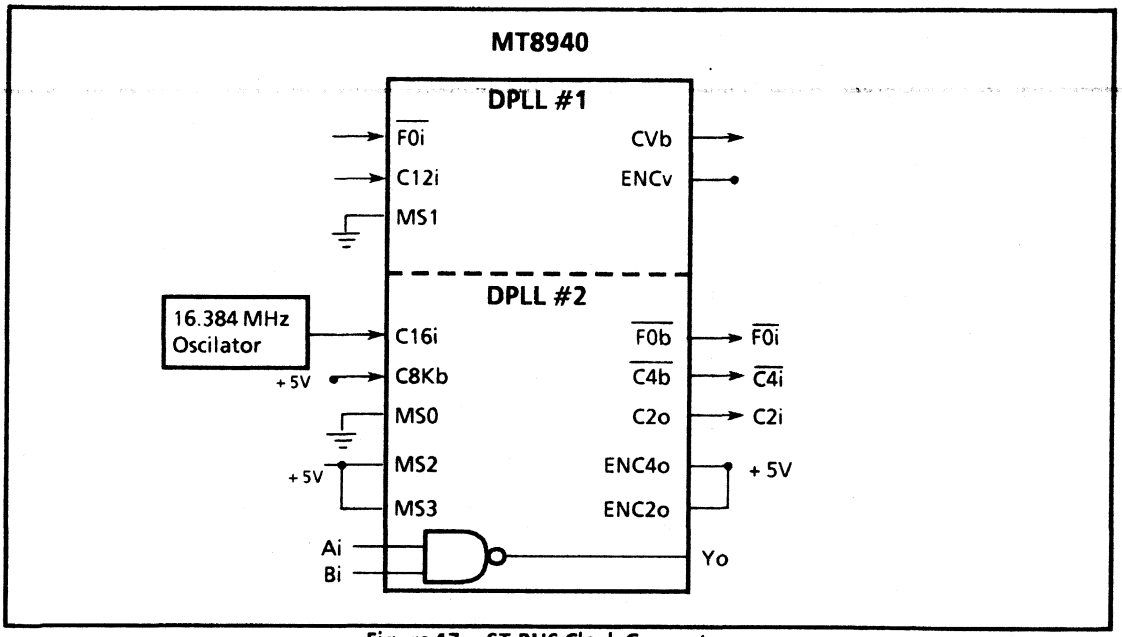


Figure 17 - ST-BUS Clock Generator

4.2 T1 Clocks

4.2.1 Transmit Clock, C1.5i

The T1 transmit clock used by the MT8975 is C1.5i. This clock must be phased-locked to the ST-BUS clocks in order for the transmit rate converter to operate properly. This means that in every frame of the ST-BUS there must be equal to 193 cycles of the 1.544 MHz clock. This can be done by an analog or a digital phase-locked loop. The MT8940 is a Dual Digital Phase-Locked Loop that will provide this function. Phase-locked loop #1 can be configured as in Figure 18 to generate a 1.544 MHz clock that is phase-locked to $\overline{F0i}$.

4.2.2 Receive Clock, E1.5i

The received clock is generated by the clock extractor, E1.5i, and is used by the receiver to clock data into the MT8975. Internally the extracted clock is divided by 193 to produce what is known as the extracted 8KHz (E8Ko). This clock is directly related to the line data rate, and can be used to synchronize the system clock to the T1 line.

4.2.3 Loop Timing, E8Ko

The extracted 8KHz output is provided to simplify loop timing the system to the line data rate. Loop timing is the process by which the transmit frequency is equal to the long term average frequency of the received data rate, i.e.: C1.5i equals E1.5i. The MT8940 will accomplish this with phase-locked loop #2. This phase-locked loop accepts E8Ko as its input and produces C2o, $\overline{C4o}$, and $\overline{F0o}$. This produces system clocks that are phase-locked to E8ko, which is directly related to E1.5i. By feeding the phase-locked $\overline{F0o}$ into the $\overline{F0i}$ of phase-locked loop number 1 the MT8940 will produce a transmit T1 clock, C1.5i that is phase locked to the received data rate via the MT8940. Figure 18 also illustrates how phase locked loops numbers 1 and 2 can be used to generate system clocks that are phase-locked to the T1 line.

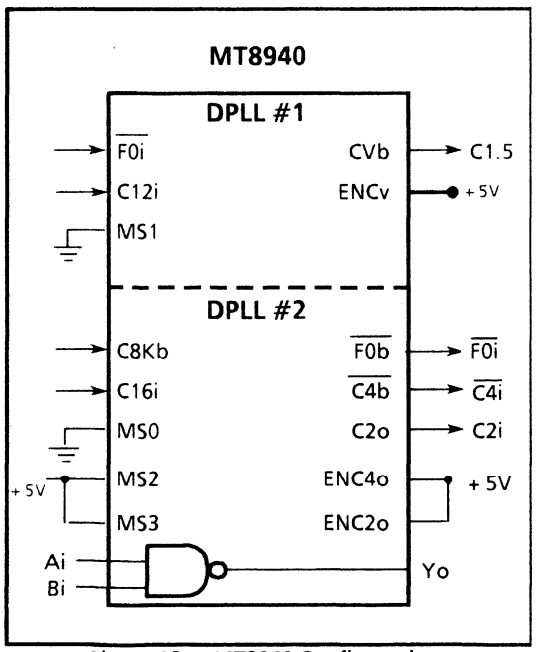


Figure 18 - MT8940 Configuration

5.0 General Description MH89750

The MH89750 is the next level of integration in Mitel's family of T1 components. The MH89750 is a ceramic hybrid that contains the MT8975 and some additional circuitry manufactured in thick film hybrid technology. Since the MH89750 is built with the MT8975 the following section will only discuss the functions provided by the additional circuits on the MH89750.

5.1 Digital Line Interface

5.1.1 Line Drivers

The MH89750 provides the line drivers that are shown in Figure 5. The hybrid will, therefore, interface directly to the line coupling transformer. The detailed transformer specification is contained in Appendix A.

5.1.2 Line Receivers

The MH89750 also provides the line receivers that are shown in Figure 10. This circuit does not contain any equalization. It is designed to operate only with the cross connect specification. That is, the shape of the pulse on the line must conform to the template shown in AT&T T.A. #34 or CCITT G.703 (Figure 6) at a distance not greater than 655 ft. from the inputs of the transformer.

5.1.3 Impedance Matching and Pre-equalizing

The MH89750 provides two equalization networks. The first is the simple 6dB pad shown in Figure 7. This is used for external loop back so that the pulse height is reduced to approximately 3 volts. The second is the equalizer shown in Figure 7. The external 7 position Dip switch produces three settings for short, medium and long lengths of line. This equalizer will produce crossconnect compatible pulses at up to 655 ft. from the output transformer.

5.2 Clock Generation and Synchronization

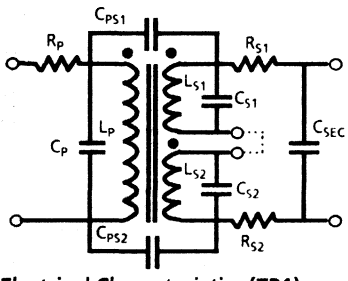
5.2.1 Clock Extractor

The only clock that is generated by the MH89750 for the user is the extracted clock, E1.5i. The clock extractor provided by MH89750 is the current injection oscillator that is shown in Figure 12. The extracted clock is an output from the hybrid and is internally connected to E1.5i on the MT8975. It is provided as a test point for tuning the clock extractor to 1.544 MHz. The 43µH to 46.5µH tunable inductor must be provided externally.

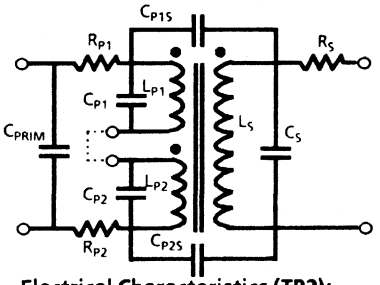
5.3 T1 Line Transformer Specification

All subscriber equipment which is to be connected to a T1/DS1 digital network, must deliver an output which satisfies the AT&T technical advisory #34. As such, the isolated pulses appearing at the DS1 cross-connect must satisfy the pulse template shown in figure 6. To assist in the design of such a requirement, specifications for the input and output transformers (as shown in figure 15) have been provided. These specifications can be used to manufacture the line transformers for use with the MH89750. A list of vendors has also been included to assist the user in purchasing all magnetics required by the MH89750.

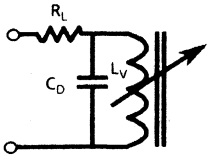
Input Transformer (TR1) Equivalent Circuit



Output Transformer (TR2) Equivalent Circuit



Variable inductor (L1) Equivalent Circuit



Electrical Characteristics (TR1):

Inductance	: L_P = 1.6 mH ±25% L_{S1} = 1.6 mH ±25% L_{S2} = 1.6 mH ±25%
Leakage	: L_P = 2.0 µH Max. L_{S1} = 4.0 µH Max. L_{S2} = 4.0 µH Max.
DCR	: R_P = 0.33 Ohms Max. R_{S1} = 1.5 Ohms Max. R_{S2} = 1.5 Ohms Max.
Capacitance	: C_P = 40 pF Max. C_{S1} = 40 pF Max. C_{S2} = 40 pF Max. C^*_{SEC} = 10 pF Max. C_{PS1} = 25 pF Max. C_{PS2} = 25 pF Max.
Turn Ratio	: S1 to S2 to P1 = 1 : 1 : 1

Electrical Characteristics (TR2):

Inductance	: L_{P1} = 1.92 mH ±25% L_{P2} = 1.92 mH ±25% L_S = 0.55 mH ±25%
Leakage	: L_{P1} = 10 µH Max. L_{P2} = 10 µH Max. L_S = 1.5 µH Max.
DCR	: R_{P1} = 1.6 Ohms Max. R_{P2} = 1.6 Ohms Max. R_S = 0.4 Ohms Max.
Capacitance	: C_{P1} = 40 pF Max. C_{P2} = 40 pF Max. C_S = 115 pF Max. C^*_{PRIM} = 10 pF Max. C_{P1S} = 25 pF Max. C_{P2S} = 25 pF Max.
Turn Ratio	: P1 to P2 = 1 : 1 P1 or P2 to S1 = 1 : 0.534

Electrical Characteristics (L1):

Inductance	: L_V = 43.9 to 49.4 µH
DCR †	: R_L = 5 Ohms Typ. : R_L = 10.0 Ohms Max.
Capacitance†	: C_D = 3.0 pF Typ. : C_D = 7.0 pF Max.

† Measures are taken with L_V = 43.9 µH

* With recommended connection

Magnetics Ordering Information :

TR1: 1- Filtran Ltd #TFS 2574
2- Vanguard Elect. #VE 40353

TR2: 1- Filtran Ltd #TFS 2573
2- Vanguard Elect. #VE 40354

L1: 1- Filtran Ltd #CFS 2575
2- PREM Magnetics #4536

Note: Specifications provided above are not the only conditions which will satisfy the template.

Figure 5 - Transformer Specifications

6.0 Applications

The following section contains a brief description and a block diagram of a few of the areas that the MT8975 and the MH89750 can be used in. The discussion will center around the general architecture that is used and the functional blocks that are required. The block diagrams have been simplified by excluding some of the signals for clarity. The following applications are:

PCM/Voice Channel Bank
ISDN Voice/Data Channel Bank/Concetrator
Digital Access Cross Connect System (DACS)
Digital Multiplex Interface (DMI)
High Speed Data Transmission Link
T1 to CEPT Digital Trunk Converter

6.1 PCM/Voice Channel Bank

The D3/D4 channel bank is one of the most widely used pieces of equipment in the North American network today. The D3/D4 channel converts 24 analog telephone lines into the 24 channels of a T1 serial stream. The channel bank is the interface point between a digital switching or transmission system and the analog telephone loop. The industry is moving towards end-to-end digital connections (ISDN), but the analog channel bank will still be in use for many years to come.

6.1.1 Functional Description

Figure 19 shows a block diagram of a channel bank that has been divided into four sections, the analog line interface, signalling interface, switch matrix, and T1 interface. The MH89620 is an analog subscriber line interface that provides interface to the telephone line, i.e. provides loop current and ringing voltage, and converts the analog voice signal into µLaw PCM. The SLIC also detects the off-hook condition for conventional POTS (Plane Old Telephone Set) signalling.

Once the voice is encoded into digital format the switch matrix transfers the 24 consecutive channels that are received from the SLICs to the 24 valid channels used by the MH89750. The MH89750 formats and transmits this information on the T1 line.

Signalling information from the telephone sets can be routed straight through to the output T1 channel, or it can be routed to the DTMF receiver pool. This is easily accomplished by the MT8980 switch matrix once the SLIC has digitized the analog signal.

Channel banks must be able to operate in a loop timed mode so that they meet the clock synchronization requirements of a level four entity. Phase-locked loop #2 of the MT8940 generates the ST-BUS clocks that are synchronized to the extracted 8KHz clock, and Phase-locked loop #1 generates the transmit T1 clock synchronized to the ST-BUS. By using the two phase-locked loops of the MT8940 the transmit T1 clock is equal to the received T1 clock, with some jitter removed.

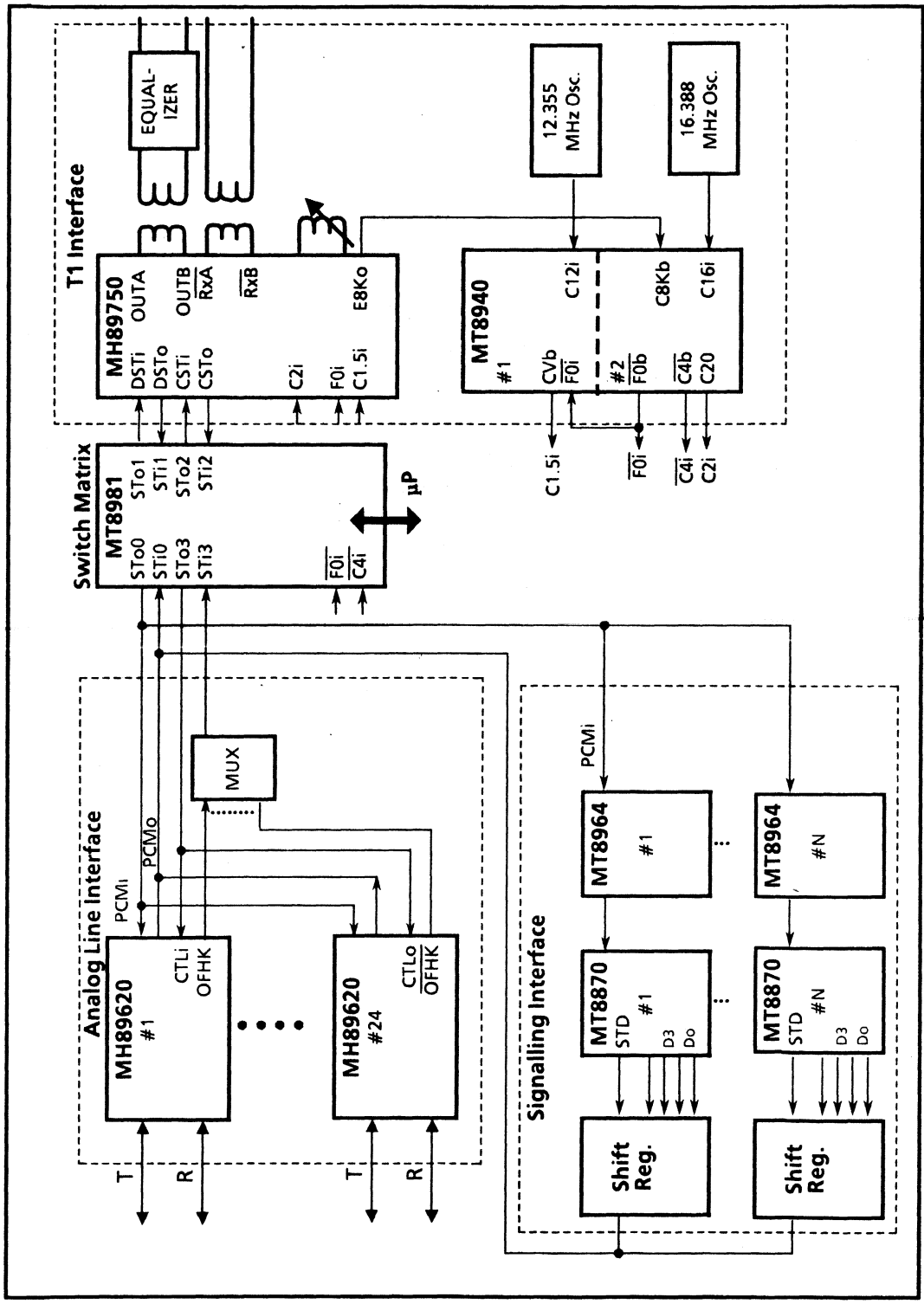


Figure 19 - PCM/Voice Data Channel Bank

6.2 ISDN Voice/Data Channel Bank/Concentrator

The ISDN channel bank is a term that is used in this context to describe a system that performs the same logical function as the D3/D4 channel bank. That is, it concentrates the subscribers digital loop into the primary digital transmission scheme, the T1 trunk.

6.2.1 Functional Description

The ISDN channel bank in Figure 20 is divided into four blocks, the digital line interface, the switch matrix, the D channel processing, and the T1 interface. Beginning with the digital line interface, the MT8972 provides 2B + D 160K bit bidirectional communication over single twisted pair wiring. The MT8972 converts the 160K bit line signal into ST-Bus format, where it can be manipulated by the MT8980 switch matrix. The data received from the MT8972 is then transferred to the D channel processor by the switch matrix. The D channel processor converts the 2B + D format used on the 160 KBit digital line into the 23B + D format used on the T1 Link.

To control and monitor the MT8972's and the T1 interface the switch matrix operates some of its input and output streams in message mode. This enables the system to control all of the functions of the MT8972's and the T1 interface through the Control ST-BUS points, (CSTi/o).

Clock synchronization is done by the MT8940. Phase-locked loop # 2 generates ST-BUS clocks that are synchronized to the extracted 8KHz output from the T1 interface. Phase-locked loop #1 generates the transmit T1 clock synchronized to the ST-BUS clocks, which are synchronized to the extracted T1 clock. This scheme will also allow the system to operate in a loop timed mode.

With appropriate multiplexing a single D channel processor can handle all 23 2B + D interfaces. If both B channels on all 24 lines are going to be used then it would be necessary to use two T1 trunk interfaces.

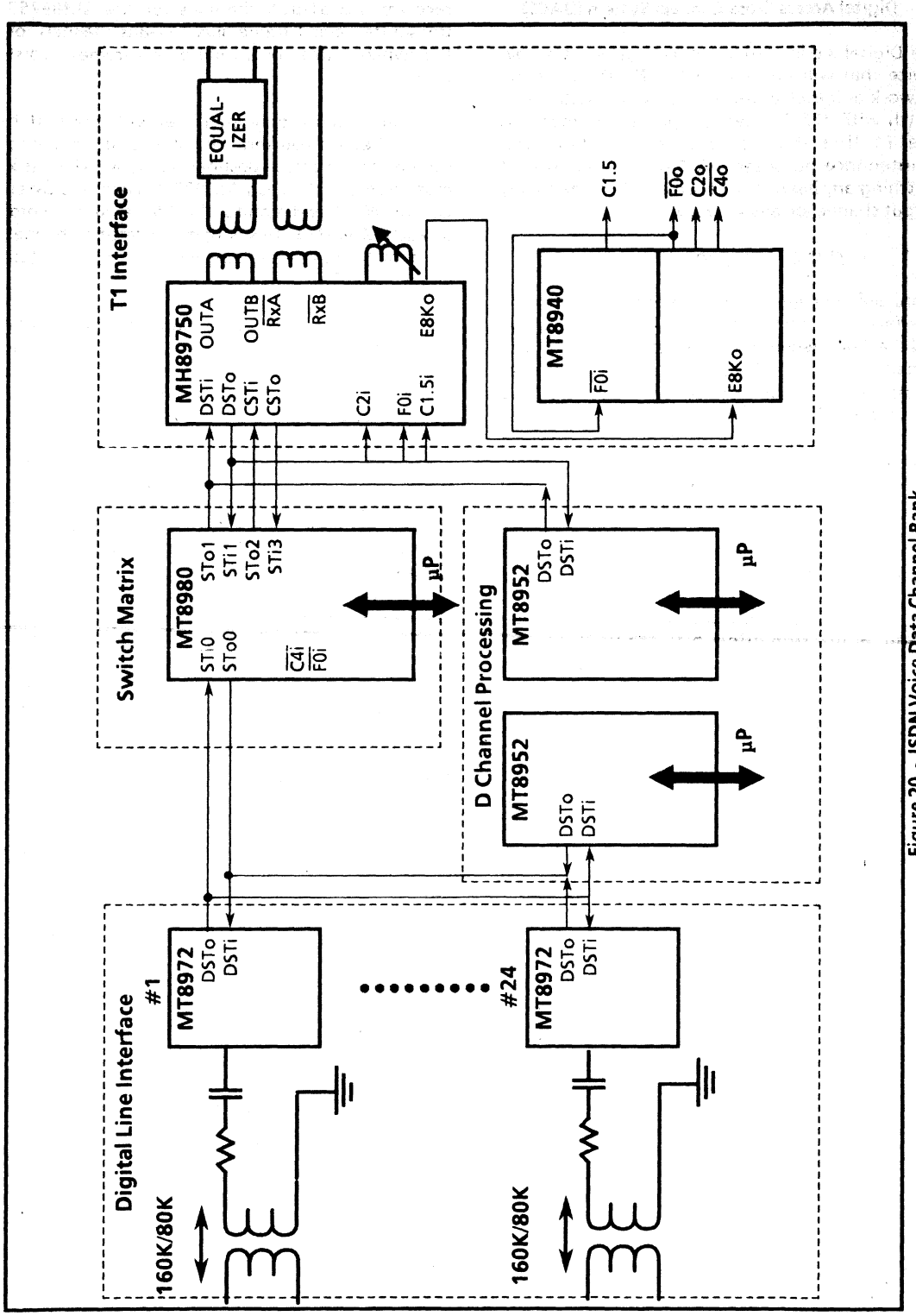


Figure 20 - ISDN Voice Data Channel Bank

6.3 Digital Access Cross Connect System (DACS)

The Digital Access Cross Connect System is a new device that will be used in the North American network as it evolves towards ISDN. A DACS is a T1 switch with 127 T1 lines as input and output plus one T1 line that is reserved for test and maintenance purposes. A DACS is capable of switching any input channel on any T1 trunk to any output channel on any T1 trunk.

6.3.1 Functional Description

There are four main blocks in Figure 21, the T1 interfaces, the switch matrix, the control matrix, and the clock generator. The digital trunk interface is made up of the MH89750 plus the additional components required to interface to the transmission line. The MH89750 handles all of the data formatting required for transmit and receive and converts the 1.544 MHz serial stream into ST-BUS format so that it can be routed through the synchronous switch matrix built with the MT8980.

The switch matrix can be built so that the maximum throughput delay is 1 frame + 2 channels. The switch matrix will not only route data channels to their destination, but it will also route the received A and B bit signalling bits through to the destination channel. This is necessary because the receiving MH89750 decodes the T1 stream, and the transmitting MH89750 has to reconstruct the outgoing T1 stream. In other words, there is no multiframe integrity between received data and transmitted data. The total throughput delay is 1 frame plus 11 ST-BUS channels for the MH89750 receiver, 2.5 ST-BUS channels for the MH89750 transmitter, and 1 frame plus 2 ST-Bus channels for the switch matrix for a total of 2.5 frames worst case.

The control block only interfaces with the switch matrix. Besides routing channels and signalling through to the proper destination the switch matrix must also supply each MH89750 with a Master Control Word, and monitor the Master Status word of each MH89750. This is done by setting channel 15, of all ST-BUS output streams that are connected directly to CSTo, to message mode.

The clock generation block supplies the ST-BUS clocks and the T1 transmit clocks that are synchronized to one of the T1 trunks. All of the extracted 8 KHz outputs are ANDed together before they are input to PLL #2 of the MT8940.

Phase-locked Loop #2 of the MT8940, will generate the ST-BUS clocks that are used by the MH89750's and the MT8980's that are synchronized with chosen T1 line. The E8Ko of all of the other MH89750's can be tristated from the Master Control Word which allows the system controller to select any one of 128 T1 lines to act as the synchronization source. By connecting the frame pulse output, $\overline{F0o}$, of PLL # 2 to $\overline{F0i}$ of PLL # 1 the MT8940 will generate the T1 transmit clock that is phase-locked to $\overline{F0o}$, which in turn is phase-locked to the master synchronization signal, E8Ko. If all of the T1 trunks are from the network any short term differences in the received data rate will be absorbed by the elastic buffer in the MH89750.

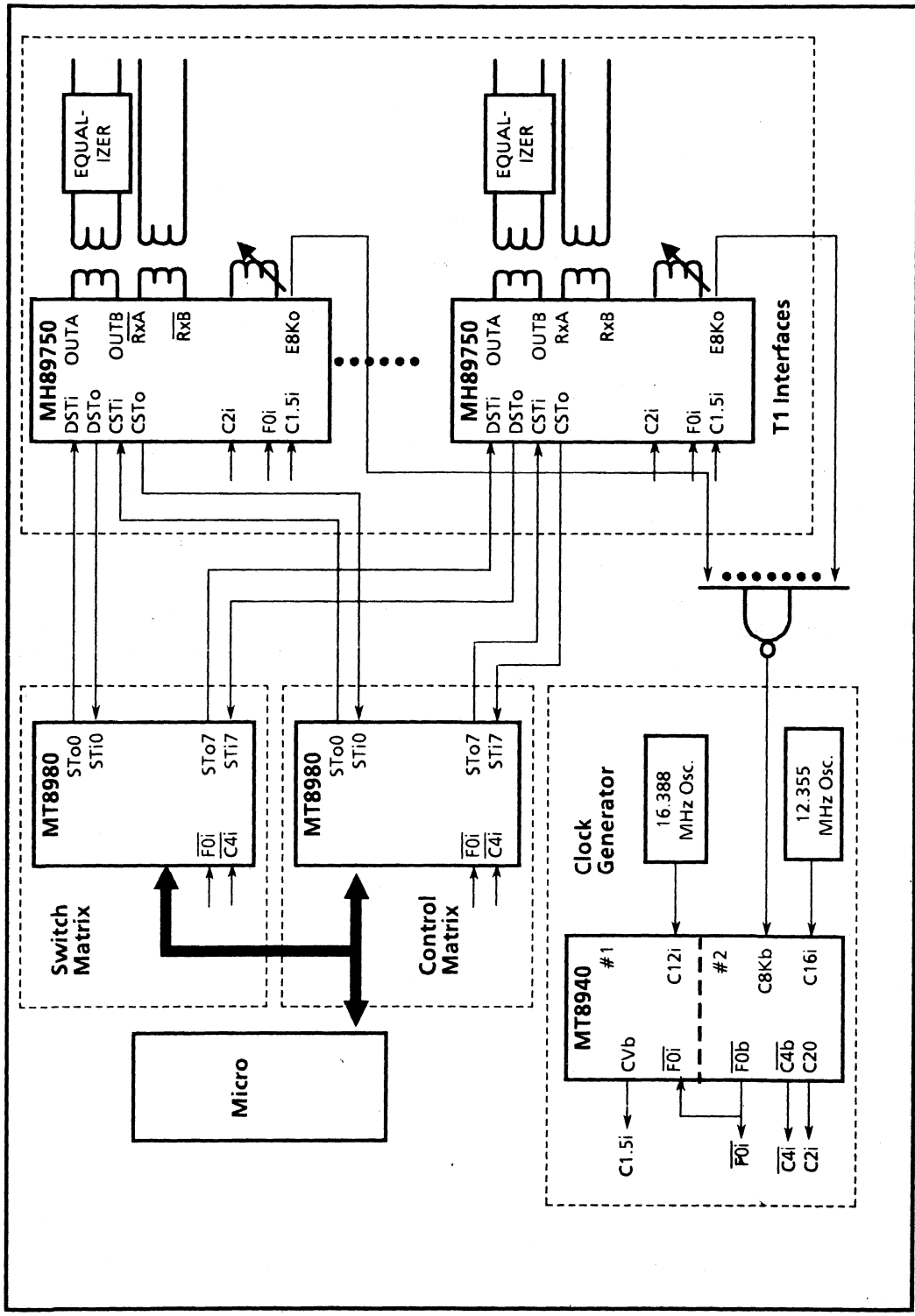


Figure 21 - Digital Access Cross Connect System (DACS)

6.4 Digital Multiplex Interface (DMI)

A new specification for computer to PBX interfaces has been presented by AT&T Communications known as Digital Multiplex Interface, or DMI. This interface will convert a number of data channels, ranging from 300 baud to 64K baud, from an asynchronous or synchronous format into T1 format with clear channel capabilities and a common channel signalling scheme. The options available range from 300 baud to 64K baud channels to statistical multiplexing of multiple logical channels within a single timeslot of the T1 interface.

6.4.1 Functional Description

The block diagram in Figure 22 is broken down into four components. These four components are the asynchronous interface (MD65SC51's), the protocol converter (micro and MT8952s), the switch matrix (MT8981), and the T1 interface (MH89750).

The MD65SC51's provide a standard RS232 interface that is capable of interfacing many off-the-shelf modems and data sets. A single microprocessor is capable of handling the protocol conversion between the RS232 ports and the MT8952 HDLC protocoller.

The MT8952 interfaces directly to the ST-BUS, which in turn interfaces directly to the T1 interface devices. Instead of the MT8952 operating at 64K bits continuously, it operates at 2.048 MHz and inputs/outputs an 8 bit burst every 125 µsec. This feature eliminates the need for an additional rate conversion circuit to multiplex the HDLC outputs up to the T1 data rate. Each of the HDLC chips is assigned a timeslot on the ST-BUS in a manner that is similar to enabling a voice codec.. When the MT8952 is not enabled the output driver is tristated. The channel assignment circuit is therefore very simple.

The switch matrix is used to monitor/control the T1 interface, and to reformat the ST-BUS streams between the protocol conversion and the T1 interface. The first function is to look after the T1 interface, the MH89750. This is done by operating ST-BUS stream 0 of the MT8981 in message mode. The microprocessor can then write control information to the MH89750 and read status information from the MH89750.

The MH89750 and the MT8940 form the T1 interface. The MH89750 converts the data received on the ST-BUS into a 1.544 MHz T1 stream. All of the formatting and decoding of the T1 signal is performed by this device. The interface to the device is through message mode on the MT8981 as described in the previous paragraph. The MT8940 provides the clock synchronization required to operate in a loop timed mode. Digital phase-locked loop #2 provides ST-BUS clocks that are synchronized to the extracted 8KHz and digital phase-locked loop #1 provides the transmit 1.544 MHz clock synchronized to the ST-BUS.

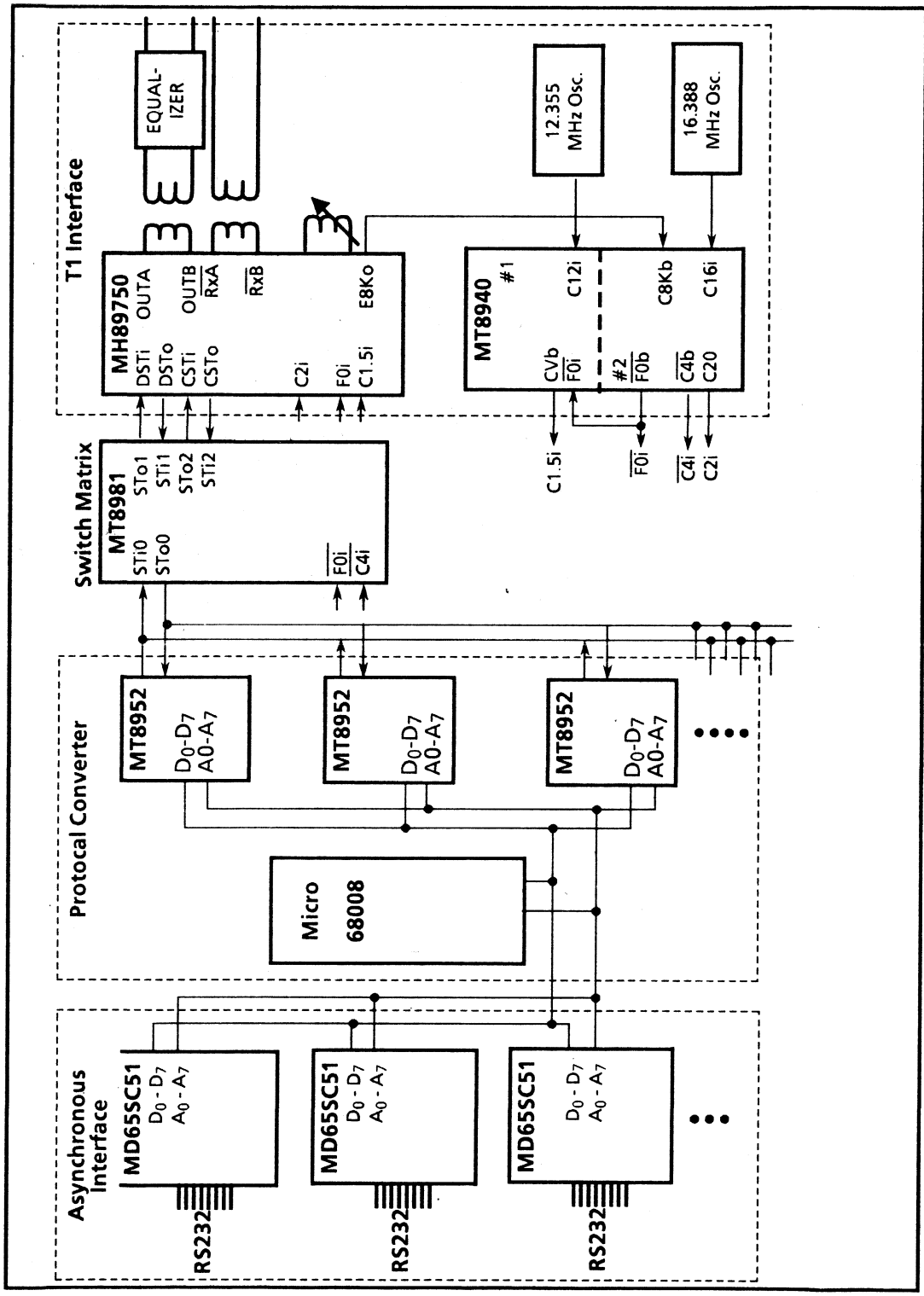


Figure 22 - Digital Multiplex Interface (DMI)

6.5 High Speed Data Transmission Link

High speed data links are becoming increasingly popular in private networks and computer communications. The basic configuration is to use the entire T1 link as a 1.536 Mbit serial channel. The data to be transmitted is usually assembled into packets such as HDLC or ethernet before being transmitted down the T1 link. If the distance to be covered is small, 1300ft. or less, then there are no T1 repeaters required and the user can string its own wire. This would be the case for a large business complex or university where there is centralized computing facilities with satellite units located in peripheral areas. If the distance travelled is greater, then the user must lease repeatered T1 line from the local telephone operating company.

6.5.1 Functional Description

The block diagram in Figure 23 is divided into three sections, protocol converter, switch matrix, and T1 interface. The protocol section is dependent on the particular format that is chosen. In this example it is assumed that the protocol is HDLC. The transmit and receive clock enables for the MT8952 are enabled for a period of 24 consecutive ST-BUS channels, and a clock speed of 2.048 MHz. This enables the protocol conversion section to interface directly to the switch matrix. Within the switch matrix the 1st 24 channels from the protocol section are redistributed in the 24 valid timeslots used by the MH89750. Once the data enters the T1 interface the MH89750 formats and transmits the data on the T1 line. Control and monitoring of the T1 interface is done through the switch matrix, the MT8980. CSTi and CSTo are connected to the ST-BUS streams that are configured for message mode so the the controlling microprocessor can access the Master Control Word and the Master Status Word.

Data is received by the opposite process. The T1 interface extracts the data from the T1 stream and formats it into ST-BUS channels, the switch matrix repositions them into the first 24 consecutive channels of the ST-BUS, and the protocol conversion section disassembles the HDLC packets.

Clock generation and synchronization is handled by the MT8940. DPLL #2 generates ST-BUS clocks that are phase-locked to the extracted 8KHz, and DPLL #1 generates the transmit T1 clock that is phase-locked to the ST-BUS frame pulse. The whole interface is therefore operating in a loop timed mode and there will be no loss of information due to slips. The MT8940 can also be configured to operate in a master timing mode if required.

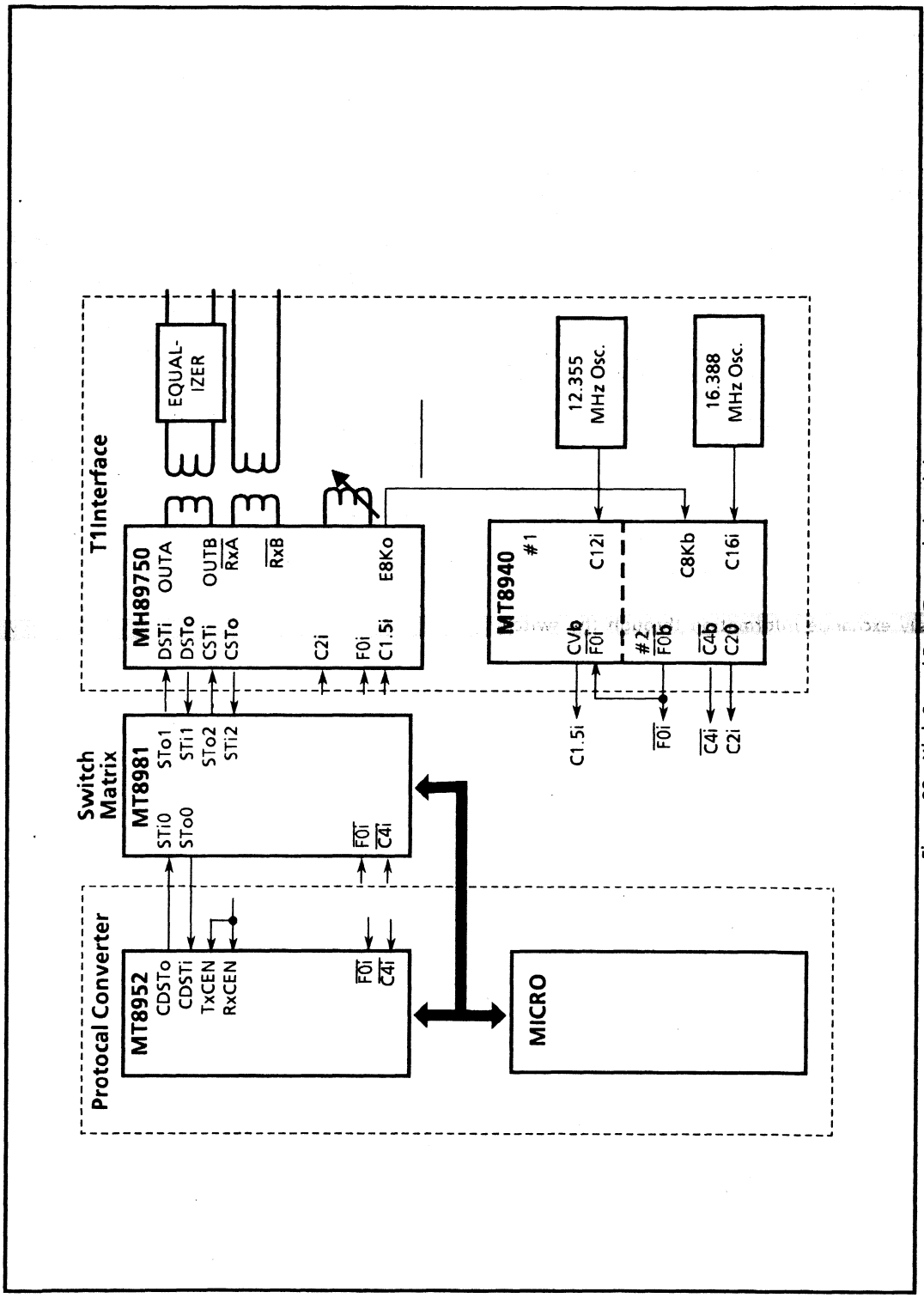


Figure 23 - High Speed Data Transmission Link

6.6 T1 to CEPT Digital Trunk Converter

There are two digital trunk transmission formats in use in the world today. They are, the T1 systems in North American and the CEPT systems in Europe. Mitel's T1 interface and CEPT interfaces both convert the digital trunk format into ST-BUS format. Therefore, the common element between the two systems becomes the ST-BUS. Once the channels have been converted to ST-BUS format they can be converted from one system to the other very easily.

6.6.1 Functional Description

The T1 to CEPT Converter is divided into four sections. Figure 24 shows the four blocks, T1 interface, switch matrix, CEPT interface, clock generation and synchronization,and DSP Element. The T1 interface converts the 1.544 MHz serial stream into the ST-BUS format where it interfaces with the switch matrix through DSTi and DSTo. The CEPT interface converts 2.048 MHz serial stream into the ST-BUS format from the other side and interfaces with the switch matrix on DSTi and DSTo.

With both the T1 data and the CEPT data converted to the ST-BUS the two digital trunk formats can easily exchange information through the switch matrix. Unfortunately, the signalling information from the two formats is not exchanged as easily. A and B signalling bits received by the T1 interface must be read by the controlling microprocessor and converted in software to the ABCD signalling bits used in the CEPT format, and vice versa. In addition to converting the signalling bits, the converter must also change the North American μLaw into CCITT standard ALaw. This is done by the block labelled DSP in Figure 24, Digital Signal Processor.

The final component of the system is the MT8940. All of the extracted 8KHz outputs from the T1 and the CEPT interfaces are combined with an AND gate before being connected to the MT8940. One of the interfaces is selected as the synchronization source by enabling its output through the Master Control Word of the chosen interface. Phase-locked loop #2 will then generate ST-BUS clocks that are synchronized to either the T1 network or the CEPT network. Phase-locked loop #1 is configured to generate the T1 transmit clock synchronized to the ST-BUS. Therefore, if the ST-BUS is synchronized to the one network then the elastic buffer in the opposite interfaces will perform controlled slips between that network and the T1 to CEPT converter.

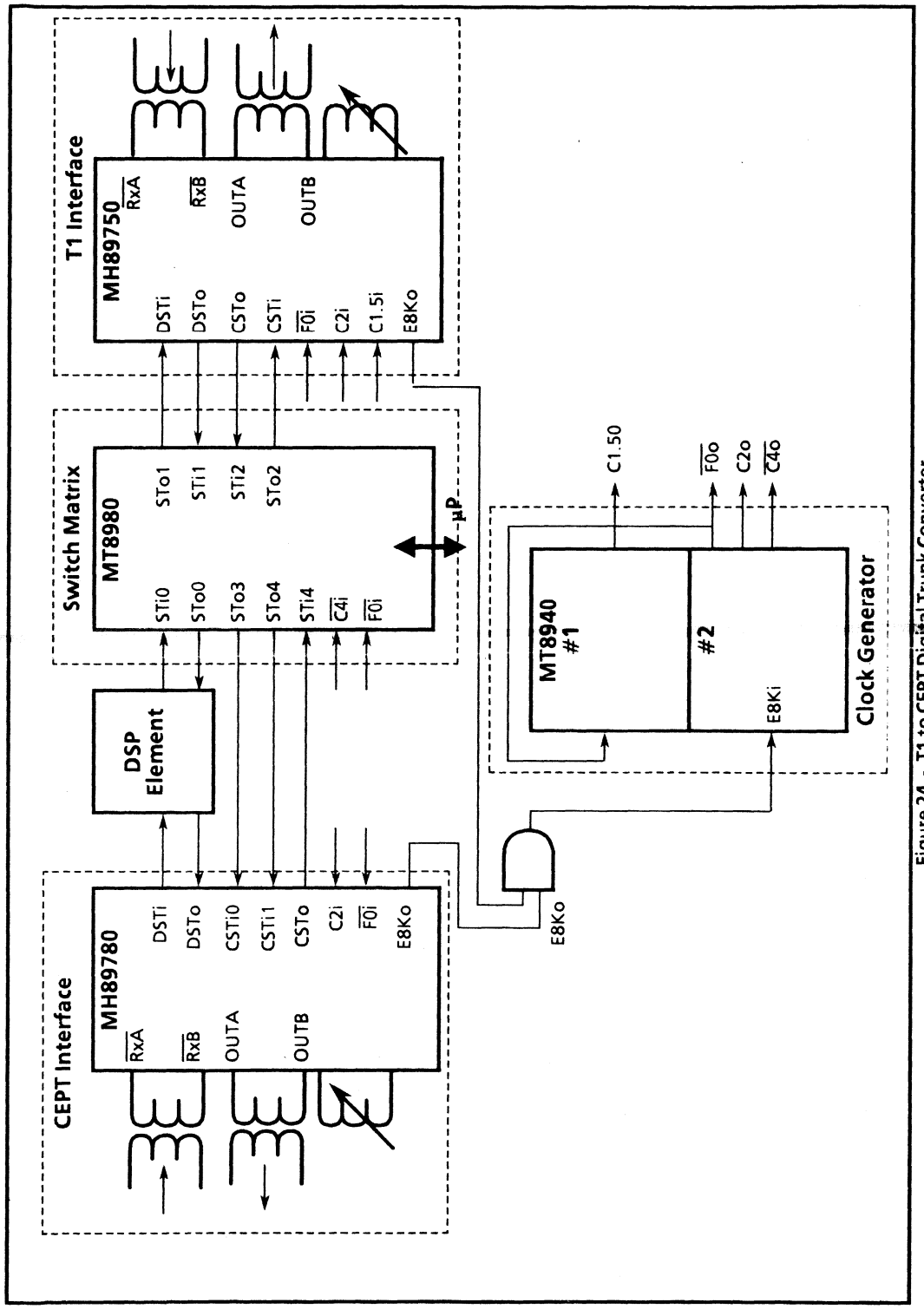


Figure 24 - T1 to CEPT Digital Trunk Converter

Notes:

Application Note MSAN-115
Software Debug Techniques Using the MD68SC49B

9161-002-021 NA ISSUE 1 JUNE 1985

The MD68SC49B Bus Monitor is an LSI device designed to monitor microprocessor address, data and control busses. When the bus condition the MD68SC49B is waiting for appears, the device interrupts the microprocessor and initiates an appropriate response. The ability to provide bus analysis on a cycle by cycle basis has enabled the Bus Monitor to greatly enhance the existing concepts of self diagnostics and microprocessor debug by increasing bus visibility.

Until now, debug services have been provided in the form of software routines resident in the microprocessor system's "monitor program". A "monitor program" is the software in ROM or EPROM that controls a microprocessor system immediately after a reset condition. It is sometimes called a "bootstrap" program. This software usually contains routines such as a routine to print a character to a terminal.

The problem with debug routines that depend entirely on software is that the microprocessor can only break the regular execution of a process by planting a software interrupt in the code that is being executed. This may only be done in areas of RAM and does not apply to program flow in areas of ROM, because program breakpoints are performed by planting software interrupts throughout the inline code (temporarily). This also limits the debug context to breaking execution if the microprocessor tries to fetch a particular instruction. In some cases it is not the fact that the code is fetched that may be of interest, it may be execution of the fetched instruction that is important. The MD68SC49B provides the hardware to make the bus "visible" to the microprocessor throughout the complete execution cycle of a particular instruction.

The following pages describe suggested debug routines and their implementation, concentrating on how the Bus Monitor is used and programmed (it is recommended that the Bus Monitor data sheet be read thoroughly before reading the application note further). These routines assume the use of a 6809 microprocessor, but could be adapted to any of the other microprocessors that the MD68SC49B can interface to, ie. the 6502, the 6802, the 8085, the Z80, the 68000, the 8086, the 8088, and the Z8000.

Each suggested command will be presented in the following format:

Mnemonic (full name)

Arguments: argument description

Description

<description of command and implementation using Bus Monitor>

The commands described are generally useful for setting breakpoints and viewing the state of the microprocessor at predetermined points of program execution. These are only suggested commands and implementations, intended to be easily modified to meet diversified requirements.

The design of a microprocessor monitor program is beyond the scope of this note, so the commands are described assuming a monitor structure that can support the interactive entry of debug commands exists. Commands that are based upon the Bus Monitor as a resource are not limited to the seven commands described in this application note, and the use of the Bus Monitor can be extended outside of the area of software debug ie. memory protection and watching for an end of message character during transmission or reception of large blocks of data.

One characteristic of the Bus Monitor must be remembered when designing these commands into a monitor program and when using them. Since a single Bus Monitor can only be set up to match on one condition at a time, and the Bus Monitor triggers the microprocessor through only one level of interrupt, a work area must be set up to keep track of what the Bus Monitor is being currently used for. This area must indicate, through the use

of flags, what command is presently using the Bus Monitor, and the area should make allowance for any qualifying attributes of the command.

The above implies that only one command may be active at one time. Provision must be made for an active/inactive attribute in the design of the routines. For each of the suggested debug commands presented here, there must be a command to remove the condition so that an alarm can be displayed if more than one command tries to use the Bus Monitor resource. Alternatively, the most recent command could take control of the Bus Monitor, however, the user might expect both commands to be active, which would be false.

The Full names of the commands described in this note are:

Byte Breakpoint
Word Breakpoint
Code Breakpoint
Range Breakpoint
Range Watch
Trace
Ram Guard

and their descriptions follow in the same order.

ByteBreak (Byte Breakpoint)

Arguments: Address of byte, relational operator, data

Description

Program execution is stopped, and control is passed to the interactive handler if the byte specified in the command line is accessed (read or written) and the data contained in the byte after the access has the correct relationship with the data specified in the command line (relational operator suggestions: <, >, >=, <=, <>, =). This command may be used for areas of RAM, ROM, or hardware address space (microprocessor support chips, etc.).

The Bus Monitor does not perform the relational comparison on the data that is needed for this command, so the Bus Monitor need only be set up for matching on the state of the address bus. This entails:

a/ Placing the specified address in the upper address boundary registers (UBADD[L] and UBADD[H], and in the lower address boundary registers LBADD[L] and LBADD[H]).

Table 1. Bus Monitor programming for ByteBreak example

Bus Monitor Register	Programmed data							
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
LBADD[L]	0	0	0	0	0	0	0	0
LBADD[H]	1	0	1	0	0	0	0	0
UBADD[L]	0	0	0	0	0	0	0	0
UBADD[H]	1	0	1	0	0	0	0	0
AMSK[L]	0	0	0	0	0	0	0	0
AMSK[H]	0	0	0	0	0	0	0	0
AIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
AIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO
DPAT	X	X	X	X	X	X	X	X
DMSK	X	X	X	X	X	X	X	X
DIMA	RO	RO	RO	RO	RO	RO	RO	RO
MODE	1	0	1	1	0	X	1	1
CCCR[L]	0	0	0	0	0	0	0	0
CCCR[H]	0	0	0	0	0	0	0	0
MCNT[L]	X	X	X	X	X	X	X	X
MCNT[H]	X	X	X	X	X	X	X	X
CIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
CIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO

Note: RO denotes Read only
X denotes Don't Care

b/ All address bits must be involved in the match, so the address mask registers (AMSK[L] and AMSK[H]) must be cleared.

c/ The access may be either a read or a write, so the state of the microprocessor must be masked from the match condition. This requires clearing the Control Code Condition registers (CCCR[L] and CCCR[H]).

d/ The Bus Monitor must be in Freeze mode (Master Mode register - MODE).

e/ Only the address image that caused the interrupt, the "new" image, is of interest (MODE).

f/ Single pass mode must be selected (MODE).

g/ Data Comparisons must be disabled (MODE).

h/ Enable address comparison, allowing matching if the address is inside the boundaries specified (MODE).

Care must be taken with regard to the use of the reset bit in the MODE register. If it is set, the Bus Monitor is armed and looking for a match (providing it has first been cleared after a freeze).

Once the microprocessor is interrupted by the Bus Monitor, the interrupt routine may obtain the data contained in the address location by reading data image register (DIMA), and then compare this with data specified in the command line. If the reset bit is cleared after a freeze, the contents of the image registers are lost (they begin to follow the state of the busses again, although a match cannot occur until the reset bit is set again).

The interrupt routine may, if the data comparison tests positively, go to the system stack to find the state of the microprocessor at the point of the interrupt. The first 12 bytes on the stack are the contents of the microprocessor's registers (except for the system stack pointer S. This may be calculated by adding 12_H to the value contained in S while the interrupt routine is executing). The microprocessor state information, the breakpoint address, and the data found in the Bus Monitor data image register may be displayed for debug information. Control should then be passed to the debug routine. If the data comparison is negative, a return from interrupt may be executed and the program can continue as before.

A command sequence could look something like this:

Debug> ByteBreak A000 > DE

The above command line would stop execution of a program, if address $A000_H$ was accessed and the value therein was greater than DE_H. The state information might be displayed as follows:

A000:FF
CC:04 A:FF B:C9 DP:00 X:0000 Y:0200 U:2050
PC:523F S:1000
Debug>

The prompt *"Debug>"* indicates that the monitor program is ready to receive interactive commands.

WordBreak (Word Breakpoint)

Arguments: Address of word, relational operator, data

Description

This command is similar to the ByteBreak command, but operates on a double byte area of memory. Therefore, any full word access on the 2 consecutive bytes starting from the specified address will cause the Bus Monitor to interrupt the microprocessor.

The differences in the implementation of this command and the previous command are:

a/ Rather than write the same address to the upper address boundary registers and the lower address boundary registers, the lower address boundary registers should contain the address specified on the command line and the upper address boundary registers should contain the next consecutive address.

b/ When an interrupt occurs, the interrupt routine should make sure that the last accessed address was the address in the upper bound register, and the previously accessed address was the address in the lower bound registers. This may be achieved by using the Old/New bit in the MODE register (see data sheet).

c/ Unlike the Bytebreak command, if the addresses in the image registers do indicate that a word access had occurred on the specified memory location, the memory location pointed to by the address in the LBADD registers must be read to obtain the data it contains. This is because the Bus Monitor does not have a double register for data pattern storage.

It must be remembered that when performing relational operations on the data contained in the specified word location, the 6809 treats the data contained in the lower address as the most significant portion of the data word.

A command sequence could look something like this:

Debug> WordBreak A000 > DE00

Table 2. Bus Monitor programming for WordBreak example

Bus Monitor Register	Programmed data							
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
LBADD[L]	0	0	0	0	0	0	0	0
LBADD[H]	1	0	1	0	0	0	0	0
UBADD[L]	1	0	0	0	0	0	0	0
UBADD[H]	1	0	1	0	0	0	0	0
AMSK[L]	0	0	0	0	0	0	0	0
AMSK[H]	0	0	0	0	0	0	0	0
AIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
AIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO
DPAT	X	X	X	X	X	X	X	X
DMSK	X	X	X	X	X	X	X	X
DIMA	RO	RO	RO	RO	RO	RO	RO	RO
MODE	1	0	1	1	0	X	1	1
CCCR[L]	0	0	0	0	0	0	0	0
CCCR[H]	0	0	0	0	0	0	0	0
MCNT[L]	X	X	X	X	X	X	X	X
MCNT[H]	X	X	X	X	X	X	X	X
CIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
CIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO

Note: RO denotes Read only
X denotes Don't Care

This would indicate that once the program started execution, if address $A000_H$ was accessed and the value therein was greater than $DE00_H$, program execution would halt and the following might be displayed:

A000: FFC9
CC:04 A:FF B:C9 DP:00 X:0000 Y:0200 U:2050
PC:523F S:1009
Debug>

CodeBreak (Code Breakpoint)

Arguments: Address of instruction where execution should stop

Description

The CodeBreak command halts execution of the program at the instruction specified by the address in the command line. This command is not actually based upon the Bus Monitor, but the Bus Monitor may be used as an error checking device. The actual break of the program's execution is performed by "planting" a software interrupt at the break address. The original code is saved when the software interrupt is inserted, and executed once the program continues after breaking.

The importance of this command is that it allows multiple breakpoints, but a constraint is that it may be used only if the program is located in RAM. The Bus Monitor may be temporarily borrowed by this command to ensure that no CodeBreaks are attempted in ROM, or in hardware address space. After the command has been implemented, the Bus Monitor should be returned to its previous use.

A command sequence could look something like this:

Debug> CodeBreak 523F

This command will stop execution of the program when the microprocessor tries to execute the code at address $523F_H$. The state of the microprocessor may be displayed as follows:

Code Break
CC:04 A:FF B:C9 DP:00 X:0000 Y:0200 U:2050
PC:523F S:1009
Debug>

RangeBreak (Range Breakpoint)

Arguments: Lower address boundary, Upper address boundary

Description

This command causes program execution to halt if an access is performed on a specified range of memory. Upon program halt, the memory address that caused the program break, the data contained in the memory location, and the state of the microprocessor's registers may be displayed. The memory range can be RAM implemented, ROM implemented, or memory mapped hardware devices. No further access of the memory address is required, like the ByteBreak command. The Bus

Table 3. Bus Monitor programming for RangeBreak example

Bus Monitor Register	Programmed data							
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
LBADD[L]	0	0	0	0	0	0	0	0
LBADD[H]	1	0	1	0	0	0	0	0
UBADD[L]	0	0	0	0	0	0	0	0
UBADD[H]	1	0	1	1	0	0	0	0
AMSK[L]	0	0	0	0	0	0	0	0
AMSK[H]	0	0	0	0	0	0	0	0
AIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
AIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO
DPAT	X	X	X	X	X	X	X	X
DMSK	X	X	X	X	X	X	X	X
DIMA	RO	RO	RO	RO	RO	RO	RO	RO
MODE	1	0	1	1	0	X	1	1
CCCR[L]	0	0	0	0	0	0	0	0
CCCR[H]	0	0	0	0	0	0	0	0
MCNT[L]	X	X	X	X	X	X	X	X
MCNT[H]	X	X	X	X	X	X	X	X
CIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
CIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO

Note: RO denotes Read only
X denotes Don't Care

Monitor must be in Freeze mode, as well as programmed to match when the address bus is "in range". The Bus Monitor must be set up in much the same manner as the ByteBreak and WordBreak commands, but the LBADD registers must contain the lower address boundary, and the UBADD registers must contain the upper address boundary. Again, the data pattern comparison is masked out, as is the condition code comparison.

A command sequence could look something like this:

Debug> RangeBreak A000 B000

Once program execution begins, if the address range from $A000_H$ to $B000_H$ is accessed, program execution would halt and the following might be displayed:

A00F:24
CC:00 A:00 B:24 DP:00 X:0000 Y:0200 U:2050
PC:523F S:1009
Debug>

RangeWatch (Range Watch)

Arguments: Lower address boundary, Upper address boundary

Description

This command is similar to RangeBreak, but rather than stopping execution and returning to interactive debug mode, this command will allow execution to continue. RangeWatch therefore provides a detailed history of program accesses to a specific range. If the range happens to be an area of code, the displayed results will in effect be a trace of program execution inside the range. This is because the 6809 will finish an instruction that has been interrupted in the middle of its execution, so when returning from the interrupt routine, the next interrupt will be caused by the execution of the instruction following the one that caused the previous interrupt. Avoid specifying the address space where the Bus Monitor routines lie. This would put the microprocessor into a loop where it is continually interrupted before it returns to execution of the main program.

Trace

Arguments: Number of instructions to be executed

Description

A command can be created that takes advantage of the Bus Monitor's ability to "trace" program execution inside of the address range the Bus Monitor is programmed to match on. The Trace command will accept a set number of instructions to trace as an argument, starting from the current position of the program counter (the PC must contain a valid instruction address).

The Bus Monitor routine must keep a count of the number of instructions executed. While instructions remain to be traced, the Bus Monitor is configured to interrupt on the entire address range except for accesses of the Bus Monitor routine itself. This may be done by specifying the range of the Bus Monitor routine in the boundary address registers, and

Table 4. Bus Monitor programming for Trace example

Bus Monitor Register	Programmed data							
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
LBADD[L]	0	0	0	0	0	0	0	0
LBADD[H]	1	1	1	1	1	1	0	0
UBADD[L]	0	0	0	0	0	0	0	0
UBADD[H]	1	1	1	1	1	1	1	0
AMSK[L]	0	0	0	0	0	0	0	0
AMSK[H]	0	0	0	0	0	0	0	0
AIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
AIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO
DPAT	X	X	X	X	X	X	X	X
DMSK	X	X	X	X	X	X	X	X
DIMA	RO	RO	RO	RO	RO	RO	RO	RO
MODE	1	0	1	1	0	X	1	0
CCCR[L]	0	0	0	0	0	0	0	0
CCCR[H]	0	0	0	0	0	0	0	0
MCNT[L]	X	X	X	X	X	X	X	X
MCNT[H]	X	X	X	X	X	X	X	X
CIMA[L]	RO	RO	RO	RO	RO	RO	RO	RO
CIMA[H]	RO	RO	RO	RO	RO	RO	RO	RO

Note: RO denotes Read only
X denotes Don't Care

programming bit 0 of the Mode register to match when the address bus is outside of this range (clear bit 0). Once again, data matches and control condition code matches are of no consequence, and masked out.

This command does require knowledge of the address of the traced instruction before execution as the PC image on the stack during execution of the interrupt routine contains the address of the next instruction. To display the code, the locations from the previous PC value to the current PC value must be accessed (Read).

A command sequence could look something like this:

Debug> Trace 3

Program execution will begin from where the last breakpoint stopped, 3 instructions will be traced, and execution will stop once more. The trace might appear as follows:

523E: 4F
CC:04 A:00 B:24 DP:00 X:0000 Y:0200 U:2050 PC:523F S:1009

523F: 9E 20 00
CC:00 A:00 B:24 DP:00 X:0420 Y:0200 U:2050 PC:5242 S:1009

523E: 5F
CC:04 A:00 B:00 DP:00 X:0000 Y:0200 U:2050 PC:5243 S:1009

Debug>

RamGuard (Ram Guard)

Arguments: Lower address boundary, Upper address boundary

Description

This command is suggested for monitor programs that have the capability to download software from a remote system. To avoid downloading software in an undesirable area, ie. hardware address space or on top of software that the user does not want to lose, the Bus Monitor may be programmed to match on accesses to those areas.

Rather than immediately program the Bus Monitor, this command dictates default Bus Monitor attributes for the downloading procedure to implement when called. When an illegal address range is accessed, the Bus Monitor will interrupt the microprocessor, downloading will cease and an error message that includes the accessed address can be displayed. The user may then take corrective measures. Data pattern matching must be masked out, in range address matching and Freeze mode specified. A command sequence could look something like this:

Debug> Ramguard A000 B000

When a download is being performed, the Bus Monitor would stop the operation if an attempt was made to place data in memory in the range $A000_H$ to $B000_H$. An error message could be displayed as follows:

>Error Downloading!! Download attempted at memory address A000! ROM located here!

Debug>

Application Note MSAN-117
Applications of the MT3530 300 BPS Single Chip Modem

9161-001-034-NA ISSUE 1 JUNE 1986

Contents

1.0 Introduction

Modems are used for exchanging information between home computers, personal computers, banks, offices and mainframes to name just a few possible applications. Computers and other data processing machines work with data in the form of binary pulses whereas the long distance communication medium, used by the telephone system, requires bandlimited analog signalling. The modem converts digital baseband data to an analog carrier and vice versa so that two devices such as a computer and a data terminal may communicate over a telephone system.

300 baud modems are among the most common data communications devices in use today. Modem system, based on the MT3530, has the advantages of full duplex communication using either Bell 103 or CCITT V.21 Recommendation Standard, a built-in interface to the industry standard RS-232C serial data port, very low system part count, and low power ISO²-CMOS single chip modem I.C.

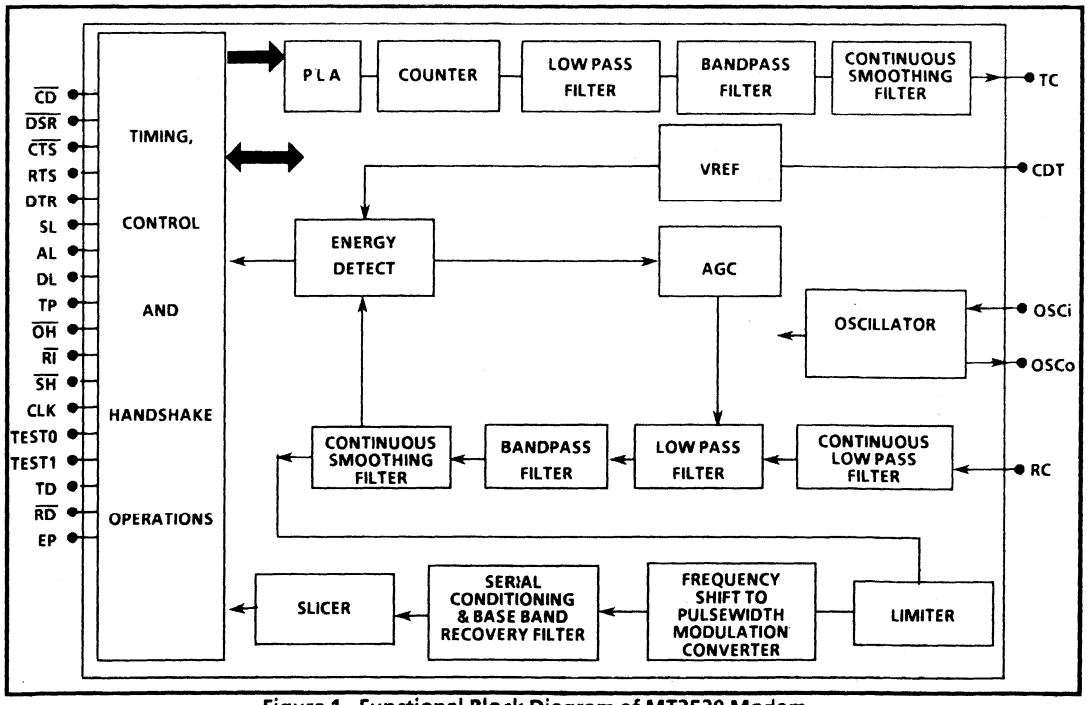


Figure 1 - Functional Block Diagram of MT3530 Modem

TABLE OF CONTENTS

LIST OF FIGURES

1.1 Why are Modems Used?

The digital data signal is, typically, a random sequence of pulses which has a continuous power spectrum. This spectrum extends to zero frequency, hence, transmission via a telephone line is not possible because a phone line is bandlimited. See Figure 2.

The purpose of a modem is to translate digital signals into analog signals compatible with the existing telephone network bandwidth of 300 Hz to 3400 Hz. In transmit mode the modem converts binary data into analog signals that the phone line can carry. In the receive mode the modem demodulates the analog signals from the phone line, converting them back to the binary form.

1.2 What is a 300 Baud FSK Modem?

Bell 103 and CCITT V.21 are both 300 baud modem specifications. They use Frequency Shift Keying (FSK) modulation for data transmission over standard phone lines. FSK encodes binary data into two discrete frequencies within the bandwidth of the media used. A logic "1" in the bit stream places a Mark frequency (Fm) on the phone line. A logic "0" places a Space frequency (Fs) on the line. See Figure 3. Full duplex operation occurs when two-way transmission happens simultaneously between two modems. Since FSK modulation encodes only one bit per baud, it uses approximately 1 Hz of bandwidth for each bit per second of data rate. At 300 bps, two independent channels can be accommodated within the line's bandwidth using Frequency Division Multiplexing (FDM). See Figures 4 and 5.

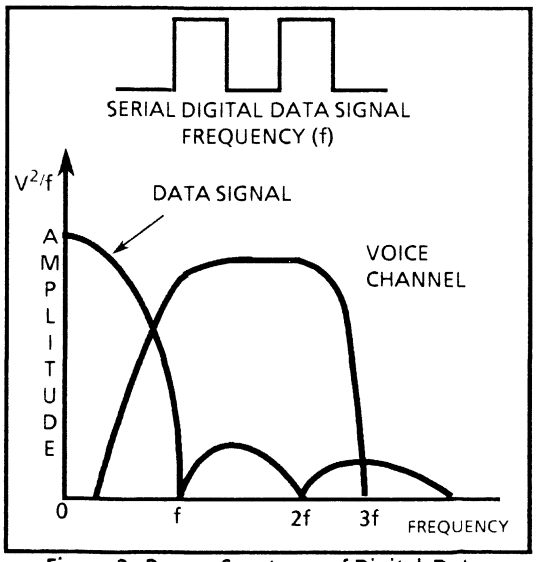


Figure 2 - Power Spectrum of Digital Data

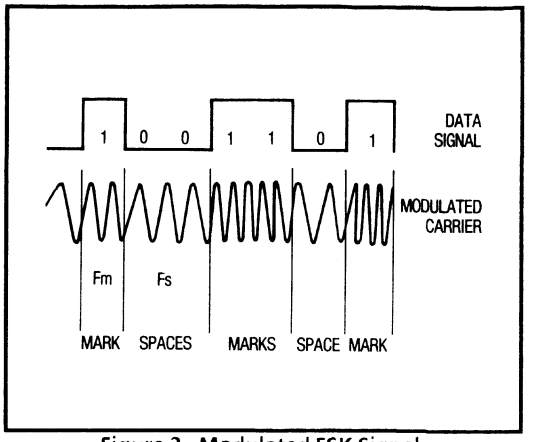


Figure 3 - Modulated FSK Signal

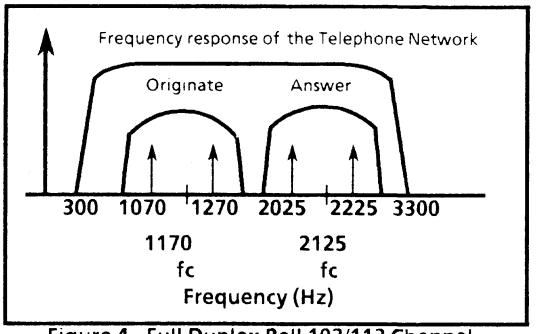


Figure 4 - Full Duplex Bell 103/113 Channel Assignment

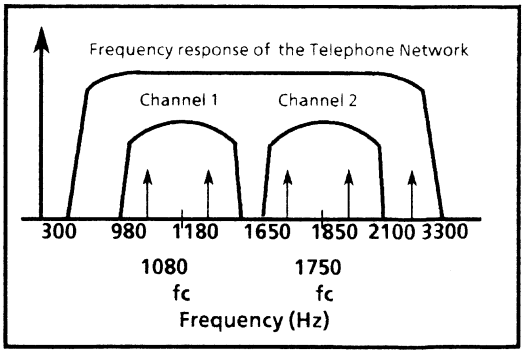


Figure 5 - Full Duplex, CCITT V.21 Channel Assignment

2.0 Inside the MT3530

The MT3530 is a single-chip 300 baud FSK Modem implemented in a 5 μm double polysilicon ISO^2-CMOS technology. It consists of six major functional blocks; modulator, transmit filter, receive filter, demodulator, energy detect circuit, and timing, control and handshake logic. A functional block diagram is shown in Figure 1.

2.1 Modulator

The FSK modulator is composed of a programmable logic array (PLA) driving counters with provision for phase continuous Mark/Space transitions i.e. the phase of the signal remains constant during a frequency transition. The output of the modulator is a square wave of the frequency corresponding to the Mark/Space being sent.

2.2 Transmit Filter

The output of the modulator is fed to the transmit filter. The frequency response when operating in Bell 103 mode is shown in Figure 6. This filter consists of three concatenated sections: a third-order elliptic low pass filter, a fourth-order elliptic bandpass filter, and a second order Sallen and Key low pass smoothing filter. The low pass filter provides the necessary smoothing for the modulator square wave output and the bandpass filter eliminates noise from the desired carrier frequencies. Finally, the carrier is passed through the antialising filter to produce the transmit modulated carrier.

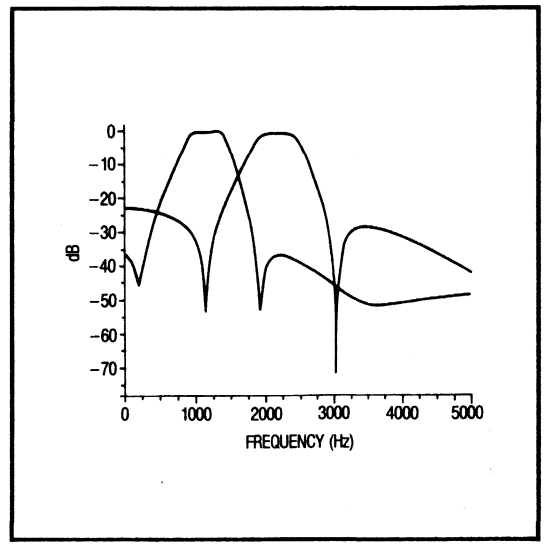


Figure 6 - Transmit Filter Bell 103

2.3 Receive Filter

The receive filter consists of four cascaded sections; a second-order continuous filter, a second-order switched capacitor prefilter for antialiasing, and an eighth-order bandpass filter, followed by a second-order continuous smoothing filter. The frequency response of the receive filter when operating in Bell 103 mode is shown in Figure 7.

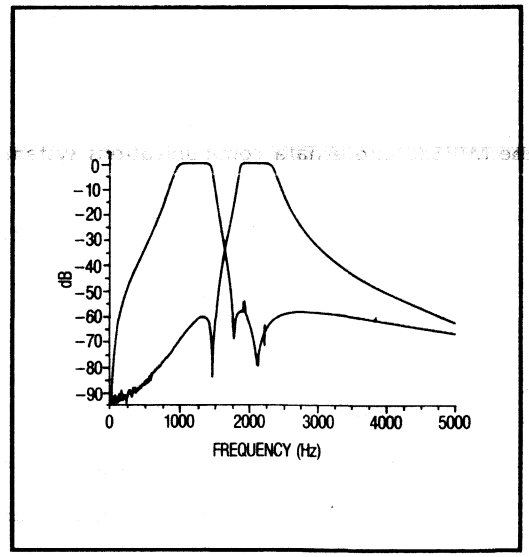


Figure 7 - Receive Filter Bell 103

The prefilter contains means for programmable gain which is used to implement an automatic gain control (AGC) function in conjunction with the on-chip energy detect circuit. This allows the usable dynamic range of the received carrier to be 0 to - 50 dBm.

2.4 Demodulator

To perform demodulation, the filtered carrier is bandlimited and converted to pulse width modulation format. This is, then, introduced to a baseband recovery filter which includes a third-order Bessel low pass filter.

2.5 Carrier Detection

The carrier detect circuit causes $\overline{CD}$ pin output to turn On and Off at receive carrier levels of - 41 and - 50 dBm, respectively, with appropriate timing. These levels can be modified by applying an external voltage to the device's CDT pin. The filtered receive carrier is rectified with programmable gain and integrated with provision for cancellation of offset voltages in the circuit. The output is compared to a reference voltage and the resulting data is retained in memory to implement an AGC function. The timing and protocol control on carrier detection is implemented digitally. The device's $\overline{RD}$ output, which presents demodulated data bits from the received carrier, is clamped High when either the carrier turns Off or DTR is set Low.

2.6 Timing, Control and Handshaking

This block, besides providing necessary timing signals to various parts of the device, also implements the RS-232C interface. Further, the control section provides the capability for automatic answering/origination/dialing. It supports Phone Line Interface and Diagonostic control. Timing for the internal operation is governed by the 3.579545 MHz clock.

2.7 Other Functions

The transmit and receive sections are programmable and can be made to work in the same frequency band to allow for true analog loopback capabilities to facilitate local testing. Remote testing is made possible by inclusion of digital loopback capabilities.

3.0 Data Communications System using the MT3530

3.1 Data Communications System Configuration

The MT3530 can be configured to operate with very few external components. However, a sophisticated application will want to incorporate the MT3530 into a data communications system consisting of many functional features. This section deals in some detail with each of the functional features. A block diagram of the data communications components required to implement a complete system using the MT3530 is given in Figure 8.

Usually, a local Data Terminal Equipment (DTE) or central processing unit (CPU) needs to transmit and receive data from a remote DTE or CPU using the telephone system as the communication path. In figure 8 the digital data communications and Automatic Calling Unit (ACU) functions are controlled by Communications System Controller (CSC). If the ACU functions are not desired then a Universal Asynchronous Receiver/Transmitter (UART) can be used to control the digital data flow between the terminal and the modem. The UART type of control function is described more thoroughly in Section 4.2. The control/data information received from the CPU is conditioned by the CSC for interface with the modem. The Hybrid provides the 2-wire to 4-wire conversion to allow the modem to be attached to the telephone network. Finally, the Phone Line Interface permits connection to the Public Switched Telephone Network (PSTN).

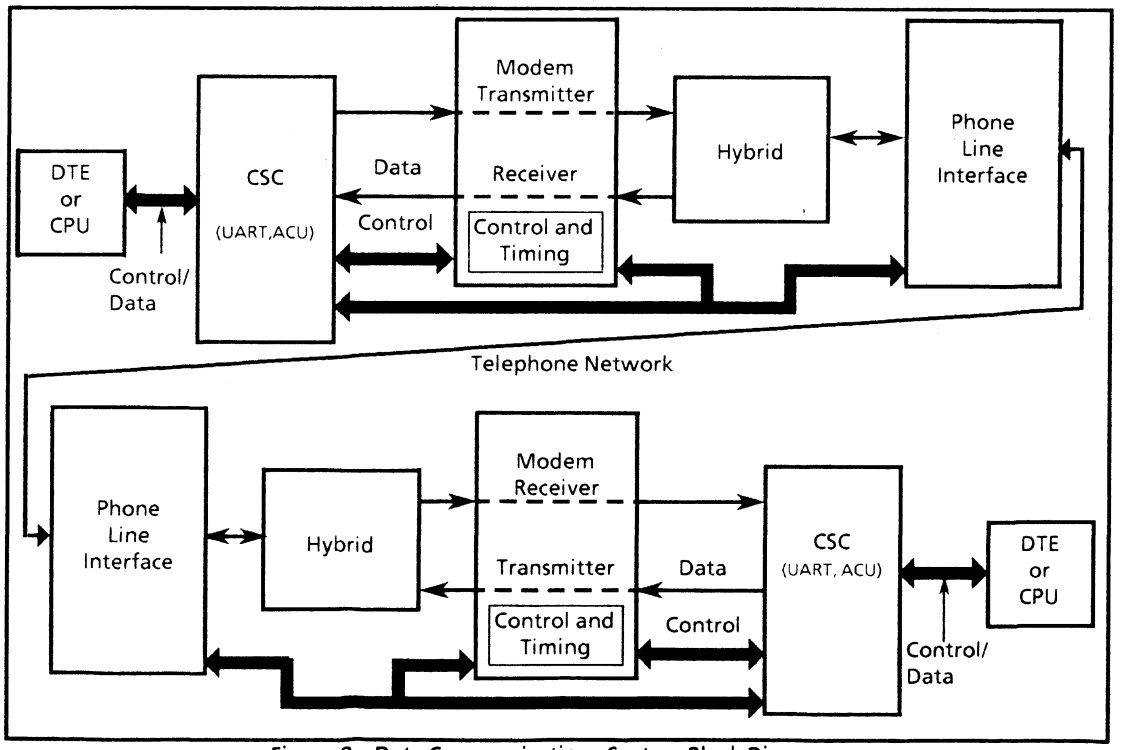


Figure 8 - Data Communications System Block Diagram

3.2 MT3530 Design-In Considerations

In this section, external connections to the MT3530 are defined. Also, special circuit and component considerations for designing the MT3530 based data communications system are explained in detail.

3.2.1 Clock Crystal

The MT3530 has an internal oscillator and clock generator that can be controlled either by an external crystal or external clock. It uses a low-cost 3.579545 MHz crystal as the master clock generator. This crystal is very popular because it is used in all NTSC colour TV's and in many low cost personal computers for interface with TV monitors. The MT3530 can, therefore, use the same system clock as the display interface. The characteristic of a crystal which is acceptable for use with the MT3530 is given below:

Quartz Crystal Specification (25 °C ± 2 °C)	
Operating Temperature Range	0 °C to + 70 °C
Frequency	3.579545 MHz
Frequency Calibration Tolerance	± 0.02 %
Load Capacitance	18 pF
Effective Series Resistance	180 ohms, max.
Drive Level-Correlation/Operating	2 mW
Shunt Capacitance	7 pF, max.
Oscillation Mode	Fundamental

When a crystal is used, terminals OSCi and OSCo are connected as shown in Figure 9a. Additional 18 pF capacitor to V_{EE} from each of the pins is required.

3.2.2 External Clock

An external 3.579545 MHz clock can be applied to OSCi pin of the MT3530. See Figure 9b. The OSCo pin should be left disconnected in this case. The duty cycle and input voltage level are important parameters when an external clock is chosen over a crystal. A TTL level, 50% duty cycle, square wave can be applied to OSCi pin through a 0.1 μF decoupling capacitor.

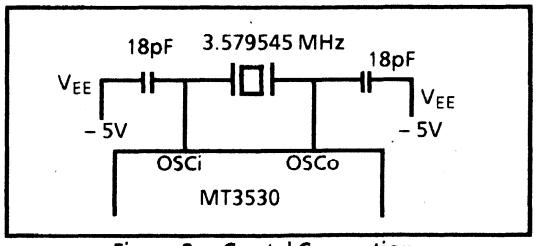


Figure 9a - Crystal Connection

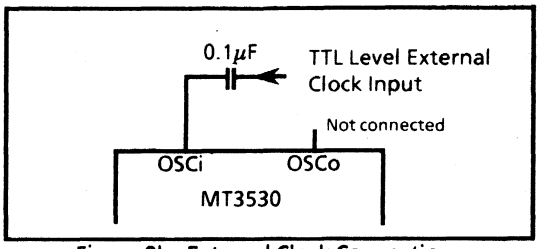


Figure 9b - External Clock Connection

3.2.3 Power Supply Decoupling

Symmetric positive and negative power supplies (± 5V) are required for the operation of the MT3530. Additionally, the reference voltage for Carrier Detect Threshold is derived from the ± 5 V rails. Decoupling V_{CC} to DGND and V_{EE} to AGND with 0.1 μF capacitors connected close to the device supply pins is recommended.

3.2.4 Reset Protocol

By ensuring that all control inputs are in their inactive states for a minimum of 2 ms before the rising edge of DTR, the MT3530 will be properly reset.

SL (Select)	Mode	Transmit Frequency (Hz)*		Receive Frequency (Hz)*	
		Mark	Space	Mark	Space
0	Bell 103 Originate Bell 103 Answer	1270 2225	1070 2025	2225 1270	2025 1070
1	CCITT V.21 Channel 1 (Originate) CCITT V.21 Channel 2 (Answer)	980 1650	1180 1850	1650 980	1850 1180
	CCITT V.25 Answer Tone	2100			

Table 1 - BELL 103 / CCITT V.21 Operating Modes

Space = Binary 0, Mark = Binary 1, Crystal Frequency = 3.579545 MHz, *Frequency drift = ± 3 Hz

3.2.5 Type Selection

MT3530 is Bell 103/113 and CCITT V.21 compatible. Table 1 illustrates the two types of operating modes. The basic principle is the same but the frequencies and the timings are switched. When in V.21 mode the V.25 Answer Tone of 2100 Hz will be generated upon answering.

3.2.6 Carrier Detect Threshold (CDT)

Applying a voltage between 0 and – 5 V_{DC} at this input allows control of the receive carrier detection threshold. This will override the internally determined threshold level of – 41 dBm for receive data carrier. Note that when the CDT pin is left open the output voltage level can vary between -1.5 V and – 4 V. Therefore, the external voltage level needed to set a required carrier detection threshold will vary from device to device.

3.2.7 Timing, Control and Handshake

The RS-232C interface feature facilitates interfacing the modem to a standard RS-232C interface in stand-alone applications or a UART in other applications where the modem is integrated into the Data Terminal Equipment. The control section, in addition, provides the capability for auto answering/origination/pulse dialing. It incorporates a 14 seconds abort timer and a loss of carrier timer which provide call termination capability.

3.3 MT3530 Phone Line Interface (PLI)

Interface of any equipment to the public switched telephone network (PSTN) is governed by the National Regulatory Agencies. There are two different ways of interfacing modems to the phone line. One of these is to use a Data Access Arrangement (DAA). In the U.S. this requires meeting FCC Part 68 Certification before connecting to the PSTN. The DAA is designed to handle the phone line interface including the 4-wire to 2-wire conversion.

Direct Connection Under FCC Rules, Part 68

The FCC registration program was created in 1975 to allow non-Bell producers of modems the right to connect their equipment directly to the public switched telephone network (PSTN). In order to comply with the requirements of Part 68 all such equipment must contain protective circuitry to provide isolation to the user equipment from the PSTN, similar to the protection formerly provided by Data Access Arrangements (DAA). FCC Rules, Part 68, requires that the protective circuitry either be an integral part of the modem and registered as the terminal device or that the protective circuitry be separate from the modem and registered as protective circuitry. Under FCC Rules, Part 68, this registration class is "Terminal Device" and equipment type is "Data Modems".

The second Public Switched Telephone Network connection scheme uses an acoustic coupler. An acoustic coupler uses the existing telephone handset and is not directly connected to the phone line.

3.3.1 Acoustic Coupling

The MT3530 can be connected to the telephone network using an acoustic coupler. Figure 10 shows how acoustic coupling is accomplished. No component values are given because the speaker and microphone impedance characteristics can vary.

Typically, the modem's transmitted carrier is amplified through a speaker and presented to the mouthpiece of a standard telephone handset. The modem received carrier signal is derived from the earpiece of the same handset by a microphone; the signal is then attenuated and presented to the modem. Note that there is a hybrid in the telephone handset that performs a 2-wire to 4-wire conversion between the public switched network and the MT3530.

The gain of the amplifier at the modem Transmit Carrier output (TC) should be adjusted such that the maximum signal power on the phone line is less than the limits set by the National Regulatory Agencies. In the U.S., this limit is – 9 dBm as measured into 600 ohms. For CCITT applications this limit is reduced to – 13 dBm. The power level on the line will be a function of a number of parameters; the modem transmit carrier output level, the gain of the external amplifier, and the characteristics of the speaker on the output of the modem transmit carrier and the handset mouthpiece.

The gain of the receive amplifier which feeds the MT3530 receive carrier should be adjusted to provide a peak signal at RC pin of no more than 0 dBm. However, it is often sufficient to compensate the gain of the receive op-amp so that signal level across the Tip and Ring is delivered to the RC pin on the MT3530.

3.3.2 Direct Connection of Data Modems

Direct connection means that the modem is connected to the telephone line through an

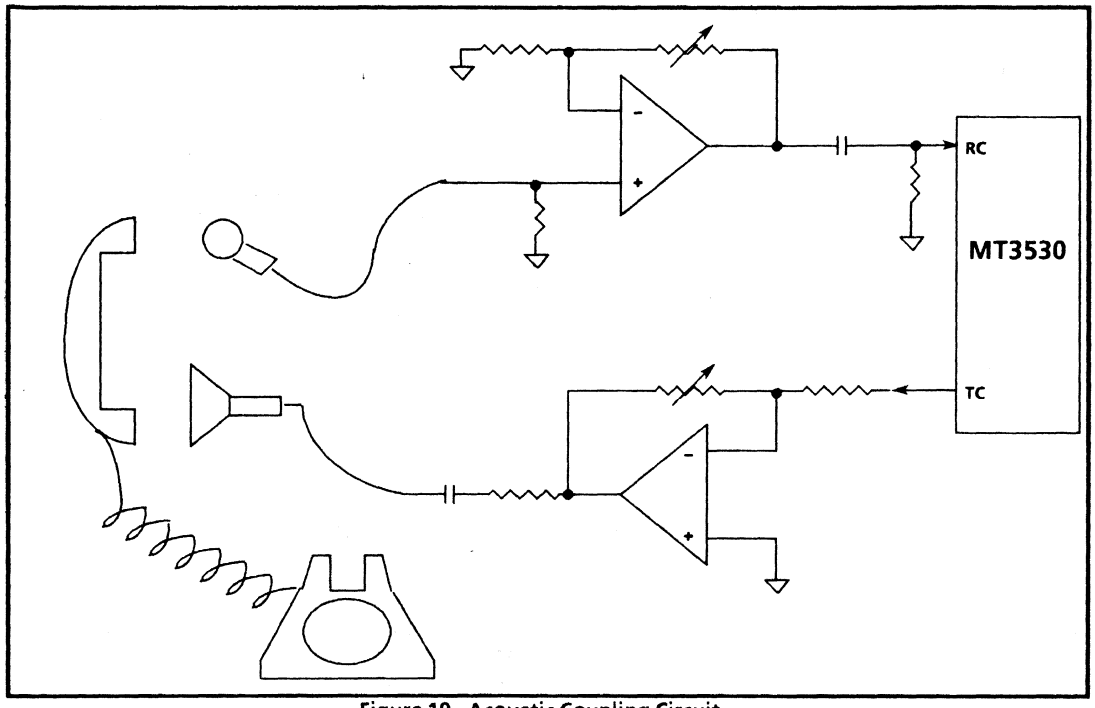


Figure 10 - Acoustic Coupling Circuit

approved interface device termed Data Access Arrangement (DAA).

The prime elements of the DAA are transmit signal level, impedance matching, line isolation, transient protection and the billing timing delay. Other functions integrated as part of the DAA include ring detect and switch-hook circuitry.

Any equipment connected to the switched telephone network must meet "permissive" or "programmable" transmit level specifications. The most commonly used is permissive specification. In this arrangement the level must not be greater than -9 dBm as measured into 600 Ω when averaged over three seconds. For CCITT applications this should be no greater than -13 dBm. The MT3530 transmit carrier output is limited at -8 ± 1 dBm.

Standard termination is defined as 600 Ω and is the reflected impedance required by the primary of the transformer. The impedance matching of the transformer (600 Ω) represents the nominal AC impedance of the phone line which changes with frequency and conductor type and size. Off-hook DC resistance of the terminal equipment circuitry is preferred to be less than 200 Ω.

Figure 11 illustrates a typical Direct Connect DAA.

A set of standard requirements for an isolation transformer is as follows:

- Primary impedance: 600 Ω;
- Secondary Impedance: 600 Ω (nominal);
- Maximum DC Current: 90 mA (*Note 1*);
- Frequency Response: 300 - 3000 Hz ± 0.5 dB;
- DC Resistance: Preferably less than 200 Ω. This is in compliance with FCC Rules, Part. 68.31;
- Echo Return Loss: 20 dB (*Note 2*);
- Harmonic Distortion: Low (Typ. 0.1% at 300 Hz, 90 mA);
- Dielectric Strength: 1500 V AC or greater between primary and secondary. The core is to comply with FCC Rules, Part 68.302 and 68.304.

***Note 1**: As an alternate design, additional electronic components may be used to shunt DC line current, thus allowing use of a smaller transformer which would only carry an AC signal component. The holding coil then provides the DC path for the holding current provided by the Central Office.*
***Note 2**: Imperfections in the isolation transformer make impedance matching a complex task. Transformers for phone line isolation reflect incoming signals back into the telephone network at a reduced level. This is known as echo return loss.*

High voltage transient suppression is usually performed with bidirectional Zener diodes which limits the potential between Tip and Ring to a specified threshold (1500 V in the U.S.). The series resistor is inserted for short circuit current limiting. Zener protection may, also, be provided on the secondary side to protect modem equipment. When automatic answering the phone, Part 68 of

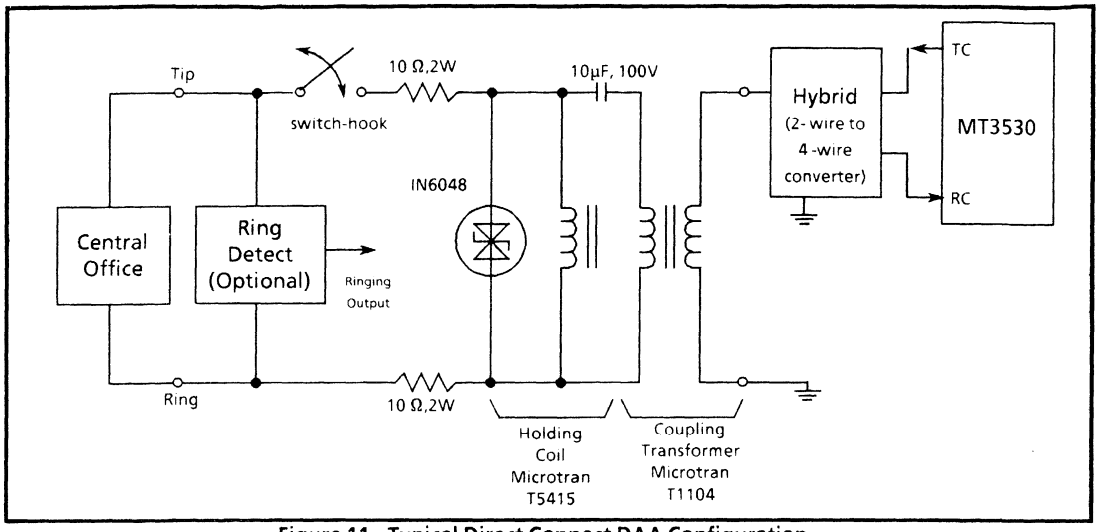


Figure 11 - Typical Direct Connect DAA Configuration

the FCC Rules specifies the user must ensure a silence (non-data) interval on the phone line of at least two seconds for billing purpose before any data or answer tone may be transmitted. CCITT specifies 1.8 to 2.5 seconds of silence. The MT3530 provides for a silence interval of 2.0 seconds mininum when in Answer mode.

The DAA circuit may be used in automatic answering applications with the addition of ringing detection circuitry. The requirements of the ring detection circuitry are as follows:

i) Meet the 1500 volt longitudinal surge requirement and 1000 volt metallic surge requirement of FCC Rules, Part. 68.302;

ii) Provide a minimum on-hook DC resistance of 10 MΩ at 100V DC and 3 kΩ at 300 V DC, and on-hook AC impedance of less than 40 kΩ but greater than 1600 Ω in compliance with FCC Rules, Part 68.312;

iii) Provide immunity to false ring detection caused by rotary dial pulses generated by other telephones which bridge the same metallic pair on the data modem;

iv) Respond to incoming ringing voltage of 40 V_{RMS} to 150 V_{RMS} at frequency of 16 Hz to 68 Hz;

v) Per Bell System Technical Reference PUB6100, the ring detection circuit should ignore valid ring bursts of 125 ms or less.

The DAA interfaces to PSTN on the Tip and Ring leads. The relay provides the on-hook/off-hook control for connection or disconnection from the line. When the DAA is off-hook, the relay is closed, loop current flows through the isolating transformer (or the holding coil) and the rest of the DAA is connected to the line. This indicates a desire to make a call or answer a call. In Answer mode once the ring signal has been detected, the modem is placed off-hook. The off-hook control line may, also, be used for pulse dialing in accordance with Bell Technical Reference PUB 1100, provided that the telephone set is on-hook.

The relay requirements nominally are:

i) Meet or exceed the criteria of FCC Rules, Part 68.302 and 68.304. These rules deal with environmental simulation and leakage current;

ii) Be available with gold capped silver palladium contacts for auto dial applications;

iii) Minimum possible power consumption;

iv) Long life rating as specified in minimum number of operations (contact transfers);

v) Rated at 75 V_{DC}, at 70 mA DC loop current and 150 V_{AC} at 130 mA AC ring current.

3.3.3 Hybrid (Duplexor)

The receiver and transmitter of the modem require one pair of wire each for physical connection. For standard PSTN connections, only one pair of wire is available. Therefore, a duplexor or electronic hybrid (also known as 2-wire to 4- wire converter) is used to interface the modem with the telephone network.

The design of the hybrid requires to take into account the following; the impedance of the telephone network is coupled through the DAA's isolation transformer. The hybrid should be designed to match the impedance of the network across the frequency band which is used for the modulation to allow maximum power transfer.

The design requirements of an effective hybrid for the MT3530 are:

i) At least – 2 dB gain from the TC pin output to the telephone network for application in the U.S. Note that for CCITT application this gain should be at least – 5 dB.

ii) A 0 dB loss from the telephone network to the RC pin input.

iii) A minimum signal transfer ratio from TC to RC.

Figure 12 illustrates a hybrid circuit using operational amplifiers. The design calculations include the following: Transformer, Transmit Amplifier and Hybrid Receive Amplifier.

3.3.3.1 Transformer (T1 in Figure 12)

Standard termination is defined as 600 Ω and is the reflected impedance required by the primary of the transformer. In this design a representative transformer is selected and the secondary termination resistance is determined (equivalent to R_1) for a reflected impedance of 600 Ω at the primary.

The receive loss (R_X Loss) from primary to secondary needs to be measured and must be compensated for by the receive amplifer R_XA. With the primary and secondary of the transformer properly terminated the transmit loss across the secondary termination resistor R_1 is measured (R_1 loss). The loss across the transformer, T_X Loss, is also measured to determine the gain of the transmit amplifier T_X A.

3.3.3.2 Transmit Amplifier

Due to the losses described above, to transmit a level of – 9.5 dB (allowing a 0.5 dB manufacturing margin), the output of transmit amplifier T_X A has a gain of:

$(-9.5 + R_1 \text{ Loss} + T_X \text{ Loss} - T_{OUT} \text{ max})$ dB.

Where:

T_{OUT} max is the maximum transmit output level. This is – 7 dBm for the MT3530.

3.3.3.3 Receive Amplifier

The hybrid receive amplifier R_XA requires that the maximum level which can be applied to the RC input of the MT3530 is 0 dB. Therefore, the voltage output of the receive amplifier should not exceed 0 dB. The receive amplifier must, also, make up for the receiver transformer amplifier loss, R_X Loss. However, it is often sufficient for the receive amplifier gain to be such that the signal across Tip and Ring is delivered to the Receive Carrier pin at the same level. The receive amplifier R_XA, then, has a gain of : R_X Loss dB.

Although, the MT3530 provides 55 dB of adjacent channel rejection, the hybrid receive amplifier can be used for additional rejection of the MT3530 transmit signal through use of differential amplifier techniques. The resistor R_2 from the Transmit Carrier pin to the inverting input of the receive amplifier is to provide side tone suppression. The

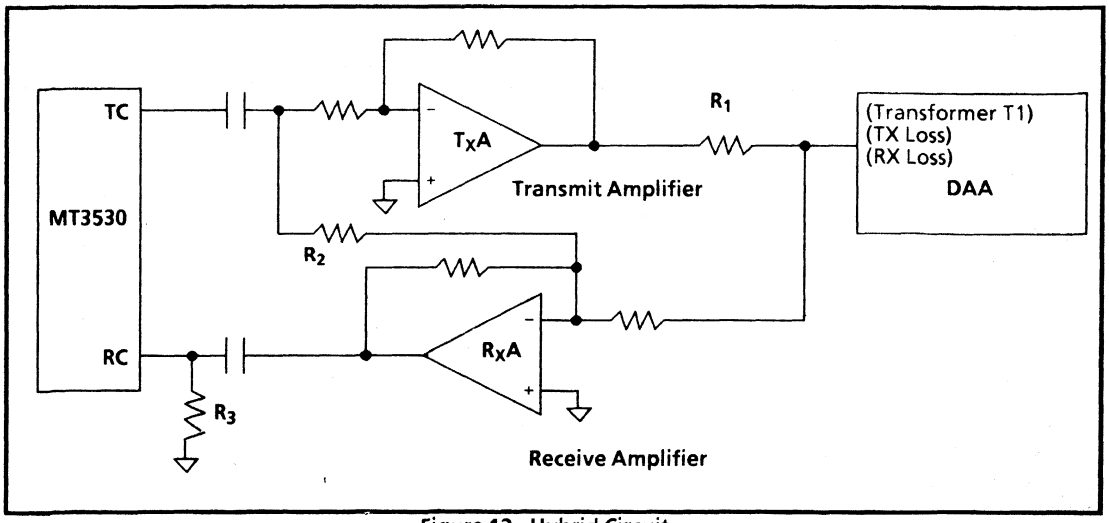


Figure 12 - Hybrid Circuit

transmit carrier is provided through R_2 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled and presented to the Receive Carrier input on the MT3530 at a reduced level. Under ideal conditions 20 dB or more of cancellation might be achieved, but because telephone lines vary considerably, a cancellation not less that 10 dB is a more realistic figure.

The purpose of the termination resistor R_3 is to provide a DC bias to the op amp of the receive filter in the MT3530.

3.4 MT3530 Operation

The modem I.C. may be operated in Bell 103/113 or CCITT V.21 type applications. Logic control on select (SL) pin defines the operating mode. See Table 1. Two diagnostic modes, analog and digital loopback, allow for system tests. Refer to Section 5.0 for details. In addition, Passthru mode is available in which the timing and the protocol handshake depedence can be suspended.

3.4.1 Auto Answer

In the Answer mode the MT3530 stands idle waiting for an incoming call. To assist in answering incoming calls, the ring indicate signal (RI) from DAA is connected to the $\overline{RI}$ pin of the MT3530. With DTR High and RTS Low, a Low from the ring detector to $\overline{RI}$ causes the MT3530 to initiate Auto Answer sequence by setting $\overline{OH}$ and $\overline{DSR}$ Low (See Figure 13). $\overline{OH}$ Low enables the hook-switch relay, thereby, connecting the modem to the telephone line. The duration of $\overline{RI}$ Low should be greater than 107 ms. Otherwise, the device will disable $\overline{OH}$ and disconnect the telephone line. The modem commences 2.0 seconds (minimum) of silence followed by Answerback Tone. This is a 2225 Hz (Mark) carrier when operating in Bell 103 mode. The generation of Answer Tone continues until:

i) The 1270 Hz (Mark) carrier from the originating modem is detected and the answering modem automatically picks up within 100 ms by setting $\overline{CD}$ and $\overline{CTS}$ Low. This completes the handshaking sequence and communication is established;

or

ii) DTR is set Low. See Reset Protocol in Section 3.2.4 for details.

If no Answer Tone is detected within 14 seconds of being put into the Answer mode, the modem will abort the call. Refer to Auto Abort section 3.4.3 for details.

When operating in V.21 mode the V.25 Answer Tone of 2100 Hz is generated for 3.4 seconds. 80 ms later 1650 Hz (Mark) carrier is generated. The rest is the same as Bell 103 except that the frequencies and timings are switched to V.21 specification. See Figure 14 and Table 1 for additional details.

If the chip is in the Answer mode and an originating modem, not following Bell or CCITT protocol, sends carrier before the MT3530 has finished the Auto Answer sequence the modem will lock-up. This means that there will be Carrier Detect but handshaking will not be completed and data will not be transferred. This is of particular importance in V.21 application because the duration of the answer sequence with the Answer Tone is almost six seconds.

3.4.2 Auto Originate Mode

With DTR High, a call is initiated by applying a High to the RTS input. This will cause $\overline{OH}$ to go Low, enabling the hook-switch relay and connecting the telephone line. This puts the MT3530 in the Auto Originate mode. When dial tone is detected, RTS can be pulsed Low/High to provide dial pulses. The $\overline{OH}$ will follow the RTS pulses, sending the desired digits over the telephone line. The proper timing for dialing must come from the Data Terminal on the RTS line.

When the answering modem comes on line it will wait for 2.0 seconds ("billing" delay) and then send the 2225 Hz Answer Tone for Bell 103 operating mode. Refer to Figure 13. Note that if the answering modem sends a carrier within 2.0 seconds the modem will lock-up. The $\overline{CD}$ pin output on the originating modem will go Low 200 ms (max.) later indicating received carrier. 236 ms (max.) later, the MT3530 will respond with 688 ms (max.) of 1270 Hz carrier. At the end of that time $\overline{CTS}$ (Clear-To-Send) will go Low indicating to the Data Terminal Equipment that the communication link has been established. If no carrier is detected within 14 seconds of being put into Originate mode, the modem will abort the call.

When in V.21 mode, the principle is the same but the frequencies and timings are switched to V.21 specifications. See Figure 14 and Table 1 for additional details.

3.4.3 Auto Abort

There is an automatic abort feature in the MT3530 to avoid tying up a system when there is a difficulty in establishing the link. If no carrier is detected within 14 seconds after the device has been put into the Answer or Originate mode it will abort the call

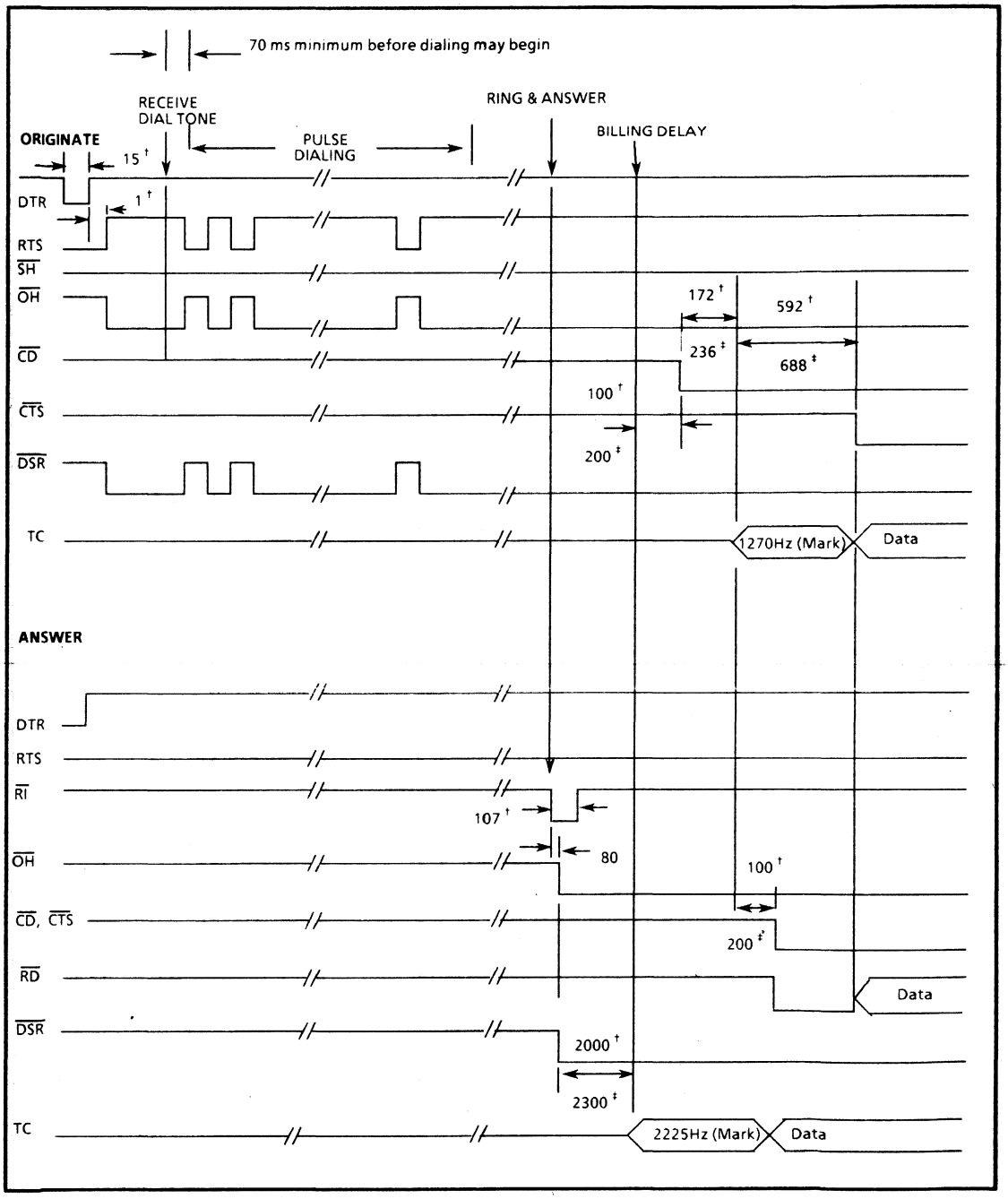


Figure 13 - MT3530 Modem Timing * Chart for Bell 103 Operating Mode

* All timing is in milliseconds and the value is typical unless specified
† Denotes the minimum value
‡ Denotes the maximum value

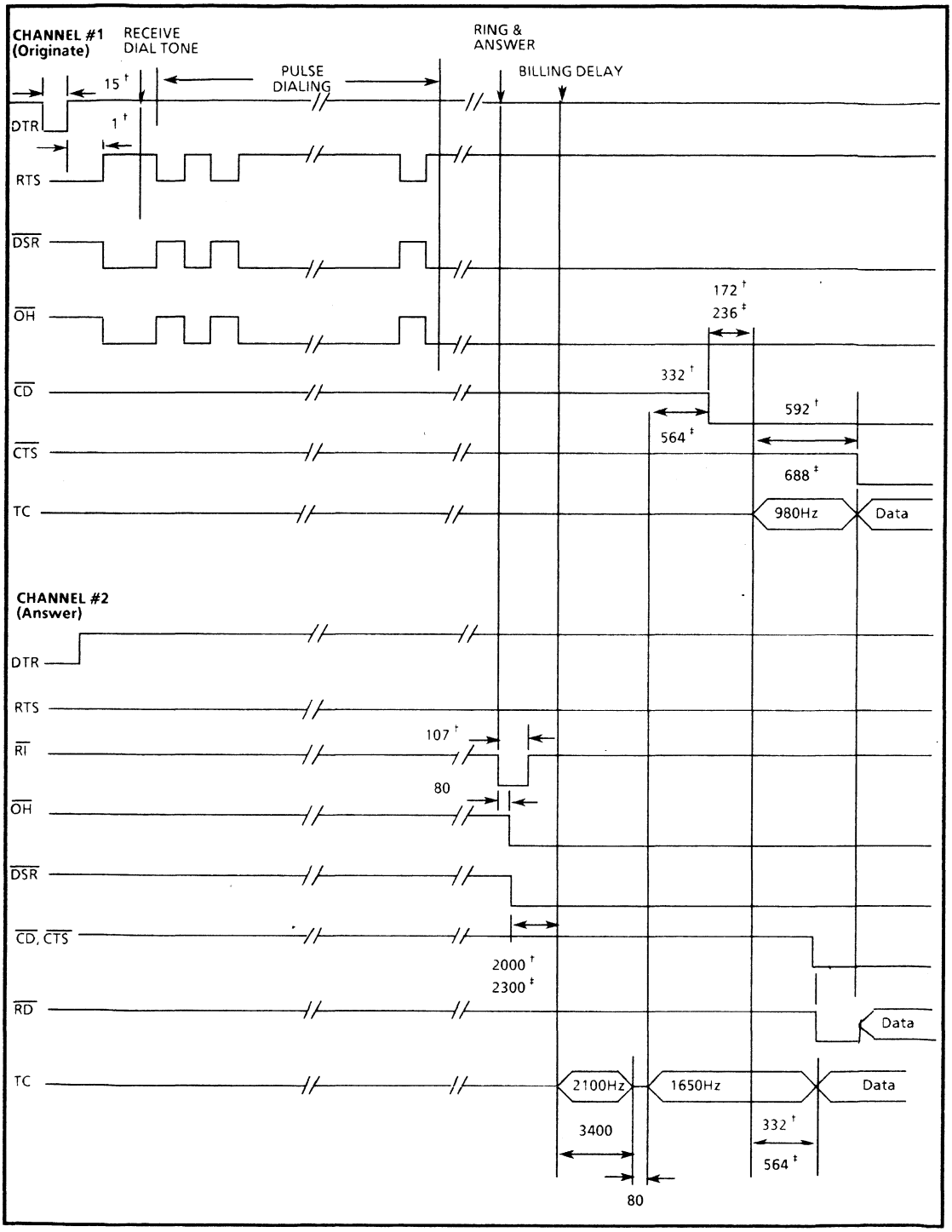


Figure 14 - MT3530 Modem Timing * Chart for CCITT V.21 Operating Mode

* All timing is in milliseconds and the value is typical unless specified

† Denotes the minimum value

‡ Denotes the maximum value

by setting $\overline{OH}$ High and disconnecting the telephone line. $\overline{DSR}$ will also go High. This abort time can be extended by pulsing RTS Low for about 1 ms before the 14 seconds have elapsed. This will reset the abort timer.

Alternatively, if it does not time out DTR will need to be pulsed Low to reset the MT3530. A High level at DTR input enables all other inputs and outputs. In fact, if DTR goes Low for more than 14 ms during a data transmission or reception period, the device will enter an irreversible disconnect sequence. To ensure that the modem is in Originate mode following Auto Abort it is necessary to Reset the device.

See Reset Protocol Section 3.2.4 for details.

3.4.4 Auto Shutdown

Should the received carrier fall below – 50 dBm during data exchange for more than 210 ms, the MT3530 will terminate the call by setting $\overline{OH}$ High and disconnecting the telephone line. To ensure that the modem is in Originate mode following Auto Shutdown it is necessary to Reset the MT3530.

3.4.5 Manual Mode

The MT3530 can be operated manually as well as automatically. With DTR High a negative pulse (– 5V) of greater than 107 ms on $\overline{RI}$ will put the MT3530 in the Answer mode. Similarly, with DTR High and $\overline{SH}$ pulled Low for greater than 54 ms will put the MT3530 in Originate mode. A Low on $\overline{SH}$ will cause $\overline{OH}$ to go Low and start the Originate sequence. The hook-switch relay is enabled and connection to the phone line is made.

3.4.6 Passthru Mode

The MT3530 can be put in Passthru mode with the control of "TEST0" and "TEST1" (see Table 2). In this mode the modem stands idle in the Originate mode. The transmit and receive functions become independent of each other. The timing and handshake protocol can be suspended depending on the status of DTR. Figure 15 illustrates the functionality of the device in Passthru Mode.

TEST0 PIN 7	TEST1 PIN 6	MT3530 STATUS	H = + 5 V (V_{DD}) L = – 5 V (V_{EE})
L	L	Normal	
H	L	Passthru	

Table 2 - Passthru Mode Control Inputs

With DTR set Low, the device is placed in Originate mode. The transmit and receive functions become independent of timing, RS-232 Interface and Phone Line Interface. See Table 3 for a summary of the status of MT3530. All the events on $\overline{SH}$, $\overline{RI}$ and RTS pins are ignored. Therefore in this mode the modem can not be set in an Answer mode. Note that $\overline{CD}$ is not active and there is no carrier lock-up in the event that the answering modem sends the carrier too early.

With DTR High the Answer or Originate mode is selected in the same manner as in the normal mode. See Tables 4a and 4b for a summary of the status of MT3530. The transmit and receive functions are dependent on timing and handshake protocol. $\overline{CD}$

MODE	STATUS LINES †						
	$\overline{SH}$	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ORIGINATE	X	X	H	H	L	H	X

Table 3 - Passthru Mode with DTR Low
†(X = Don't Care, L = Low, H = High)

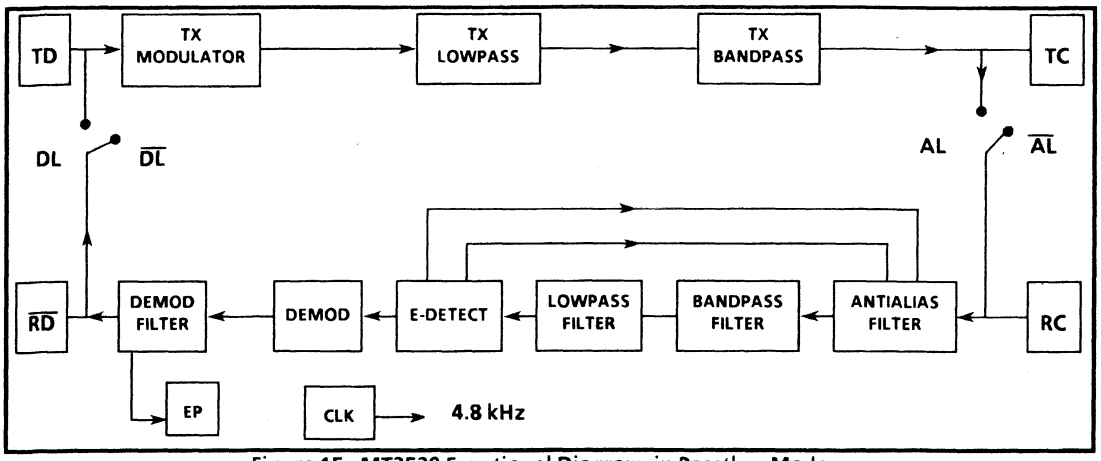


Figure 15 - MT3530 Functional Diagram in Passthru Mode

MT3530 Auto Mode

MODE	STATUS LINES †						
	$\overline{SH}$	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ANSWER	H	L	L	L	L	L	L
ORIGINATE	H	H	L	L	L	L	H

Table 4a - Passthru Mode with DTR High

MT3530 Manual Mode

MODE	STATUS LINES †						
	$\overline{SH}$	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ANSWER	H	L	L	L	L	L	L
ORIGINATE	L	L	L	L	L	L	H

Table 4b - Passthru Mode with DTR High

†(L = Low, H = High)

operates as in the normal mode. It should be noted that, if a Space is sent before a Mark, $\overline{CD}$ will not be active until it sees a Mark first. In Passthru mode with DTR High Auto Shutdown applies where as Auto Abort does not apply. After call termination the modem is placed in the Originate mode.

In Passthru mode the analog and digital loopback functions are available as in the normal mode.

3.4.7 Call Termination Procedures

The MT3530 modem offers the following three features which permits call termination:

i) Data Terminal Ready not active

ii) Abort Disconnect

iii) Loss of Carrier Disconnect

3.4.7.1 Data Terminal Ready not active

The DTR signal must be High (active) in order for the modem to remain connected to the telephone line. If DTR is set Low for greater than 15 ms, the MT3530 resets and $\overline{OH}$ pin goes High. This disconnection procedure is the only method that the DTE has of terminating a call. The exception is when the modem is in Auto Originate mode. In this case RTS Low will cause $\overline{OH}$ to go High.

3.4.7.2 Abort Disconnect

This sequence is not an option and is employed when the Data Set Ready ($\overline{DSR}$) is Low (activated). See Section 3.4.3 for details. This sequence should be implemented on automatic answering modems in case the modem is called by mistake, i.e. the modem will not stay connected to the telephone line in anticipation of a received carrier.

3.4.7.3 Loss of Carrier Disconnect

The MT3530 modem will terminate the call by setting $\overline{OH}$ High when a loss of carrier energy is detected. The loss of carrier disconnect sequence begins when the received signal level goes below – 50 dBm. Figure 16 shows that the modem carrier loss disconnect timing diagram.

3.5 Automatic Calling Functions

The MT3530 can be used in systems which require automatic calling. In these systems, calls are generated automatically by a host processor which has been programmed to perform the tasks. The steps involved in automatic calling are:

i) Generate the off-hook command to the DAA
ii) Detect dial tone from the Central Office
iii) Generate dial pulse or DTMF dialing tones
iv) Detect remote modem Answer Tone
v) Transmit data

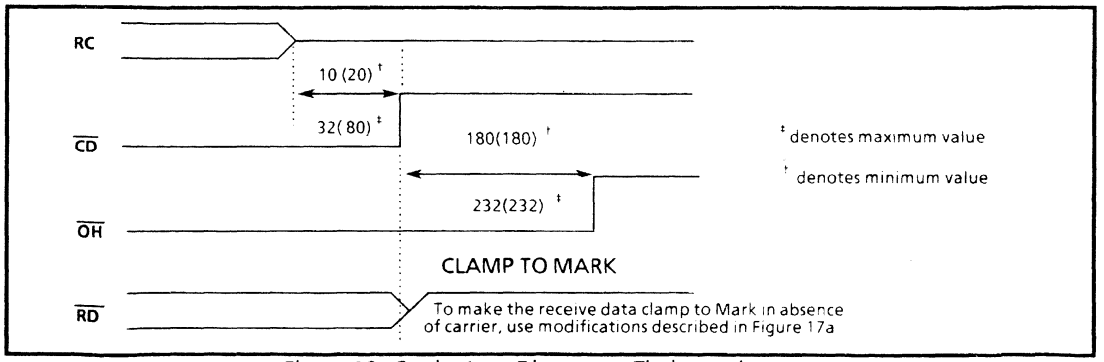


Figure 16 - Carrier Loss Disconnect Timing * Diagram

*Bell 103 (CCITT V.21) timing is in milliseconds

3.5.1 Generation of Off-Hook

In automatic calling systems, normally the connection to the phone line is controlled by an off-hook relay lead. With DTR High, and a High applied to the RTS input, $\overline{OH}$ pin 24 will go Low. This enables the hook-switch relay and connects the telephone line. This puts MT3530 in the Auto Originate mode.

3.5.2 Dial Tone Detection

After going off-hook, the C.O. will provide dial tone to the subscriber. In modern central offices which accept DTMF dialing, the C.O. will provide a "precise" dial tone which is a composite of 350 and 400 Hz. In older central offices which do not accept DTMF dialing it is difficult to predict exactly what the frequency spectrum of the dial tone will look like. It is nominally in the 300 to 700 Hz range. A call progress detection chip is required.

It is assumed that if automatic calling functions are performed there is a host processor in the system which can provide the control. Once dial tone has been detected by the host processor, dialing may begin.

3.5.3 Dial Pulsing

Pulse dialing is the process of opening (breaking) and closing (making) the loop connection. This is accomplished in MT3530 by pulsing RTS Low/High to provide dial pulses. The $\overline{OH}$ will follow the RTS pulses. The proper timing for dialing must come from the Data Terminal or Host Processor on the RTS line.

If the making and breaking of the loop conforms to requirements set by the Bell System, the Central Office will count the number of breaks in determining each digit to be dialed. The number of breaks in a digit equals to the digit to be dialed. The exception to this rule is the digit "0" which requires ten break intervals in it. The timing required by the Bell System is as follows:

Pulse Repetition Rate: 8 to 11 break intervals per second (normally ten);

Break Percentage: 58% to 64% during this interval;

Interdigit delay: 600 milliseconds to 3.0 seconds in the make condition.

3.5.4 DTMF Dialing

The easiest way of generating DTMF tones is to use a DTMF tone generator integrated circuit.

3.5.5 Answer Tone Detection

After the host processor has dialed the desired number, a number of events may occur. Assuming that the call goes through, the remote (answer) modem will provide an Answer Tone to the calling (originate) modem. When an Answer Tone is detected by the MT3530, $\overline{CD}$ pin output will go Low. When in Bell 103 mode, the Answer Tone is 2225 Hz carrier (Mark). This will set $\overline{RD}$ pin output of the MT3530 High. The 2100 Hz Answer Tone is followed by 1650 Hz carrier. This causes the $\overline{CD}$ pin output to go Low and the $\overline{RD}$ pin will be Low. Once an Answer Tone has been detected the calling modem responds with transmit carrier. This is a 1270 Hz carrier (Mark) for Bell 103 operation and 980 Hz carrier (Mark) for V.21 operation. Data exchange may begin after detection of an Answer Tone by the far end (answering) modem. Refer to Figures 13 and 14 for timing details.

If Answer Tone is not detected by the MT3530 after a user determined length of time, the host processor may retry the call later. See Section 3.4.3 for details.

4.0 MT3530 Modem System Configurations

The MT3530 can be interfaced to either parallel or serial I/O ports of standard data terminal equipment. Connection to an intelligent terminal or serial computer port is accomplished using only line receivers and drivers. An Asynchronous Communications Interface Adapter (ACIA) is required to connect the MT3530 modem system to a parallel microcomputer bus.

4.1 Serial Interface Application

A stand-alone modem can be configured using the MT3530, RS-232C/V.24 line drivers and receivers, a phone line interface and a 2-wire to 4-wire hybrid. Figures 17a, 17b and 18 are for a stand-alone RS-232C interface modem to be used as a peripheral accessory to a terminal or serial computer port.

Figure 17a is a serial interface schematic for upto 300 bps asynchronous operation. Figure 17b shows a phone line interface schematic. This is intended as a suggested starting point only and should be adapted to fit each particular application. It is not FCC Part 68 approved.

If one wants to avoid the protection/certification details, a certified DAA can be used instead. Figure 18 shows a suggested application diagram.

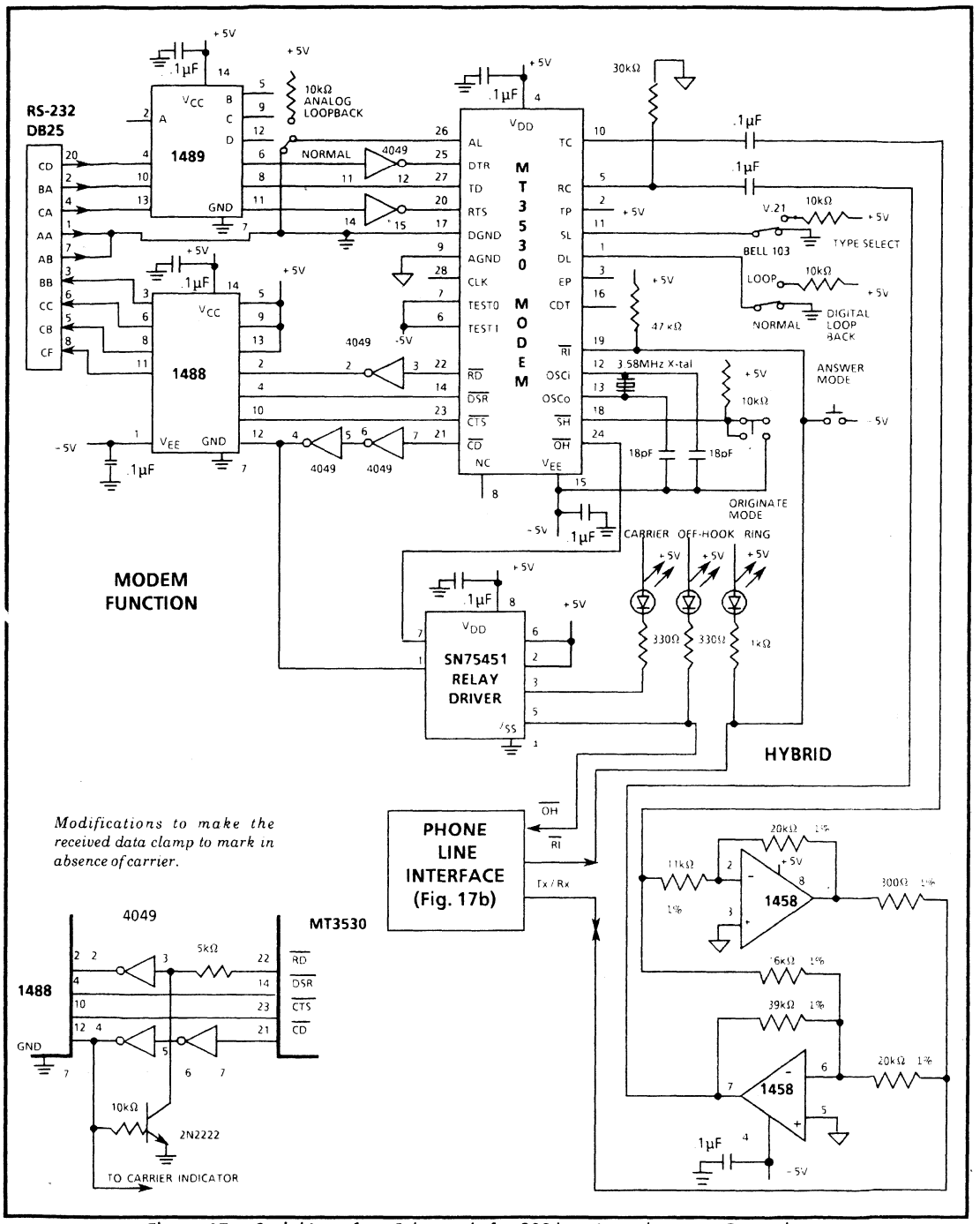


Figure 17a - Serial Interface Schematic for 300 bps Asynchronous Operation

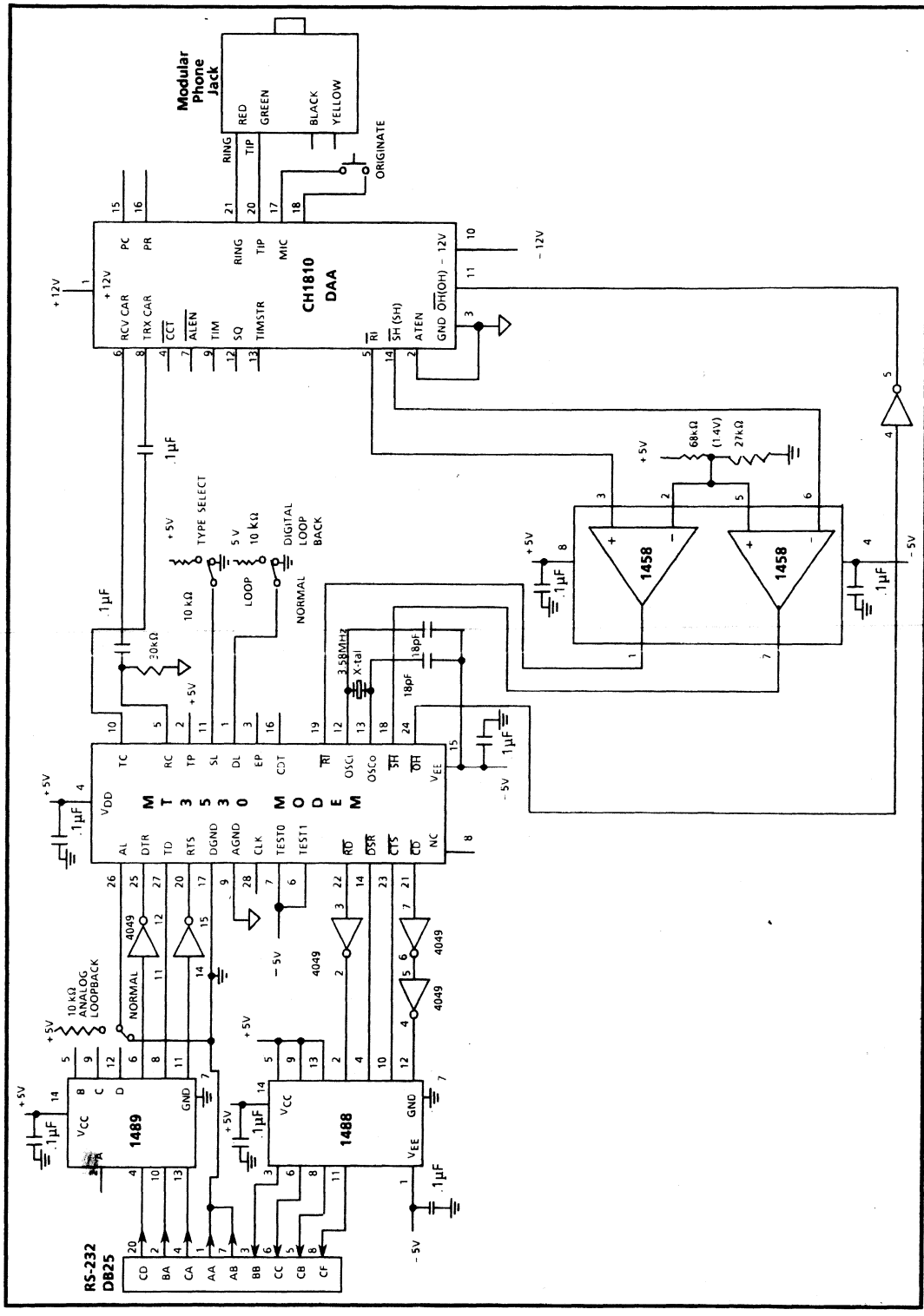


Figure 18 - Suggested Application Schematic Using Part 68 Certified DAA

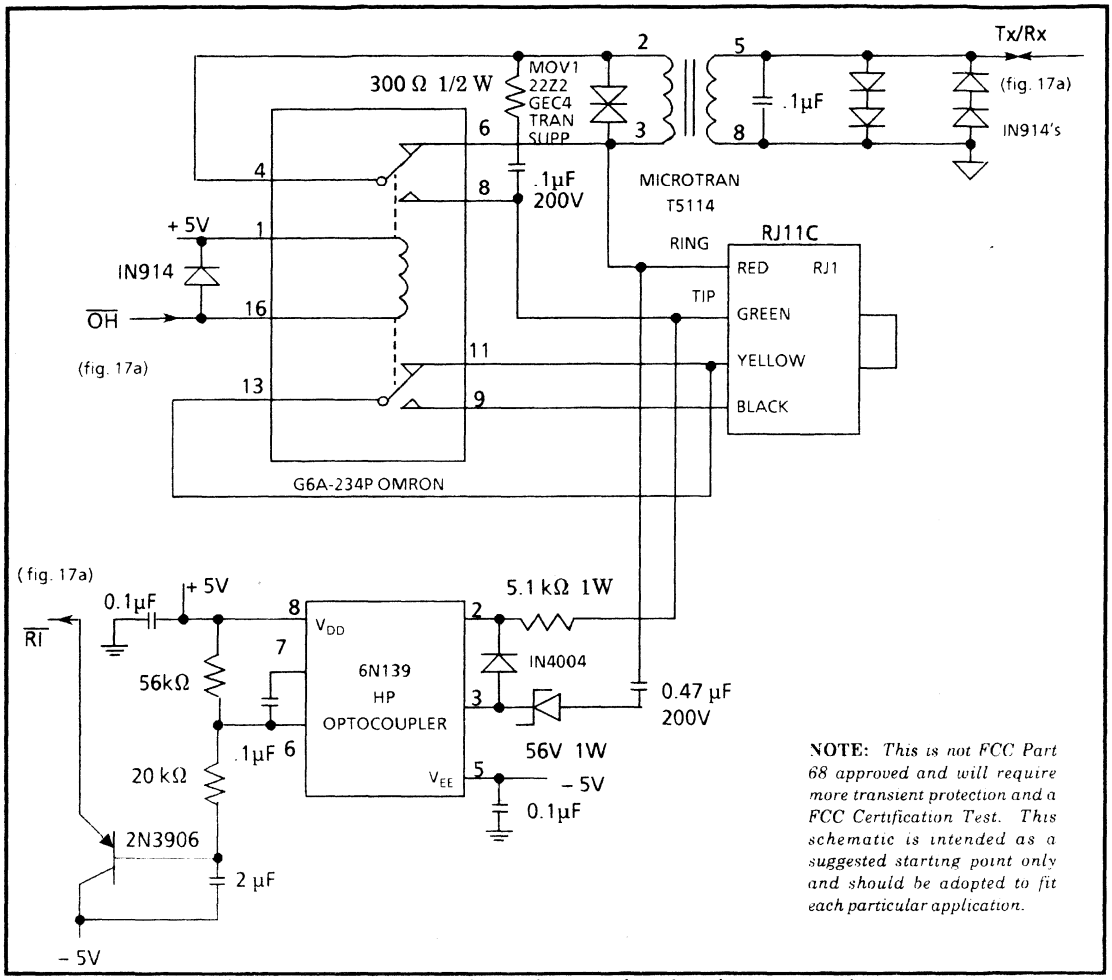


Figure 17 b - Suggested Phone Line Interface for Direct Connection of Modem to the Telephone Line

The DAA is designed to handle the phone line interface including the 4-wire to 2-wire function and is already registered with FCC.

4.1.1 Details of Serial Interface Design

In the circuit, Figure 17a, the hybrid 4-wire to 2-wire converter utilizing the dual op amp was configured to provide 1:1 conversion in each direction. The Transmit Carrier output from the MT3530 is amplified by the op amp to compensate for the losses in the 300 Ω matching resistor and the coupling transformer. The transmit carrier is delivered to the line at - 9 dBm. For CCITT applications this should be reduced to - 13 dBm.

In the receive direction the loss in the coupling transformer is compensated for by the other half of the op amp. If there is a - 20 dBm signal across Tip and Ring then a - 20 dBm signal is delivered to the Receive Carrier input on the MT3530.

The 300 ohm resistor is to provide the proper termination so that Tip and Ring look like a 600 Ω AC impedance to the line. The 16 kΩ resistor from the Transmit Carrier pin to the inverting input of the receive op amp is to provide sidetone suppression. The transmit carrier is provided through the 16 kΩ resistor 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled and presented to the Receive Carrier pin on the MT3530 at a reduced level.

Under ideal conditions 20 dB or more of cancellation might be achieved, but because telephone lines vary considerably, a cancellation of around 10 dB is a more realistic number.

For the phone line interface circuit, Figure 17b, the transformer listed is rated to 75 mA loop current. To go to the maximum loop current the Microtran part would be T5115 for 120 mA loop current capability. The DC resistance may be slightly different and various components may need to be adjusted to retain the necessary AC and DC specifications.

4.2 Parallel Interface Application

The parallel interface system is an add-on modem built into the internal parallel bus structure of the microcomputer. The ACIA (or UART) controls communications between the computer's CPU and the modem chip. It converts 8-bit parallel data bus signals from the computer into 8-bit serial inputs for the modem, and it converts the modems serial inputs into 8-bit parallel inputs for the computer's data bus. A separate 1.8432 MHz clock can provide timing for the ACIA or the 4.8 kHz LSTTL-compatible clock output (CLK) of the MT3530 can be used. This 4.8 kHz output is 16 times the chip's 300 baud data rate.

Figure 19 shows how the MT3530 is interfaced to a standard 8-bit parallel data bus by the use of Mitel's MD65SC51B. The MD65SC51B is inhibited until CS1 is asserted. Once the MD65SC51B is selected, it is programmed by the PC or computer. This places the MD65SC51B in asynchronous mode, selects the baud rate clock multiplication factor, parity, the word length setting, and the number of stop bits attached to the word. Substituting a microcontroller for the ACIA turns the MT3530 into a smart modem. Besides regulating communications between the CPU and the modem, the microcontroller frees the computer's CPU from managing many of the communications functions. The microcontroller makes possible automatic dialing and the storage and retrieval of telephone numbers.

5.0 Diagnostics

The MT3530 has two diagnostic modes for either local or remote testing. Table 6 shows the control logic during diagnostic modes. To establish diagnostic modes in either Originate or Answer, first establish handshaking in the preferred mode, then enter the diagnostic mode.

TEST MODE	STATUS LINES †						
	DTR	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RD}$
AL	H	H	L	L	L	L	L
DL	H	H	H	L	H	H	H

Table 6 - Control Logic During Diagnostic Modes
†(L = Low, H = High)

5.1 Analog Loopback

By putting the AL pin High while DTR is High, the device enters the analog loopback mode. $\overline{OH}$ goes Low to busy out the phone line. The receive filter center frequency is switched to the transmit center frequency and the TC signal is internally connected to the RC input. The transmit signal, also, remains available on the TC pin. Thus, any digital data input at TD is coded and sent out via TC, and at the same time back through the analog input, decoded, and out on the $\overline{RD}$ pin. This is essential for smart modems. The PC or microcontroller can, thus, determine if the modem is working correctly by comparing what is sent to the modem, to what the modem sent down the phone line.

5.2 Digital Loopback

By putting the DL pin High (On) the MT3530 enters the digital loopback mode. In this mode any data received from the remote end of the phone line is retransmitted back to its source and $\overline{DSR}$ is forced High (Off). The digital or decoded data is not available at the $\overline{RD}$ output in this mode.

This mode is useful in cutting maintenance costs. The manufacturer (or service company) can call up the consumer's computer and send it a data stream. The modem would then retransmit the received data to the manufacturer's field service center. If the received data is correct, then both the phone line and the modem are working correctly, localizing the problem to the computer or a cable, eliminating the modem as a problem.

6.0 Modem Performance

The MT3530, unlike most integrated modem components, is a complete analog and digital system in a single I.C. Thus, performance is necessarily measured at the system level. A widely used means of measuring modem performance is a Bit Error Rate (BER) test. Also, what needs further consideration is distortion manifested in asynchronous transmission, for this distortion affects BER.

6.1 Asynchronous Modem Distortion

The transitions in the data received by the data terminal equipment (CPU, computer, terminal) will not be exactly at the points where they occurred in the test transmission. This is because modulation, network imperfections and demodulation affect the analog carrier adversely. Additionally, transitions in both the modulation and demodulation processes are not instantaneous, producing another form of distortion in the digital

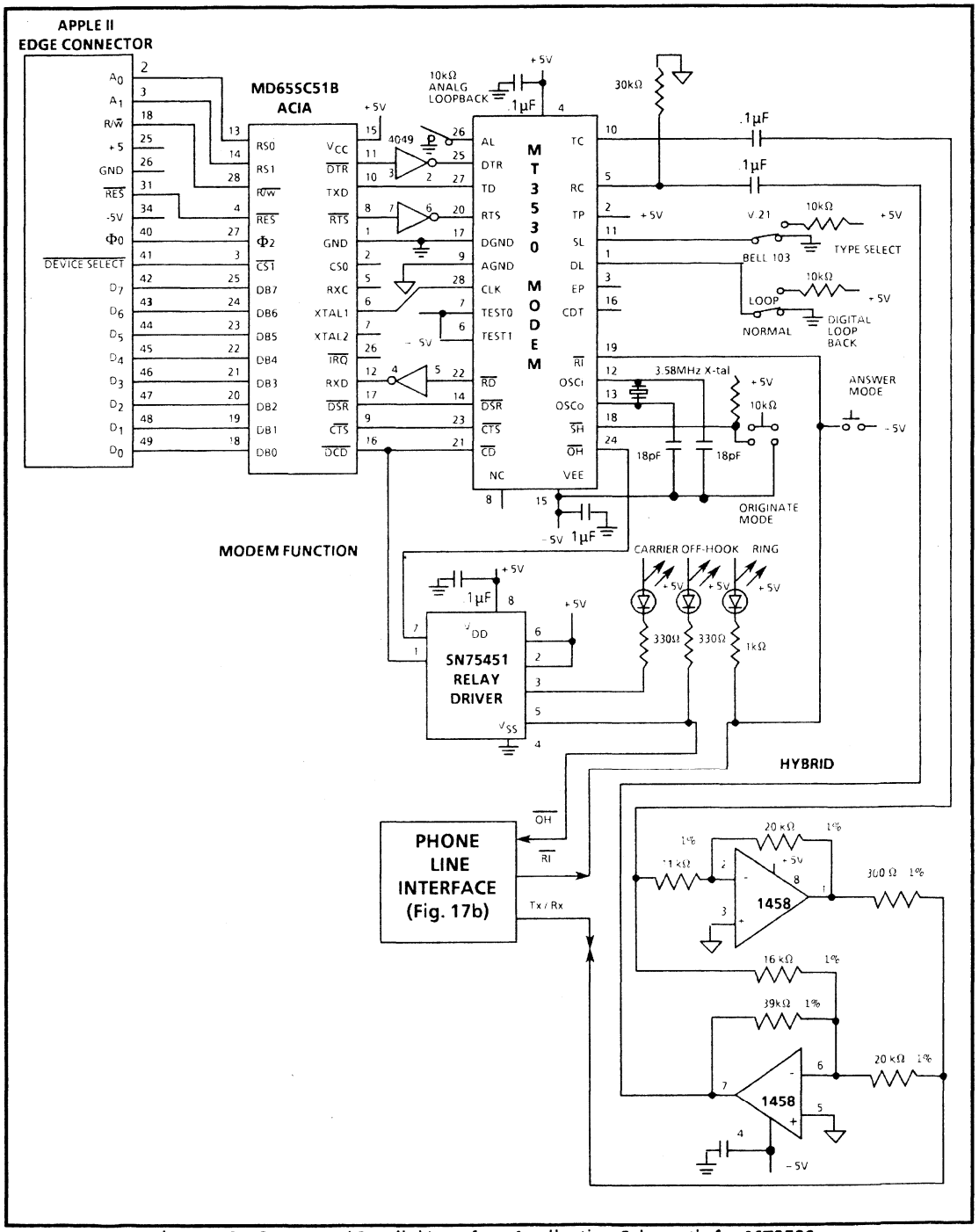


Figure 19 - Suggested Parallel Interface Application Schematic for MT3530

waveform. While this distortion is only manifested in asynchronous transmission there are various names and definitions given to this digital distortion. Two of the best known forms of digital distortion are: bias distortion and bit jitter.

6.1.1 Bias Distortion

Bias distortion is a measure of whether a Mark (1) or a Space (0) is more readily demodulated. "Positive Bias" refers to a bias towards mark. "Negative Bias" refers to space bias. By comparing the ideal sampling instant in an isochronous transmission to the actual transition instant, the difference between Mark and Space periods can be measured. See Figure 20.

Bit bias is most easily observed when an alternating Mark-Space pattern is demodulated. Ideally, the Mark and Space periods would be equal, but the difference in period is defined as bias distortion:

$$\% \text{ Bias Distortion} = \tfrac{1}{2}(T_M - T_S)\,100 / (T_M + T_S)$$

Excessive bit bias will cause an ACIA (or UART) to incorrectly deserialize data. Most ACIA (or UART) make majority judgements of data on the basis of several samples. This makes modems with bias distortion of a magnitude greater than 25% unusable. For the MT3530 typical bias distortion is 3 %.

6.1.2 Bit Jitter

The data transition edges in the demodulated (recovered) data, also, tend to move about where they should ideally be, leading to bit jitter. See Figure 21.

$$\text{Bit Jitter} = T_{MAXIMUM} - T_{MINIMUM}$$

The bit jitter is usually specified in percent, indicating what percentage of the bit frame the peak to peak jitter is.

$$\text{Peak to Peak Bit Jitter \%} = (T_{MAX} - T_{MIN}) / T_B$$

Excessive bit jitter can lead to incorrect operation of the ACIA (or UART) used to deserialize the data. For the MT3530 the bit jitter is typically 100 µs.

These distortion mechanisms characterize the quality of a modem and directly affect the bit error rate of the modem.

6.2 Bit Error Rate Analysis

The bit error rate is defined as:

$$P_e = \frac{\text{number of bits received in error}}{\text{number of bits transmitted}}$$

By sending a large number of bits through the simulated voiceband telephone channel, the bits in error can be counted at the receiving end of the data error analyzer. The test system generates a 511-bit pseudo-random bit sequence (PRBS) in order to modulate a standard transmitter. BER is usually given as a function of various impairments which the modulated data may encounter in the voiceband telephone line.

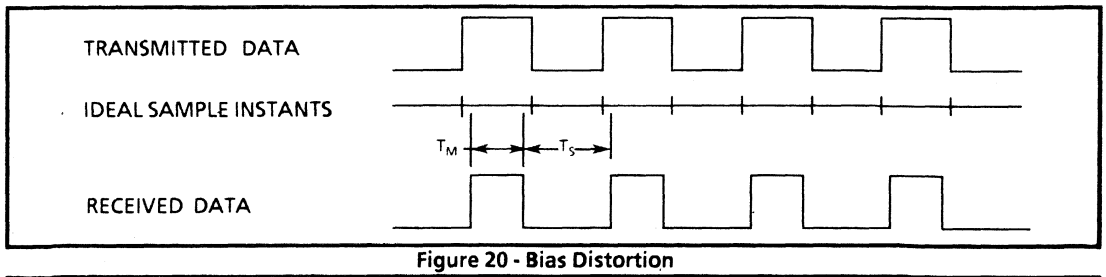


Figure 20 - Bias Distortion

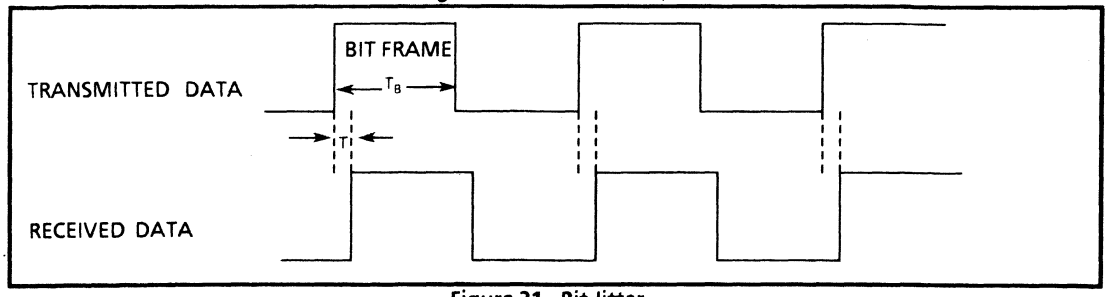


Figure 21 - Bit Jitter

Notes:

Application Note **MSAN-118**

Rate Adaptation, Switching and Transmission of RS-232 Signals

9161-001-027 NA ISSUE 1 JANUARY 1986

Contents

1. Introduction

The advent of monolithic devices capable of switching large numbers of PCM encoded voice signals has been instrumental in making the design of digital PBXs practical and cost effective. Traditionally, the role of telecommunication equipment has involved the transfer of voice signals. As a result, the cost of integrated circuit components to handle voice traffic has continued to decline dramatically.

The Mitel MT8950 Data Codec is a device which can be used to capitalize on the low cost of voice band (64 kbps) switching and transmission for data communications. It converts low speed digital signals originating from RS-232 type sources into a format which occupies a single 64 kbps channel on a serial communications stream. The Data Codec can accept digital signals at any speed from 0 to 8 kbps. It can also handle data rates of 9.6 and 19.2

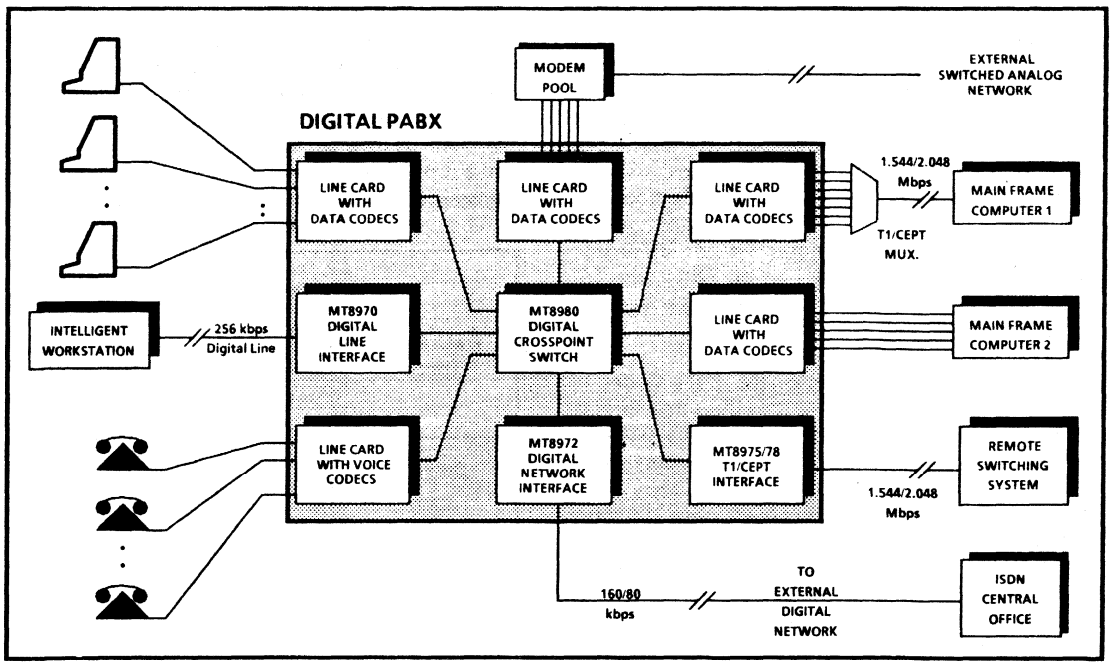


Figure 1 - Voice-Data Integrated PABX Using the Data Codec and Other ST-BUS Components

kbps. The data can be asynchronous or synchronous. The only restriction for asynchronous data at 19.2 kbps is that it must have two stop bits. The device is completely protocol independent for the other data rates. The incoming low speed data is effectively sampled at 256kHz. The sampled information is encoded on to a single 64 kbps channel. The proprietary encoding/decoding scheme used by the device, significantly reduces the bit period timing error in the regenerated data.

The Data Codec is fully compatible with Mitel's ST-BUS. The ST-BUS is a time division multiplexed serial stream with an aggregate bit rate of 2048 kbps. In a telecommunications environment, the ST-BUS is generally divided into 8 kHz frames with 32 channels per frame. The effective bandwidth of each channel is 64 kbps.

This note will highlight some of the functional features of the MT8950 using practical application circuits. Solutions to specific problems, including the handling of RS-232 control signals and call set up procedures, are also discussed. This document is designed to complement the data sheet. For a more detailed description of the device pinouts and parametric information, the reader should refer to the MT8950 data sheet.

2. General System Application Overview

A typical star configuration of an integrated Voice-Data switching system is illustrated in Figure 1. In this configuration all communication lines terminate in a central unit that contains the switching intelligence required to allow any caller to be connected to any destination. For data communication systems, the callers are usually terminals or personal computers. The destinations are usually mainframe computers, printers or modems. However, any number of different combinations are possible. In all cases, digital equipment operating at low speed is interfaced to the system through the Data Codec.

One of the main attributes of the Data Codec is that the output of the device is in the same format as that of the Voice Codec. Thus, in systems utilizing ST-BUS components, true voice-data integration is possible. The central switching matrix can handle both the encoded voice and data signals. This provides for a flexible system which can be reconfigured to accommodate changing voice and data communications requirements. The encoded information generated by the Data Codec can be transmitted over digital lines to a remote location using one of the ST-BUS transmission components shown in Figure 1.

3. Functional Overview of Data Codec Operation

The Data Codec uses a Mitel proprietary encoding/decoding scheme referred to as Transition Encoded Modulation (TEM). The low speed data is sampled at a frequency of 256 kHz. The position of the first transition, the total number of transitions and the time interval between consecutive transitions within a 125 µs time period is encoded as an eight bit word. The Data Codec at the remote end accepts this eight bit word and regenerates the original signal from it. A summary of the capabilities of the device and the maximum error in the bit period timing introduced due to the encoding/decoding of the signal is presented in Table 1.

The circuit presented in Figure 2 shows a simple RS-232 interface to the ST-BUS. This particular configuration is designed to illustrate the use of the Data Codec in a very basic application where only the rate adaptation features of the device are utilized.

The data originating from the RS-232 TXD pin is level shifted and input at D_X1. Since the data is in the NRZ format, the Data Format (DF) pin on the Codec is tied LOW. This will ensure that the codec receives and transmits data in the NRZ format. The secondary input (D_X2) is not utilized in this particular application and is therefore tied to V_{SS}. The low speed data is encoded by the encoder section to generate an eight bit word. This 8 bit encoded word is transmitted via the DSTo output to the digital switch (the MT8980). The byte can be switched by the MT8980 to any specific remote Data Codec within the PBX. It can also be transmitted using one of the ST-BUS transmission

Data Rate (bps)	Restrictions		Maximum Bit Period Timing Error*
	Sync. Data	Async. Data	
0-8000	None	None	3.9µs
9600	None	None	
19200	None	Minimum 2 stop Bits	

Table 1 - Summary of Data Codec Capabilities

** Refers to the maximum timing error in the bit period of the regenerated signal.*

interfaces to a remote location where another Data Codec is used to decode the received information.

At the same time as the encoded 8 bit word is being output by the codec, the DSTi input accepts an 8 bit word from the switch. This word is decoded by the codec to regenerate the low speed NRZ signal which is output at D_R1. After level conversion from TTL to RS-232 compatible levels, the regenerated signal is input to the DTE directly.

The Data Codec does not require any programming to indicate to it the bit rate of the data originating from the RS-232 terminal. As mentioned previously, any low speed digital signal transmitted at the specified bit rates will be encoded correctly.

The Framing Type 1 ($\overline{F1i}$) and the Control Address ($\overline{CA}$) inputs are used to enable the ST-BUS interface (DSTi, DSTo and CSTi) on the chip. The relationship between the signals is illustrated in Figure 3. When the $\overline{F1i}$ and the $\overline{CA}$ inputs are both set LOW, the Data Codec will output a serial eight bit word via the DSTo pin. During this same time, serial 8 bit words are also clocked into the device via the CSTi and DSTi inputs. Thus, by enabling the interface at a specific time in the ST-BUS frame, the codec can be assigned a unique channel timeslot during which it will output and accept encoded information.

The eight bit serial word input via the CSTi pin is used to load the internal Control Register. In very simple applications where only the rate conversion feature of the codec is utilized, the CSTi input pin can be tied to V_{SS}. This will load all zeros into the internal Control Register and cause the device to operate in its normal mode. If other modes such as loop-back, local carrier mode, idle, etc. are to be used, an 8 bit word can be loaded into the Control Register via the CSTi serial input. A summary of the various modes of operation affected by the Control Register is presented in Table 2. The internal register is loaded once every ST-BUS frame. The correct 8 bit word can be loaded into the register by using the messaging capabilities of the MT8980. The appropriate channel on the ST-BUS stream connecting the MT8980 digital switch to the CSTi input of the MT8950, is put in message mode (refer

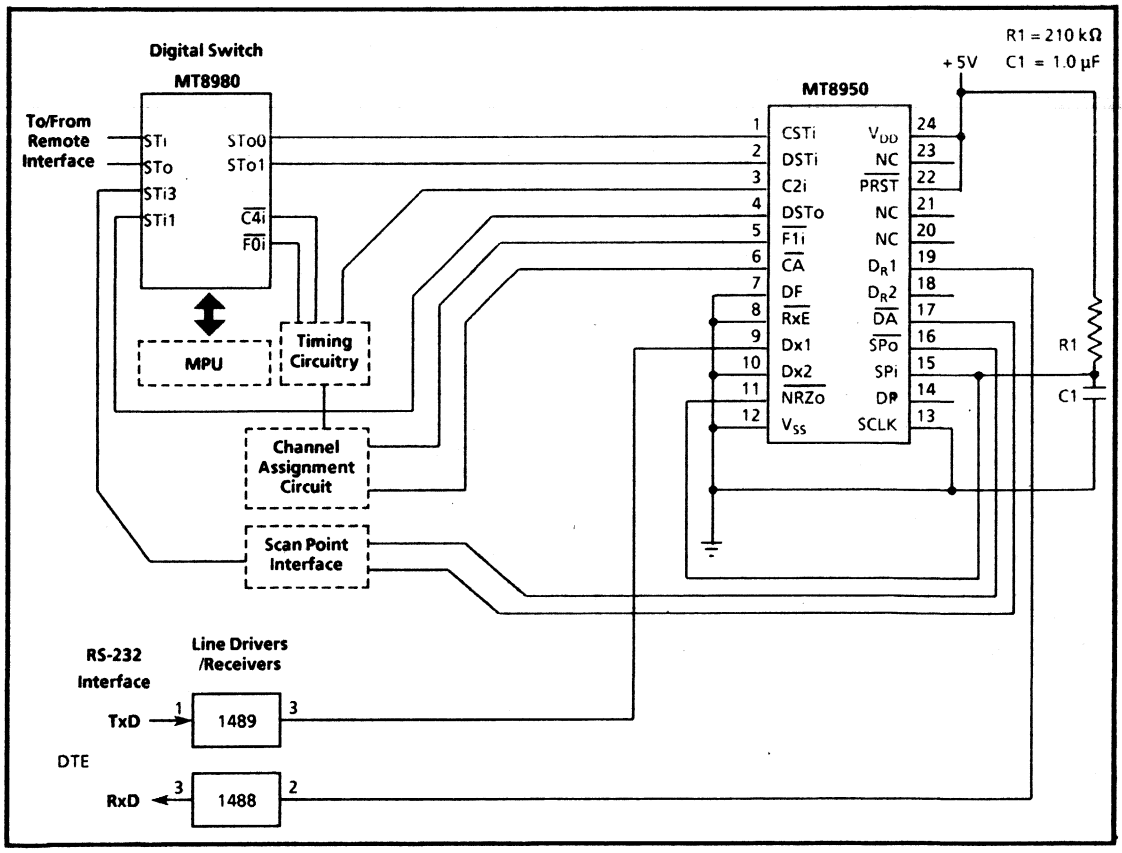


Figure 2 - Simplified RS-232 Interface Using the Data Codec.

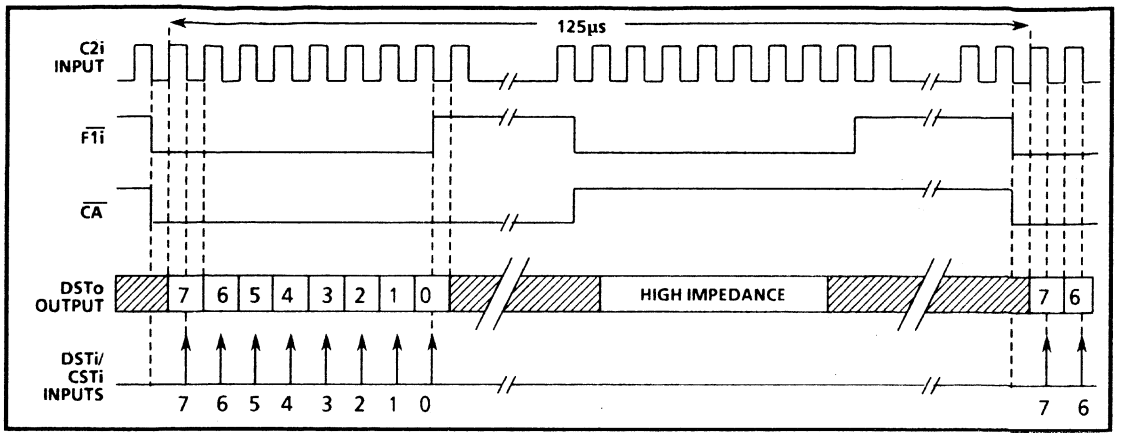


Figure 3 - Timing Diagram - 125µs Frame Period

to the MT8980 Data Sheet for more details on how this is done). In the MT8980 when a specific output channel is put in message mode, the 8 bit word placed in its connection memory is output during that channel timeslot. For example in Figure 2, output Stream 0 (STo0) from the MT8980 is shown connected to the CSTi pin of the Data Codec. If channel 1 on this stream has been assigned to the Data Codec, then channel 1 on Stream 0 of the MT8980 is put in message mode. The contents of the connection memory corresponding to this channel and stream, will be output by the MT8980 during the specific channel timeslot and subsequently accepted by the Data Codec at the CSTi pin and loaded into the internal Control Register.

Bit	Function
7,6,5	Device mode control bits. These bits select one of eight modes of operation
4,3,2	These bits control the logic level of bits 1, 4 and 5 in the violation word output in the Local Carrier mode.(See section 4.1)
1	Resets the Data Activity Scan point
0	Resets the Uncommitted Scan point

Table 2 - Summary of Control Register Function

The Received Energy ($\overline{RxE}$) pin is used for assigning a specific polarity to the D_X1 and D_X2 pins when the Data Codec is being used in the Return to Zero mode (see MT8950 data sheet for more details). In the Non-Return-to-Zero (NRZ) format, polarity detection is not required. The $\overline{RxE}$ pin can, therefore, be tied LOW. In both cases, this pin should be asserted LOW for the duration of the call.

There are two output pins on the Data Codec which can be used for monitoring the device. The Data Activity ($\overline{DA}$) pin goes from HIGH to LOW when the first MARK to SPACE transition occurs in the data. The $\overline{DA}$ output can be set HIGH by writing a '1' to bit one of the Control Register. This output pin can be monitored by the system processor to detect the beginning of data activity and used to disconnect a line which has been inactive over a predefined period of time during the initial call set up. It may also be used as a 'request for service' signal by an interface.

The second monitoring feature is the Scan Point Output ($\overline{SPo}$). The level on this output is asserted LOW when the Scan Point Input (SPi) undergoes a HIGH to LOW transition. The $\overline{SPo}$ pin can be set to its original HIGH state by loading a '1' into bit 0 of the Control Register. In conjunction with the $\overline{NRZo}$ pin, the Scan Point output can be used to detect a space signal of varying time durations. The circuitry required to implement this is shown in Figure 4. The values of R1 and C1 in Figure 2 have been chosen to permit detection of a long SPACE exceeding 150ms. In most data terminal equipment, a 150ms long SPACE is generated when the BREAK key on the keyboard is pressed. Thus pressing the BREAK key will cause the Scan Point output to go LOW. The system processor monitoring this output can interpret this as a prompt from the peripheral. The prompt may initiate a call set up process or it may direct the system processor to execute some other predefined routine, in the middle of a communication session.

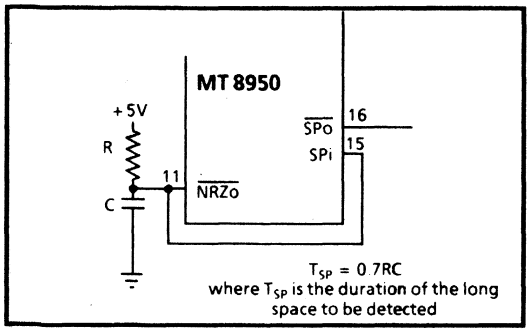


Figure 4 - Long Space Detection Circuit

The specific applications depend on the architecture of the system.

The Secondary Clock (SCLK) is an external clock input that is used for modulating the signal output on D_R2 in the Local Carrier mode. This clock signal is also used for generating the "synchronization" pulses which are output on D_R2 when the data decoded from the remote end is idling or when the device is operating in mode 2. Since none of these features are required for this particular application, the SCLK pin is tied LOW and the output at D_R2 is not monitored (see Section 4.2 for more information on the uses of this clock).

The Drive Point output (DP) is an uncommitted output pin which is asserted HIGH when the codec is operated in mode 6. It is LOW in all other modes. This output pin can be used to control external circuitry.

4. RS-232 Signalling and Control Through the ST-BUS.

The EIA RS-232 standard defines the interface between Data Terminal Equipment (DTE) and Data Communications Equipment (DCE). In the majority of asychronous applications, only a subset of the extensive list of signal elements defined in the standard is implemented. A summary of the more commonly used signal elements is presented in Table 3. The abbreviations shown in Table 3 are used throughout this document when any reference to these signals is made. Signals such as DTR, RTS, CTS, etc., which are not directly involved in transmitting and receiving data, are collectively referred to as control signals.

In a data switching system such as the one described in Section 2, the handling of the control signals depends on the specific type of connection made through the switch. In DTE-DCE type connections (i.e. a terminal connected through the switch to a modem) the two peripheral devices should effectively believe that they are connected to each other directly. Therefore, RTS turned ON by the terminal is relayed to the modem transparently. Conversely, a CTS turned ON by the modem is relayed back to the terminal. In a switched circuit, this would require transmission of the control information transparently from one interface to the other as shown graphically in Figure 5.

Pin NO.	Signal Description	EIA Ckt.	Common Abbrev.	From DCE	To DCE
1	Protective Ground	AA	GND	X	X
2	Transmitted Data	BA	TXD		X
3	Received Data	BB	RXD	X	
4	Request to Send	CA	RTS		X
5	Clear to Send	CB	CTS	X	
6	Data Set Ready	CC	DSR	X	
7	Signal Ground / Common Return	AB	SG	X	X
8	Received Line Signal Detector	CF	DCD	X	
20	Data Terminal Ready	CD	DTR		X
22	Ring Indicator	CE	RI	X	

Table 3 - RS-232 Pin Description

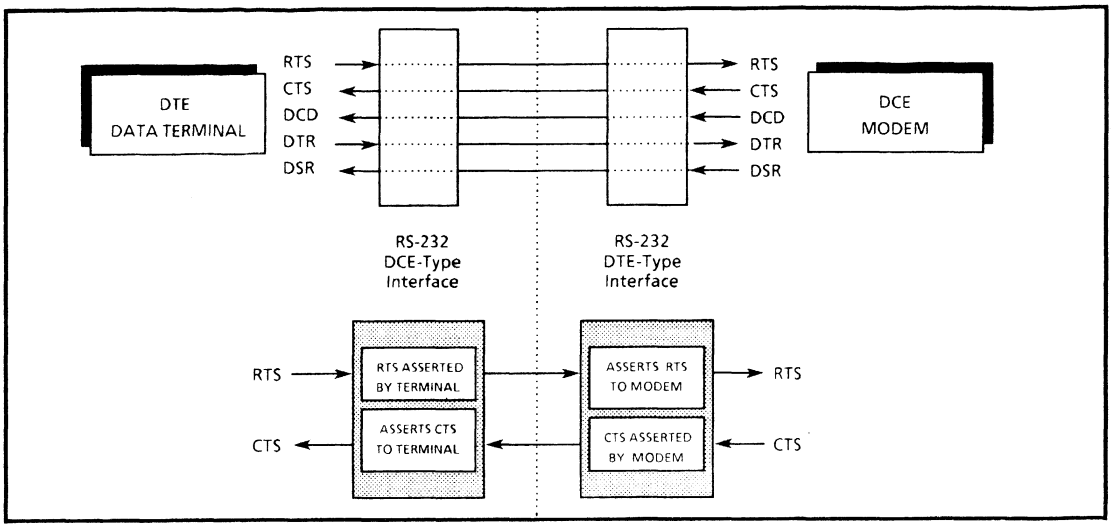


Figure 5 - RS-232 Signal Exchange in a DTE-DCE Type Connection

When the two devices connected through the data switch are both terminating type devices, e.g. a terminal connected to a computer, both the RS-232 interfaces on the PBX should appear as DCE to the respective devices. Transparent switching of the control signals from one side to the other would not necessarily serve any useful purpose. Thus some sort of system intervention would be required to interpret the signals asserted by one interface and transmit the appropriate information to the remote interface. In the example protocol illustrated in Figure 6, RTS turned ON at one interface is used to turn ON DCD at the remote end. The remote end echoes back a signal which causes the originating side to turn ON CTS. Since the actual control information exchange uses the same transmission media as the data, the CTS signal indicates that a secure communication channel is available. The

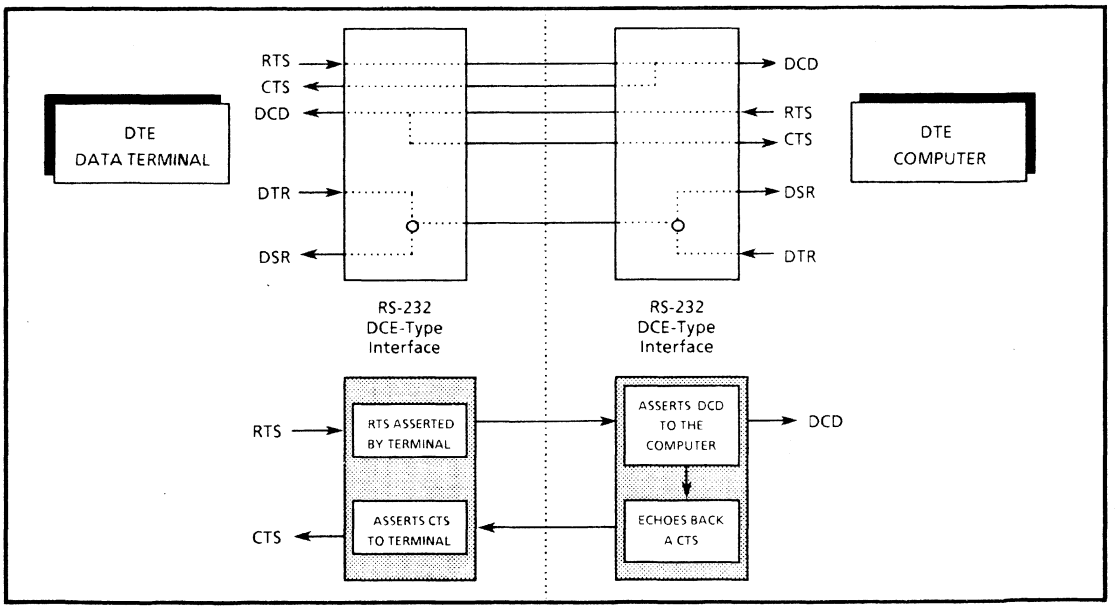


Figure 6 - RS-232 Signal Exchange in a DTE-DTE Type Connection

local interface has effectively interrogated the remote end to ensure that communication is possible before turning over the channel to the DTEs. Note that if the DTEs connected through the interface were to operate in half duplex, the signal exchange would still be valid.

In this particular example, DSR is turned ON by the interface circuit when it has been connected to the destination interface, or when the main switching controller is ready to receive call set up instructions. The Data Codec interface described above complies with all the RS-232 requirements outlined in the EIA standard specification.

From the preceding discussion it is apparent that two types of interface circuits are required to provide the flexibility of connecting various devices through the data switch. In this document, the circuit configuration which permits direct connection to a DTE is referred to as a 'DCE-type' interface. The signal flow direction for this interface is the same as that for an RS-232 interface on a DCE. Conversely, the circuit which allows direct connection to a DCE is referred to as a 'DTE-type' interface.

A variety of different circuits can be devised around the Data Codec to implement the functionality discussed above. Figure 7 illustrates, in block diagram format, three different configurations which can be implemented with a minimum of extra circuitry.

The block diagram in Figure 7(a), illustrates a technique in which the control information is transmitted and received on the same channel pair as the data. This submultiplexing of the control information with the data can be done most effectively using a single chip microcontroller. In the second configuration, shown in Figure 7(b), the control signals are transmitted and received on one ST-BUS channel pair while the encoded data is transmitted and received on another pair. Both of these configurations are discussed in more detail in subsequent sections.

The third configuration has been presented merely to show how the combination of the techniques described above could be used to submultiplex the control signals on to the data channel and yet still provide the main switching controller with a direct indication of a request for service originating from the peripheral. In this case the PBX directly monitors the level on the DTR line of the interface. The turning ON of DTR by the terminal indicates to the main controller in the PBX that the specific interface has requested service. This is analogous to a phone going off-hook. The Status Point Interface circuit depicted in the block diagram in Figure 7(c) is similiar to the circuit used for the second configuration. In this case, however, the Status Point Interface circuit is shared among a number of interfaces (up to a maximum of eight). Thus an ST-BUS channel originating from this circuit would be made up of individual bits reflecting the status of the DTR lines of eight interfaces.

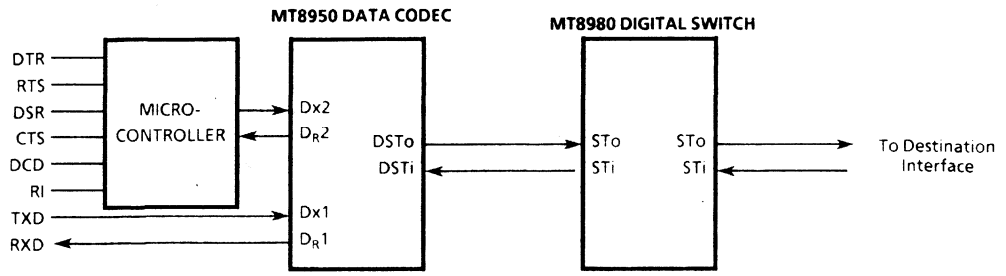
The choice of configuration depends on the architecture of the switching system and the call processing procedures to be utilized. Generally, if ST-BUS components are used to transmit the information to a remote location, the in-band signalling scheme illustrated in Figure 7(a) would utilize the bandwidth more efficiently. However, if the interface is contained within a single piece of equipment, it may be just as cost effective to use an extra channel to transmit the control information.

In all of the following discussions and illustrations, only the circuit at the local end is described. It is assumed that the remote interface has an identical circuit. The remote interface may be located within the same switching sytem or it may be in some remote location as discussed previously.

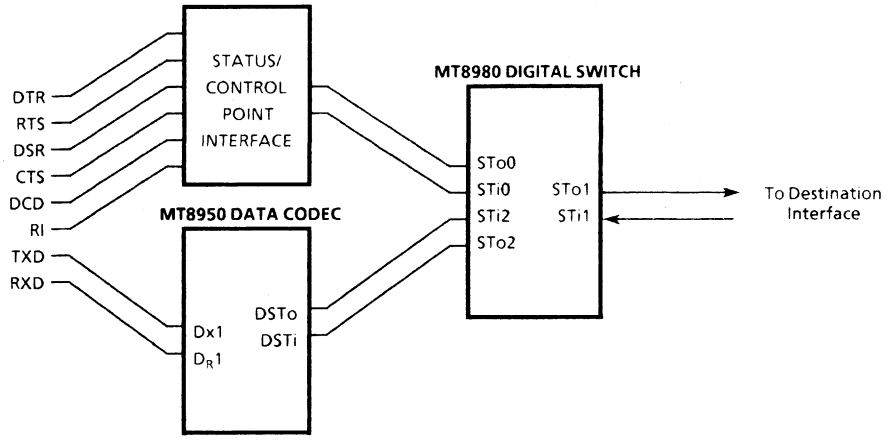
4.1 Submultiplexing RS-232 Control Signals with the Data

When the Data Codec is operating in the NRZ format, it accepts data signals at the primary input - D_X1. The secondary input pin, D_X2, can accept a digital signal which is encoded only when there is no activity on the D_X1 pin. The format of this secondary signal is slightly different from that of the primary data signal. Each pulse on the D_X2 input is encoded as a single transition. The minimum time between two consecutive pulses is limited to 125µs. The maximum data rate attainable using the D_X2 input is, therefore, 8 kbps. At the remote end, the regenerated signal appears as a square wave on output pin D_R2. Each transition on this output corresponds to a pulse input at the transmitting end. The general format of the input/output signal is illustrated in Figure 8. This secondary input/output capability can be used to transmit and receive RS-232 control signals when there is no activity on the D_X1 pin (i.e. the data signal is either steady MARK or steady SPACE).

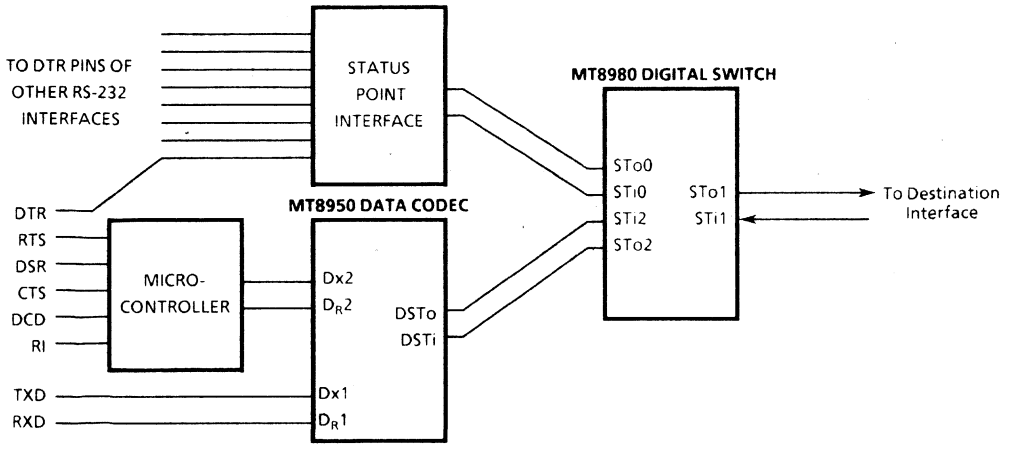
The circuit diagram illustrated in Figure 9 shows an example of how the Data Codec in conjunction with a microcontroller can be used to implement the interface shown in Figure 7(a).



(a) Submultiplexing RS-232 Control Signals with the Data onto a Single ST-BUS Channel



(b) RS-232 Control and Signalling Through a Separate ST-BUS Channel



(c) DTR is Monitored Through a Separate ST-BUS Channel - Other Control Signals Submultiplexed with Data

Figure 7- Implementation of a Complete RS-232 Interface to the ST-BUS Using the Data Codec.

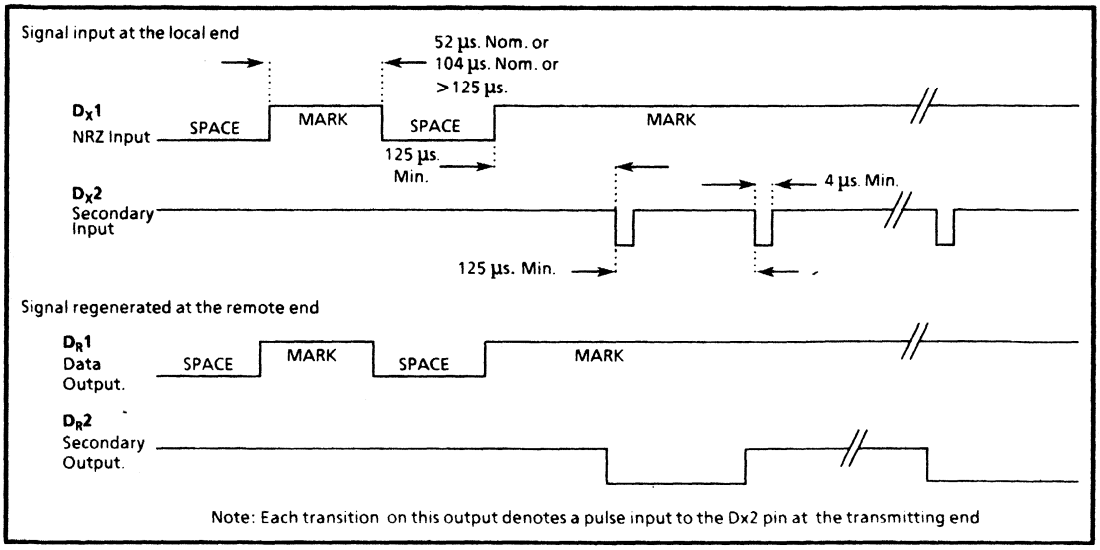


Figure 8 - Example Input/Output Waveform in the NRZ Format (DF = LOW)

The microcontroller is used to monitor the status of the RS-232 control lines. Based on the logic levels detected, it generates a seven bit word. This word along with the synchronization bit is input at the D_X2 pin of the Codec using a pulse width modulation scheme. The microcontroller also accepts the signal output by the codec at the D_R2 pin and decodes the seven bit word transmitted by the remote end. The information contained within the received word is used to update the status of the control lines. The format of the signal generated and received by the microcontroller is illustrated in Figure 10. In the signal generated by the microcontroller, the time duration between consecutive pulses reflects the logic value of the specific bit in the transmitted word. A logic '1' is

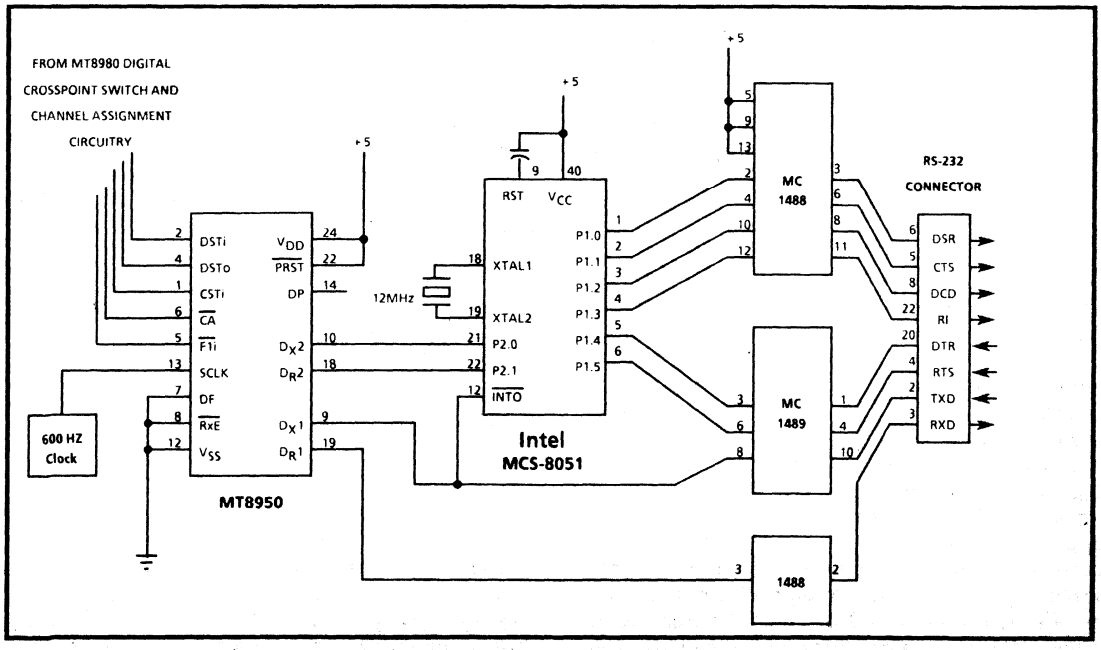


Figure 9 - Submulitplexing RS-232 Signals with Data onto a Single ST-Bus Channel.

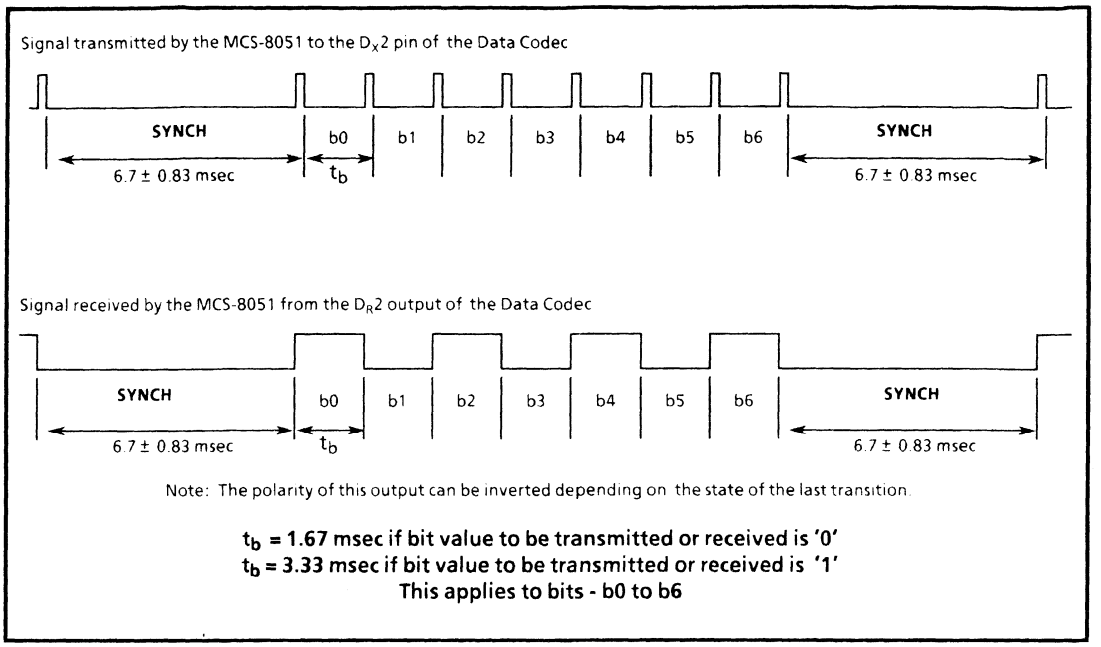


Figure 10 - Signal Received and Generated by the MCS-8051 Microcontroller

represented by a duration of 3.33ms between consecutive pulses while a logic '0' is represented by a duration of 1.67ms. The first bit in each transmitted word is referred to as the synchronization bit. It is represented by a period of 6.7ms between consecutive pulses. Transmission of the signal to the Data Codec is started after a certain minimum time (125µs) has elapsed since the last transition on the TXD data line. Transmission is ceased when any activity is detected on the data line. The microcontroller does not in any way manipulate the data originating from the TXD pin. This signal is transmitted transparently from one end to the other.

This particular circuit configuration can also be used to interpret the 8 bit word generated by the Data Codec in the Local Carrier Mode. The Data Codec can function in any one of eight modes. The required mode of operation is selected through the internal Control Register. When the device is programmed to operate in the Local Carrier mode, it generates an 8 bit word which is output at the D_R2 pin by modulating the secondary clock (SCLK) signal. In the NRZ format, the modulated signal appears as a square wave. The time interval between consecutive transitions in this signal specifies a binary value. A logic '0' is represented by one SCLK time period between the transitions. A logic '1' is represented by two SCLK periods. The first bit in this eight bit word is referred to as the Synchronization bit. It is made up of four clock periods. The logic levels of bits 0, 2, 3 and 6 are fixed as zeros. Bits 1, 4 and 5 can be set to '1' or '0' through the Control Register as illustrated in Figure 11. If a 600 Hz clock signal is used as the SCLK input, the time period between consecutive transitions will correspond to bit logic levels which can be decoded using the decoding scheme described above for the microcontroller circuit. This feature may be used in setting or resetting specific signals (such as DTR, RI, etc.) in the RS-232 interface through the ST-BUS Control Stream (CSTi) originating from the digital crosspoint switch. The central switching controller can therefore exert direct control over some of these signals. This may be used during initial call setup before the connection between two peripheral interfaces is established (see Section 5).

An example of the bit assignment that may be used for the transmitted control word is presented in Table 4. In the seven bit word generated and transmitted by a DCE type interface, bits 0, 2 and 4 are not used. Bit 6 is always set HIGH. This indicates to the remote receiving end that the transmitting interface is a DCE type interface. Bits 1 and 3 reflect the status of the control lines DTR and RTS respectively. Thus bit 1 will be reset to '0' if DTR is turned ON by the terminal connected to the

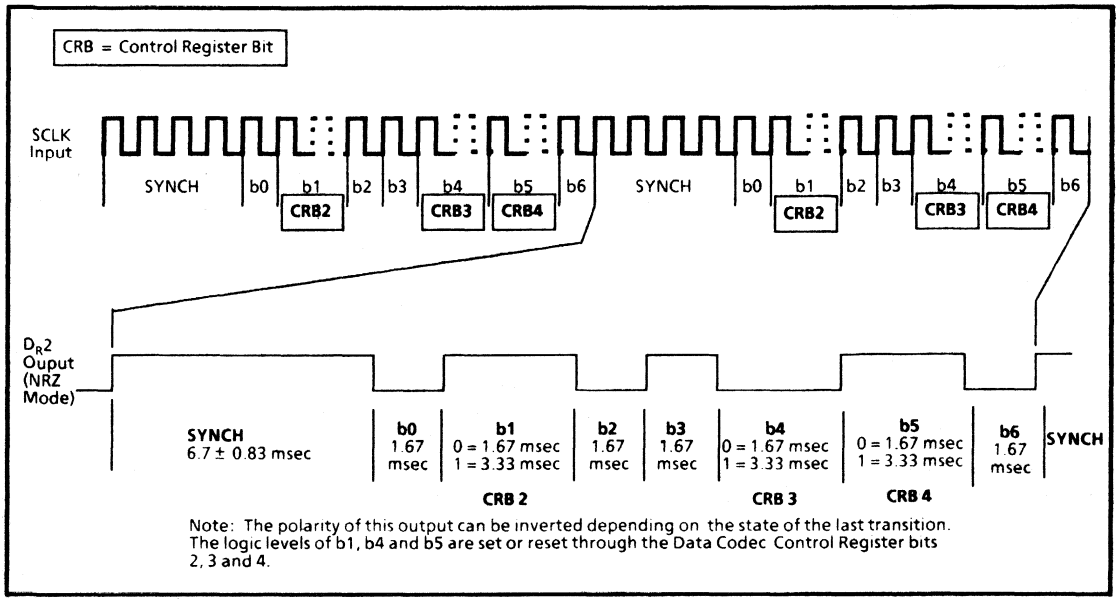


Figure 11 - Signal Output by Data Codec at D_R2 in the Local Carrier Mode for a 600Hz Input to SCLK

interface. The RTS signal has a similar effect on bit 3. Bit five in the transmitted word is set or reset in response to a RTS from the remote end. It is reset to '0' if an asserted RTS (bit 3) is decoded from the received word. Note that in all cases negative true logic is used in setting or resetting the specific bit in the control word.

For an interface configured as a DTE, the transmitted control word bits 1, 2, 4 and 5 reflect the value of input control lines DSR, DCD, RI and CTS on the interface. Bits 0 and 3 are not used. To indicate to the remote end that the transmitting interface is of a DTE type, bit 6 is reset to '0'.

The control word received by a DCE-type interface can be decoded in one of two ways. If bit 6 in the received word is '0', then it is assumed to have been transmitted by a DTE type interface. If it is '1', then the remote interface is assumed to be a DCE

Transmitted Control Word			
Bit	**Generated By DCE -TYPE Interface**	**Generated By DTE-TYPE Interface**	**Generated By MT8950 in Local Carrier Mode**
0	X	X	0
1	DATA TERMINAL READY	DATA SET READY	DATA SET READY
2	X	DATA CARRIER DETECT	0
3	REQUEST TO SEND	X	0
4	X	RING INDICATOR	RING INDICATOR
5	ECHO CLEAR TO SEND	CLEAR TO SEND	CLEAR TO SEND
6	1	0	0

Table 4 - Control Word Bit Assignment

type. In the former case the four bits in the received word corresponding to DSR, DCD, RI and CTS will be used to control the respective local output signals. For example, if the received word bit corresponding to DSR is '0' (indicating that the DSR has been turned ON by the modem at the remote interface) then the receiving end will turn ON DSR to the terminal. The other bits are handled in a similar manner.

In the latter case where bit 6 in the received word is '1', it will be decoded as follows. If the local DTR line is turned ON, the microcontroller will turn ON DSR to the DTE. A logic '0' in bit 3 indicates that the remote end has asserted its RTS. In response to this, the microcontroller resets bit 5 to '0' in the outgoing control word and also asserts DCD to the terminal equipment. A logic '0' in bit 5 in the received word causes the microcontroller to turn ON CTS to the terminal.

The control word received by a DTE-type interface can orginate only from a DCE-type interface. Bit 6 in this word will, therefore, always be '1'. The two bits corresponding to DTR and RTS will be used to control the respective local output signals.

It should be noted that, the signal carrying the control information is transmitted only when there is no activity on the D_X1 input. Thus, there can be a delay between when a change of state occurs in one of the control lines and when that information is made available to the remote end.

As indicated earlier, this particular circuit configuration can also be used to interpret the seven bit word transmitted by the Data Codec in the Local Carrier mode. Depending on the manner in which the received Control Word is decoded by the microcontroller, it is possible to set or reset the level on any of the RS-232 control lines. If, for example, the Data Codec is part of a DCE-type interface, it would be possible to control the DSR, CTS and RI lines by setting or resetting the appropriate bit in the Data Codec Control Register. As mentioned earlier, this register can be written to by the MT8980 via the ST-BUS interface. Note that bit 6 in the Control Word generated by the Codec is fixed as '0'. Thus the microcontroller will decode this word as if it had originated from a DTE type interface. The bit assignment shown in Table 4 could be then used.

The Local Carrier mode could be used during call setup to assert the appropriate control signals for the initial interactive communication between the switching system and the terminal device. For example, if it is necessary to turn ON RI at a called DCE - Type interface, the Data Codec in the interface circuit is put in the Local Carrier mode. Resetting bit 3 in the Data Codec Control Register to '0' will result in a '0' being transmitted to the microcontroller in bit 4 of the control word. The microcontroller will decode this as a signal to assert RI to the interface. Bit 2 in the control word is fixed as '0'. As mentioned earlier, a logic '0' in this bit position will be decoded by the microcontroller as a signal to assert DCD.

4.1.1 Hardware Description

The microcontroller used in the circuit shown in Figure 9 is an Intel MCS-8051. It has two on board timer/counters and three latched input/output ports. The instruction set provides for direct bit addressing and manipulation. Since the Data Codec operates in full duplex, the microcontroller has to generate the output signal and also receive the incoming signal. Thus the microcontroller resources have to be continually shared by the different routines used. It is therefore essential to minimize the processing time required for any one subroutine. The boolean processing capabilities of the Intel MCS-8051 greatly aid in this task.

The configuration of the RS-232 control lines depends on whether the interface is to appear as a DCE or DTE to the external world. The circuit shown in Figure 9 is configured as a DCE-type interface. Pins 0 to 3 on the MCS-8051 port 1 are used as outputs. These pins set or reset the levels on the DSR, CTS, DCD and RI lines of the RS-232 connector. Pins 4 and 5 are used as inputs to monitor the status of the DTR and RTS lines. The TXD line is connected to the external interrupt pin. A transition on this line will generate an interrupt. The MC-1489 converts RS-232 levels to TTL compatible levels. The MC-1488 provides the inverse function. Serial communication between the Data Codec and the MCS-8051 is via port 2 pins 0 and 1.

4.1.2 Software Description

The software flowcharts of programs that can be used in this application have been presented in Appendix-1. A more descriptive pseudocode has been included in Appendix-2. Note that the protocol presented has not been fully tested. It has been described here merely as a possible example.

The main routine in the program initializes the microcontroller and configures the input and output pins. The routine reads the status of the input control lines and stores the information in a bit addressable register as the 'Transmit Control

Word'. The bits in this control word are assigned different functions depending on whether the interface is a DCE-type or a DTE-type as discussed earlier. One of the two timers is dedicated for timing incoming signals from the Data Codec. The second timer/counter is initially used in conjunction with the external interrupt pin ($\overline{INT0}$) to detect inactivity on the TXD line for a predefined period of time. Upon detecting this inactivity, the program calls a subroutine (OUT_WORD) to generate the outgoing pulse stream. The logic levels of the various bits in the pulse stream are dictated by the contents of the Control Word stored in the bit addressable register. The second timer is reconfigured to time the interval between outgoing consecutive pulses. The timer is loaded with different values depending on the logic level of the specific bit to be transmitted. For example, if the value of the bit is '1', the timer is programmed to expire in 3.33ms. A logic '0' is represented by a time duration of 1.67ms. Every seven bit word is preceded by a SYNC bit which is characterized by 6.7ms between consecutive pulses. The timer is checked every time the routine is executed. Upon expiry of the timer, a 6µs pulse is generated on the output pin. Pulse generation is ceased when activity on the TXD line is detected.

The subroutine IN_WORD is called by the main routine continually, irrespective of whether an outgoing word has to be transmitted or not. This routine measures the time interval between consecutive transitions in the signal received from the Data Codec's D_R2 output. It first looks for the synchronization bit (i.e. a time interval of 6.7ms). Upon detecting this bit, the subsequent transitions are timed to obtain the seven bit received word. Small errors in timing values may be introduced due to the fact that other routines have to be executed before the timer is checked. The magnitude of the error depends on the worst case execution time of the other routines. This has to be taken into account before time decision levels for the bit values are defined. In the algorithm described, a time interval greater than 5.9ms and less than 10ms is assumed to be the SYNC signal. Similarily a time interval greater than 2.9ms but less than 5.9ms is decoded as a logic '1'. A logic '0' is decoded if the time interval between consecutive pulses is less than 2.9ms. All of these decision points reflect worst case execution times not exceeding 400µs. Thus the appropriate timers in each of the routines are accessed at least once in each 400µs time interval.

Two consecutive identical words have to be received for the microcontroller to begin decoding. The DEC_WORD subroutine is called to decode the received word and update the status of the local control lines. The decoding is done in accordance with the different requirements for DTE and DCE type interfaces, as discussed earlier.

4.2 Using a Separate ST-BUS Channel for RS-232 Control Information

If bandwidth considerations are not too important, a separate distinct channel may be used to convey the control information from one interface to the other. The 'control' channel will then have to be switched along with the 'Data' channel. An example of a circuit which may be used to generate and receive the control signals in the ST-BUS channel format is illustrated in Figure 12. This is the circuit implementation of the Scan and Control Point interface depicted in Figure 7(b). The parallel signals from the RS-232 connector are first serialized using an eight bit parallel in - serial out shift register. This register is clocked with the 2.048 MHz system clock used for the Data Codec and other ST-BUS peripheral devices. The output of the shift register is passed through a tristate gate which is enabled during a specific channel timeslot (in the same way as the ST-BUS interface on the Data Codec is enabled). It is tristated during the remainder of the frame. Thus the serialized control information is contained within one channel timeslot. This channel can be switched using the MT8980 to any remote interface. At the remote interface the serialized eight bit word is converted into parallel format using a serial in - parallel out shift register. The status of the eight lines is latched into an eight bit latch once in each ST-BUS frame when the specified channel has been received. The outputs of the latch are connected, after level conversion, to the appropriate RS-232 lines. Note that in the circuit illustrated in Figure 12, only four of the eight outputs of the latch (74HCT574) and only two of the eight inputs of the parallel to serial converter have been used. The remaining input/ouput lines can be used in a similar manner if more control signals are to be transmittted or received (up to a maximum of eight in each direction).

The circuit, as described, can be used for transparently switching the control information from one interface to the other. If system intervention is required, the status of the control signals can be monitored by the microprocessor connected to the MT8980 digital switch which is responsible for switching the specific control channel. In order to do this, the microprocessor reads the MT8980's data memory and interprets the eight bits contained within. The required signal status can be transmitted to the remote interface

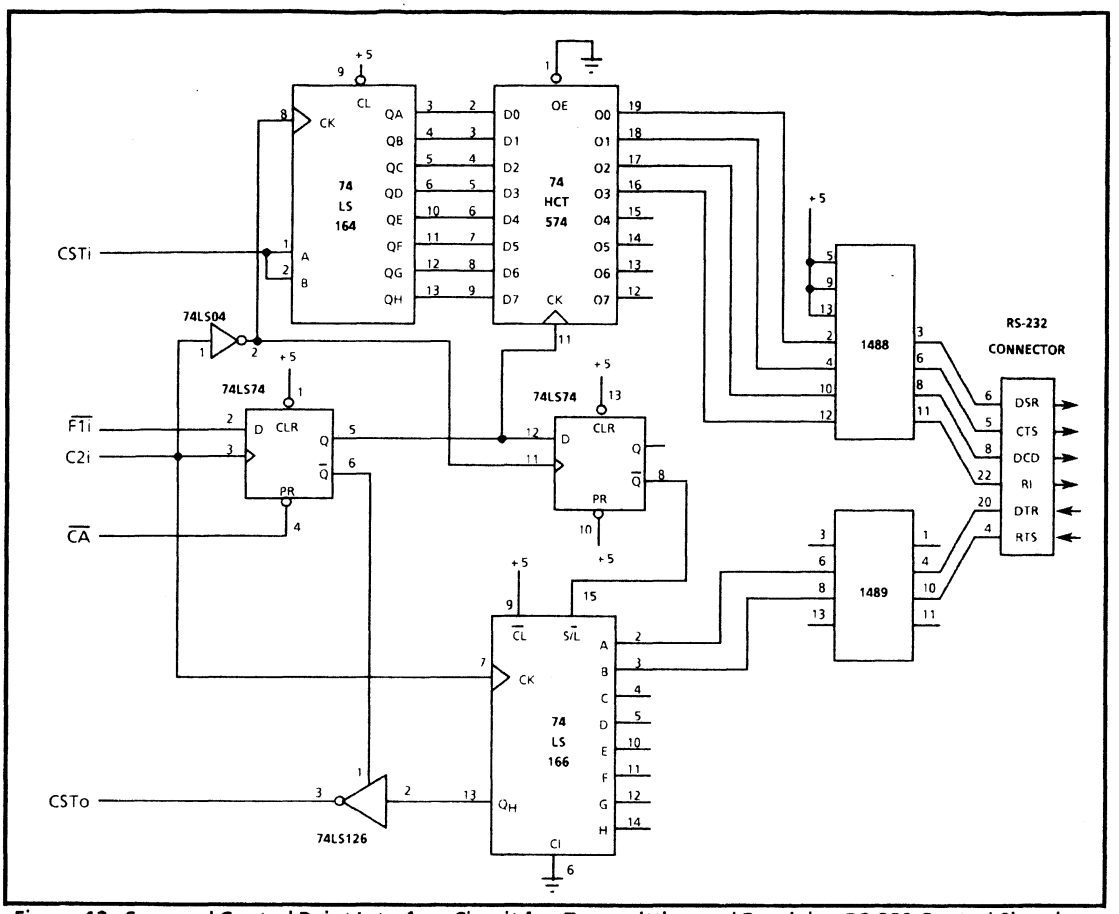


Figure 12 - Scan and Control Point Interface Circuit for Transmitting and Receiving RS-232 Control Signals. The RS-232 Connector Appears as a DCE to the External Equipment.

using the messaging mode of the MT8980. The central processor interfaced to the MT8980 could set or reset any particular control line by setting or resetting the appropriate bit in the Connection memory. The contents of the Connection memory would be transmitted to the interface circuit via the ST-BUS as explained earlier.

5. Data Call Set up Techniques

The basic steps involved in setting up a connection between any two peripheral devices through the PBX include the following:

-Detect a request for service and acknowledge
-Receive call destination instructions
-Make the connection
-Break the connection when the service is no longer required

In setting up a normal telephone connection, the PBX senses a request for service by detecting an Off-Hook condition and acknowledges the request with a dial tone. The caller provides the destination address by dialling the appropriate number. In order to interpet the incoming dial pulses or the DTMF tones generated by the telephone set, the controller assigns a special card to the interface originating the call. Once all the digits have been received this card communicates the information to the controller which makes the connection. The connection may be broken once an On-Hook condition is detected.

Essentially the same steps outlined above have to be followed when a connection involving two digital devices has to be made. The signalling methods used, however, can vary depending on the overall archictecture of the switching system. Two different approaches are discussed below. The

first approach describes an in-band signalling technique while the second outlines an example of an out-of-band signalling protocol.

5.1 In-Band Signalling

If both the signalling information and the actual data is transmitted over the same path, then the signalization is referred to as being in-band.

In order to detect when a peripheral device connected to an interface wants service, the PBX has to monitor the interface for specific signals. The PBX controller may, for example, be programmed to interpret an asserted DTR as a request for service. It is also possible to use circuitry at the interface which detects energy on the data line. The presence of energy on the line would indicate that the peripheral wants service. The PBX then has to provide some kind of acknowledgement signal to the peripheral and receive call destination instructions. In order to do this, the switch controller may connect a special card, the Data Call Setup (DCS) card, to the calling peripheral interface. A microprocessor on this card communicates with the peripheral device and obtains instructions for making the connection. The complexity of the DCS card effectively determines the capabilities of the overall system.

Some functional features that would be required in a typical DCS card are illustrated in the block diagram in Figure 13. A Data Codec is used on this card to convert the encoded information transmitted by the codec, on the peripheral card, into a format which the microprocessor can accept. The microprocessor on the card in conjunction with a timer determines the baud rate of the incoming signal. It then sets its own UART baud rate to match that of the terminal so that interactive communication is possible. The MT8980 on the DCS card is used for interprocessor communication. This allows the microprocessor on the DCS card to communicate with the main switching matrix control processor (which makes or breaks the connection) through the ST-BUS. The MT8980 could be shared by a number of other Data Codecs on the card.

In a typical session, the terminal equipment asserts DTR. This is detected by the main processor which assigns a DCS card to the calling data interface. The Data Codec at the calling interface is put in its Local Carrier Mode to turn ON the appropriate RS-232 Control Signals. It is necessary to turn ON DSR, CTS and DCD at the interface to initiate interactive communication. The DCS card waits for a predefined sequence to be transmitted by the DTE to determine the baud rate of the calling party. This predefined protocol may, for example, require that the user press the RETURN key a number of times until the terminal receives a valid prompt from the PBX. The caller is prompted to provide the destination address which could be letters or numbers specifying a certain system or port. This information is made available to the system main processor which then sets up the connection. If it is necessary to turn ON the RI at the called interface, the Data Codec in that circuit is put in the Local Carrier mode and the appropriate bit in its Control Register is reset to '0'. When the peripheral device responds by turning ON its DTR, the two devices are

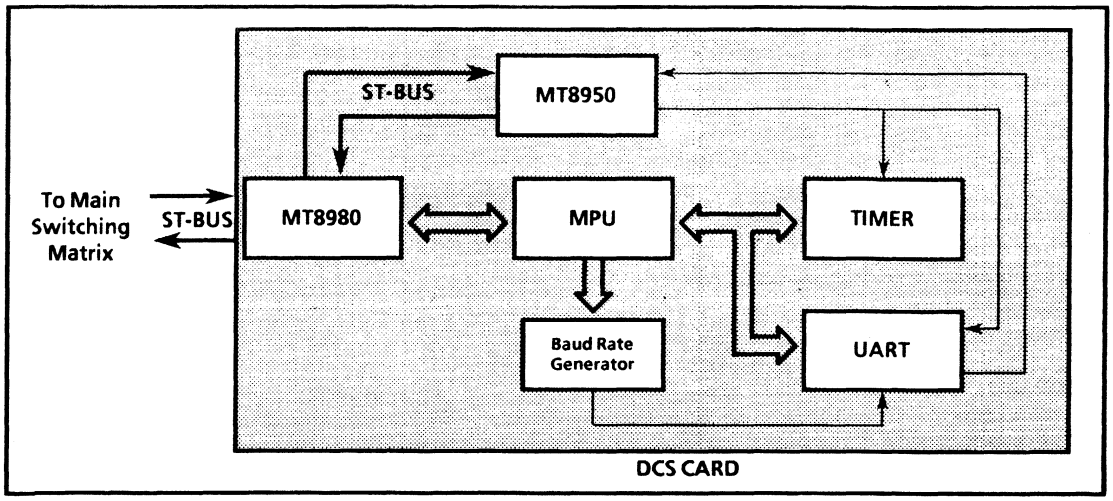


Figure 13 - Data Call Setup Card Block Diagram

connected. If the port is not available the main switching controller gives the appropriate message to the DCS card indicating that the port is busy. The DCS card in turn passes the message onto the calling terminal.

Note that although it is necessary for the DCS card in the PBX to determine the baud rate of the digital signal for the initial interactive communication, the Data Codec on the line card does not have to be programmed to accept any specific data rate. Thus the line cards can be made relatively dumb and inexpensive. The intelligence and the complexity of the more expensive DCS board is shared among a number of peripheral units and therefore it does not have to be duplicated for every line.

5.2 Out of Band Signalling

The signalling information is said to be out-of-band, if it is passed over a separate and distinct channel or path from the data.

In many modem products currently on the market, turning RTS line ON and OFF by the terminal results in the telephone line circuit to which the device is connected, being pulsed in a manner similar to that used by rotary dial phones. The same principle can be used for call set up with the Data Codec RS-232 interface. In this case the calling equipment has to have software capable of pulsing the RTS line and conveying the information to the PBX using a pulse coding scheme. A typical session would be as follows. The main processor in the PBX detects an Off-Hook condition (DTR asserted) and assigns a pulse decoder card to the particular interface. DSR is turned ON by the interface at this time. This indicates to the DTE that the PBX is ready to receive the dialed pulses. The DTE then pulses the RTS line to indicate to the decoder card the destination address. If the connection can be made, the main processor asserts RI to the called destination. When the remote side answers, the two interfaces are connected to each other. The main processor then asserts CTS and DCD to both sides. This scheme can be more easily implemented in systems where the main switching processor has direct access to the input and output control signals as would be the case if the circuit described in Section 4.2 were to be used.

The principle advantage of using this scheme is that the decoding of the dialed pulses from the caller and the subsequent identification of the destination line, requires circuitry which is similiar to the type used for a normal voice telephone call setup. No baud rate detection is required. Thus any data rate acceptable to the Data Codec can be used. The disadvantage is that the terminal equipment has to have the appropriate software to provide the pulsing for the dialed digits. This imposes a severe restriction on the types of terminal equipment that can be used. If the complexity is to be contained within a stand alone unit such as a Data Set, then the cost of this unit would correspondingly be high.

Appendix - 1 Software Flowcharts

Software Flow Charts of Programs For Submultiplexing RS-232 Control Signals with the Data

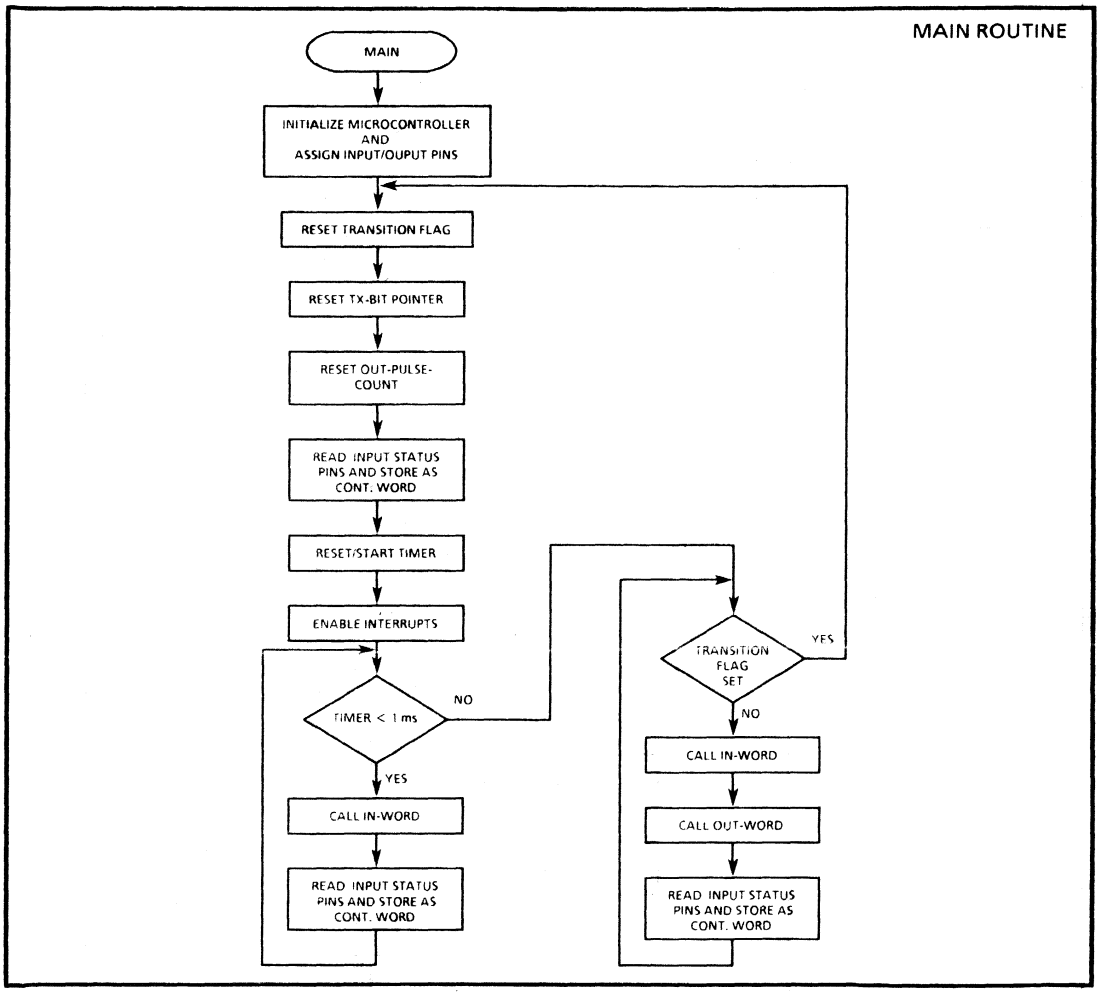


Figure 14 - Flow Chart of MAIN Routine

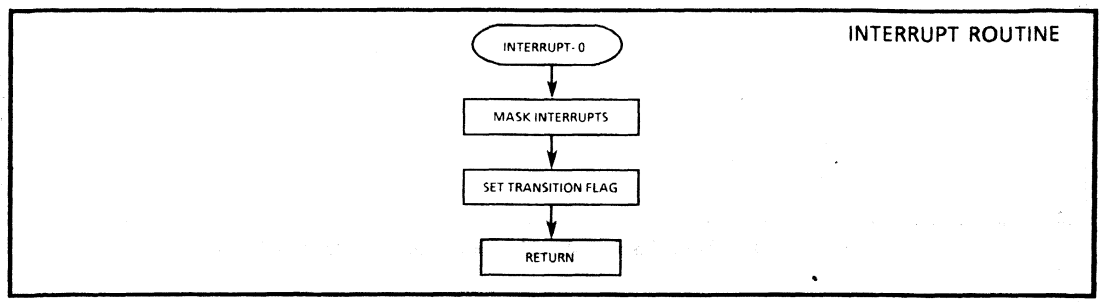


Figure 15 - Flow Chart of INTERRUPT Routine

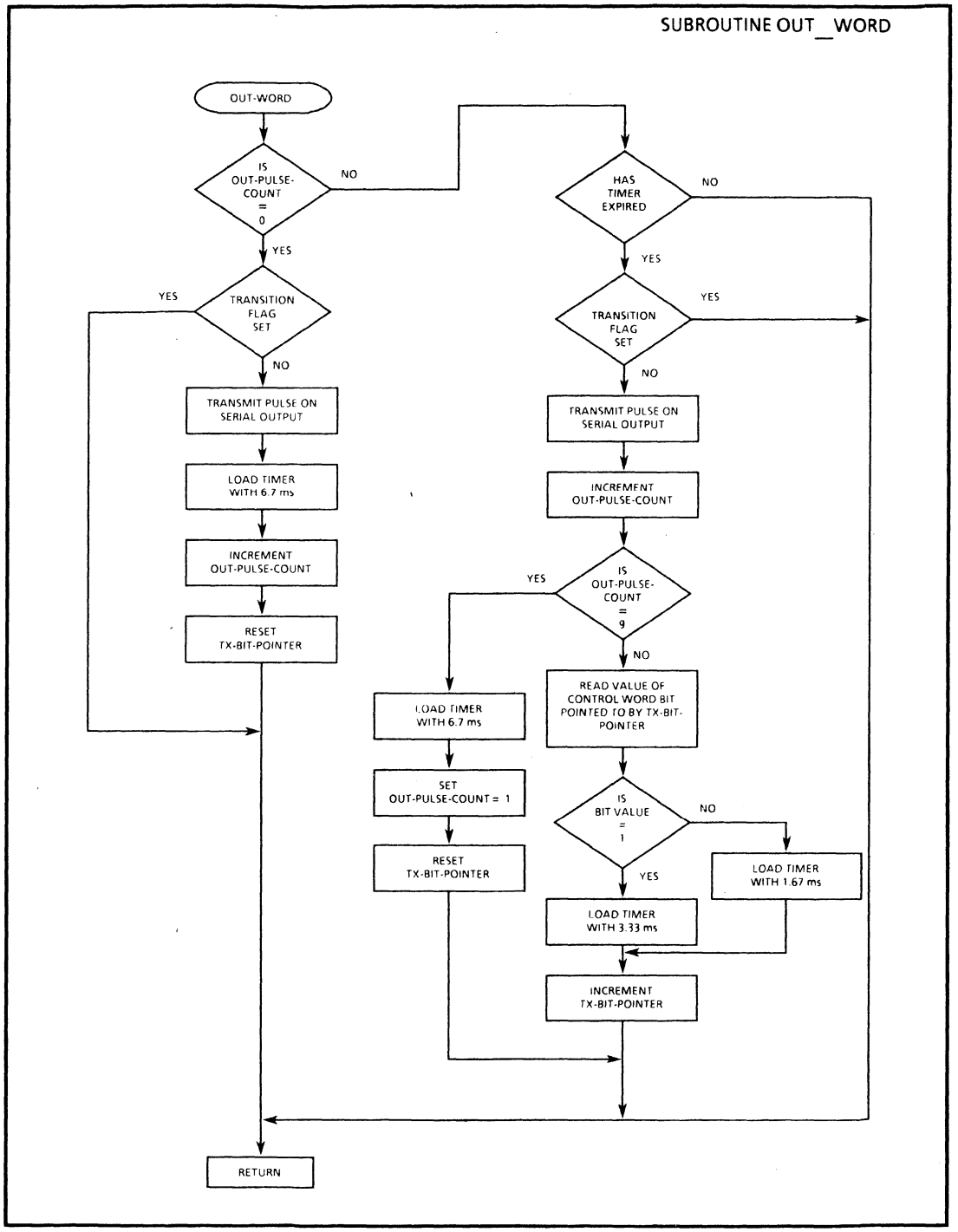


Figure 16 - Flow Chart of Subroutine to Generate Serial Output Word

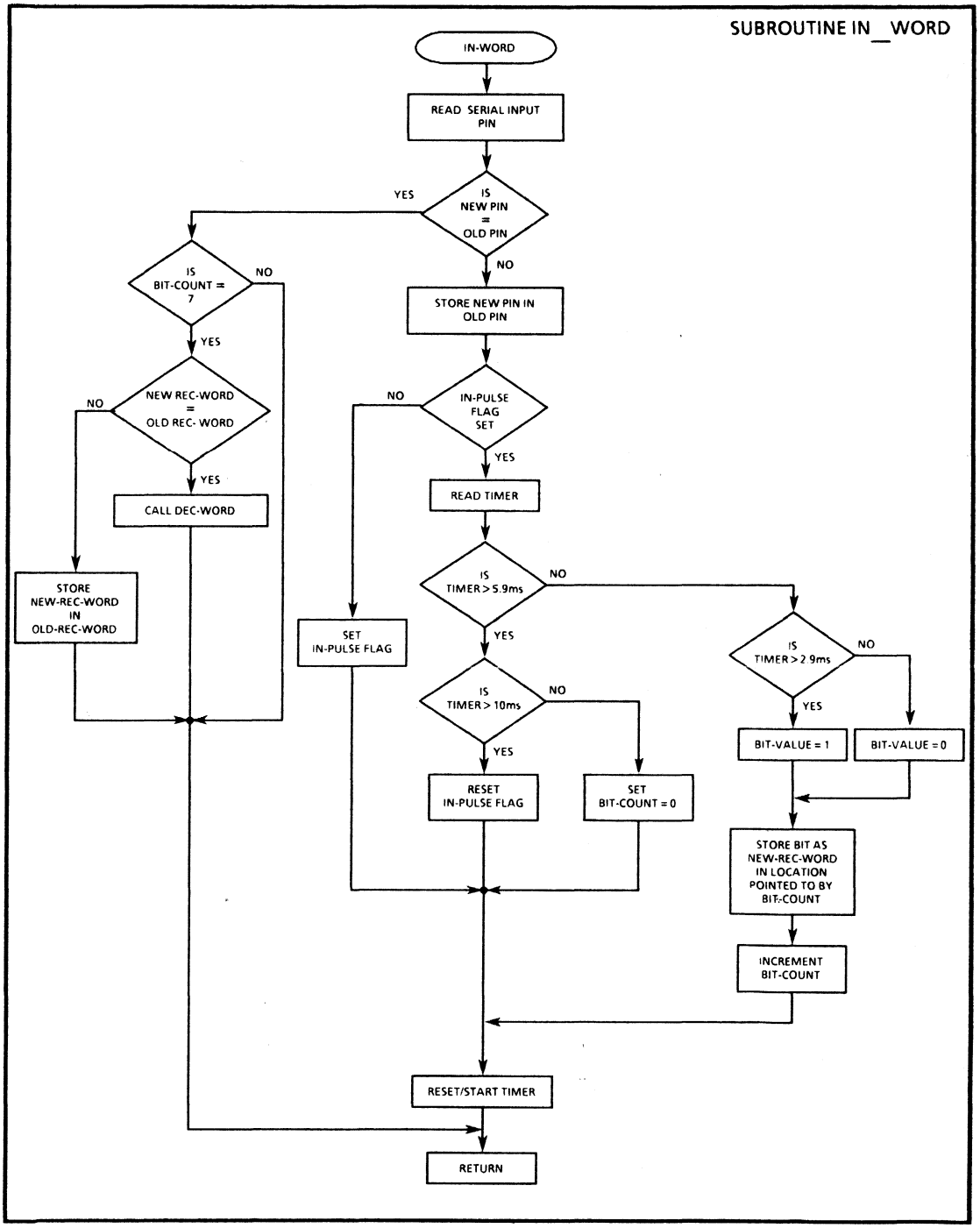


Figure 17 - Flow Chart of Subroutine to Read Incoming Serial Data

SUBROUTINE DEC_WORD

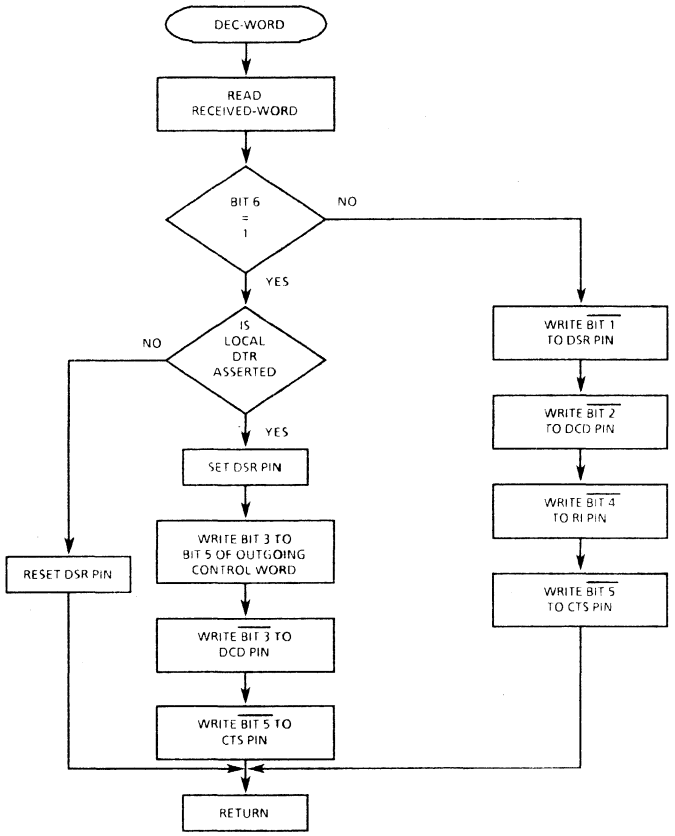


Figure 18 - Flow chart of Subroutine to Decode Received Control Word.

Appendix - 2 Software Documentation

The Software documentation described below has not been tested. It is presented here as an example of the type of protocol that is required to implement the functionality discussed in the application note.

SOFTWARE DOCUMENTATION FOR SUBMULTIPLEXING RS-232 CONTROL SIGNALS WITH DATA ONTO A SINGLE ST-BUS CHANNEL - USING AN MCS-8051 MICROCONTROLLER

MAIN PROGRAM FOR DCE-TYPE INTERFACE

```
MAIN
CONFIGURE INPUT/OUTPUT PINS      /* INPUTS: 1.4, 1.5, 2.1. OUTPUTS: 1.0, 1.1, 1.2, 1.3, 2.0 */
RESET POINTERS AND FLAGS
EXTERNAL INTERRUPTS-EDGE TRIGERRED
INITIALIZE TIMER MODES - BOTH TIMERS RUN IN MODE - 1

DO WHILE (FOREVER)

    RESET TRANSITION FLAG        /* WHEN SET, INDICATES THAT TRANSITIONS HAVE BEEN DETECTED ON THE TXD LINE */
    RESET TX__BIT__POINTER       /* POINTER INDICATING NUMBER OF BITS IN THE CONTROL WORD THAT HAVE BEEN
                                 TRANSMITTED */
    RESET OUT__PULSE__COUNT      /* REPRESENTS THE NUMBER OF OUTPUT PULSES THAT HAVE BEEN GENERATED ON THE SERIAL
                                 OUTPUT PIN */
    READ INPUT STATUS PIN AND STORE AS CONTROL WORD      /* P1.4 AND P1.5 */
    LOAD TIMER-0 TO EXPIRE IN 1 ms -- START TIMER
    ENABLE EXTERNAL INTERRUPTS

    DO WHILE (TIMER-0 < 1 ms)
        CALL IN__WORD
        READ INPUT STATUS PINS AND STORE AS CONTROL WORD
    ENDWHILE

    DO WHILE (TRANSITION FLAG NOT SET)
        CALL IN__WORD
        CALL OUT__WORD
        READ INPUT STATUS PINS AND STORE AS CONTROL WORD
    ENDWHILE

END WHILE.
```

INTERRUPT VECTOR /* THIS ROUTINE IS EXECUTED WHEN AN INTERRUPT IS RECEIVED BY THE MICROCONTROLLER */

```
INTERRUPT - 0            /* INTERRUPT GENERATED BY INTO PIN */
MASK EXTERNAL INTERRUPT
SET TRANSITION FLAG
RETURN FROM INTERRUPT
```

```
SUBROUTINE OUT_WORD     /* THIS ROUTINE GENERATES THE SERIAL SIGNAL WHICH IS OUTPUT AT PIN 2.0 OF THE
                           MICROCONTROLLER */

OUT_WORD
IF (OUT_PULSE_COUNT = 0) THEN
DO:
    IF (TRANSITION FLAG NOT SET) THEN
    DO:
        TRANSMIT 6 MICROSECOND PULSE ON SERIAL OUTPUT
        LOAD TIMER WITH 6.7 ms
        INCREMENT OUT_PULSE_COUNT
        RESET TX_BIT_POINTER
    ENDIF
ELSE
    IF (TIMER-0 HAS EXPIRED) THEN
    DO:
        IF (TRANSITION FLAG NOT SET) THEN
        DO:
            TRANSMIT 6 MICROSECOND PULSE ON SERIAL OUTPUT
            INCREMENT OUT_PULSE_COUNT
            IF (OUTPUT_PULSE_COUNT = 9) THEN
            DO:
                LOAD TIMER WITH 6.7 ms
                SET OUT_PULSE_COUNT = 1
                RESET TX_BIT_POINTER
            ELSE
                READ TRANSMIT CONTROL WORD BIT (ADDRESS POINTED TO BY TX_BIT_POINTER)
                IF (BIT VALUE = 1) THEN
                DO:
                    LOAD TIMER-0 TO EXPIRE IN 3.33 ms -- START TIMER
                ELSE
                    LOAD TIMER-0 TO EXPIRE IN 1.67 ms -- START TIMER
                ENDIF
                INCREMENT TX_BIT_POINTER
            ENDIF
        ENDIF
    ENDIF
ENDIF
RETURN
```

```
SUBROUTINE IN__WORD          /* THIS ROUTINE READS INCOMING DATA FROM THE INPUT PIN P2.1 OF THE MICROCONTROLLER */

IN__WORD
READ SERIAL PIN        /*P2.1 */
IF (NEW__PIN__VALUE = OLD__PIN__VALUE) THEN                    /* CHECK FOR TRANSITIONS ON DR2 */
DO:
    IF (RECEIVED__BIT__COUNT = 7) THEN
    DO:
        IF (NEW RECEIVED WORD = OLD RECEIVED WORD) THEN
        DO:
            CALL DEC__WORD
        ELSE
            STORE NEW__RECEIVED__WORD IN OLD__RECEIVED__WORD
        ENDIF
    ENDIF
ELSE
    STORE NEW__ PIN__VALUE IN OLD__PIN__VALUE LOCATION
    IF (IN__PULSE FLAG SET) THEN
    DO:
        READ TIMER-1
        IF (TIMER-1 > 5.9 ms) THEN
        DO:
            IF (TIMER-1 > 10 ms) THEN
            DO:
                RESET IN__PULSE FLAG
            ELSE
                SET RECEIVED__BIT__COUNT = 0
            ENDIF
        ELSE
            IF (TIMER-1 > 2.9 ms) THEN
            DO:
                RECEIVED BIT VALUE = 1
            ELSE
                RECEIVED BIT VALUE = 0
            ENDIF
            STORE BIT VALUE AS NEW RECEIVED__WORD IN BIT POSITION INDICATED BY RECEIVED__BIT__COUNT
            INCREMENT RECEIVED__BIT__COUNT
        ENDIF
    ELSE
        SET IN__PULSE FLAG
    ENDIF
    RESET TIMER -1 = 0 -- START TIMER
ENDIF

RETURN
```

```
SUBROUTINE DEC__WORD        /* THIS ROUTINE DECODES THE SEVEN BIT RECEIVED CONTROL WORD */

DEC__WORD
READ NEW RECEIVED WORD
IF (BIT 6 IN WORD = 1) THEN
DO:
    IF (LOCAL DTR IS SET) THEN
    DO:
        SET DSR                         /*PIN 1.0 */
        WRITE BIT 3 TO BIT 5 OF OUTGOING CONTROL WORD
        COMPLEMENT BIT 3
        WRITE BIT 3 TO DCD              /* PIN 1.2 */
        COMPLEMENT BIT 5
        WRITE BIT 5 TO CTS              /* PIN 1.1 */
    ELSE
        RESET DSR                       /*PIN 1.0 */
    ENDIF
ELSE
    COMPLEMENT BIT 1
    WRITE BIT 1 TO DSR              /* PIN 1.0 */
    COMPLEMENT BIT 2
    WRITE BIT 2 TO DCD              /* PIN 1.2 */
    COMPLEMENT BIT 4
    WRITE BIT 4 TO RI               /* PIN 1.3 */
    COMPLEMENT BIT 5
    WRITE BIT 5 TO CTS              /* PIN 1.1 */
ENDIF
RETURN.
```

Application Note MSAN-119
How To Interface Mitel Components to Microprocessors

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TABLE OF CONTENTS

Introduction

Mitel Semiconductor manufactures a wide variety of components oriented towards microprocessor applications. Obviously, there are many different microprocessors, and many different bus architectures. This abundance of unique designs makes it difficult to interface a component directly to more than one type of microprocessor without running into complications for at least one type. The purpose of this application note is to provide assistance in interfacing Mitel components to various microprocessors.

Most of Mitel Semiconductor's products have been designed around Motorola microprocessors, so extra circuitry may be needed to interface to microprocessors designed by other manufacturers. Even across Motorola's product line, there are several different bus structures in evidence (segmented primarily by data bus size, i.e. 8 and 16 bit bus structures). Mitel Semiconductor's products reflect these two bus structures, in that some products are designed specifically for a microprocessor such as the 6809 (8 bit) and some are designed specifically for the 68000 (16 bit). A component designed for the 68000 is not always easily interfaced to the 6809, however, a 6809 peripheral is easily interfaced to the 68000, because the 68000 is designed to accommodate 6802/09 peripherals.

This application note will provide examples of how Mitel components may be interfaced to several of the major microprocessor types. The intent of the

Processor / Component	6800	6802	6809	68000	68010	68008	8085	8086	8088	Z80	Z8002
MD65SC22	4	2	3	5	5	5	7	9	9	*	11
MD65SC51	4	2	3	5	5	5	6	10	10	8	12
MD68SC21	4	2	3	5	5	5	6	10	10	8	12
MD68SC40	4	2	3	5	5	5	7	9	9	*	11
MT8880	4	2	3	5	5	5	6,7	9,10	9,10	8	11,12
MT8952	4	2	3	5	5	5	6	10	10	8	12
MT8980	15	14	13	16	16	16	17	19	19	18	20
MT8981	15	14	13	16	16	16	17	19	19	18	20
MT8920	23	22	21	24	24	24	25	27	27	26	28

Table 1 - Table of Circuits Cross Referenced by Microprocessor and Mitel Part Number

* no circuit

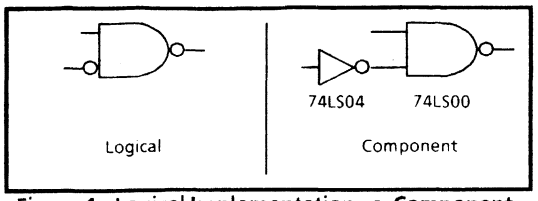


Figure 1 - Logical Implementation vs. Component Implementation

examples is to categorize interface architectures and microprcessor types, in order to help designers incorporate Mitel components in their systems. The microprocessors for which interfacing examples have been created for are:

a/ The 68000
b/ The 68010
c/ The 68008
d/ The 6809
e/ The 6802
f/ The 6800
g/ The 8085
h/ The Z80
i/ The 8086
j/ The 8088
k/ The Z8002

These microprocessors are believed to be the industry's most popular. In most cases, microprocessors not included in the list will have architectures similar to one of those mentioned.

To minimize the number of interfaces that have to be dealt with, it is possible to segment the listed microprocessors into groups. Members of a group are related by similar bus structures. The microprocessors that can be grouped together are:

a/ 68000, 68010, 68008
b/ 8088, 8086

The remaining microprocessors have subtle differences between each other that cause a need for individual interface circuits.

Grouping Mitel's components on the basis of similar interfacing requirements also minimizes the total number of interface circuits. Mitel devices with similar bus architectures are grouped as follows:

Group 1

a/ MD68SC40 Programmable Interval Timer (PTM)
b/ MD68SC21 Peripheral Interface Adapter (PIA)
c/ MD65SC22 Versatile Interface Adapter (VIA)
d/ MD65SC51 Asynchronous Communications Interface Adapter (ACIA)
e/ MT8952 HDLC Controller
f/ MT8880 DTMF Transceiver

Group 2

a/ MT8980 Digital Time/Space Crosspoint Switch
b/ MT8981 Digital Time/Space Crosspoint Switch

Group 3

MT8920 ST-Bus Parallel Access Device (STPA)

The majority of the application note is dedicated to describing the interface circuits and explaining their operation. Each interface shall have an accompanying block diagram to enhance understanding of the circuit. To keep the interfaces independent of a particular system, as few actual "glue" components as possible will be shown in the diagrams. Instead of showing commercially available components, only the logical symbol representing the desired operation shall be shown.

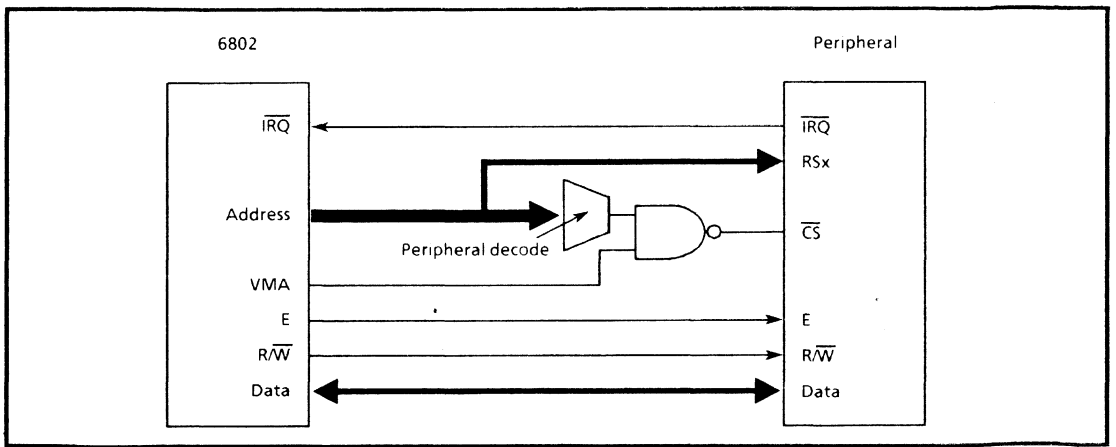


Figure 2 - Interfacing the MD68SC40, MD68SC21, MD65SC22, MD65SC51, MT8952, and the MT8880 to the 6802.

This will leave the actual implementation to the designer (see Figure 1).

Table 1 (below) is a cross reference of interface circuit diagrams, referenced by microprocessor and Mitel Semiconductor part number. To find the appropriate interface circuit, select the column corresponding to the microprocessor being used, and select the row corresponding to the Mitel component being used. The figure number of the required circuit diagram(s) is indicated in the table element common to the row and the column.

1.0 Group 1 Components

Group 1 consists of the MD68SC40, the MD68SC21, the MD65SC22, the MD65SC51, the MT8952, the MT8970 and the MT8880. All of these components have the same basic interface, but a subtle requirement causes several of the parts to use a separate and more complex circuit design (depending on the microprocessor interfaced to).

The Group 1 interface consists of:

a/ an 8 bit data port,

b/ several inputs used for selecting internal registers (register selects),

c/ chip select input(s),

d/ a read/write control that specifies the direction of data flow (to or from the component),

e/ an enable strobe that synchronizes component timing to the microprocessor's timing,

f/ an interrupt output that is used to alert the microprocessor that a specific event has occurred at the component.

The subtle difference mentioned above divides Group 1 components into two sub-groups: those components that require a constantly active Enable clock and those components that do not. The MD65SC22, the MD68SC40 and the MT8880 are the components that require a constant clock on the E input (in some of their operating modes). This may cause a more complicated circuit design when interfacing to microprocessors that have more than one clock cycle per bus cycle ie. 8085, 8086, 8088, Z80 and the Z8000. When interfacing to the 6802/09, 6800, and the 68000, the circuit design is the same for both sub-groups.

1.1 Interfacing to the 6802

Interfacing Group 1 components to the 6802 is the simplest interfacing task. The 6802 has the following interface:

a/ an 8 bit data port,

b/ 16 bit address bus for addressing 64 kbytes of memory or I/O,

c/ a read/write output that specifies the direction of data flow (to or from the microprocessor),

d/ an enable strobe output that synchronizes component timing to microprocessor timing, (This signal strobes with a constant frequency unless the microprocessor is in the reset condition. Cycles may be stretched, but should only be stretched for several normal E cycles. Note that, because E is constant, all group 1 devices may use the same circuit when interfacing to the 6802. Also note that one bus cycle is equivalent to one E cycle.)

e/ an interrupt input that is used to alert the microprocessor that a specific event has occurred at the component.

The 6802's signals relate to Group 1 signals almost directly. The data port of the 6802 may be connected directly to the data port of any of the Group 1 components. Information is transferred between microprocessor and the component on this bus. The address bus of the microprocessor must be decoded to produce the chip select(s) needed by a component before it will participate actively on the data bus. In a decode of the address bus, the validity of the address bus state must be qualified by the VMA (Valid Memory Address) signal. Any of the address bits may be connected directly to the register select inputs of the component (the least significant bits are the bits most commonly used).

When the chip select is active, and the enable signal is active, the data bus will be carrying either information from the microprocessor, or information from the component. The source of the information is dependent on the state of the R/$\overline{W}$ signal from the 6802. If the R/$\overline{W}$ is high (read), the selected Group 1 component will turn on its data bus drivers and the contents of the selected register will be transferred to the data bus. If the R/$\overline{W}$ signal is low (write), the Group 1 device's data port will be high impedance and the microprocessor will transfer information to the data

bus. The bus cycle is terminated by the falling edge of the E clock (strobe is a more appropriate term). When a write bus cycle is ended, the Group 1 component will latch the state of the data bus into the selected register. When a read bus cycle is ended, the component holds the data bus in the same state for a short period of time (hold time) before relinquishing control of the bus. Note that some of the components "acquire" the data from the bus on the rising edge of E. Appropriate set up time before this rising edge must be observed. Set up time is applicable to control signals, data and address information.

The interrupt output of Group 1 devices is an open drain configuration (analogous to open collector in TTL devices), therefore it must be pulled up to V_{CC} by a resistor. This output can be connected directly to the 6802 or to a priority encoder, which is then connected to the 6802. Group 1 components signify the presence of an interrupt condition by pulling this line low. The microprocessor must clear this interrupt through an established procedure that is dependent on the type of component that initiated the interrupt. The resistor used to pull up any open drain outputs is not shown any of the diagrams in this note.

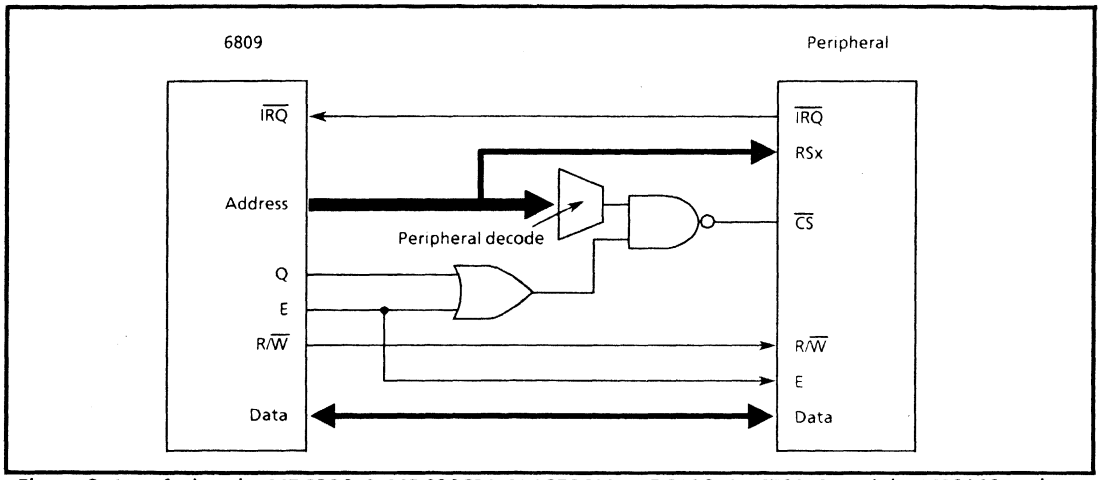


Figure 3 - Interfacing the MD68SC40, MD68SC21, MD65SC22, MD65SC51, MT8952, and the MT8880 to the 6809.

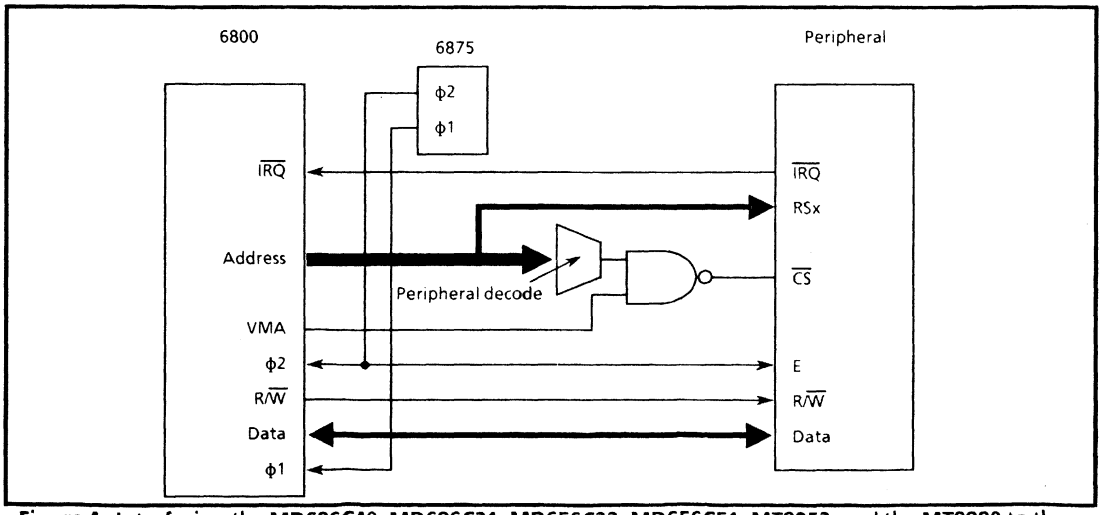


Figure 4 - Interfacing the MD68SC40, MD68SC21, MD65SC22, MD65SC51, MT8952, and the MT8880 to the 6800.

Figure 2 shows the connection of data bus as a straight connection; in reality, there will probably be a buffer intervening to give the microprocessor more driving capability. R/$\overline{W}$ and E are also shown to be a straight connection. These signals are also usually buffered. In further figures, details such as buffers will be omitted as they are dependent on the design of the target system.

The address bits are shown connected to a box labelled "peripheral decode". This can refer to any circuitry that produces an active high signal when the correct address is on the bus. The active signal is 'NAND'ed with VMA to produce an active low chip select. Most Group 1 components have at least 2 chip select inputs, usually of opposite active logical states, so the active low signal in Figure 2 could have been a high signal, depending on the device and the select used (remaining unused chip selects can be used to decode the address bus further, or may be tied to their active voltage levels). The most important point implied by the presence of the NAND gate is that the 6802's VMA signal must qualify any decode of Group 1 components (VMA could have been tied to the active high chip select input to save an external gate).

1.2 Interfacing to the 6809

The circuit needed to interface the 6809 to Group 1 devices (Figure 3) is almost the same as the circuit used to interface to the 6802, due to the similarity between the two microprocessors' bus architectures. The only difference between the two circuits is that the 6809 does not have a VMA signal, so an equivalent signal must be generated by 'OR'ing the E and the Q signals of the 6809.

1.3 Interfacing to the 6800

Interfacing the 6800 to Group 1 devices requires the same circuit used for interfacing Group 1 components to the 6802. The only difference between the circuits is that in Figure 4 the 6875 clock generator IC is shown connected to the 6800.

1.4 Interfacing to the 68000/10/08

Motorola's 68000 16 bit microprocessor takes advantage of the broad line of interfaces designed around its 8 bit microprocessors. Normally, information transferral between the 68000 and a peripheral is performed asynchronously, as opposed to the synchronous method used by the 8 bit microprocessors (6800, 6802, 6809 etc.). The 68000, however, can be forced to perform a synchronous transfer.

Synchronous transfers are achieved by referencing all bus events to the edges of the E strobe. Asynchronous transfers involve a handshake between the 68000 and the component involved in the data transfer. When the 68000 wants to read or write a device, the 68000 asserts $\overline{LDS}$ or $\overline{UDS}$ ($\overline{DS}$ in the 68008) and when the component has accepted the data (write) or has put valid data on the data bus (read), the component asserts an open drain signal called $\overline{DTACK}$ (Data Acknowledge). This signal causes the 68000 to end the bus cycle by removing the data strobe signal. Following $\overline{DS}$ negation, a read latches data into the microprocesor, the peripheral releases the data bus and negates $\overline{DTACK}$. If a write, the data is latched into the peripheral and it then negates $\overline{DTACK}$.

Motorola designed a mechanism to accommodate peripherals that do not have the capability to perform an asynchronous transfer with the 68000. The 68000 supplies an E clock, a $\overline{VMA}$ signal and an input called $\overline{VPA}$. If an address supplied by the 68000 (qualified by $\overline{AS}$) causes the $\overline{VPA}$ signal to be asserted, the 68000 synchronizes the data transfer to the E clock (see 68000 data sheet for timing details).

To synchronize, the 68000 waits for the E clock to go low (E clock timing has no relation to normal 68000 bus cycles), then the 68000 asserts $\overline{VMA}$ and finishes out the bus cycle like an 8-bit microprocessor. The finishing sequence is as follows: E goes high, data is transferred, the bus cycle terminates with E falling, $\overline{VMA}$ is negated, $\overline{AS}$ and the data strobes are negated).

The 68000's exception handling is very different from the 8-bit processors. Peripherals can take an active role in the determination of the exception vector. Any state on the Interrupt Priority Level inputs (IPL0-2), other than all ones (level 0), indicates an interrupt. If an interrupt is indicated, the state of the $\overline{IPL0\text{-}2}$ inputs codes the level of the interrupt's priority. The information encoded on these inputs is inverted in the 68000 to represent the priority level on the 3 bit interrupt mask in the internal status register.

When the instruction that is being executed at the time of the interrupt is finished, the 68000 performs an interrupt acknowledge cycle. During an interrupt acknowledge cycle, the 20 most significant bits of the address are set high, the three least significant bits reflect the interrupt level, and the FC0-2 pins on the 68000 are all set (the real indicator that an interrupt acknowledge cycle is occurring). $\overline{AS}$ is asserted, and then $\overline{LDS}$ is asserted (an interrupt vector may only be transferred on the lower half

of the data bus in the 68000). The R/$\overline{W}$ pin will be high because the 68000 is expecting the peripheral to place vector information on the data bus, as if the 68000 was reading one of the peripheral's internal registers. A peripheral designed for the 68000 will complete the handshake with the data required and return $\overline{DTACK}$ just like a normal exchange.

Group 1 components do not have the above facility to provide the 68000 with an interrupt vector, just as they cannot perform an asynchronous transfer. However, Motorola has provided for 6800 peripherals in 68000 exception processing, just as provision was made for data transfers with 6800 peripherals. If the information that the 68000 provides to indicate an interrupt acknowledge cycle and the level of the interrupt can cause $\overline{VPA}$ to be asserted, the 68000 will automatically fetch an exception vector at an address determined by the level of the interrupt (Motorola calls this autovectoring). There are seven autovector locations (7 interrupt priority levels) and they are located at address 000064_H to $00007C_H$.

The circuit to interface Group 1 components to the 68000 (Figure 5) must be able to assert $\overline{VPA}$ not only when the component is directly addressed, but also when the 68000 is indicating that the component was the source of the interrupt. Figure 5 shows a block symbol to represent the decode of a group 1 device. The input of this block is the address bus and $\overline{AS}$; the output is a signal that has two destinations: the in put to the circuit that asserts $\overline{VPA}$ and the input to the circuit that asserts the group 1 components chip select.

To select the component for data transfer, the output of the peripheral decode circuitry is further decoded by $\overline{VMA}$. To generate $\overline{VPA}$, the peripheral decode ouput is 'NOR'ed with an interrupt acknowledge (IACK) signal. The IACK signal is formed by 'AND'ing the FC0-2 outputs, asserting $\overline{AS}$, and placing the correct priority level information on the 3 least significant address pins. All this information is 'AND'ed to produce IACK. Figure 5 shows a possible interrupt encoding scheme implemented with the Group 1 component's $\overline{IRQ}$ line driving a 74LS348 eight to three encoder. The 74LS348, in turn, drives the $\overline{IPL}$ inputs (remember that the logic level is inverted to form the internal priority level).

The remaining signals that Group 1 components require are derived in a more standard manner. R/$\overline{W}$ from the 68000 can be connected directly to the component, as can E and one half of the 16 bit data bus (the component will be found at either odd or even addresses from the base address). The 68008 has only two interrupt inputs, with $\overline{IPL0}$/$\overline{IPL2}$ being functionally equivalent to tying

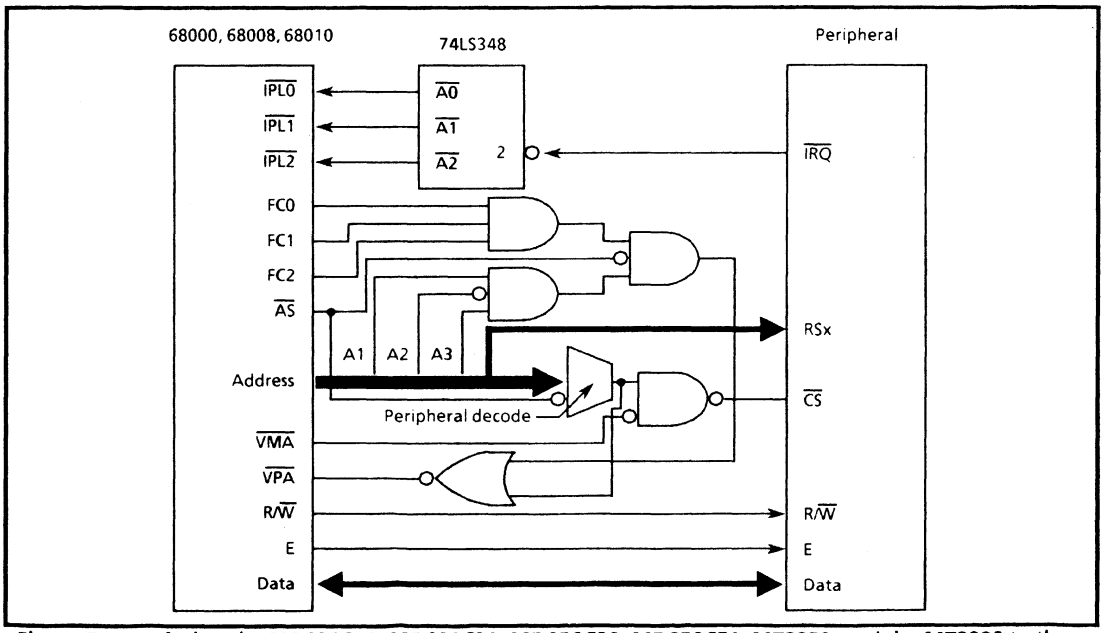


Figure 5 - Interfacing the MD68SC40, MD68SC21, MD65SC22, MD65SC51, MT8952, and the MT8880 to the 68000, 68010 and the 68008.

$\overline{IPL0}$ and $\overline{IPL2}$ together on the 68000 (only priority levels 0, 2, 5 and 7 are available on the 68008).

1.5 Interfacing to the 8085

There are two circuits needed to interface group 1 components to the 8085, depending on the requirement for a continuous E clock on the MT8880, the MD68SC40 and the MD68SC22. The circuit in Figure 6 assumes that the application can accommodate the lack of a continuous E clock; in some applications the MT8880, the MD68SC40 and the MD65SC22 can do so.

The circuit is different from the interface to the Motorola 8 bit microprocessors in many respects. The first difference is that the Intel 8085 has a multiplexed address/data bus, the Motorola parts do not. The first step in decoding an address generated by the 8085 is to demultiplex the least significant half of the address from the data. Intel provides a latch, the 8212, that does this. It is strobed by the ALE (Address Latch Enable) signal from the 8085, when the address on the Address/data bus is valid. The demultiplexed address may then be decoded as in the Motorola system. The register select pins may be derived from any of the address bits.

The second difference is that rather then using the combination of a R/$\overline{W}$ direction pin and an E strobe, the 8085 uses a $\overline{Read}$ strobe and a $\overline{Write}$ strobe. When either of these strobes are active, the active period is equivalent to the period in a Motorola bus cycle where the E strobe is active. The direction of the data transfer is determined by which strobe, the $\overline{RD}$ or the $\overline{WR}$, is present. For correct operation of Group 1 components, R/$\overline{W}$ and E must be generated from $\overline{RD}$ and $\overline{WR}$. To generate E, $\overline{RD}$ and $\overline{WR}$ are 'NAND'ed together. The generation of the R/$\overline{W}$ signal is done by driving the Set input and the Reset input of a RS flip flop with $\overline{RD}$ and $\overline{WR}$, respectively. The Q output may be connected directly to R/$\overline{W}$. R/$\overline{W}$ will maintain the same state until the opposite operation occurs, but it will only affect the Group 1 component when the device is selected, and then it will have the correct state with ample set up and hold times. It is important to note that R/$\overline{W}$ has a minimum set up time with respect to the rising edge of E. This must be accounted for in the circuit design, therefore E may have to be delayed.

The final difference in the 8085 circuit is that the interrupt input RST is active high, so the $\overline{IRQ}$ output of the Group 1 component must be inverted.

As stated before, the reason that a different interface is required for several Group 1 components in various applications is that these components require a regular E strobe. The MD68SC40 uses the E strobe to clock its timers; if an external strobe other than E is used to clock a timer (optional) then this external strobe is synchronized to the E strobe. E can be removed for periods of time, but when the timers are intended to be operational a regular clock should be present.

The MD65SC22 has a similar requirement for a constant E strobe for its timer operation and for shift register operation. MD65SC22 parallel port operation does not require a regular E strobe. The MT8880 uses the E strobe to update the status of the $\overline{IRQ}$ pin and a bit in the status register that shows a valid DTMF (Dual Tone Multiple Frequency) tone has been received. These MT8880 signals will only become active if E is strobed during a period when a

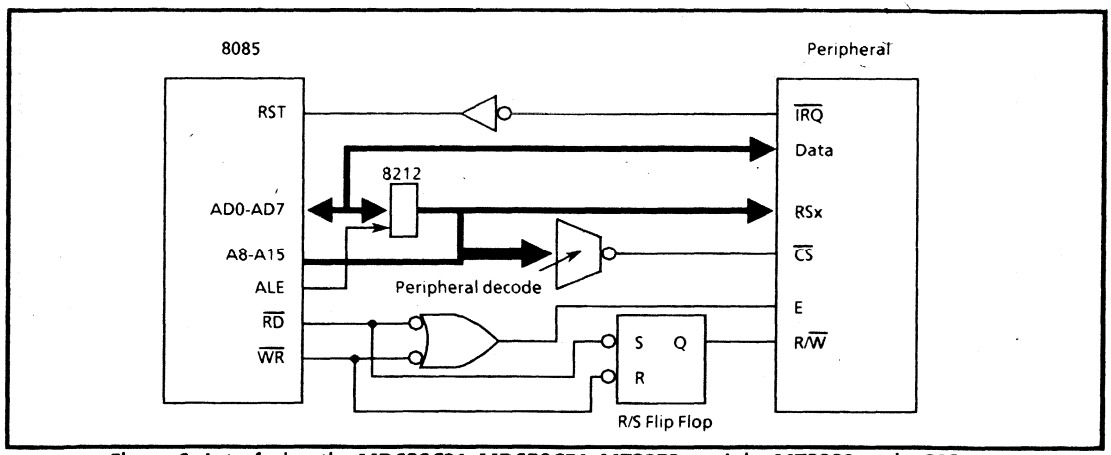


Figure 6. Interfacing the MD68SC21, MD65SC51, MT8952, and the MT8880 to the 8085.

DTMF tone is actually present (the device retains no memory of such an event if it has already passed when E is strobed), so the period between E strobes should not be quite as long as the minimum time a DTMF tone must be present. The clock need not be present if no tones are expected.

Given that these devices have the above requirements, the circuit in Figure 6 must be modified to provide an E strobe with some regularity. The clock of the 8085 cannot be used directly because this clock has several cycles per bus cycle (four for opcode fetches, and three for data reads/writes to memory and I/O). It would be possible to keep using the signal derived by 'NAND'ing the $\overline{RD}$ and $\overline{WR}$ that is used in Figure 6, if it could be guaranteed that the microprocessor would not be placed in a hold state ($\overline{RD}$ and $\overline{WR}$ will cease to toggle until the microprocessor is released). If this cannot be guaranteed, then the circuit in Figure 7 may be required.

The circuit in Figure 7 is only different from the circuit of Figure 6 in the way E is generated. To generate a constant E strobe, the circuit takes advantage of the fact that ALE and the system clock (CLK) never get placed into a high impedance state (even in hold conditions). Also, events involving the $\overline{RD}$ strobe, $\overline{WR}$ strobe, ALE and CLK have a constant relationship that allows ALE to initiate an "event sequence" that is sustained by CLK and results in an E strobe synchronized with the termination of the $\overline{WR}$ and $\overline{RD}$ strobes (See Timing Diagram 1).

ALE occurs a minimum of 15 nS before the falling edge of clock cycle 1 in any 8085 bus cycle. The next falling edge of clock cycle 1 will clock the output of the first flip flop through the second flip flop to drive the E input of the group 1 component. This output is input into a third flip flop that is clocked by the rising edge of CLK, so on the rising edge of the clock cycle 2 the output of the third flip flop will be clocked low. This output drives the D input of a fourth flip flop, which will propagate this signal on the next rising edge of CLK (clock cycle 3). A low on the fourth flip flop's output will clear the first two flip flops and coincidently clear the signal driving the E input of the Group 1 component. This is also the point where data may be removed from the bus by the component if a read is occurring and where data is still valid from the microprocessor if a write is occurring, so the proper relationship between the microprocessor and the Group 1 component is maintained. Flip flops 3 and 4 are preset by ALE

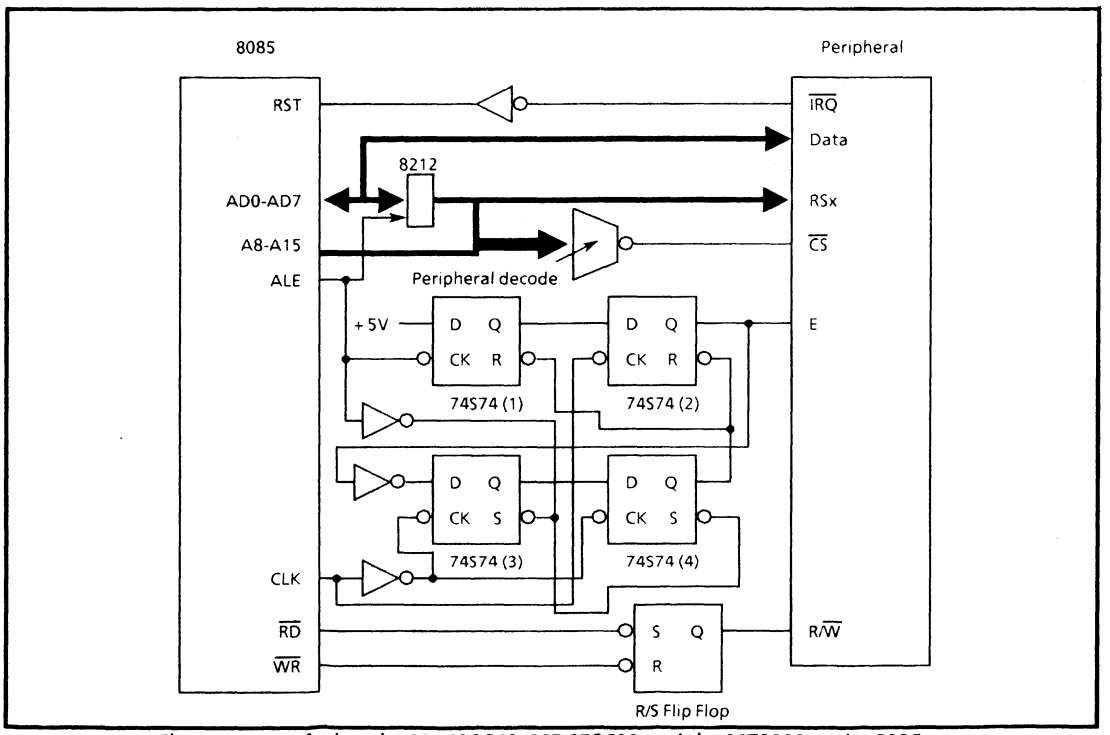


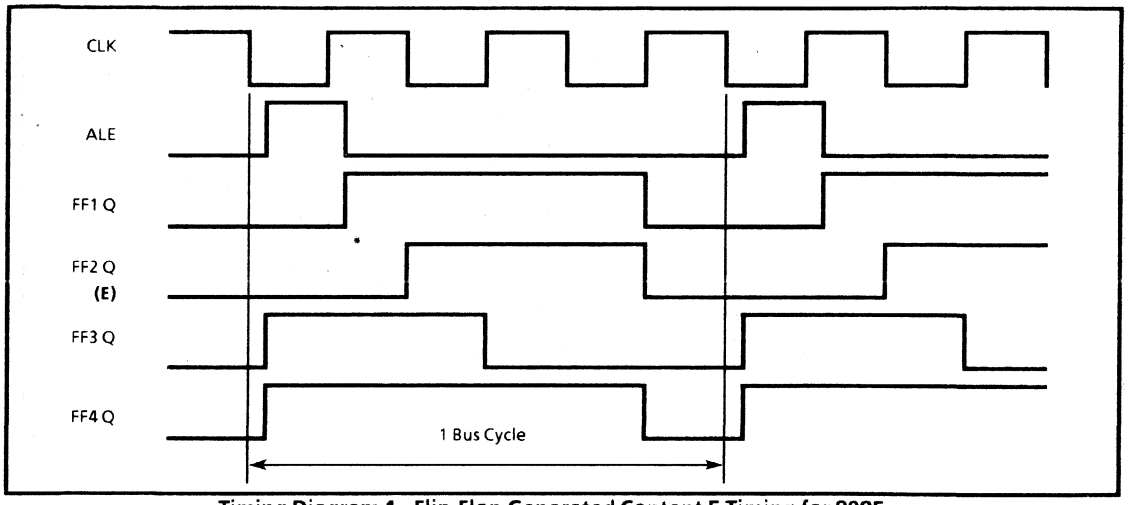
Figure 7 - Interfacing the MD68SC40, MD65SC22 and the MT8880 to the 8085.

going high, so all flip flops are initialized for the next bus cycle.

1.6 Interfacing to the Z80

The circuit in Figure 8 is very similar to the circuit in Figure 6 in that the Z80 must transform a $\overline{RD}$ strobe and a $\overline{WR}$ strobe into an E strobe and a R/$\overline{W}$ signal (recall the set up time for the R/$\overline{W}$ signal with respect to the E signal). This portion of the circuit is exactly the same as the circuit used for the 8085 ,i.e. 'NAND'ing $\overline{RD}$ and $\overline{WR}$ to form E and the RS flip flop used to create R/$\overline{W}$. In the Z80 circuit the peripheral decode has been arbitrarily chosen to include $\overline{IORQ}$ (I/O request) active. By doing this, the 8 most significant address bits need not be decoded, as an I/O access doesn't allow specification of more than an 8-bit address. Another difference between this circuit and the 8085 circuit is that the address bus of the Z80 is not multiplexed so no latch is needed for a portion of the address. $\overline{INT}$, the interrupt input does not need an inverter between the Z80 and the Group 1 component. Both the 8085 and the Z80 have autovectored interrupts or vector acquisition modes (like the 68000). The autovectored interrupts should be used.

It is impossible to generate a regular E strobe, that is not based on the $\overline{RD}$ and $\overline{WR}$ signals from the Z80. This is because the Z80 does not have a signal like ALE to unconditionally indicate the start of a bus cycle when $\overline{RD}$ and $\overline{WR}$ are not present. This may make it difficult to use the MT8880, the MD68SC40 and the MD65SC22 with the Z80, given the constraints on E mentioned earlier.



Timing Diagram 1 - Flip-Flop Generated Contant E Timing for 8085

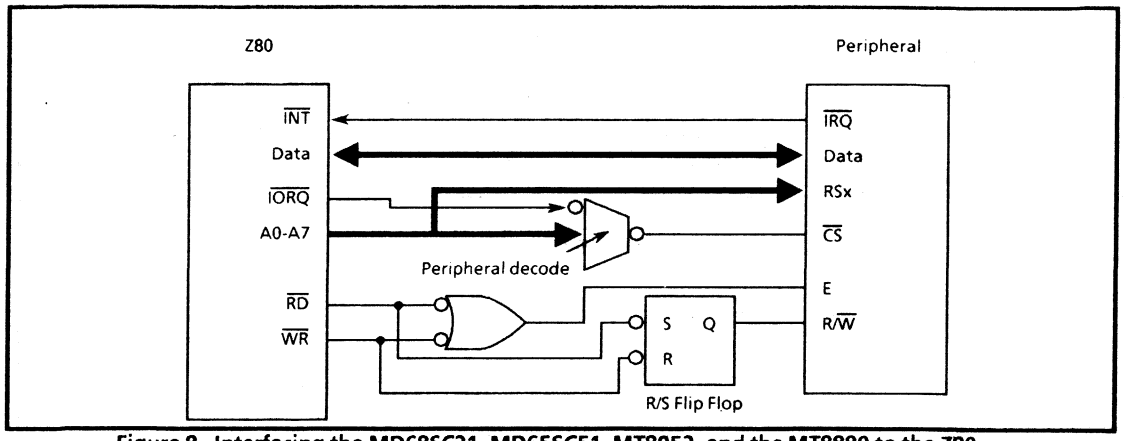


Figure 8 - Interfacing the MD68SC21, MD65SC51, MT8952, and the MT8880 to the Z80.

1.7 Interfacing to the 8086/88

The 8086/88 can interface to Group 1 components in a very similar manner to the way the 8085 does. The 8086/88 has a multiplexed address/data bus (AD0-15 for the 8086 and AD0-8 for the 8088), ALE strobes and $\overline{RD}$ and $\overline{WR}$ strobes. Conveniently, there is a signal that can be inverted and connected directly to the R/$\overline{W}$ inputs of Group 1 components, DT/$\overline{R}$ (Data Transmit/Receive).

$\overline{BHE}$ (Bus High Enable) is an output used to indicate that information is on the high portion of the data bus (8086 only). This signal is used to qualify chip selects. To generate the E signal in applications

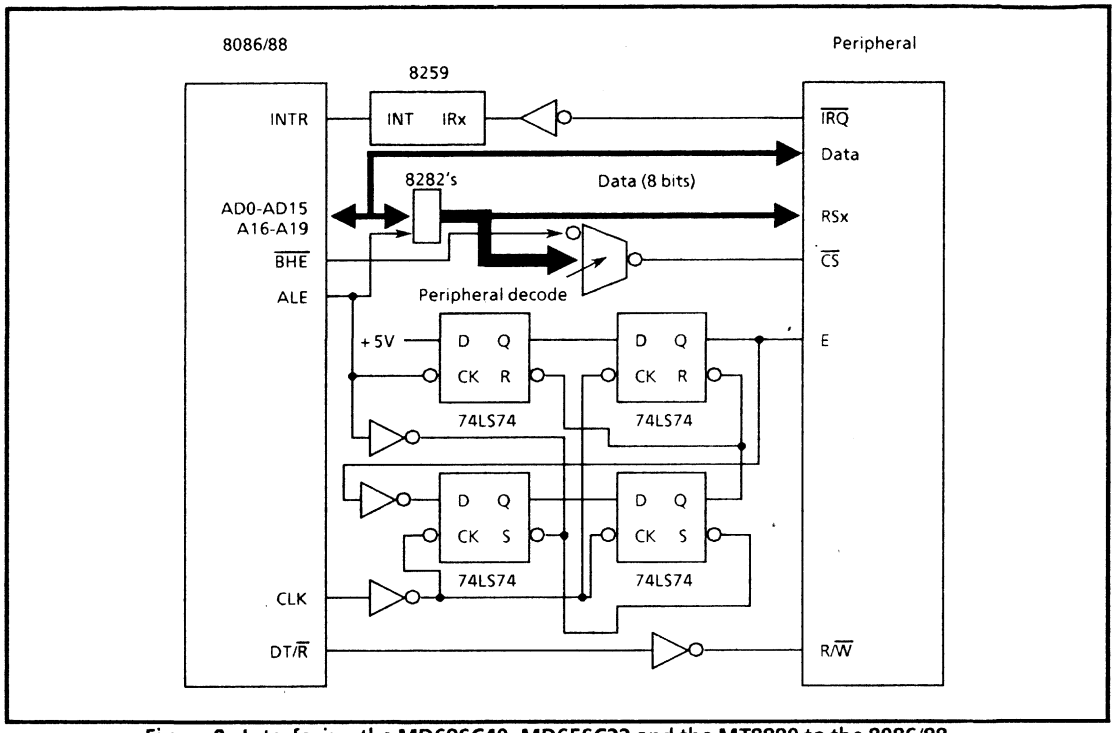


Figure 9 - Interfacing the MD68SC40, MD65SC22 and the MT8880 to the 8086/88.

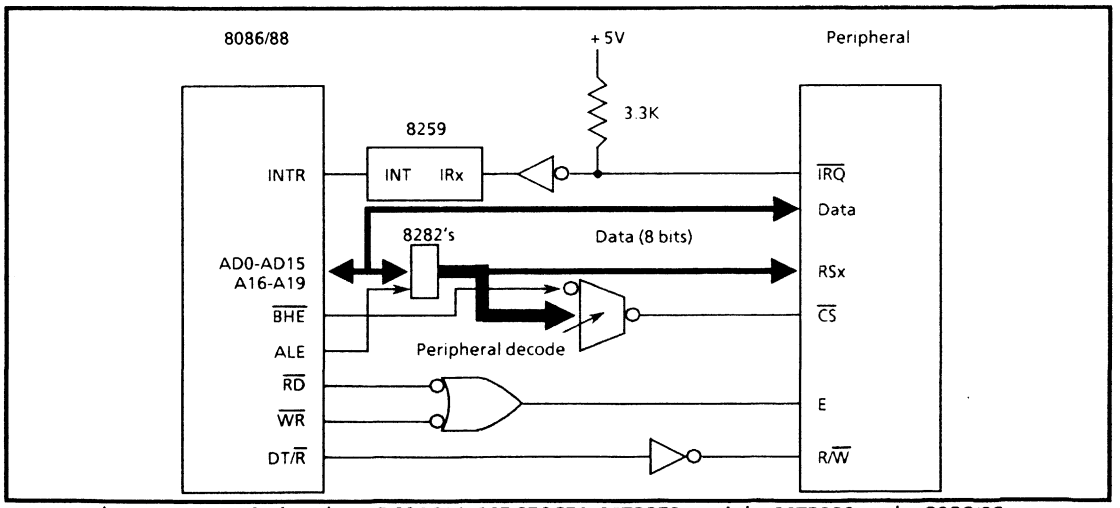


Figure 10 - Interfacing the MD68SC21, MD65SC51, MT8952, and the MT8980 to the 8086/88.

where E need not be constant, $\overline{RD}$ and $\overline{WR}$ may be 'NAND'ed together (Figure 10). The difference in the interrupt circuitry is that an 8259 Programmable Interrupt Controller may be used to handle the 8086/88's need for acquiring an interrupt vector (the 8086/88 does not provide autovectoring).

Note that although the 8086/88 has a minimum and maximum mode, the only difference in the signals required by Group 1 components is that when in maximum mode the signals may be generated by an 8288 bus controller rather than the 8086/88 itself. This is not shown in Figure 9 and Figure 10.

To generate the constant E strobe for the MT8880, the MD68SC40 and the MD65SC22, a slightly altered 4 flip flop circuit that uses ALE and CLK as its inputs is shown in Figure 9. This circuit accommodates differences in the sequence of events between the 8086/88 and the 8085.

1.8 Interfacing to the Z8002

The circuits for interfacing the Z8002 to Group 1 components (Figures 11 and 12) are similar to the circuits for the 8086/88. The differences are:

a/ The Z8002 has an active low "autovector" input (the 8259 PIC is not needed)

b/ $\overline{AS}$, the Zilog version of ALE, is active low and must be used to strobe the multiplexed address bits from the Address/Data bus into a 16-bit latch.

c/ The Z8002 supplies a R/$\overline{W}$ signal

d/ The Z8002 $\overline{DS}$ signal is the equivalent of the 8086/88 $\overline{RD}$ and $\overline{WR}$ strobes. This signal can be inverted to form E (Figure 12) for Group 1 components.

e/ Differences between the four flip flop circuit in Figure 11 and that in Figure 9 reflect the differences in event sequencing between the Z8002 and the 8088/86.

These two circuits complete the Group 1 components. Fortunately, the following two groups are not complicated by the need for a constant E clock.

2.0 Group 2 Components

The interface of a Group 2 component is different from that of a group 1 component in only two ways. The first difference is that there is no requirement for a Group 2 component to interrupt the microprocessor. This simplifies the circuit required by most of the microprocessors minimally, but for others (68000/10/08, 8086/88) the simplification is

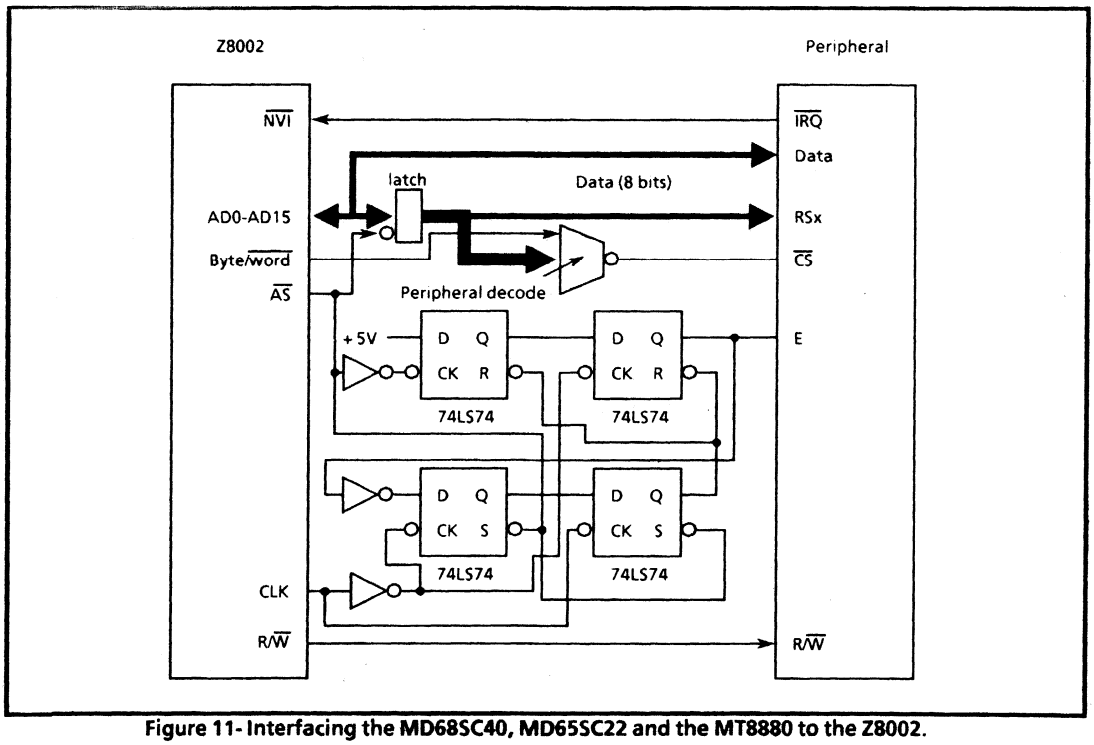


Figure 11- Interfacing the MD68SC40, MD65SC22 and the MT8880 to the Z8002.

extensive. The other difference is that a Group 2 device may respond more slowly to microprocessor accesses. This suggests a requirement for a Memory Ready output from the Group 2 component.

Actually, Group 2 components have an output called $\overline{DTA}$ which can also serve as an input to $\overline{DTACK}$ on the 68000/10/08. In fact, $\overline{DTA}$ was designed for the 68000, so it needs extra circuitry to interface to the "memory ready" schemes of the

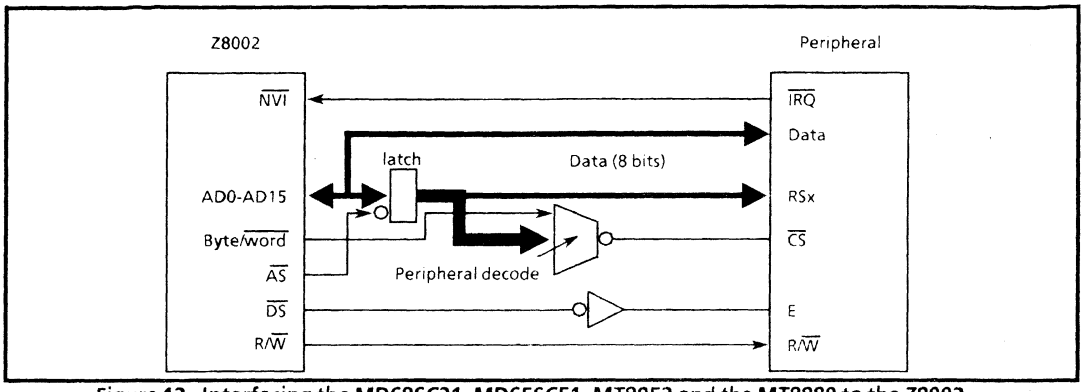


Figure 12 - Interfacing the MD68SC21, MD65SC51, MT8952 and the MT8880 to the Z8002.

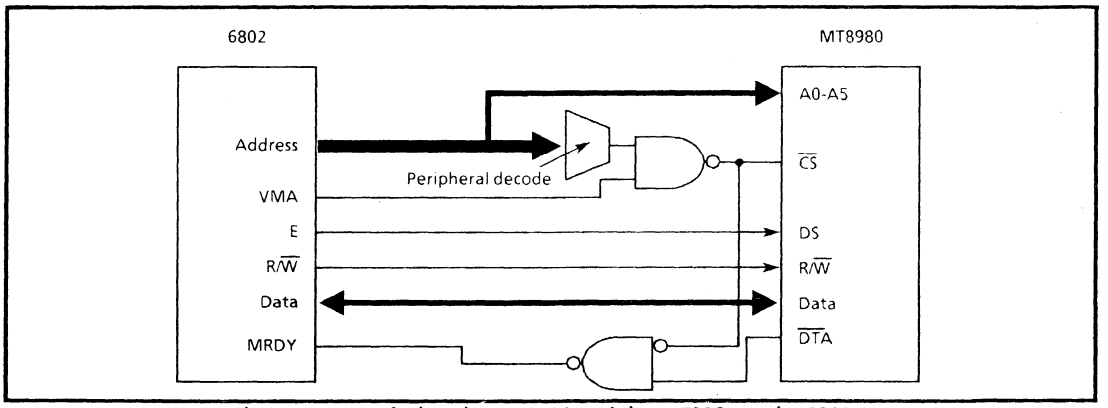


Figure 13 - Interfacing the MT8980 and the MT8981 to the 6802

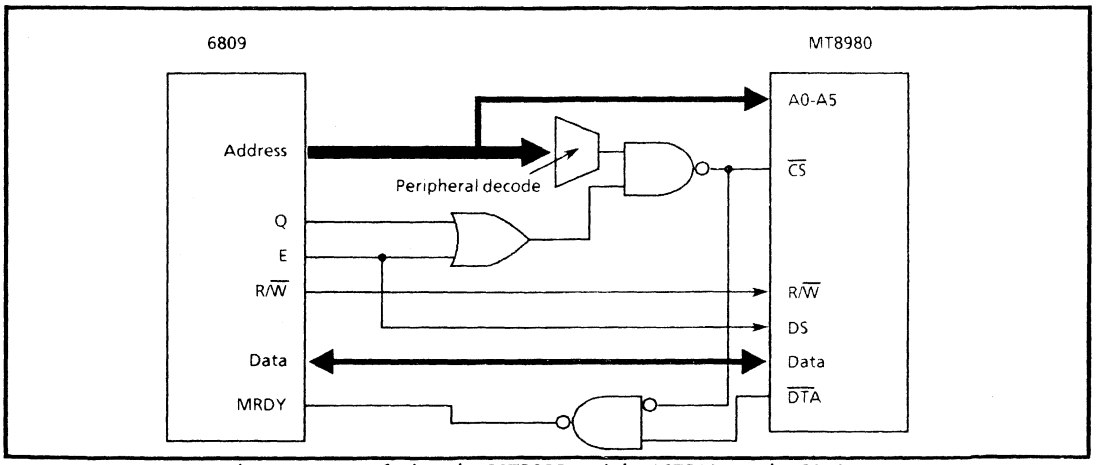


Figure 14 - Interfacing the MT8980 and the MT8981 to the 6809.

synchronous microprocessors. This circuit consists of 'NAND'ing the signal that selects the Group 2 component with the $\overline{DTA}$ signal.

Aside from the above circuit changes, each Group 2 interface circuit is the same as the Group 1 circuit, so a discussion on each circuit is not necessary. However, note that the 68000/10/08 circuit does not require the use of the E/$\overline{VMA}$/$\overline{VPA}$ interface (data strobe from the microprocessor must be inverted). Interfaces for Group 2 components are shown in Figures 13 to 20.

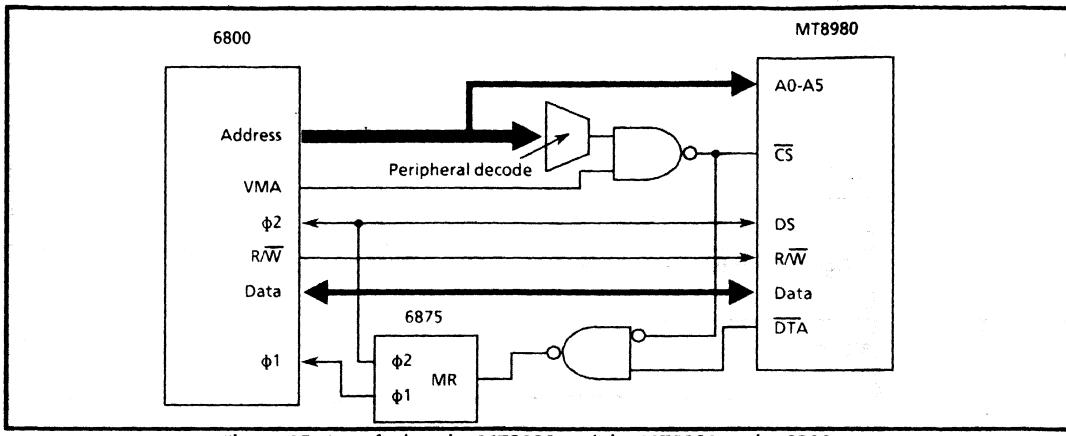


Figure 15 - Interfacing the MT8980 and the MT8981 to the 6800.

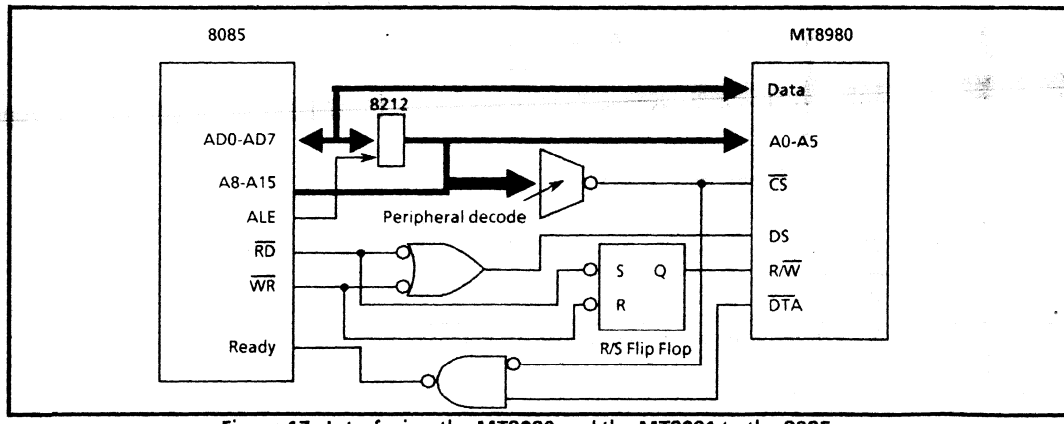


Figure 17 - Interfacing the MT8980 and the MT8981 to the 8085.

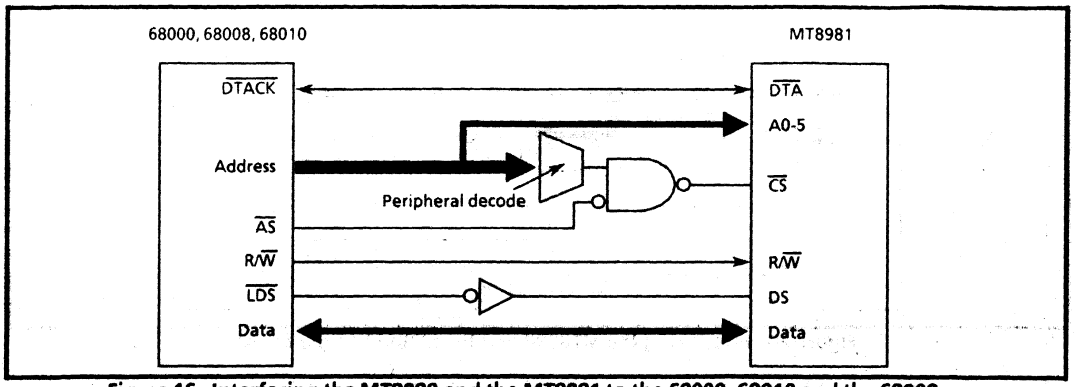


Figure 16 - Interfacing the MT8980 and the MT8981 to the 68000, 68010 and the 68008.

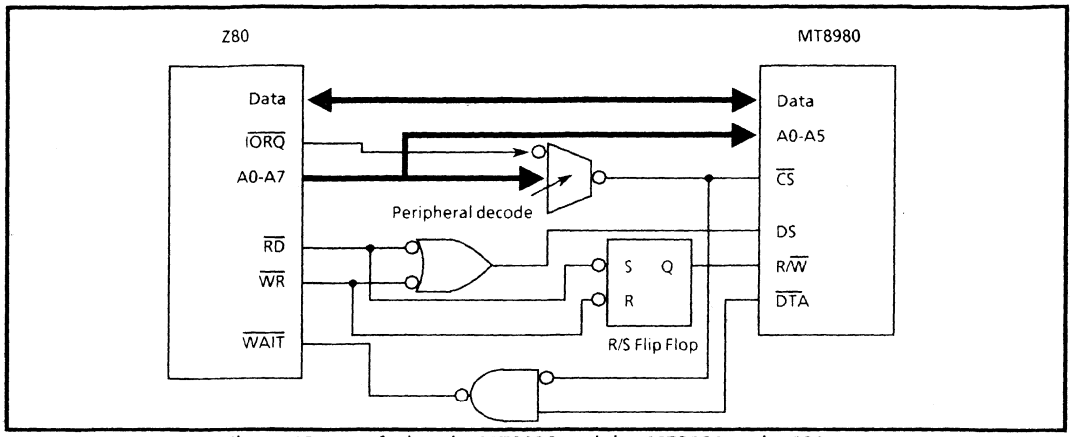


Figure 18 - Interfacing the MT8980 and the MT8981 to the Z80.

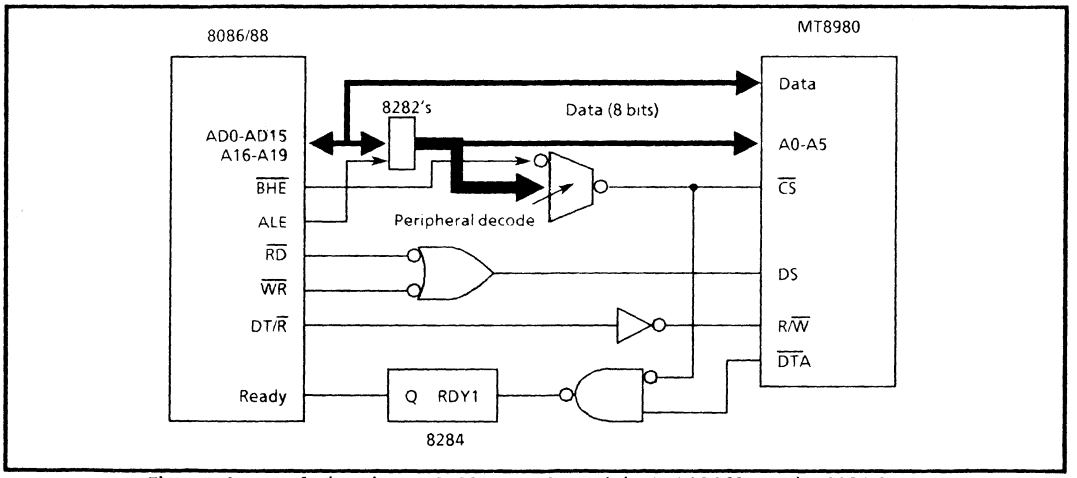


Figure 19 - Interfacing the MT8980, MT8981 and the MD68SC84 to the 8086/88.

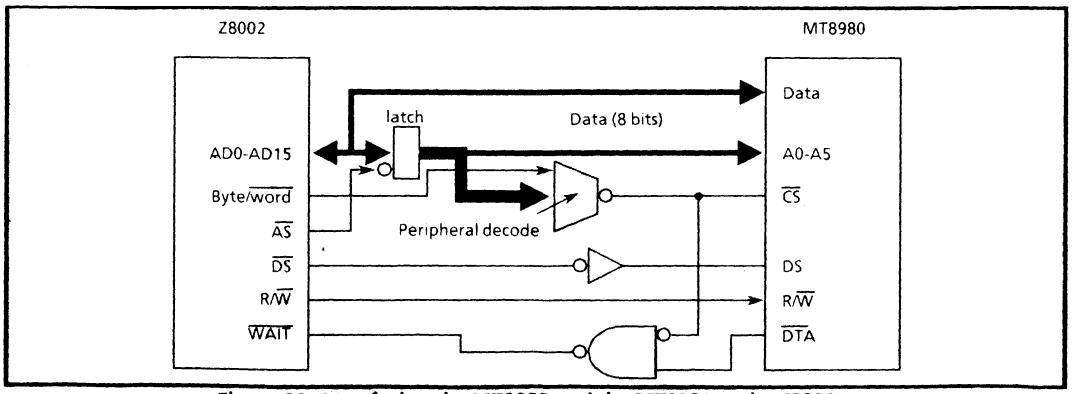


Figure 20 - Interfacing the MT8980 and the MT8981 to the Z8002

3.0 Group 3 Components

The Group 3 component is a device called the ST-BUS Parallel Access (STPA). The STPA has three operating modes, but only one mode was designed specifically for microprocessor control, so the others shall not be covered. The STPA has almost the same interface as the Group 1 devices. The differences are:

a/ Data strobe is the proper polarity for the 68000 which means it must be inverted for Motorola 8-bit microprocessors. Only slight modifications are performed for other microprocessors.

b/ The STPA can provide vectored interrupts for the 68000. This will change the 68000/10/08 interface circuit (Figure 24), but other microprocessors should ignore this capability and use the "autovectoring" schemes already described.

Figures 21 to 28 show diagrams of Group 3 interfaces.

3.1 Interfacing to the 68000/10/08

Figure 24 shows the circuit required to interface the MT8920 to the 68000. Note that $\overline{IACK}$ is decoded, but rather than being combined with the chip select signal to produce $\overline{VPA}$, $\overline{IACK}$ combines with the state of A1-3 to provide an alternative select to the MT8980 (as opposed to the normal decode of the address bus). This dual approach to selecting the MT8980 is used because an interrupt acknowledge cycle transfers information from the MT8920 in the same manner as any normal read cycle. The decoded signal $\overline{IACK}$ tells the MT8920 that it must transfer the interrupt vector programmed into it onto the data bus.

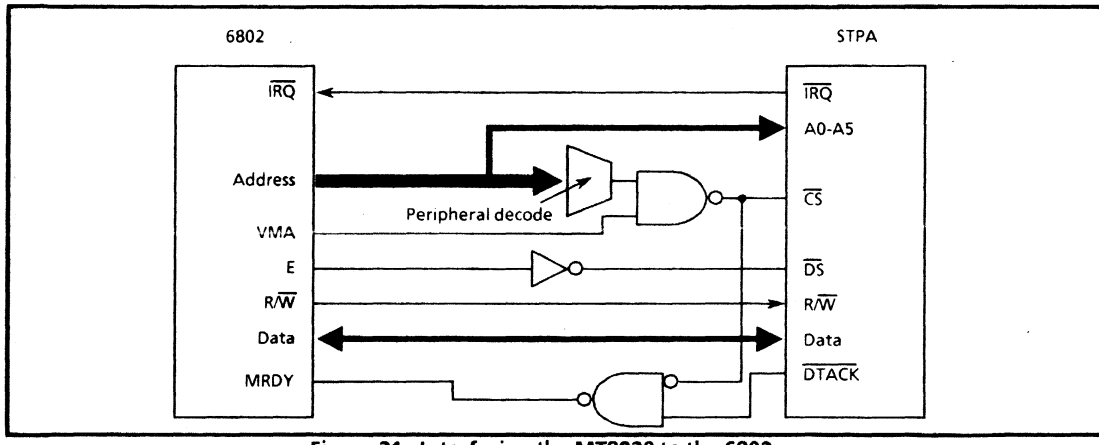


Figure 21 - Interfacing the MT8920 to the 6802.

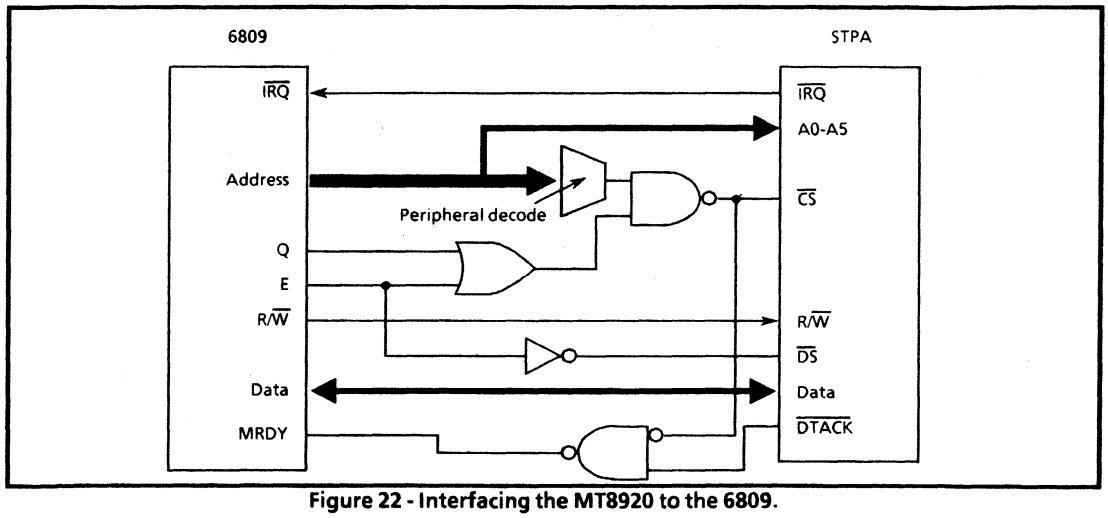


Figure 22 - Interfacing the MT8920 to the 6809.

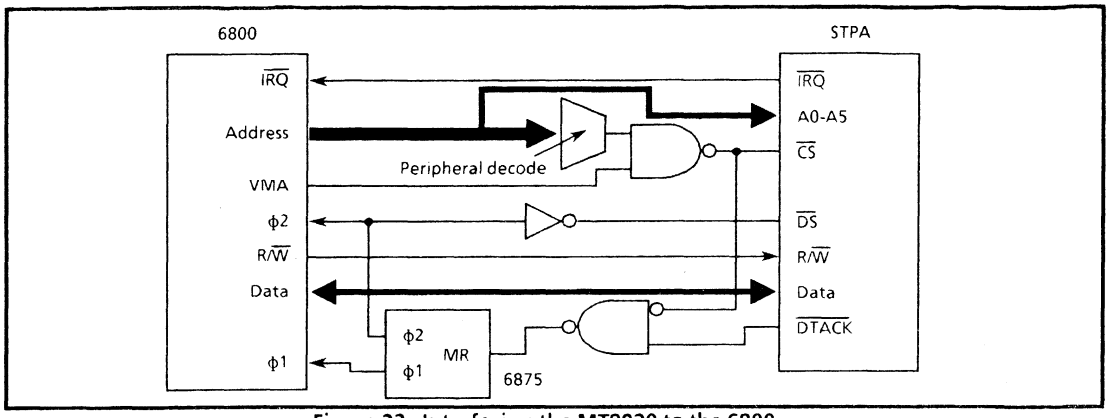


Figure 23 - Interfacing the MT8920 to the 6800.

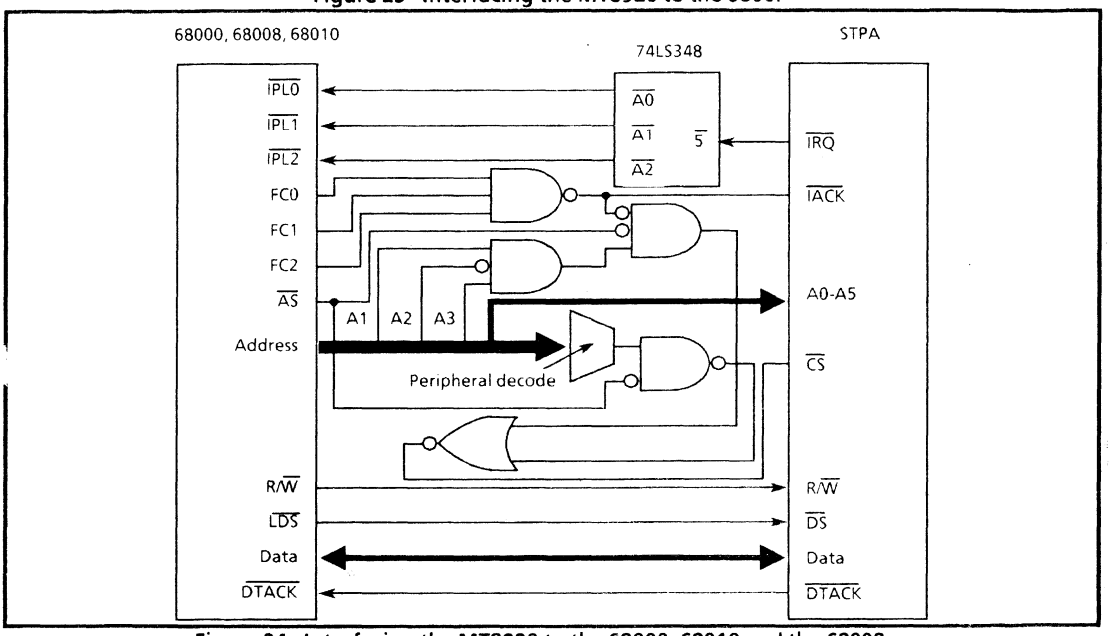


Figure 24 - Interfacing the MT8920 to the 68000, 68010 and the 68008.

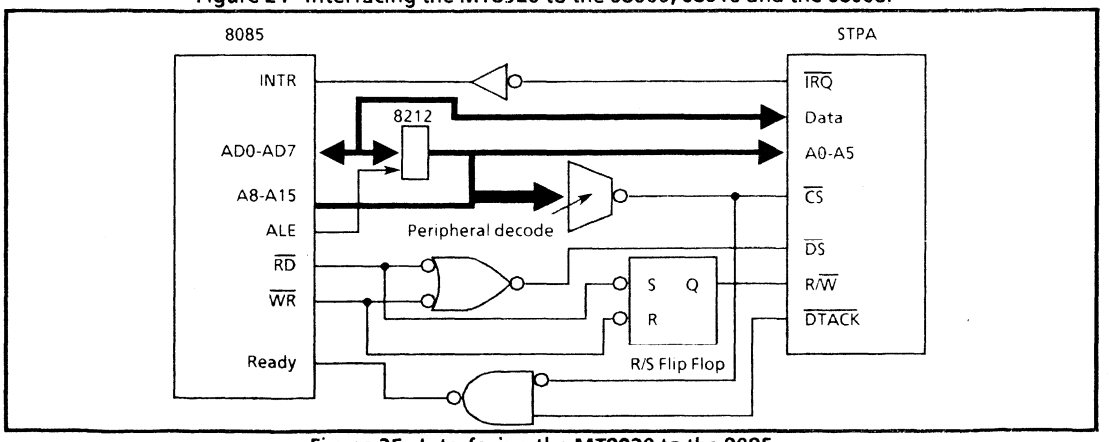


Figure 25 - Interfacing the MT8920 to the 8085.

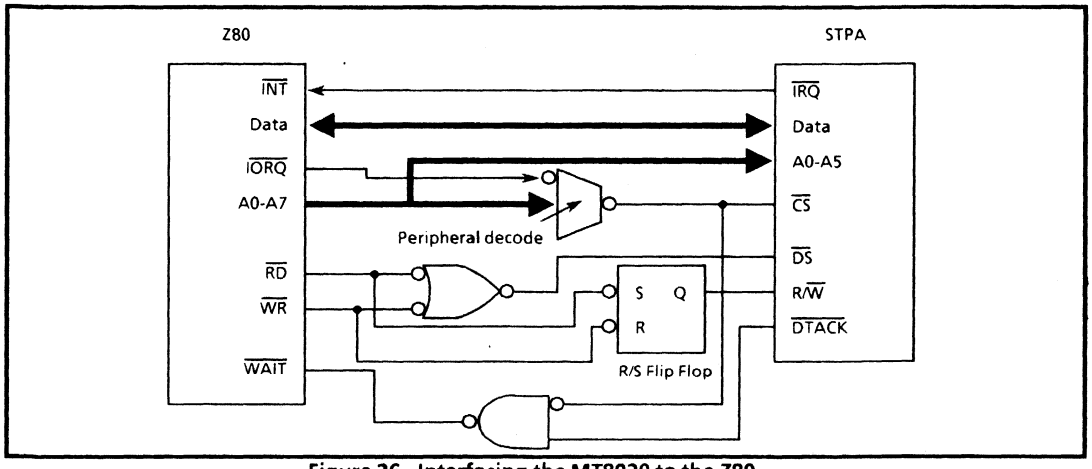


Figure 26 - Interfacing the MT8920 to the Z80.

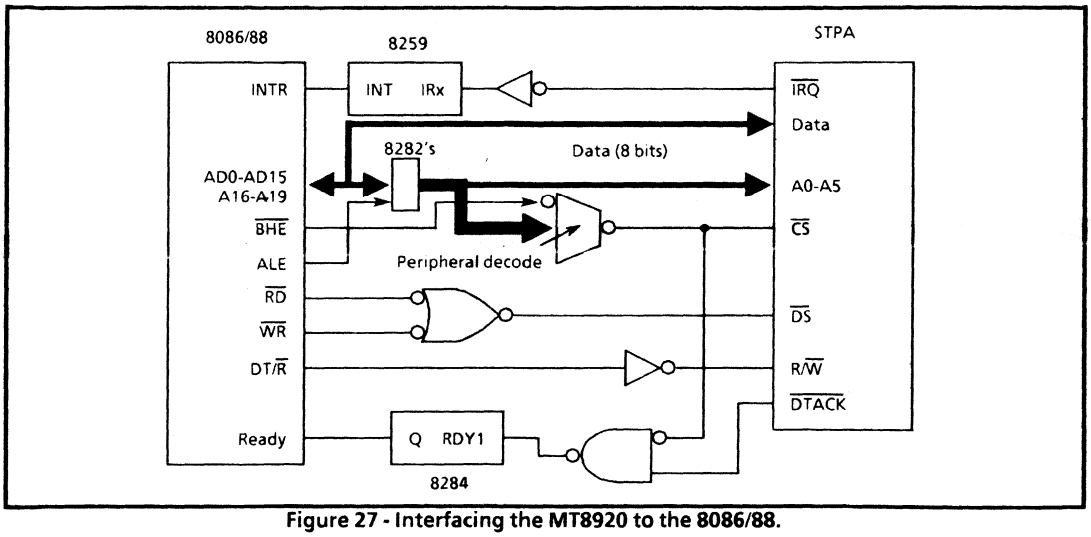


Figure 27 - Interfacing the MT8920 to the 8086/88.

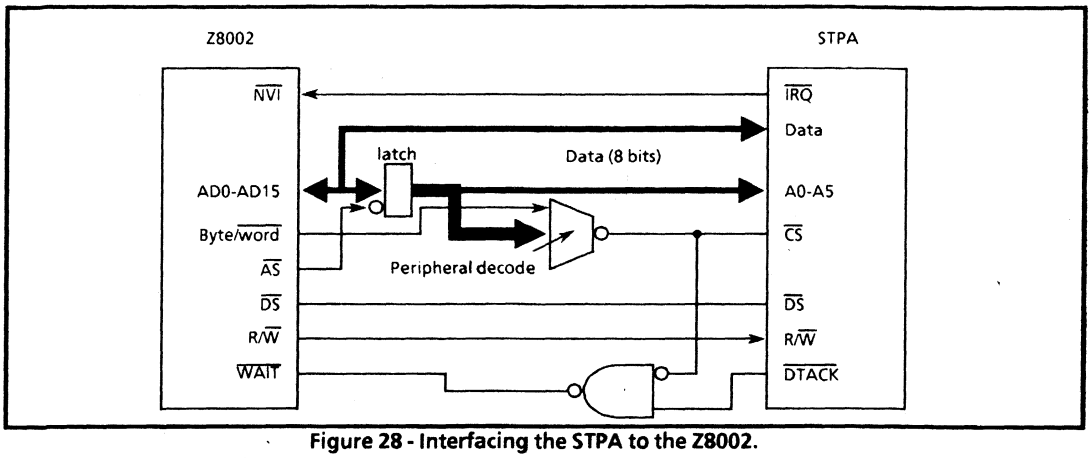


Figure 28 - Interfacing the STPA to the Z8002.

MITEL®

Applications Note **MSAN-120**

MT8880 DTMF Transceiver Applications

9161-001-003 NA ISSUE 1 JUNE 1986

Contents

1.0 Introduction

With voice grade telephone lines available globally coupled with the vigorous growth of personal computers and microprocessor based products, it comes as no surprise to see more of these products employing DTMF (Dual Tone Multi-Frequency) devices. Product designs requiring the use of a DTMF transmitter, receiver and microprocessor have also required a collection of various buffers, latches and counters. In addition automatic dialer applications (mobile radio and alternate common carrier access) require filters, latches and timers to monitor the wide range of supervisory tones currently in use in the telephone network. The Mitel MT8880 saves costly board space by applying innovative circuitry to effectively integrate the entire DTMF transceiver function. The MT8880 DTMF transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator employing a switched capacitor digital to analogue converter and automatic burst mode counters. A call progress mode is also available. A Motorola microprocessor interface is included allowing access to five internal

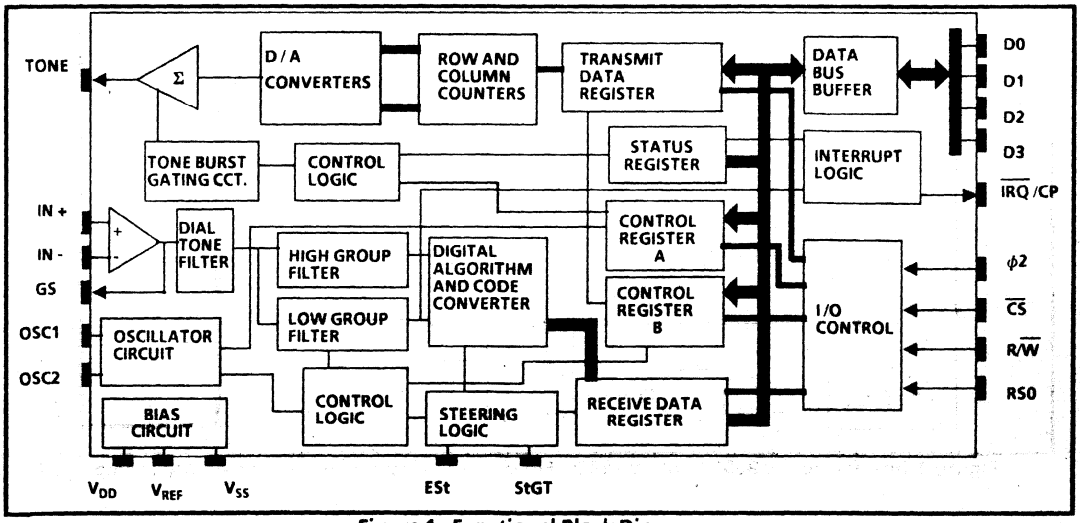


Figure 1. Functional Block Diagram

registers. Refer to the Mitel MT8880 data sheet for details.

2.0 Interface to a Microprocessor

2.1 INTEL 8051 Interface

The Intel 8051 is a microcomputer which can provide a cost effective solution for many controller applications. Very compact systems including autodialers, secure access modems, credit card verification and telemetry systems can be implemented with the MT8880 and the 8051.The circuitry shown in Figure 2 shows how the MT8880 and 8051 can be interfaced. The application outlined here uses the internal program memory on the 8051 and accesses the MT8880 via external data memory. By using external data memory the $\overline{RD}$ and $\overline{WR}$ pins (alternate functions of P3.7 and P3.6) are activated which can be used to generate the required Phase 2 clock and R/$\overline{W}$ signals on the MT8880. When external data memory is not being accessed there will be no activity on the $\overline{RD}$ and $\overline{WR}$ outputs, however, the MT8880 requires a clock input on the Phase 2 pin at all times. Activity is necessary to update the internal registers and provide interrupt signals used in servicing the DTMF receiver or transmitter functions. If the MT8880 is not being accessed, the frequency of the Phase 2 signal may be reduced. The recommended maximum Phase 2 period (when the MT8880 is not selected) is 2 ms. Durations longer than this may result in failure to produce an interrupt at the correct time or failure in updating the Status Register. Suitable activity for the Phase 2 input can be obtained by writing or reading to external data memory with attention given to the maximum Phase 2 period mentioned above. If external program memory is being used, this allows the output $\overline{PSEN}$ to be used as a source of activity suitable for the MT8880 Phase 2 input. The circuit shown in Figure 4 could be modified to make Phase 2 a function of $\overline{RD}$, $\overline{WR}$ and $\overline{PSEN}$. When external program memory is not being used, the 8051 internal timer can be used as a baud rate generator set up in mode 0. This mode sets up a baud rate which is 1/12 the oscillator frequency. The output is transmitted through TXD.

During the period when the MT8880 is being accessed (external data memory) the circuit shown in Figure 4 will provide proper timing. The $\overline{RD}$ and $\overline{WR}$ signals are NANDed and fed to the Reset input on RS latch 1 (see Figure 2). The output of RS latch 1 is connected to the phase 2 input of the MT8880. A $\overline{WR}$ signal from the

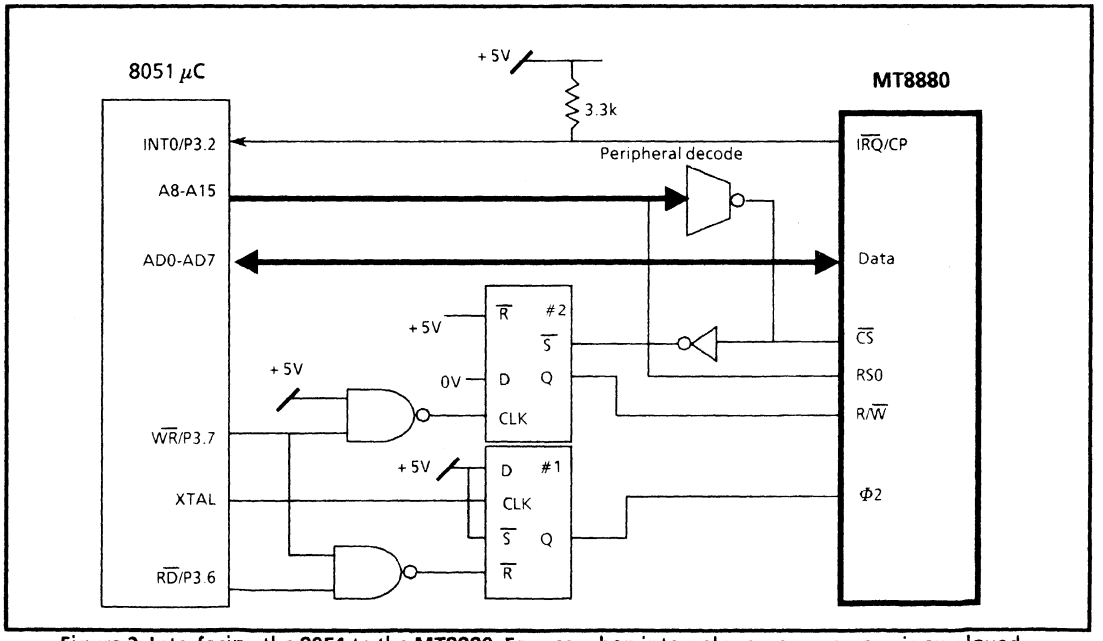


Figure 2. Interfacing the 8051 to the MT8880. For use when internal program memory is employed

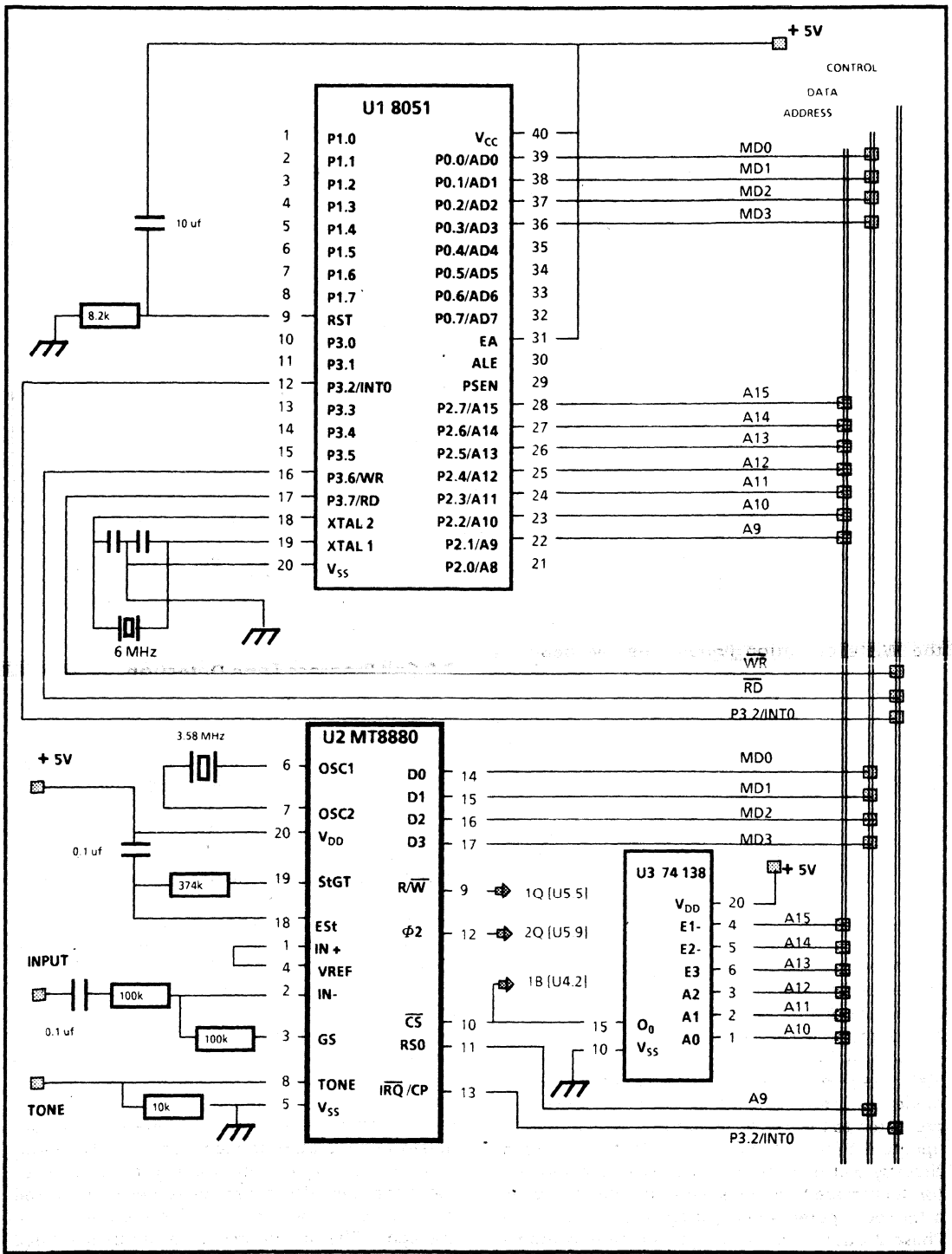


Figure 3. Mitel MT8880 to Intel 8051 Evaluation Circuit

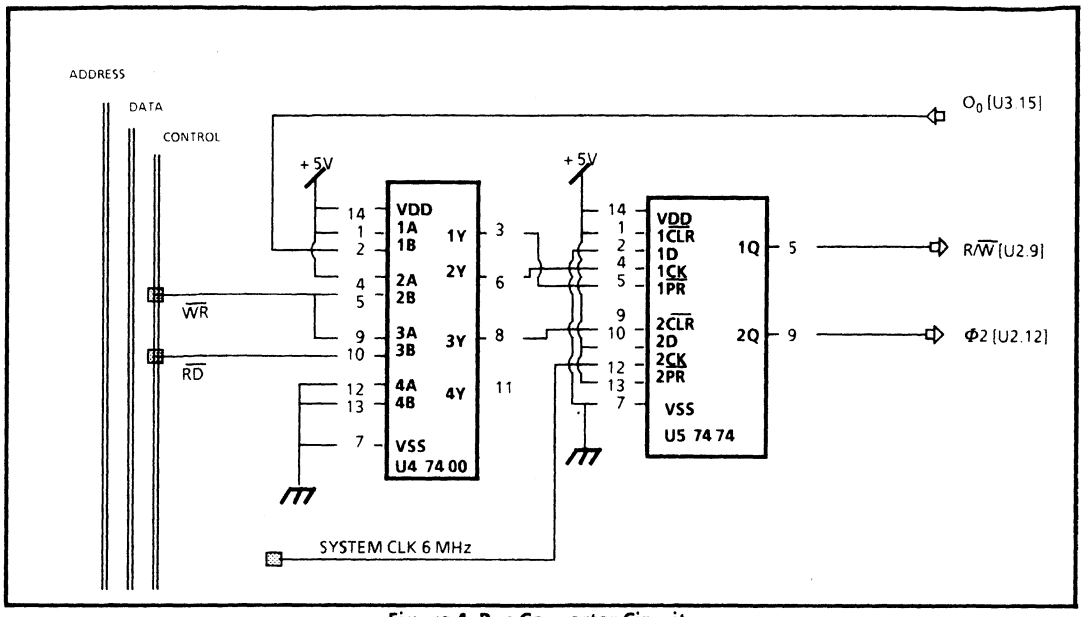


Figure 4. Bus Converter Circuit

8051 will set the output of latch 2 low inducing a Write condition at the MT8880 R/$\overline{W}$ input. Phase 2 will be asserted on the next rising edge of the system clock allowing suitable setup time. Following the Write operation (when the MT8880 is deselected), Phase 2 is reset to a logic low condition and the output of RS latch 2 (see Figure 2) will be set to a logic high which will induce a "read" condition. When accessing external memory the low byte of the address is time multiplexed with the data byte on port 0. However, in this application the low order address byte is not used and as such no demultiplexing circuitry is used. Note that EA must be tied high to execute instructions from the internal ROM.

2.2 MOTOROLA Interface

The MT8880 architecture is optimized for the Motorola 6802 bus structure. This implies the use of a Phase 2 signal to latch the control status, address and data from the microprocessor. The Phase 2 signal must be present at all times in order that the Status Register is updated. For example if Interrupt mode has been selected and DTMF frequencies are presented to the device, Phase 2 must be present to update the internal registers such that the interrupt circuitry will operate. This activity is also required for Burst mode transmit activity. In situations where a Microcomputer is being used where there is no Phase 2 output signal, a software timing loop is acceptable providing that the activity to the Phase 2 input is shorter than 2 ms during the period when no data transfers are taking place. Figures 6,7 and 8 show the recommended connections to Motorola microprocessors.

3.0 Call Progress Tone Detection

In addition to the MT8880's ability to simultaneously transmit and receive DTMF signals, a Call Progress detection mode is also available such that many call progress tones used internationally can be detected.

Call progress tones are signals which give information regarding the status of telephone calls to operators and customers. These tones are generally easy to interpret, however, the frequency content and level are not documented for all tones. Tones falling in the range 320 Hz to 510 Hz can be detected with the MT8880. A precise tone plan used in the No. 1/1A, 2/2B, 3 and 4 electronic switching systems (ESS) uses four pure tones of known amplitude. In the precise tone plan, tones can be issued in pairs or individually. Call progress tones are usually accompanied by an interruption rate or cadence such that the tone or tones are pulsed in an ON/OFF fashion. Table 3 lists various precise call progress tones and their associated cadence pattern. Note that the frequency of the call progress tone is not necessary for identification of the signal. The call progress tone can be identified in most cases by monitoring all frequencies in a

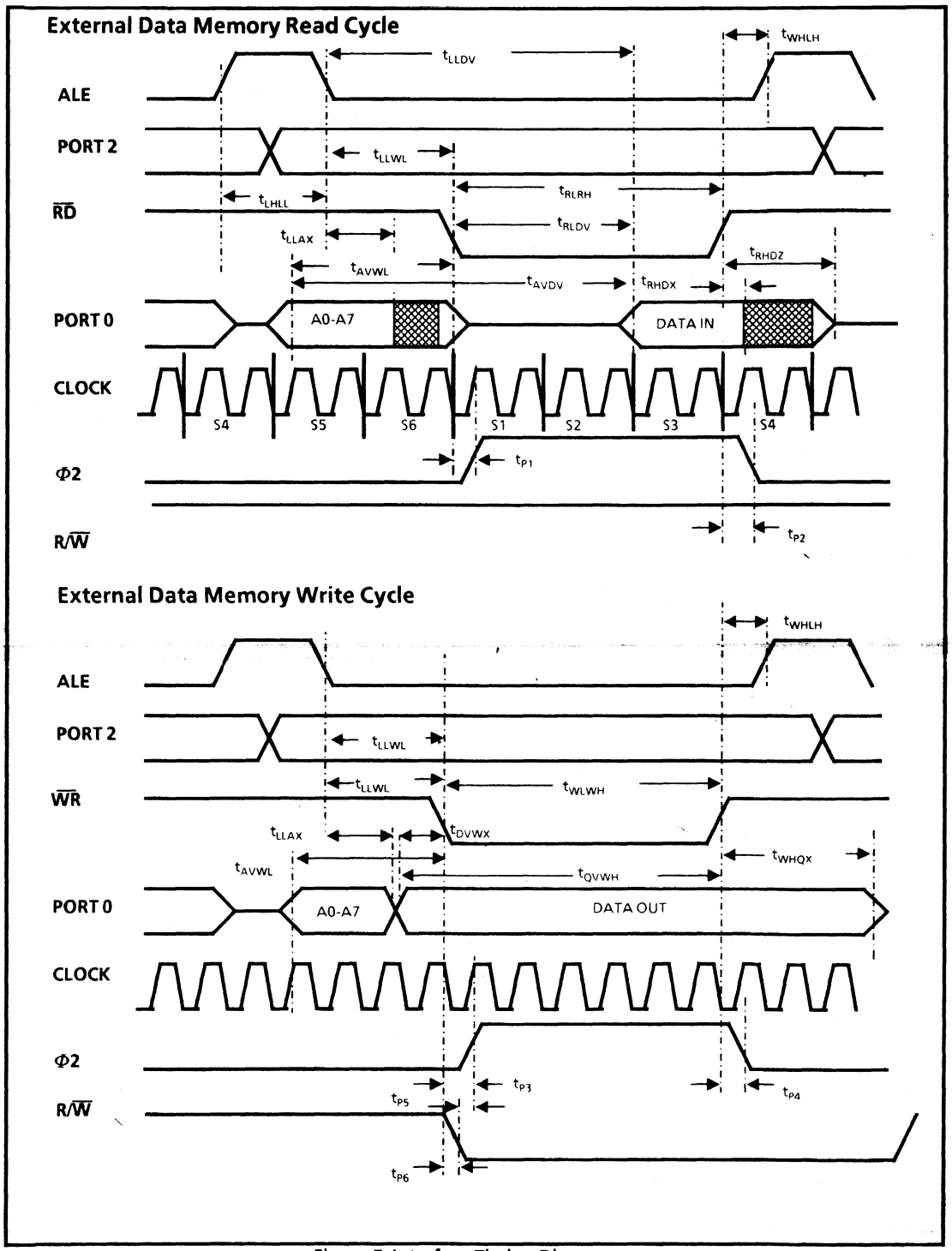


Figure 5. Interface Timing Diagrams

	Parameters	Symbol	Min	Max	Units
1	ALE pulse width	t_{LHLL}	295		ns
2	Read pulse width	t_{RLRH}	900		ns
3	Write pulse width	t_{WLWH}	900		ns
4	Address hold after ALE	t_{LLAX}	35		ns
5	Read to valid data in	t_{RLDV}		670	ns
6	Data hold after Read	t_{RHDX}	0		ns
7	Data float after Read	t_{RHDZ}		265	ns
8	ALE to valid data in	t_{LLDV}		1185	ns
9	Address to valid data in	t_{AVDV}		1335	ns
10	ALE to Write or Read	t_{LLWL}	450	550	ns
11	Address to Write or Read	t_{AVWL}	540		ns
12	Write or Read high to ALE high	t_{WHLH}	130	210	ns
13	Data valid to Write transition	t_{DVWX}	110		ns
14	Data setup before Write	t_{QVWH}	1020		ns
15	Data hold after Write	t_{WHQX}	120		ns
16	Address float after Read	t_{RLAZ}		0	ns
17	$\phi 2$ after $\overline{RD}$ or $\overline{WR}$	t_{P1}, t_{P3}	85		ns
18	R/$\overline{W}$ Setup before $\phi 2$	t_{P5}	65		ns
19	$\overline{WR}$ to R/$\overline{W}$	t_{P6}		20	ns
20	$\overline{\phi 2}$ after $\overline{RD}$, $\overline{WR}$	t_{P2}, t_{P4}		20	ns

Table 1. Bus Converter Timing (*Propagation times are calculated assuming a **6 MHz** clock.*)
These values have been extracted from data supplied by INTEL and Mitel does not guarantee the accuracy of this data.

Address (Hex)	R/$\overline{W}$	Description
20XX-21XX	0	Write to Transmit Data Register
20XX-21XX	1	Read from Receive Data Register
22XX-23XX	0	Write to Control Register A/B
22XX-23XX	1	Read Status Register

Table 2. MT8880 Address Map

specific bandwidth and identifying the cadence of the signal within the detect bandwidth.

3.1 Using The MT8880

The MT8880 call progress mode is selected using bit one in Control Register A (b1 = 1). When call progress mode is selected, the master clock frequency is divided by two such that the DTMF low group filter will provide a suitable bandpass. Note that only call progress signals will be detected in this mode and not DTMF signals. The filter output is used to drive a Schmitt trigger which has a fixed detection threshold level. The output from the schmitt trigger is internally switched to the $\overline{IRQ}$/CP output buffer when call progress mode is selected. Since the detection level is set quite low, noise on the power supply should be kept below 100 mV at the device. Excessive noise will result in random activity on the $\overline{IRQ}$/CP output. The output signal from the call progress circuitry is a rectangular waveform having the same frequency as the call progress input signal. The resultant output from the call progress circuit can be monitored by a general

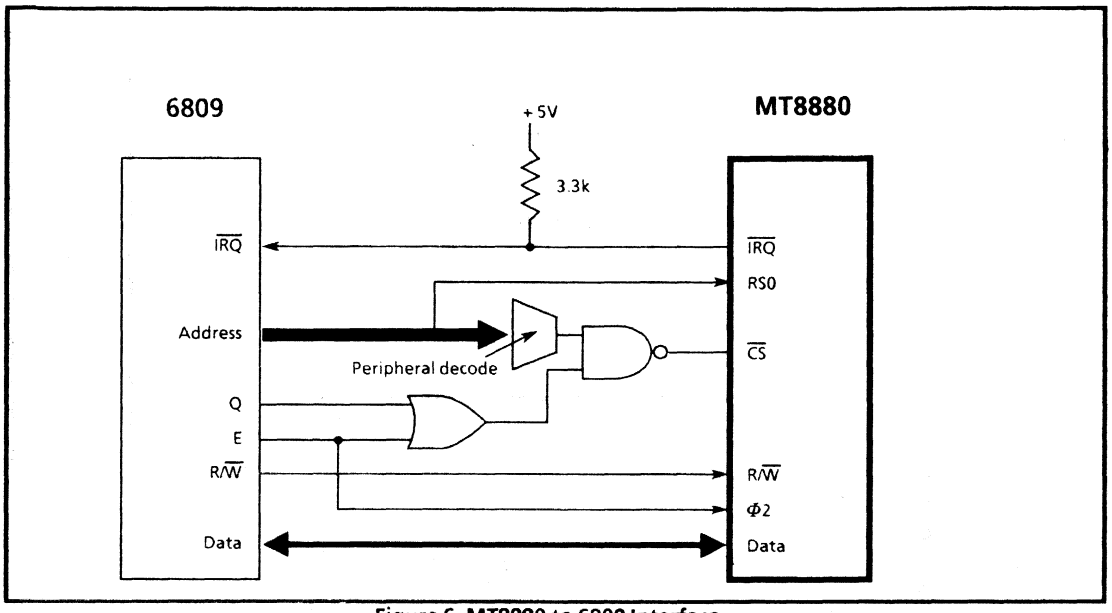


Figure 6. MT8880 to 6809 Interface

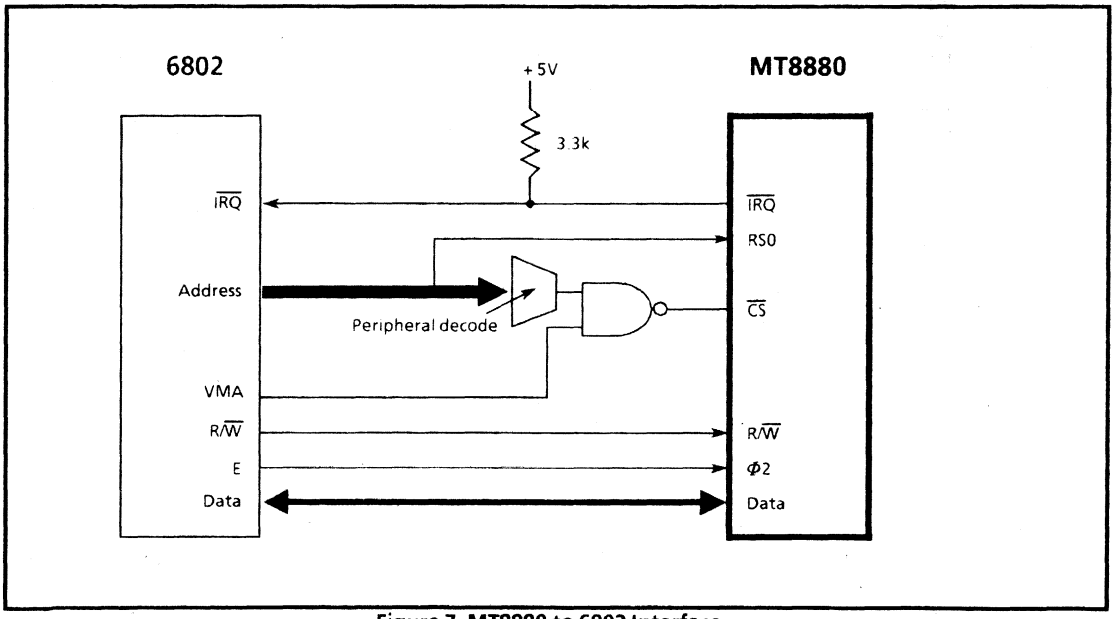


Figure 7. MT8880 to 6802 Interface

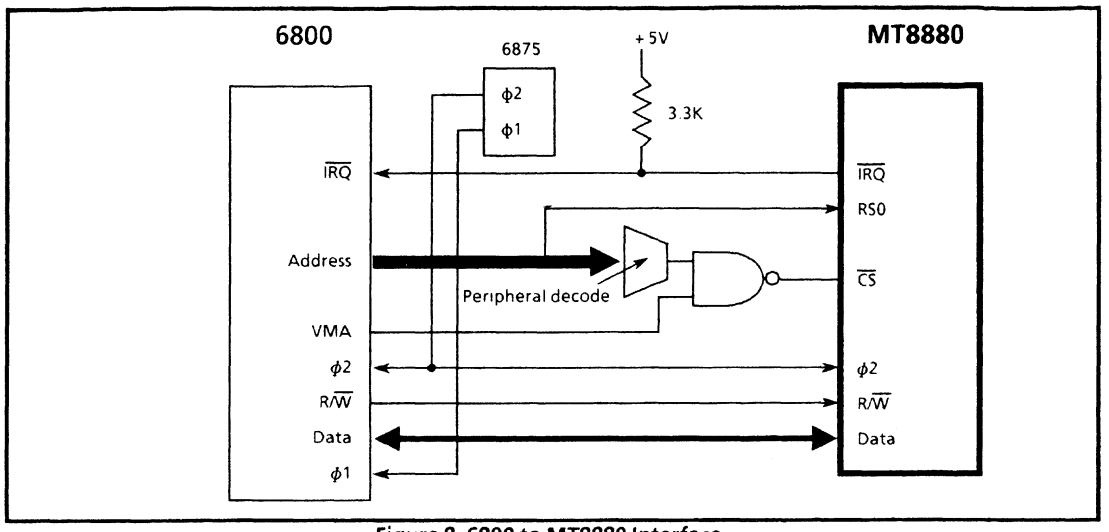


Figure 8. 6800 to MT8880 Interface

purpose I/O pin on a microcomputer. A software routine examines the frequency and the interruption rate of the rectangular wave such that the nature of the call progress tone is determined.

In a system where no I/O ports are available, as is the case in the microprocessor arrangements shown in Figures 6,7 and 8, a very simple solution exists. The call progress output can be used to drive the steering circuitry (tone verification circuity) normally used for DTMF which will update the Status Register already existing on chip. In a situation where call progress tones are being monitored, the Status Register is polled by the microprocessor. Bit three will indicate the interruption rate or cadence of the call progress signal. The circuit shown in Figure 9 illustrates the details concerning the interface between the $\overline{IRQ}$/CP output and the guard time steering input. Note that when call progress mode is selected, the $\overline{IRQ}$/CP output drives low and the 3k pullup resistor (normally used for interrupt) will pull high when there is a zero crossing induced by the call progress signal. Call progress signals are applied at the gain setting amplifier input and are affected by the gain setting resistors. A unity gain (which is normally used for DTMF applications) has been found to be adequate for call progress applications. Figure 8 shows a circuit which can be used to allow the MT8880 to monitor and identify call progress tones. The timing diagram in Figure 10 shows the waveforms associated with the call progress detection circuit. When Q1 turns ON (no Call Progress tone), ESt is forced high and will stay in the high state unless the tone present guard time has elapsed. The threshold voltage on U1 is set by the MT8880 V_{REF} output. The tone present guard time is determined by the time constant formed by R3 and C2 plus the time constant determined by R5 and C3. R3 and C2 determine the value for t_{GTA} in DTMF mode. The circuit shown in Figure 9 is transparent in DTMF operation. Timing is not adversly affected as a result of using the circuit since Q1 is high impedance when $\overline{IRQ}$/CP is high. Interrupts must be acknowledged within 100 ms (using the components shown) otherwise the St/GT pin will be forced high. The interrupt acknowledge time can be adjusted with C3 and R6 in Figure 9. A diode (D2) can be connected as shown in the diagram such that interrupts from other devices are ignored.

3.2 Call Progress Detection Program

The program shown in Appendix 1 was used in conjunction with the circuit shown in Figure 9 to provide a means of detecting the following call progress signals;

1) North American Dial Tone 350/440Hz, -13dBm
2) European dial tone 425 Hz, -6 dBm
3) Far East dial tone 400 Hz, -15 dBm
4) Busy tone 480/620 Hz, -24 dBm, 0.5 sec ON 0.5 sec OFF
5) Ring back tone 440/480 Hz, -24 dBm 2 sec ON 4 sec OFF

NAME	FREQUENCIES (Hz)	INTERRUPTION RATE	LEVEL	DESCRIPTION
DIAL TONE	350 + 440	STEADY	-13 dBm/frequency	Indicates that the receiving end is ready to receive dial pulse or DTMF signals.
AUDIBLE RINGBACK	440 + 480	2 sec. ON 4 sec. OFF	-19 dBm/frequency	Indicates that called line has been reached and that ringing has started.
LINE BUSY	480 + 620	0.5 sec. ON 0.5 sec. OFF	-24 dBm/frequency	Called customer's line has been reached but line is currently in use.
REORDER	480 + 620	0.25 sec. ON 0.25 sec. OFF	-24 dBm/frequency	Indicates that the local or toll switching transmission paths to the C.O. or equipment serving the customer are busy. May also indicate unassigned code.
PARTIAL DIAL TONE	480	STEADY	-17 dBm	Notifies calling party that dialing has not commenced in the preallotted time or that not enough digits have been dialed.
AUTOMATIC CREDIT CARD DIALING PROMPT TONE	941 + 1477 followed by 440 + 350	940 ms exponentially decayed from -10 dBm/freq. at a time constant = 200ms	-10 dBm/frequency	Informs the customer that credit card information must be keyed in.

Table 3. Various Call Progress Tones

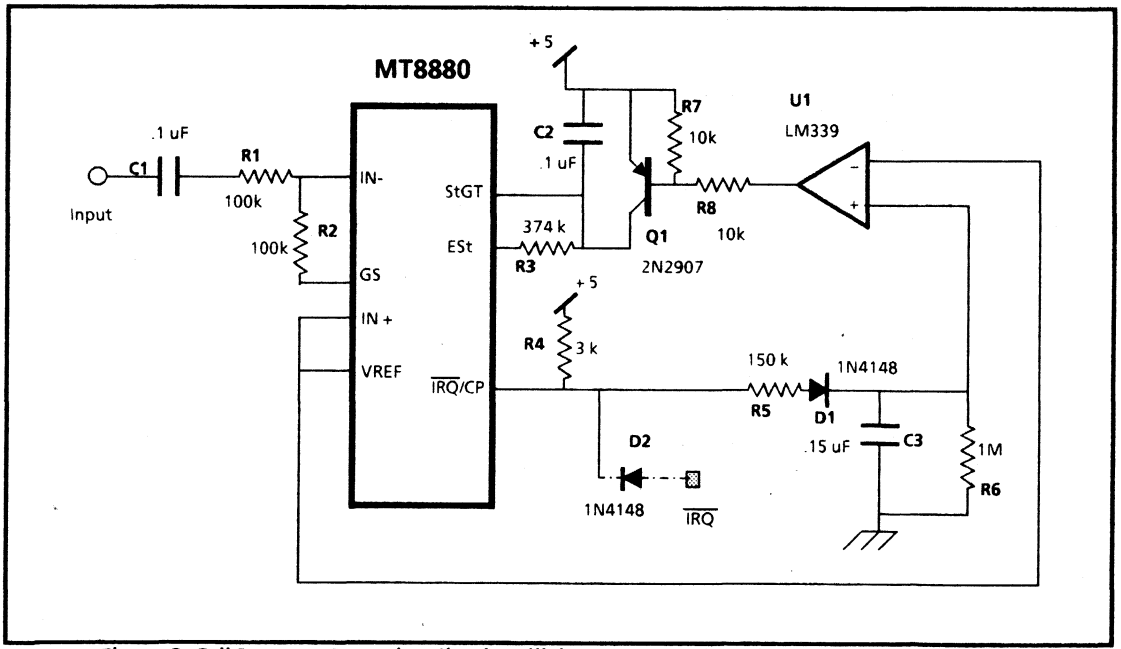


Figure 9. Call Progress Detection Circuit Utilizing Status Register for Cadence Verification

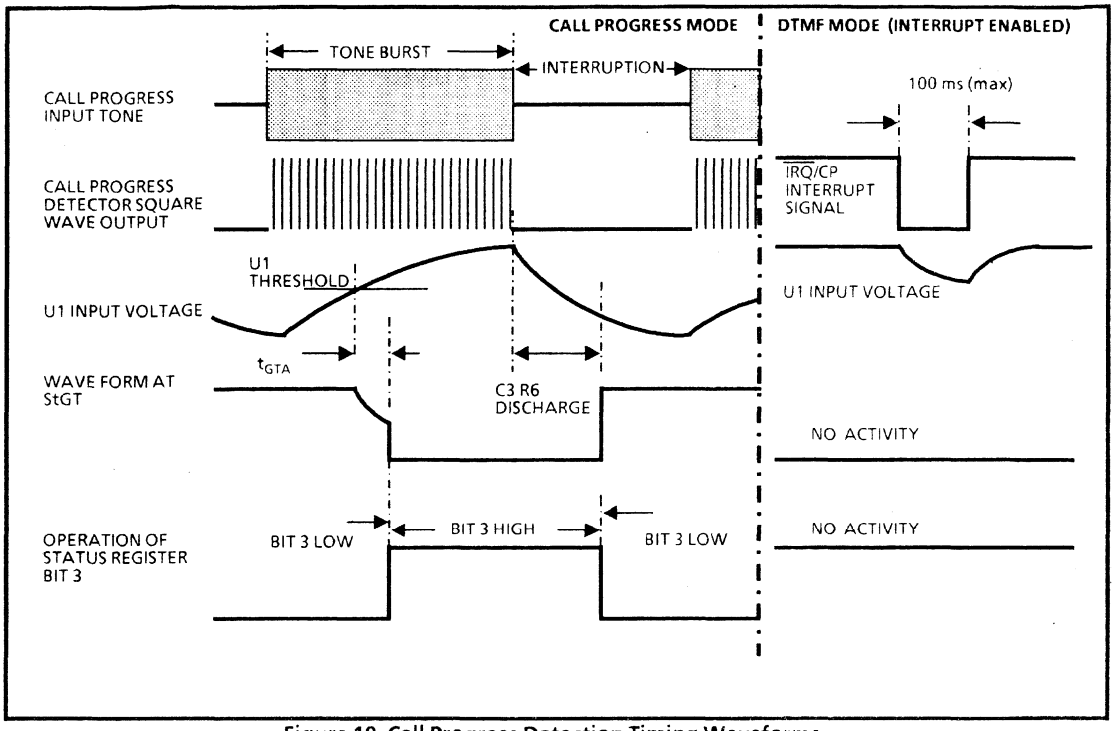


Figure 10. Call Progress Detection Timing Waveforms

6) Reorder tone 480/620 Hz -24 dBm, 0.2 sec ON 0.5 sec OFF

Also, the detection scheme correctly ignored the 850 Hz European dial tone second harmonic at -44 dBm. The detection program makes use of two software counters in real time and as such the values shown in the program for counter verification limits must be tailored for every system due to the different clock rates in various microprocessor systems. Counter one monitors the time that the tone was interrupted (tone absent) and counter two monitors the time the tone was present. The two resulting counts are compared against the upper and lower limits initially specified in the program. These limits were found experimentally by checking the average count and then assigning suitable tolerances. An error counter allows one error from each counter and an error from the tone identification register. Reference to the flowchart in Figure 11 will clarify details.

3.3 Voice Detection Using the MT8880

Voice signals can, in fact, be detected with the MT8880. The fact that voice signals are concentrated in the 500 Hz region (on the average), allows these signals to be detected using the Call Progress mode. A very useful application for this function is in telemarketing systems that must detect when the called party has answered. The fact that most people usually respond will the word "hello" or some other short response can be used as a criteria to indicate that the called party has gone off hook and is waiting for a response. The speech detection is accomplished in exactly the same way as other call progress tones with the only difference being the accept/reject limits in the detection algorithm. The detection algorithm shown in Appendix 1 incorporates the voice detection function and can correctly detect "hello" with a 90% success rate. A typical scenerio using this technique would involve; 1) check for dial tone, 2) auto-dial DTMF signals 3) monitor call progress tone 4) if a called party responds with "hello", send a prerecorded sales message 5) have the customer respond with DTMF codes 6) go to on hook status. 7) repeat for balance of mailing list.

4.0 Simple Telephone Line Interface

Many applications employing the MT8880 require an interface to the telephone line to provide access

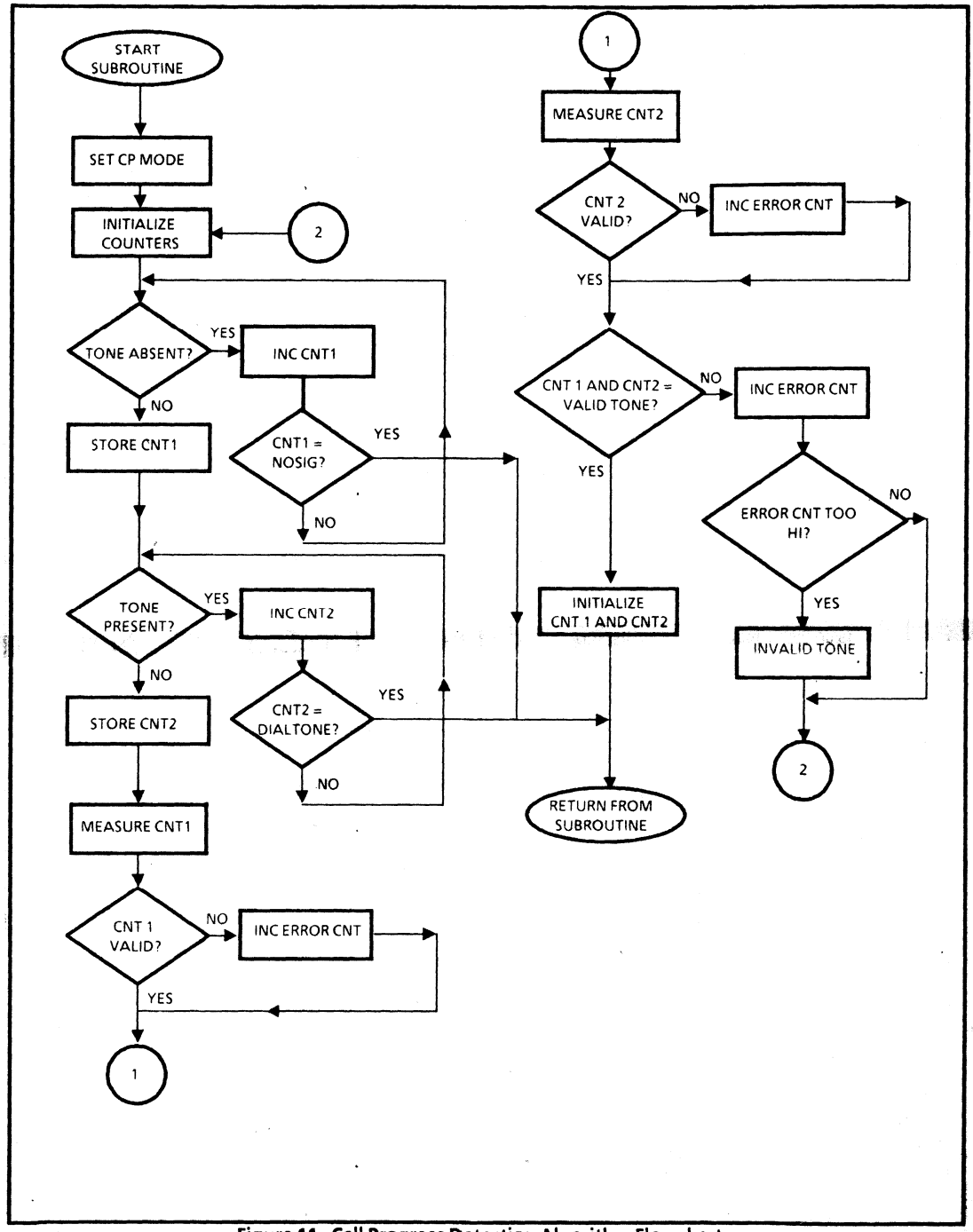


Figure 11. Call Progress Detection Algorithm Flowchart

to the outside world. Any system which connects to the telephone network must employ an FCC or DOC (in Canada) approved interface. FCC regulations allow the manufacturer to assume the responsibility of providing a protection and interface circuit commonly referred to as a data access arrangement (DAA). Historically, the manufacturer was not given this freedom and had to purchase a DAA from the telephone company. FCC Rules and Regulations part 68 provides a set of standards designed to protect the network from possible damage that could occur as a result of connecting terminal equipment. The DAA also protects equipment and personel from lightning and other transients. Provision must also be made to allow proper billing for connection time. Designers wishing more information on these regulations can refer to Volume X of FCC Rules and Regulations part 68: Connection of terminal equipment to the telephone network. A copy of the document can be obtained from the Government Printing Office, Washington, DC 20402: phone (202)-783-3238. Also another useful reference is Notes on the Network, Section 4, issued by AT&T Network Planning Division.

Although a DAA can be purchased seperately, the cost of such a device is usually quite high and is often single sourced. The circuit shown in Figure 12 is a DAA which is optimized for the MT8880 DTMF transceiver. Although the circuit shown has not gone through the FCC approval cycle, it should not require to many alterations to gain the necessary approval. The circuit provides transient protection, ringing detection, proper DC loop

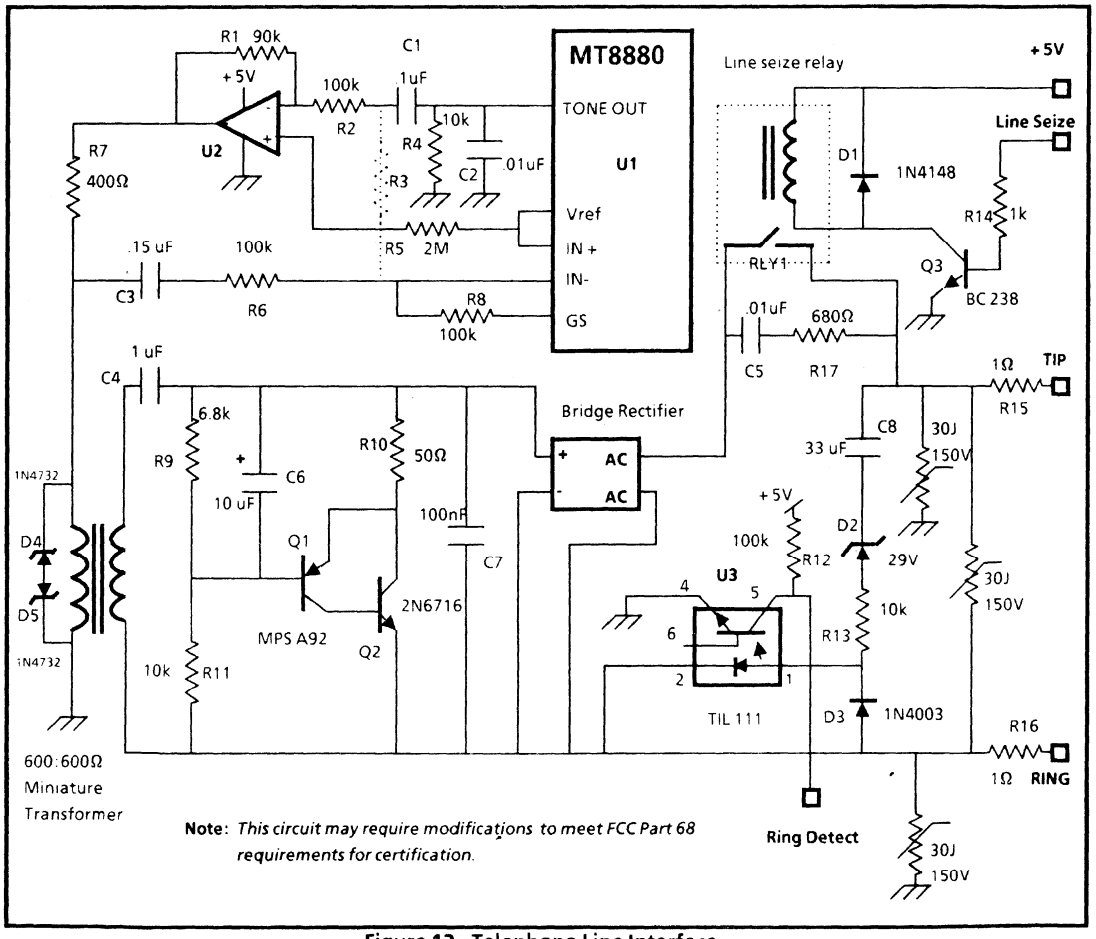


Figure 12. Telephone Line Interface

current, DC isolation and two to four wire conversion. A line seize relay allows on/off hook control and can be used for pulse dialing, if necessary. The two to four wire converter consisting of U2 and the the internal gain setting op-amp on the MT8880 allows DTMF signal transfer. The two to four wire converter shown allows half duplex DTMF signalling and is suitable for applications such as meter reading, building security, intelligent payphones and secure dial up computer ports.

The transmitted signal is coupled into the transformer and the DTMF input amplifier. Therefore, the applications software should simply ignore the Receive Data Register when the device is transmitting. The transformer used in the interface is a small low cost unit since the loop current is handled by Q2 and associated resistors. Since the MT8880 can simultaneously transmit and receive DTMF signals, an optional balancing resistor could be employed to cancel the transmit signal with the receive signal allowing full duplex DTMF signalling. This resistor is shown as R3 in Figure 12. The value of R3 depends on loop impedance and other component values.

4.1 Smart Ring Detect

Applications requiring the use of a ring detector can be enhanced by making use of the circuits in Figure 9 (Call Progress Detection Circuit) and Figure 12. The circuit in Figure 9 could be modified to allow the ring detector output (U3 in Figure 12) to trigger the Steering/Guard Time circuit normally used for the DTMF receiver. This would provide a means of detecting the presence of ringing voltage with the MT8880 (in Call Progress mode) by monitoring the state of bit 3 in the Status Register. A counter in the applications software could monitor the number of ring bursts and cause an off hook condition when a predetermined number of rings has been counted. Or, a specific ring cadence pattern could be detected which would be useful for party lines where every user has a specific ring pattern. Applications such as electronic answering systems, appliance control and electronic call diversion can all be enhanced with smart ring detection.

5.0 Design-In Summary

5.1 Non Burst Mode

Although the DTMF Transceiver has an innovative Transmit Burst Mode which produces DTMF bursts and pauses of predetermined duration, it is sometimes necessary to generate tone bursts of non-standard duration. This can easily be done by setting Non Burst mode using Control Register B (b0 = 1) and enabling or disabling the Tone Output pin using the Tone Output Enable bit in Control Register A. However, if the DTMF receiver is to operate with Interrupt mode enabled, a read from the Status Register must occur in the transmit counter loop. This is necessary such that if a DTMF signal is received causing an interupt to occur, the

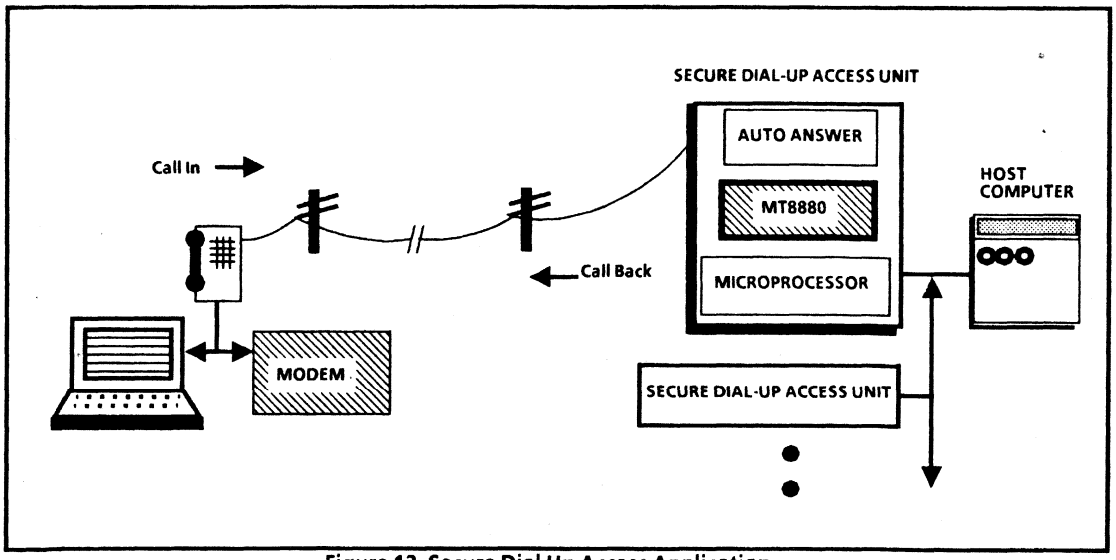


Figure 13. Secure Dial Up Access Application

interrupt is acknowleged. The receiver is then ready for new data. An example of this is shown in Appendix 2.

5.2 Clock Oscillator

The MT8880 employs an on chip oscillator circuit that is completed with the addition of a 3.5795 MHz crystal. Multiple devices can be driven with a single clock source by driving OSC 1 on all devices. The driver should be capacitively coupled through a 0.01 uf capacitor. Alternatively, the devices can be daisy chained (with limitations) such that the first device in the chain is the master oscillator.

5.3 Power Supply

Steps should be taken through the use of decoupling capacitors or other means to reduce power supply noise at the device. This is especially important in Call Progress mode since noise in excess of 100 mV p-p may cause random toggling on the $\overline{IRQ}$/CP output.

The Call Progress detect threshold is set to a level which is determined by the hysteresis on the Schmitt trigger used in the DTMF low group bandsplit filter. This level is quite low and is not adjustable. However, some adjustment can be obtained by altering the gain of the on chip op-amp.

5.4 Software Reset

A software reset is necessary on power up since the device may come up in an unknown state. The sequence is quite simple and should be used at the beginning of all programs.
Reset Sequence:

Write 00(hex) to CONTROL REGISTER
Write 00(hex) to CONTROL REGISTER
Write 08(hex) to CONTROL REGISTER
Write 00(hex) to CONTROL REGISTER

5.5 Use of Phase 2 (ϕ2) Input

The bus architecture is optimized for the MOTOROLA 6802 Microprocessor and as such requires a Phase 2 signal. This signal is not only necessary for data transfers but must also be present to update the Status Register. If data is not being transfered, the Phase 2 clock period can be increased to as long as 2 ms. A period longer than 2ms may result in lost data.

5.6 CP Mode to DTMF Mode Delay

The transition from Call Progress mode to DTMF mode requires a finite time determined partially by the filter circuitry. Applications that require DTMF signals to be received directly after exiting Call Progress mode, which could be the case for smart ring detection, require at least 10 ms when switching to DTMF mode to insure that no DTMF data is lost.

6.0 APPLICATIONS

6.1 Secure Dial-Up Port for Modems

There has been an increasing interest in providing additional protection for computer systems. There are certainly many aspects to consider in a total security system ranging from secure operating system techniques to secure data base management systems. A hardware oriented secure access system and the systems mentioned above can be combined to achieve a highly secure network. Hardware oriented secure access systems are becoming popular as a result of the increased use of microprocessor based computers to access networked systems through dial up telephone links. The Mitel MT8880 DTMF transceiver can serve as the heart of a call-back-telephone-access product which provides a high level of security.

A popular method for limiting access to a dial up port in the past has been to simply refrain from listing the telephone number. This action will certainly limit abuse of the computer to a certain degree but may introduce problems to personnel which should have access. However, for the person looking for a computer to abuse, it is a simple matter to dial sequential phone numbers and search for the modem carrier tone. At this point it is then possible to try passwords or attempt to get past encryption schemes. As more attempts are made, the probability of gaining access increases. A fairly recent scheme employs a call-back protocol whereby a unit connected between the modem (at the host end) and the telephone line automatically answers an incoming call without an acknowledgement tone. Alternatively, when the call is answered a false busy signal can be issued such that unauthorized persons will be led to believe that the line is in a busy condition. Whatever scheme is used, once the host has answered the call an access code is entered using DTMF signalling. Once a code has been entered, the secure access unit goes on hook. After matching the access code with a preprogrammed telephone number the call is returned at which time normal modem

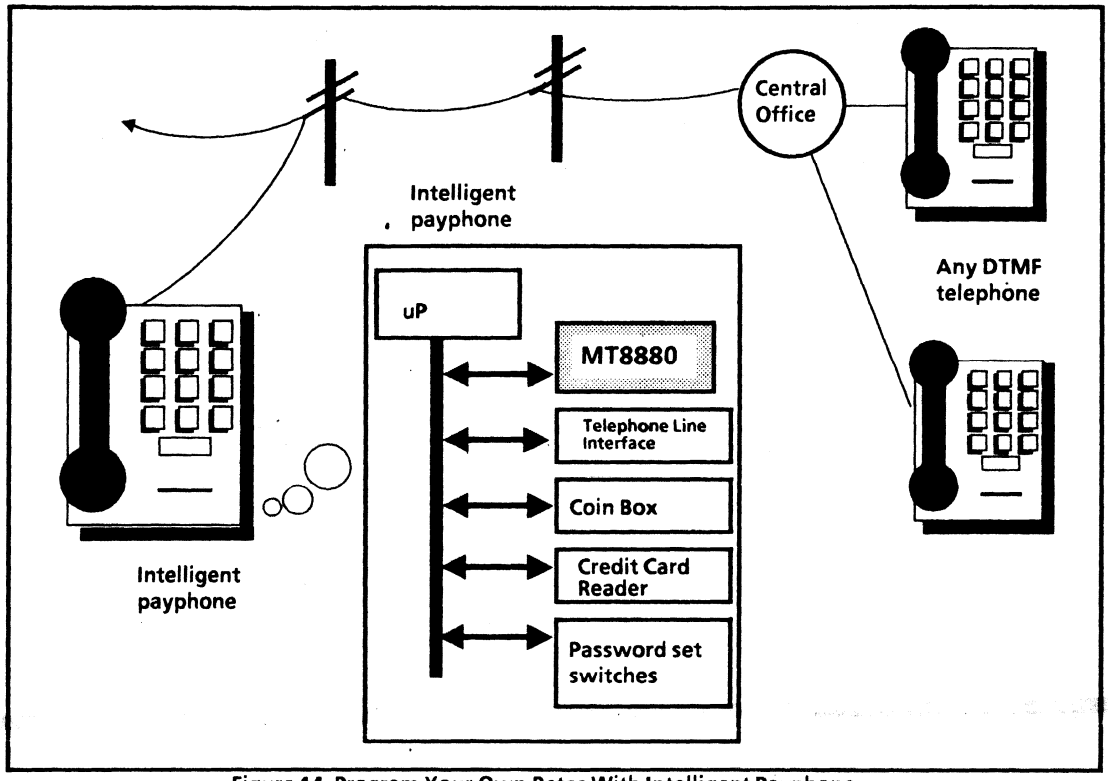


Figure 14. Program Your Own Rates With Intelligent Payphone

handshaking activity occurs followed by data transmission. A slightly different scheme which would allow the user to change locations at will involves the use of an encoded telephone number which is entered after the access code. The secure access unit decodes the telephone number and does a call back to that location. Attempts to gain access by unauthorized personnel could trigger an alarm condition such that the system operator would be notified and appropriate action taken. A data switch serving a large network could be fitted with a secure access unit at each dial up port providing a high level of security for sensitive data. Also, users of smaller networks such as those found in real estate or sales applications could benefit from added security. Figure 13 shows a typical arrangement.

6.2 Intelligent Payphone

Intelligent payphones can be installed in such places as variety or convenience stores, bowling alleys and other suitable locations and used as a source of income for the owner. Persons wanting to use the phone must deposit the fee as programmed by an authorized user. The MT8880 can play a key role in such an intelligent pay telephone system and is illustrated in Figure 14.

Any person having the phone number and password of a specific intelligent payphone can do such things as program the calling rates, check the amount of coin in the box or even check to see if the phone has been vandalized. An FCC approved data access arrangement must be used to connect the system to telephone lines with an automatic ring detect circuit answering incoming calls. Upon receiving an incoming call, the software could be set up such that the payphone issues a false ringback tone or busy tone to discourage unauthorized users. Personel with the password, however, could simply enter DTMF codes over the false call progress tones to gain access. Once the password has been correctly entered (from any DTMF phone) commands can then be entered.

APPENDIX 1
Call Progress and Voice Detection Algorithm

```
1                *
2                * THIS PROGRAM PROVIDES AN ALGORITHM TO CHECK THE
3                * CADENCE OF CALL PROGRESS SIGNALS. THE CALL PROGRESS DETECT CIRCUIT
4                * MUST BE USED. THE CIRCUIT UTILIZES A CHARGE PUMP WHICH FEEDS INTO
5                * THE ANALOG GUARD TIME CIRCUIT NORMALLY USED FOR DTMF. WHEN IN
6                * DTMF MODE, TRANSISTOR Q1 IS IN A HIGH IMPEDANCE STATE
7                * THUS NOT AFFECTING THE NORMAL OPERATION OF THE GUARD TIME CIRCUIT.
8                * IF OPERATING IN INTERRUPT MODE IRQ/CP IS NORMALLY HIGH, HOWEVER
9                * INTERRUPTS MUST BE SERVICED WITHIN 200MS OR THE DTMF TIMING WILL BE
10               * TEMPORARILY CORRUPTED. THIS INTERRUPT SERVICE TIME CAN BE ADJUSTED
11               * WITH C3 AND R6.
12               * IN PRACTICE THE STATUS REGISTER (BIT 3) IS POLLED LOOKING FOR THE
13               * CONDITION OF BIT 3. THIS PROGRAM HAS TWO COUNTERS. COUNTER 1 DETERMINES
14               * HOW LONG THERE IS AN ABSENCE OF ENERGY IN THE PASSBAND AND COUNTER 2
15               * DETERMINES HOW LONG THERE IS A PRESENCE OF ENERGY IN THE PASSBAND.
16               * AN ERROR COUNTER ALLOWS ERRORS FROM THE SIGNAL ABSENT AND SIGNAL PRESENT
17               * COUNTERS IN ADDITION TO THE COUNT MATCH REGISTER.
18               * THE RESULT OF THE DETECT ALGORITHM IS PRINTED ON THE CRT
19               * ALSO, A FORM SPEECH DETECTION ALGORITHM INDICATES WHEN THE WORD 'HELLO'
20               * HAS BEEN RECEIVED AT THE INPUT OF THE MT8880.
21               *
22   4400        START EQU $4400
23   2000        TXRX EQU $2000
24   2001        CRSR EQU $2001
25   8662        CRLF EQU $8662
26   867B        HEX4 EQU $867B
27   8655        HEAD EQU $8655
28   8686        HEX2 EQU $8686
29   866E        SPACE2 EQU $866E
30               *                    M.J.R. MAR 1986
31               * CPVREF.LST
32   4400        ORG START
33               *
34               * PROGRESS TONE IDENTIFIER DATA
35               *
36   4400 A  86  00    LDAA #$00
37   4402 A  B7  479D STAA REORDR ; TONE 1 REORDER TONE
38   4405 A  86  01    LDAA #$01
39   4407 A  B7  479C STAA RNGBK ; TONE 2 RINGBACK TONE
40   440A A  86  02    LDAA #$02
41   440C A  B7  479B STAA BUSY ; TONE 3 BUSY TONE
42   440F A  86  03    LDAA #$03
43   4411 A  B7  479E STAA DIALTN ; TONE 4 DIAL TONE
44   4414 A  86  04    LDAA #$04
45   4416 A  B7  479F STAA NOTONE ; TONE 5 NO SIGNAL
46   4419 A  86  05    LDAA #$05
47   441B A  B7  47A0 STAA HELLO ; TONE 6 HELLO
48               *
49               * ERROR COUNT
50               *
51   441E A  C6  04    LDAB #$04
```

```
52    4420 A  B7  47A3 STAA ERRCNT
53            *
54            * TONE IDENTIFIERS
55            *
56    4423 A  CE  0000 LDX #$0000
57    4426 A  FF  47A8 STX REORDX
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 2

```
1     4429 A  CE  0101 LDX #$0101
2     442C A  FF  47A6 STX RNGBKX
3     442F A  CE  0002 LDX #$0002
4     4432 A  FF  47A4 STX BUSYX
5     4435 A  CE  0303 LDX #$0303
6     4438 A  FF  47AA STX DIALX
7     443B A  CE  0404 LDX #$0404
8     443E A  FF  47AC STX NOTONX
9     4441 A  CE  0505 LDX #$0505
10    4444 A  FF  47AE STX HELLOX
11            *       TONE 1 PRESENT LIMITS
12            *
13    4447 A  CE  0400 LDX #$0900 ;LOWER LIMIT
14    444A A  FF  4848 STX TLO1LL
15    444D A  CE  04FF LDX #$0AFF ;UPPER LIMIT
16    4450 A  FF  484A STX TLO1UL
17            *
18            *       TONE 1 ABSENT LIMITS
19            *
20    4453 A  CE  0A00 LDX #$0500 ;LOWER LIMIT
21    4456 A  FF  484C STX THI1LL
22    4459 A  CE  0C00 LDX #$0600 ;UPPER LIMIT
23    445C A  FF  484E STX THI1UL
24            *
25            *       TONE 2 PRESENT LIMITS
26            *
27    445F A  CE  6D00 LDX #$7200 ;LOWER LIMIT
28    4462 A  FF  4850 STX TLO2LL
29    4465 A  CE  6EFF LDX #$74FF ;UPPER LIMIT
30    4468 A  FF  4852 STX TLO2UL
31            *
32            *       TONE 2 ABSENT LIMITS
33            *
34    446B A  CE  4050 LDX #$3B00 ;LOWER LIMIT
35    446E A  FF  4854 STX THI2LL
36    4471 A  CE  4255 LDX #$3DFF ;UPPER LIMIT
37    4474 A  FF  4856 STX THI2UL
38            *       TONE 3 PRESENT LIMITS
39            *
40    4477 A  CE  0400 LDX #$0900 ;LOWER LIMIT
41    447A A  FF  4858 STX TLO3LL
42    447D A  CE  04FF LDX #$0AFF ;UPPER LIMIT
43    4480 A  FF  485A STX TLO3UL
44            *
45            *       TONE 3 ABSENT LIMITS
46            *
47    4483 A  CE  13A0 LDX #$0E00;LOWER LIMIT
```

```
 48    4486 A  FF  485C      STX THI3LL
 49    4489 A  CE  1460 LDX #$0F20 ;UPPER LIMIT
 50    448C A  FF  485E STX THI3UL
 51            *
 52            *       TONE 4 PRESENT LIMITS
 53            *
 54    448F A  CE  5000 LDX #$5000 ;LOWER LIMIT
 55    4492 A  FF  4860 STX THI4LL
 56    4495 A  CE  5010 LDX #$5010 ;UPPER LIMIT
 57    4498 A  FF  4862 STX THI4UL

MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 3
  1           *
  2           *       NOTONE 5  SIGNAL ABSENT LIMITS

  3           *
  4    449B A  CE  9000 LDX #$9000
  5    449E A  FF  4864 STX TLO5LL
  6    44A1 A  CE  9010 LDX #$9010
  7    44A4 A  FF  4866 STX TLO5UL
  8           *
  9           *
 10           *       HELLO 6  SIGNAL PRESENT LIMIT
 11           *
 12    44A7 A  CE  05BA LDX #$05BA ;TONE 6 LOWER LIMIT
 13    44AA A  FF  486C STX THI6LL
 14    44AD A  CE  0CFF LDX #$08FF ;TONE 6 UPPER LIMIT
 15    44B0 A  FF  486E STX THI6UL
 16           *
 17           *
 18           *       HELLO 6 SIGNAL ABSENT LIMIT
 19           *
 20    44B3 A  CE  1000 LDX #$1000 ; TONE 6 LOWER LIMIT
 21    44B6 A  FF  4868 STX TLO6LL
 22    44B9 A  CE  8000 LDX #$8000 ; TONE 6 UPPER LIMIT
 23    44BC A  FF  486A STX TLO6UL
 24           *
 25           * RESET
 26           *
 27    44BF A  86  00    LDAA #$00
 28    44C1 A  B7  2001 STAA CRSR
 29    44C4 A  B7  2001 STAA CRSR
 30    44C7 A  86  08    LDAA #$08
 31    44C9 A  B7  2001 STAA CRSR
 32    44CC A  86  00    LDAA #$00
 33    44CE A  B7  2001 STAA CRSR
 34           *
 35           * CALL PROGRESS MODE WITH IRQ ENABLED
 36           *
 37    44D1 A  86  06    LDAA #$06
 38    44D3 A  B7  2001 STAA CRSR
 39           *
 40           * MAIN PROGRAM
 41           *
 42    44D6 A  BD  44FA JSR RESET
 43    44D9 A  BD  4516 JSR CHECB3
```

```
44    44DC A  BD   4536 JSR PRIME
45    44DF A  BD   452C MORINC JSR MORB3
46    44E2 A  BD   4516 JSR CHECB3
47    44E5 A  BD   45B3 JSR MEASLO
48    44E8 A  BD   4548 JSR MEASHI
49    44EB A  BD   4621 JSR MATCH
50    44EE A  BD   4689 JSR CHERR
51    44F1 A  BD   469F JSR PRINT
52    44F4 A  BD   4536 JSR PRIME
53    44F7 A  7E   44DF JMP MORINC
54            *
55    44FA A  CE   0000RESET LDX #$0000
56    44FD A  FF   4844 STX CNT1
57    4500 A  FF   4846 STX CNT2
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 4

```
1             *
2             * SET ERROR COUNTER
3             *
4     4503 A  F6   47A3 LDAB ERRCNT
5     4506 A  F7   47A1 STAB MATERR
6     4509 A  39        RTS
7             *
8             * START OF DETECT ALGORITHM
9             * COUNTER 1 CHECKS TO SEE HOW LONG
10            * BIT 3 IS HI (ABSENCE OF SIGNAL)
11            *
12    450A A  FE   4844INCCNT LDX CNT1
13    450D A  08   INX
14    450E A  FF   4844 STX CNT1
15    4511 A  BC   4862 CPX THI4UL
16    4514 A  22   32   BHI MEASHI
17            *
18    4516 A  F6   2001CHECB3 LDAB CRSR
19    4519 A  C4   08   ANDB #$08
20    451B A  C1   08   CMPB #$08
21    451D A  27   EB   BEQ INCCNT
22    451F A  39        RTS
23            *
24            *
25            *
26            * COUNTER 2 CHECKS TO SEE HOW LONG ENERGY IS PRESENT
27            *
28    4520 A  FE   4846MORCNT LDX CNT2
29    4523 A  08   INX
30    4524 A  FF   4846 STX CNT2
31    4527 A  BC   4866 CPX TLO5UL
32    452A A  22   1A   BHI PATCH1
33            *
34    452C A  B6   2001MORB3 LDAA CRSR
35    452F A  84   08   ANDA #$08
36    4531 A  81   08   CMPA #$08
37    4533 A  26   EB   BNE MORCNT
38    4535 A  39        RTS
39            *
```

```
40    4536 A  CE  0000PRIME LDX #$0000
41    4539 A  FF  4844 STX CNT1
42    453C A  FF  4846 STX CNT2
43    453F A  CE  FFFF LDX #$FFFF
44    4542 A  FF  4842 STX MATCHA
45    4545 A  39       RTS
46            *
47            *
48    4546 A  20  6B   PATCH1 BRA MEASLO
49            *
50            * COMPARE THE LOWER LIMIT AND UPPER LIMIT TO CNT1 WHICH
51            * CONTAINS THE TIME THE PROGRESS TONE WAS PRESENT
52            *
53    4548 A  FE  4844MEASHI LDX CNT1
54            *
55    454B A  BD  867B JSR HEX4
56            *
57    454E A  FE  4844 LDX CNT1
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 5

```
1     4551 A  BC  484C CPX THI1LL
2     4554 A  22  17   BHI CHH1UL
3     4556 A  BC  4854TH2LL CPX THI2LL
4     4559 A  22  1A   BHI CHH2UL
5     455B A  BC  485C TH3LL CPX THI3LL
6     455E A  22  1D   BHI CHH3UL
7     4560 A  BC  4860TH4LL CPX THI4LL ;ONLY CHECK THE LOWER LIMIT TONE PRESENT FOR DIALTONE
8     4563 A  22  3D   BHI T4HIID
9     4565 A  BC  486C TH6LL CPX THI6LL
10    4568 A  22  1B   BHI CHH6UL
11    456A A  7E  4676 JMP NONID
12            *
13    456D A  BC  484ECHH1UL CPX THI1UL
14    4570 A  23  1B   BLS T1HIID
15    4572 A  7E  4556 JMP TH2LL
16    4575 A  BC  4856CHH2UL CPX THI2UL
17    4578 A  23  1A   BLS T2HIID
18457A A  7E  455B JMP TH3LL
19    457D A  BC  485ECHH3UL CPX THI3UL
20    4580 A  23  19   BLS T3HIID
21    4582 A  7E  4560 JMP TH4LL
22    4585 A  BC  486ECHH6UL CPX THI6UL
23    4588 A  23  22   BLS T6HIID
24    458A A  7E  4676 JMP NONID
25            *
26            * IDENTIFY THE MEASURED VALUE
27            *
28    458D A  B6  479D T1HIID LDAA REORDR
29    4590 A  B7  4843 STAA MATCHB
30    4593 A  39       RTS
31            *
32    4594 A  B6  479C T2HIID LDAA RNGBK
33    4597 A  B7  4843 STAA MATCHB
34    459A A  39       RTS
35            *
```

```
36   459B A  B6  479B T3HIID LDAA BUSY
37   459E A  B7  4843STAA MATCHB
38   45A1 A  39       RTS
39           *
40   45A2 A  B6  479ET4HIID LDAA DIALTN
41   45A5 A  B7  4842 STAA MATCHA
42   45A8 A  B7  4843 STAA MATCHB ;STORE IN MATCHA AND MATCHB SINCE ONLY CHECKING PRESENT TIME
43   45AB A  39       RTS
44           *
45   45AC A  B6  47A0  T6HIID LDAA HELLO
46   45AF A  B7  4843 STAA MATCHB
47   45B2 A  39       RTS
48           *
49           * COMPARE THE LOWER LIMIT AND UPPER LIMIT TO CNT2
50           * WHICH CONTAINS THE TIME THE PROGRESS TONE WAS ABSENT
51           *
52   45B3 A  FE  4846MEASLO LDX CNT2
53           *
54   45B6 A  BD  867B JSR HEX4
55   45B9 A  BD  866E JSR SPACE2
56           *
57   45BC A  FE  4846 LDX CNT2
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 6

```
1    45BF A  BC  4848 CPX TLO1LL
2    45C2 A  22  17   BHI CHL1UL
3    45C4 A  BC  4850TL2LL CPX TLO2LL
4    45C7 A  22  1A   BHI CHL2UL
5    45C9 A  BC  4858TL3LL CPX TLO3LL
6    45CC A  22  1D   BHI CHL3UL
7    45CE A  BC  4864TL5LL CPX TLO5LL
8    45D1 A  22  3D   BHI T5LOID
9    45D3 A  BC  4868TL6LL CPX TLO6LL
10   45D6 A  22  1B   BHI CHL6UL
11   45D8 A  7E  4676 JMP NONID
12           *
13   45DB A  BC  484A CHL1UL CPX TLO1UL
14   45DE A  23  1B   BLS T1LOID
15   45E0 A  7E  45C4 JMP TL2LL
16   45E3 A  BC  4852CHL2UL CPX TLO2UL
17   45E6 A  23  1A   BLS T2LOID
18   45E8 A  7E  45C9 JMP TL3LL
19   45EB A  BC  485A CHL3UL CPX TLO3UL
20   45EE A  23  19   BLS T3LOID
21   45F0 A  7E  45CE JMP TL5LL
22   45F3 A  BC  486A CHL6UL CPX TLO6UL
23   45F6 A  23  22   BLS T6LOID
24   45F8 A  7E  4676 JMP NONID
25           *
26           * IDENTIFY THE MEASURED VALUE
27           *
28   45FB A  B6  479D T1LOID LDAA REORDR
29   45FE A  B7  4842 STAA MATCHA
30   4601 A  39       RTS
31           *
```

```
32    4602 A  B6  479C T2LOID LDAA RNGBK
33    4605 A  B7  4842 STAA MATCHA
34    4608 A  39        RTS
35            *
36    4609 A  B6  479B T3LOID LDAA BUSY
37    460C A  B7  4842 STAA MATCHA
38    460F A  39        RTS
39            *
40    4610 A  B6  479FT5LOID LDAA NOTONE
41    4613 A  B7  4842STAA MATCHA
42    4616 A  B7  4843STAA MATCHB
43    4619 A  39        RTS
44            *
45    461A A  B6  47A0 T6LOID LDAA HELLO
46    461D A  B7  4842 STAA MATCHA
47    4620 A  39        RTS
48            *
49    4621 A  FE  4842MATCH LDX MATCHA
50    4624 A  BC  47A4 CPX BUSYX
51    4627 A  27  1C    BEQ BUSY1
52    4629 A  BC  47A6 CPX RNGBKX
53    462C A  27  20    BEQ RNGBK1
54    462E A  BC  47A8 CPX REORDX
55    4631 A  27  25    BEQ REORD1
56    4633 A  BC  47AA CPX DIALX
57    4636 A  27  2A    BEQ DIALT1
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 7

```
1     4638 A  BC  47AC CPX NOTONX
2     463B A  27  2F    BEQ NOTON1
3     463D A  BC  47AE CPX HELLOX
4     4640 A  27  3D    BEQ HELLO1
5     4642 A  7E  4676 JMP NONID
6             *
7             *
8             *
9     4645 A  CE  46A9 BUSY1 LDX #MSG1
10    4648 A  C6  02    LDAB #$02
11    464A A  F7  47A1 STAB MATERR
12    464D A  39        RTS
13    464E A  CE  46CD RNGBK1 LDX #MSG2
14    4651 A  F6  47A3 LDAB ERRCNT
15    4654 A  F7  47A1 STAB MATERR
16    4657 A  39        RTS
17    4658 A  CE  46F5REORD1 LDX #MSG3
18    465B A  F6  47A3 LDAB ERRCNT
19    465E A  F7  47A1 STAB MATERR
20    4661 A  39        RTS
21    4662 A  CE  471C DIALT1 LDX #MSG4
22    4665 A  F6  47A3 LDAB ERRCNT
23    4668 A  F7  47A1 STAB MATERR
24    466B A  39        RTS
25    466C A  CE  4740NOTON1 LDX #MSG5
26    466F A  F6  47A3      LDAB ERRCNT
27    4672 A  F7  47A1      STAB MATERR
```

```
 28   4675 A  39        RTS
 29   4676 A  CE  474ENONID LDX #MSG6
 30   4679 A  C6  00    LDAB #$00
 31   467B A  F7  47A2 STAB ERFLAG
 32   467E A  39        RTS
 33   467F A  CE  4770HELLO1 LDX #MSG7
 34   4682 A  F6  47A3 LDAB ERRCNT
 35   4685 A  F7  47A1 STAB MATERR
 36   4688 A  39        RTS
 37   4689 A  F6  47A1 CHERR LDAB MATERR
 38   468C A  F1  47A2 CMPB ERFLAG
 39   468F A  2F  04    BLE UNIDEN
 40   4691 A  7A  47A1 DEC MATERR
 41   4694 A  39        RTS
 42   4695 A  CE  4776UNIDEN LDX #INVLD
 43   4698 A  F6  47A3 LDAB ERRCNT
 44   469B A  F7  47A1 STAB MATERR
 45   469E A  39        RTS
 46              *
 47   469F A  BD  8662PRINT JSR CRLF
 48   46A2 A  BD  8655 JSR HEAD
 49   46A5 A  BD  866E JSR SPACE2
 50   46A8 A  39        RTS
 51              *
 52              *
 53              *
 54              *
 55              *
 56   46A9 A  54  48    MSG1 FCC 'THE SIGNAL NOW PRESENT IS BUSY TONE'
 57   46CC A  00        FCB 0
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 8

```
  1   46CD A  54  48    MSG2 FCC 'THE SIGNAL NOW PRESENT IS RINGBACK TONE'
  2   46F4 A  00        FCB 0
  3   46F5 A  54  48    MSG3 FCC 'THE SIGNAL NOW PRESENT IS REORDER TONE'
  4   471B A  00        FCB 0
  5   471C A  54  48    MSG4 FCC 'THE SIGNAL NOW PRESENT IS DIAL TONE'
  6   473F A  00        FCB 0
  7   4740 A  4E  4F    MSG5 FCC 'NO SIGNAL...'
  8   474D A  00        FCB 0
  9   474E A  50  4C    MSG6 FCC 'PLEASE WAIT... PROCESSING TONE ID'
 10   476F A  00        FCB 0
 11   4770 A  48  45    MSG7 FCC 'HELLO'
 12   4775 A  00        FCB 0
 13   4776 A  54  48    INVLD FCC 'THE TONE NOW PRESENT IS UNIDENTIFIED'

 14   479A A  00        FCB 0
 15              *
 16              *
 17   479B A            BUSY RMB 1
 18   479C A            RNGBK RMB 1
 19   479D A            REORDR RMB 1
 20   479E A            DIALTN RMB 1
 21   479F A            NOTONE RMB 1
 22   47A0 A            HELLO RMB 1
```

```
 23                *
 24     47A1 A             MATERR RMB 1
 25     47A2 A             ERFLAG RMB 1
 26     47A3 A             ERRCNT RMB 1
 27                *
 28     47A4 A             BUSYX RMB 2
 29     47A6 A             RNGBKX RMB 2
 30     47A8 A             REORDX RMB 2
 31     47AA A             DIALX RMB 2
 32     47AC A             NOTONX RMB 2
 33     47AE A             HELLOX RMB 2
 34                *
 35     47B0 A             RAMSG RMB 146
 36     4842 A             MATCHA RMB 1
 37     4843 A             MATCHB RMB 1
 38     4844 A             CNT1 RMB 2 ;TONE ABSENT COUNT
 39     4846 A             CNT2 RMB 2 ;TONE PRESENT COUNT
 40                *
 41     4848 A             TLO1LL RMB 2 ;TONE 1 ABSENT LOWER LIMIT
 42     484A A             TLO1UL RMB 2 ;TONE 1 ABSENT UPPER LIMIT
 43     484C A             THI1LL RMB 2 ;TONE 1 PRESENT LOWER LIMIT
 44     484E A             THI1UL RMB 2 ;TONE 1 PRESENT UPPER LIMIT
 45                *
 46     4850 A             TLO2LL RMB 2 ;TONE 2 ABSENT LOWER LIMIT
 47     4852 A             TLO2UL RMB 2 ;TONE 2 ABSENT UPPER LIMIT
 484854 A           THI2LL RMB 2 ;TONE 2 PRESENT LOWER LIMIT
 49     4856 A             THI2UL RMB 2 ;TONE 2 PRESENT UPPER LIMIT
 50                *
 51     4858 A             TLO3LL RMB 2 ;TONE 3 ABSENT LOWER LIMIT
 52     485A A             TLO3UL RMB 2 ;TONE 3 ABSENT UPPER LIMIT
 53     485C A             THI3LL RMB 2 ;TONE 3 PRESENT LOWER LIMIT
 54     485E A             THI3UL RMB 2 ;TONE 3 PRESENT UPPER LIMIT
 55                *
 56     4860 A             THI4LL RMB 2 ;TONE 4 PRESENT LOWER LIMIT
 57     4862 A             THI4UL RMB 2 ;TONE 4 PRESENT UPPER LIMIT

MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 9

  1                *
  2     4864 A             TLO5LL RMB 2 ;TONE ABSENT LOWER LIMIT
  3     4866 A             TLO5UL RMB 2 ;TONE ABSENT UPPER LIMIT
  4                *
  5     4868 A             TLO6LL RMB 2
  6     486A A             TLO6UL RMB 2
  7     486C A             THI6LL RMB 2
  8     486E A             THI6UL RMB 2
  9                *
 10                END

MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 10
SYMBOL TABLE

BUSY  479B  BUSYX  47A4     BUSY1  4645
CHECB34516      CHERR  4689
CHH1UL 456D     CHH2UL 4575     CHH3UL 457D     CHH6UL 4585     CHL1UL 45DB
CHL2UL 45E3     CHL3UL 45EB     CHL6UL 45F3     CNT1  4844  CNT2  4846
```

```
CRLF = 8662      CRSR = 2001      DIALTN 479E      DIALT1 4662      DIALX 47AA
ERFLAG 47A2      ERRCNT 47A3      HEAD = 8655      HELLO 47A0       HELLOX 47AE
HELLO1 467F      HEX2 = 8686      HEX4 = 867B      INCCNT 450A      INVLD 4776
MATCH 4621       MATCHA 4842      MATCHB 4843      MATERR 47A1      MEASHI 4548
MEASLO 45B3      MORB3 452C       MORCNT 4520      MORINC 44DF      MSG1 46A9
MSG2 46CD        MSG3 46F5 MSG4 471C       MSG5 4740       MSG6 474E
MSG7 4770        NONID 4676       NOTONE 479F      NOTONX 47AC      NOTON1 466C
PATCH1 4546      PRIME 4536       PRINT 469F RAMSG 47B0       REORDR 479D
REORDX 47A8      REORD1 4658      RESET 44FA RNGBK 479C       RNGBKX 47A6
RNGBK1 464E      SPACE2 = 866E    START = 4400     THI1LL 484C      THI1UL 484E
THI2LL 4854 THI2UL 4856       THI3LL 485C      THI3UL 485E      THI4LL 4860
THI4UL 4862      THI6LL 486C      THI6UL 486E      TH2LL 4556 TH3LL 455B
TH4LL 4560 TH6LL 4565 TLO1LL 4848       TLO1UL 484A      TLO2LL 4850
TLO2UL 4852      TLO3LL 4858      TLO3UL 485A      TLO5LL 4864      TLO5UL 4866
TLO6LL 4868      TLO6UL 486A      TL2LL 45C4 TL3LL 45C9 TL5LL 45CE
TL6LL 45D3 TXRX = 2000       T1HIID 458D      T1LOID 45FB      T2HIID 4594
T2LOID 4602      T3HIID 459B      T3LOID 4609      T4HIID 45A2      T5LOID 4610
T6HIID 45AC      T6LOID 461A      UNIDEN 4695      X %

0000
. ASCT   487000

MODULE: MODULE
ERRORS DETECTED: 0

FREE CORE: 8569. WORDS
)USR_VSI_6800:MA6800 CPDEMOFIN,CPDEMOFIN/-SP = CPDEMOFIN/C

MODULE;      MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE S-1
CROSS REFERENCE TABLE


BUSY  1-41* 5-36  6-36  8-17#
BUSY1  6-51  7-9#
BUSYX  2-4*  6-50  8-28#
CHECB3 3-43  3-46  4-18#
CHERR  3-50  7-37#
CHH1UL  5-2  5-13#
CHH2UL  5-4  5-16#
CHH3UL  5-6  5-19#
CHH6UL  5-10  5-22#
CHL1UL  6-2  6-13#
CHL2UL  6-4  6-16#
CHL3UL  6-6  6-19#
CHL6UL  6-10  6-22#
CNT1  3-56* 4-12  4-14* 4-41* 4-53  4-57  8-38#
CNT2  3-57* 4-28  4-30* 4-42* 5-52  5-57  8-39#
CRLF  1-25#  7-47
CRSR  1-24#  3-28* 3-29* 3-31* 3-33* 3-38* 4-18  4-34
DIALT1  6-57  7-21#
DIALTN  1-43* 5-40  8-20#
DIALX  2-6*  6-56  8-31#
ERFLAG  7-31* 7-38  8-25#
ERRCNT  1-52* 4-4  7-14  7-18  7-22  7-26  7-34  7-43

8-26#
```

APPENDIX 2
Transmitter in Non Burst mode, Receiver in Interrupt mode

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 2-APR-86 10:21:00 PAGE 1

```
1* THIS PROGRAM DEMONSTRATES THAT THE MT8880 CAN SEND TONE BURSTS IN THE NON
2* BURST MODE, OF DURATION DETERMINED BY A SOFTWARE COUNTER LOOP  THE RECEIVER
3* IS SET TO OPERATE IN INTERRUPT MODE AND ON DETECTING A TONE PRODUCES AN
4* INTERRUPT WHICH MUST BE ACKNOWLEDGED BY A READ FROM THE STATUS REGISTER.
5*
6*  EQUATES
7*
8       4500    START EQU $4500
9       2000    TXRX EQU $2000
10      2001    CRSR EQU $2001
11      8723    READ EQU $8723
12      8655    HEAD EQU $8655
13      5100    RAMMSG EQU $5100
```

```
14    8662      CRLF EQU $8662
15    5000      DIGIT EQU $5000
16              *
17    4500      ORG START
18              *
19              * * RESET
20              *
21    4500 A    86  00    LDAA #$00
22    4502 A    B7  2001 STAA CRSR
23    4505 A    86  00    LDAA #$00
24    4507 A    B7  2001 STAA CRSR
25    450A A    86  08    LDAA #$08
26    450C A    B7  2001 STAA CRSR
27    450F A    86  00    LDAA #$00
28    4511 A    B7  2001 STAA CRSR
29              *
30              * ENABLE OUTPUT,IRQ,RSEL...NON BURST
31              *
32    4514 A    86  0D    LDAA #$0D
33    4516 A    B7  2001 STAA CRSR
34    4519 A    86  01    LDAA #$01
35    451B A    B7  2001 STAA CRSR
36              *
37              * TYPE MESSAGE
38              *
39    451E A    BD  8662 JSR CRLF
40    4521 A    BD  8662 JSR CRLF
41    4524 A    CE  5100 LDX #MSG1
42    4527 A    BD  8655 JSR HEAD
43    452A A    BD  8662 JSR CRLF
44              *
45              * READ FROM THE KEYBOARD
46              *
47    452D A    BD  8723DATA JSR READ
48    4530 A    24  08    BCC UPDATE
49    4532 A    B7  5000 STAA DIGIT
50    4535 A    B7  2000 STAA TXRX
51    4538 A    20  06    BRA OK
52    453A A    B6  5000UPDATE LDAA DIGIT
53    453D A    B7  2000 STAA TXRX
54              *
55              * COUNTER
56              *
57    4540 A    FE  FFFF OK LDX $FFFF
MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  2-APR-86 10:21:00 PAGE 2


1     4543 A    09  COUNTB DEX
2               *
3               * READ FROM THE STATUS REGISTER TO ACKNOWLEGDE IRQ
4               *
5     4544 A    F6  2001 LDAB CRSR
6     4547 A    9C  00    CPX $0000
7     4549 A    26  F8    BNE COUNTB
8               *
9               * TURN OFF OUTPUT BUT ENABLE IRQ
```

```
10                *
11   454B A   86  04   TONOFF LDAA #$04
12   454D A   B7  2001 STAA CRSR
13   4550 A   FE  FFFF LDX $FFFF
14   4553 A   09       COUNTP DEX
15                *
16                * READ FROM STATUS REGISTER TO ACKNOWLEGDE IRQ
17                *
18   4554 A   F6  2001 LDAB CRSR
19   4557 A   9C  00   CPX $0000
20   4559 A   26  F8   BNE COUNTP
21                *
22                * ENABLE OUTPUT, IRQ AGAIN
23                *
24   455B A   86  05   LDAA #$05
25   455D A   B7  2001 STAA CRSR
26   4560 A   7E  452D     JMP DATA
27                *
28    5100       ORG RAMMSG
29   5100 A   4E  4F   MSG1 FCC 'NON BURST MODE, RX IRQ .. ENTER DIGIT FOR TX'
30   512C A   00       FCB 0
31                END
```

```
MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  2-APR-86 10:21:00 PAGE 3
SYMBOL TABLE

COUNTB 4543     COUNTP 4553     CRLF  = 8662     CRSR  =

2001   DATA  452D
DIGIT = 5000     HEAD  = 8655     MSG1  5100     OK

4540   RAMMSG = 5100
READ  = 8723     START = 4500     TONOFF 454B     TXRX  =

2000   UPDATE 453A
X   %0000
.ASCT  512D 00

MODULE: MODULE
ERRORS DETECTED: 0

FREE CORE: 8901. WORDS
)USR__VSI__6800:MA6800 TXNONBUR,TXNONBUR/-SP = TXNONBUR/C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CROSS REFERENCE TABLE


COUNTB  2-1#   2-7
COUNTP  2-14#  2-20
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APPLICATION NOTE MSAN-122
Approaches to Digital Line Card Design

9161-001-037-NA ISSUE 1 JUNE 1986

Table of Contents

1.0 Introduction

Two devices manufactured by Mitel allow easy implementation of digital communications over existing twisted-pair wire as recommended for ISDN 'U' interface applications. These devices, the MT8952 HDLC Protocol Controller and the MT8972 Digital Network Interface (DNIC) can provide a link with a loop attenuation of up to 34 dB (4.0 km on 24 AWG @ 160 kbit/s) consisting of two 64 kbit/s B-channels and one 16 kbit/s signalling D-channel. The D-channel signalling information is formatted in HDLC protocol.

While these devices are designed to meet standards being developed for the public ISDN networks they also find applications in private networks. This note is intended to show a typical application in a private network environment - that found behind a PABX. The note will show, in particular, how the HDLC Protocol Controller can be used as a D-channel interface in a digital line card comprised of multiple DNICs. Three basic approaches are presented and are intended to give the telecommunications engineer a starting point for the development of his/her application. In addition, a design approach is presented for special-feature digital telephones/datasets for use at the far end of the link.

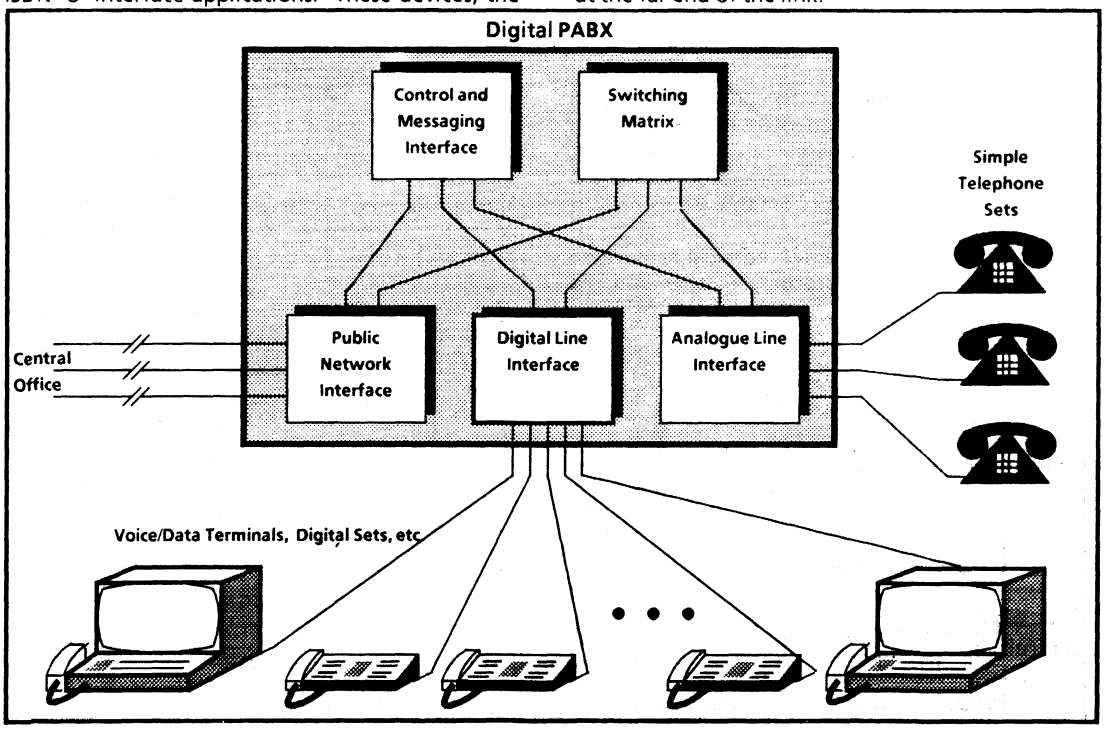

Figure 1. Typical DPABX Configuration

Figure 1 illustrates a typical PABX configuration comprising an interface to the central office (public network) and interfaces to simple analogue telephone sets, feature-rich digital sets and data terminals. This application note will concentrate on the block labelled 'Digital Line Interface'.

Using the suggestions presented here and the unlimited possibilities offered by two clear 64 kbit/s channels and a 16 kbit/s channel over a simple analogue telephone line, PABX designers can design and offer advanced features in their PABX's previously considered impossible.

2.0 General Description

As a model for a high speed digital link, Figure 2 shows a configuration consisting of an interface for voice/data channels and an interface for a signalling channel. The Digital Network Interface Circuit (MT8972) and the HDLC Protocol Controller (MT8952) integrate these two functions respectively.

Voice and/or data arrives at the digital line interface as two 64 kbit/s channels embedded in a 32 channel time division multiplexed stream known as the ST-BUS. Control and signalling information arrives at the signalling interface in parallel mode, perhaps from a local µP. This signalling information is then converted to ST-BUS format for input to the digital line interface.

The signalling channel and the voice/data channels are combined and then adapted for transmission on a single twisted-pair wire. One end of the link, the master, sources clock information while the slave end extracts this clock from the line.

The following provides a brief technical description of the MT8952 HDLC Protocol Controller and the MT8972 Digital Network Interface Circuit (DNIC).

2.1 MT8952 General Description

The MT8952 HDLC Protocol Controller formats packets of information in accordance with ISO HDLC and Layer 2 of CCITT X.25 recommendations. It delimits and synchronizes frames using a unique eight bit Flag sequence (01111110). It also performs a cyclic redundancy check (CRC) on the data and inserts this into the packet prior to the closing flag. In order to ensure the flag sequence is not mimicked, the MT8952 inserts zeros after five consecutive ones have been transmitted. It then extracts these upon reception making the zero-insertion/deletion function transparent to the user. The packet structure is shown in Figure 3.

The MT8952 is capable of generating and detecting the various line states defined by HDLC protocol as well as other defined sequences. The device will generate and detect idle state (15 or more consecutive 1's), interframe time fill (continuous flags), abort sequence and a special Go-Ahead (GA) nine bit sequence (011111110). This special GA sequence is not defined as part of the ISO HDLC protocol but is very useful in some applications as will be shown in this note.

Functionally, the MT8952 may be regarded as a FIFO structure interfacing between a parallel µP bus and a serial bus. The transmit and receive FIFO's are both 19 bytes deep. Information loaded into the Tx FIFO will have the framing flags and the CRC automatically appended to it for transmission on the serial bus. Information arriving at the serial input has the frame structure stripped from the data before it is loaded into the Rx FIFO. Figure 4 provides a functional interface diagram showing the signals associated with the different ports. The MT8952 is controlled by a number of internal registers accessed via the parallel port.

The serial port can be configured in two ways depending on a bit in the Timing Control register.

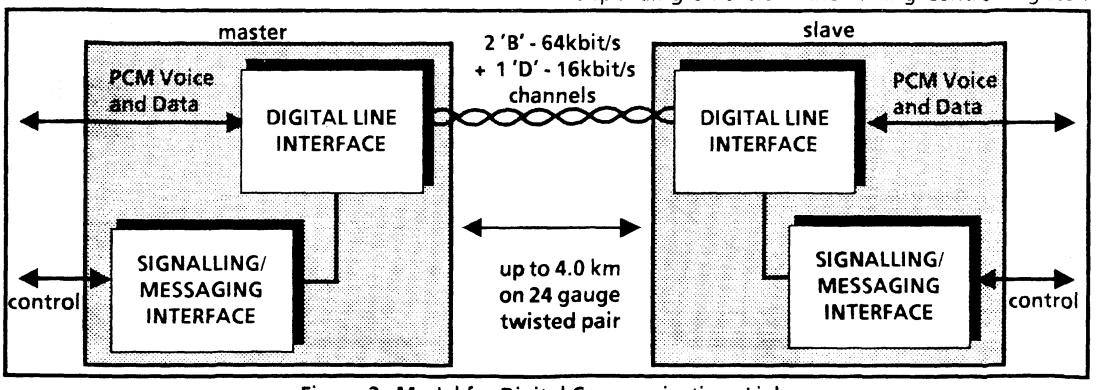

Figure 2. Model for Digital Communications Link

FLAG	DATA FIELD	CRC	FLAG
1 BYTE	n BYTES (n ≥ 2)	2 BYTES	1 BYTE

Figure 3. HDLC Frame Format

It can transmit/receive packets on selected timeslots in ST-BUS format or it can, using enable signals $\overline{TXCEN}$ and $\overline{RXCEN}$, transmit/receive packets at a bit rate equal to the clock input CKi.

In the first mode called the 'Internal Timing mode' packets are shifted in/out serially in ST-BUS format using the timing signals $\overline{F0i}$ and $\overline{C4i}$/C2i. The number of bits and the timeslots on the ST-BUS during which the packets are shifted in/out are determined by bits in the Timing Control register. In this mode, the transmitter and receiver are both active at the same time and are therefore not independent as in the 'External Timing mode'. In the 'Internal Timing mode' the µP can access two registers called C-channel control/status. The device outputs the information stored here during ST-BUS channel 1 and conversely stores the information arriving during this channel in the status register. This feature is particularly useful when the MT8952 is used with the DNIC since it provides direct access to the DNIC's control/status channel.

In the External Timing mode the transmit and receive sections operate independently and are controlled by $\overline{TXCEN}$ and $\overline{RXCEN}$ pins. These can be enabled during desired bit/channel times to allow the device to either transmit or receive packets in predetermined channel designations. As well, two pins labelled TEOP and REOP provide high going signals of one bit duration which indicate the completion of a packet transmission or reception respectively. These 'end of packet' signals are useful in multiplexing several data links onto a single HDLC Protocol Controller.

The µP port allows parallel data transfers between the Protocol Controller and a µP. This interface consists of the data bus (D0-D7), the address bus (A0-A3), E clock, chip select ($\overline{CS}$) and R/$\overline{W}$ control. As well, an open-drain $\overline{IRQ}$ pin allows the MT8952 to interrupt the µP on certain conditions as set up by the Interrupt Flag register and the Interrupt Enable register.

Complete technical data for the HDLC Protocol Controller can be found in the MT8952 Data Sheet.

2.2 MT8972 General Description

The MT8972 Digital Network Interface Circuit (DNIC) is a multi-function device providing a high speed full duplex digital transmission link over a single pair of twisted wires. The DNIC interfaces two serial ports to a high speed line port which may be operated at either 80 or 160 kbit/s. The application in which it is used here requires transmission at 160 kbit/s. It may be driven by a fixed external timebase or it may extract the timebase from the line depending on whether it is in master or slave mode.

At the line port the DNIC supports the 2B + D channel format (two 64 kbit/s B channels, one 16 kbit/s D channel) over two wires as recommended

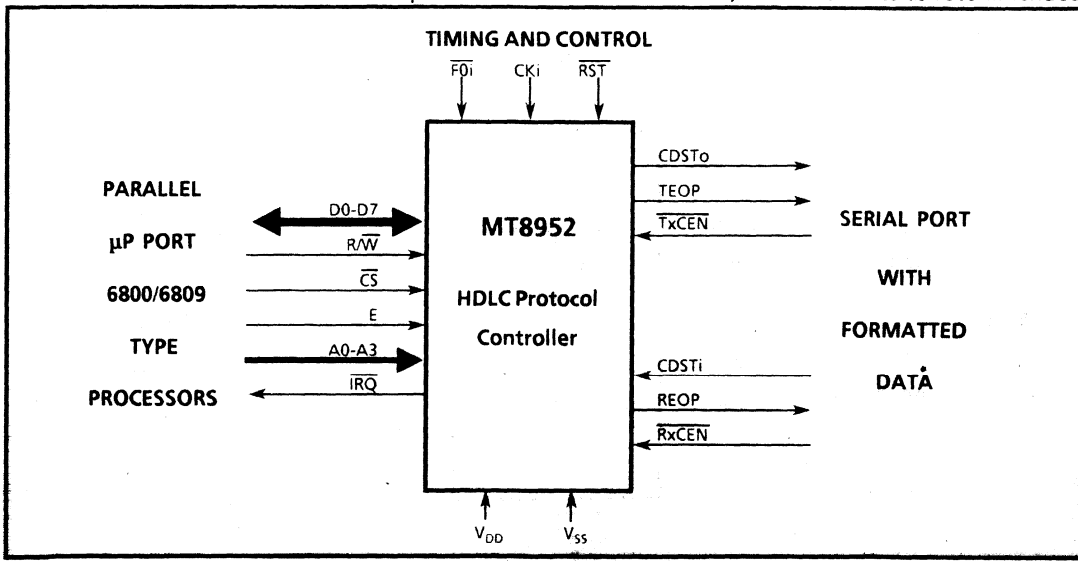

Figure 4. HDLC Protocol Controller Interface Diagram

for emerging ISDN 'U' reference standards. The other two ports on the device are in ST-BUS format. These ports are known as the DV and CD ports and are used to deliver the data/voice information and the control/data information respectively.

A functional interface diagram of the DNIC is shown in Figure 5. The DNIC has various modes of operation which are selected using the mode select pins MS0-2. In this application the DNIC is configured for Digital Network mode in which the information arriving at the CD and/or DV ports is in ST-BUS format. In Digital Network mode it may be further configured for Dual Port mode or Single Port mode. The B1 and B2 channels arrive at the DV port (DSTi/DSTo) while the C and D channels arrive at the CD port (CDSTi/CDSTo) in dual port mode. The B1/B2 channels are active during channels 0 and 16 respectively as are the C and D. In single port configuration the information is combined into one serial stream and arrives at the DV port (DSTi/DSTo) only. In this mode channels D, C, B1 and B2 are active during time slots 0, 1, 2 and 3 respectively.

In order to connect more than one DNIC to the same ST-BUS stream, an $\overline{F0o}$ signal is generated which is a delayed frame pulse output. This signal is useful for 'daisy-chaining' several devices together in line card applications. With this arrangement, only the first DNIC would receive system $\overline{F0i}$ and subsequent DNIC's would be enabled after its predecessor has finished accessing the ST-BUS.

Complete technical data for the Digital Network Interface Circuit can be found in the MT8972 Data Sheet.

3.0 Digital Line Card Implementation

Using the HDLC Protocol Controller and the DNIC one can easily implement digital line card solutions using various approaches. The choice of approach will depend on criteria such as system response time, cost and circuit card density desired. Presented below are the three basic approaches to implementing a line card using the MT8952 and the MT8972.

Expanding on the notion of a digital link presented in Figure 2, Figure 6 provides a functional representation of a line card consisting of several of these links. Each Digital Line Interface requires a source for the voice/data 64 kbit/s channels. This will originate elsewhere in the system hierarchy and will be interfaced via the block labeled 'PCM Voice/Data Interface' which is typically no more than a buffering mechanism. The bus structure used to transport these channels will be the ST-BUS.

The next block, labelled 'Control and Messaging Interface', is the one on which this application note focuses. It is the source of the Messaging information supplied to each line. The messaging channel utilizes HDLC format for error-free communications and can be implemented in one of three ways. The first uses a dedicated HDLC transceiver per line circuit and the last two share the resources of one HDLC transceiver over a number of lines. The second and third methods are feasible since messaging information is generally sporadic in nature and, when combined and queued, can be handled by a single non-dedicated device.

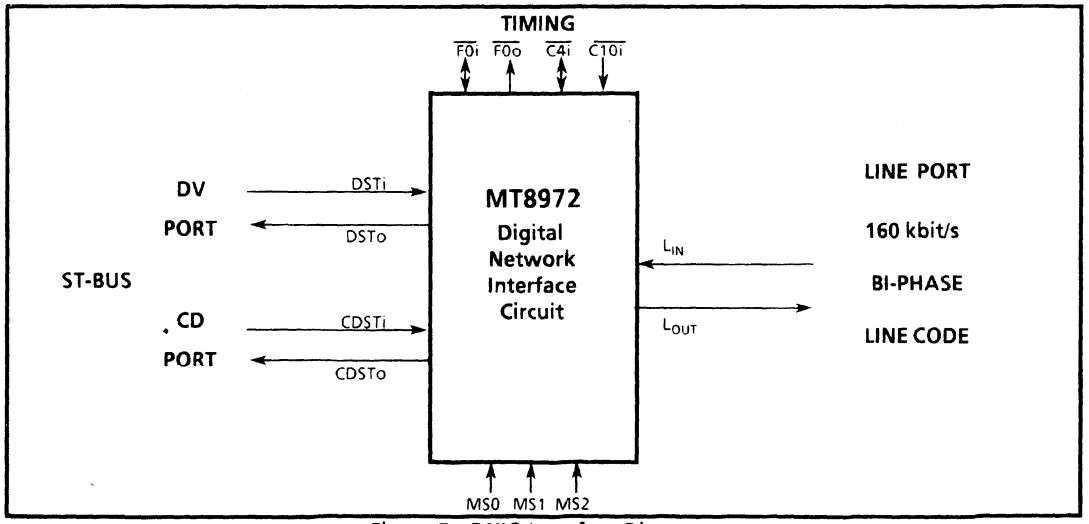

Figure 5. DNIC Interface Diagram

Section 3.1 provides an example of a dedicated HDLC transceiver per line circuit application while sections 3.2 and 3.3 provide two examples of time-shared HDLC transceiver resources. These examples illustrate the basic interconnection of the MT8952 with the MT8972 and their utilization of the ST-BUS.

In Figure 6 the block titled 'clock synchronization/generation' provides a phase-locked clock source to each of the digital line interfaces for synchronization with the system. Actual implementation of this block is shown in Figure 8.

3.1 Dedicated HDLC Interface per line

This method, as stated earlier, allocates a dedicated HDLC transceiver per line circuit. Figure 7 shows the typical inter-connection of the devices.

In this setup the MT8952 is used in the internal timing mode and is programmed to output the HDLC D-channel in ST-BUS channel 0. In addition, the µP has access to each DNIC's control channel through the MT8952 C-channel registers. This C-channel is active on the ST-BUS during timeslot 1. The MT8952 is shown using $\overline{C4i}$. However, in internal timing mode it may alternatively be programmed to use C2i clock.

The DNIC in this case is operated in single port, digital network mode as shown in Figure 16. In this mode the DNIC expects the D and C channels to be active during ST-BUS timeslots 0 and 1 respectively. It also expects B1 and B2 channel information to be present on channels 2 and 3 respectively. The B1 and B2 channels arrive at and depart from the line card at STi and STo.

This approach connects all devices to the same ST-BUS serial link by making use of the delayed frame pulse ($\overline{F0o}$) from the DNIC. In single port, digital network mode the DNIC supplies a frame pulse output at the end of channel three. This is used to activate the next DNIC to retrieve information from the ST-BUS during the subsequent four channels. In this application, this signal is also supplied to the next HDLC Protocol Controller so that it will activate its D and C channels exactly four channels after the previous HDLC device in the chain. Using this approach, up to eight digital lines with

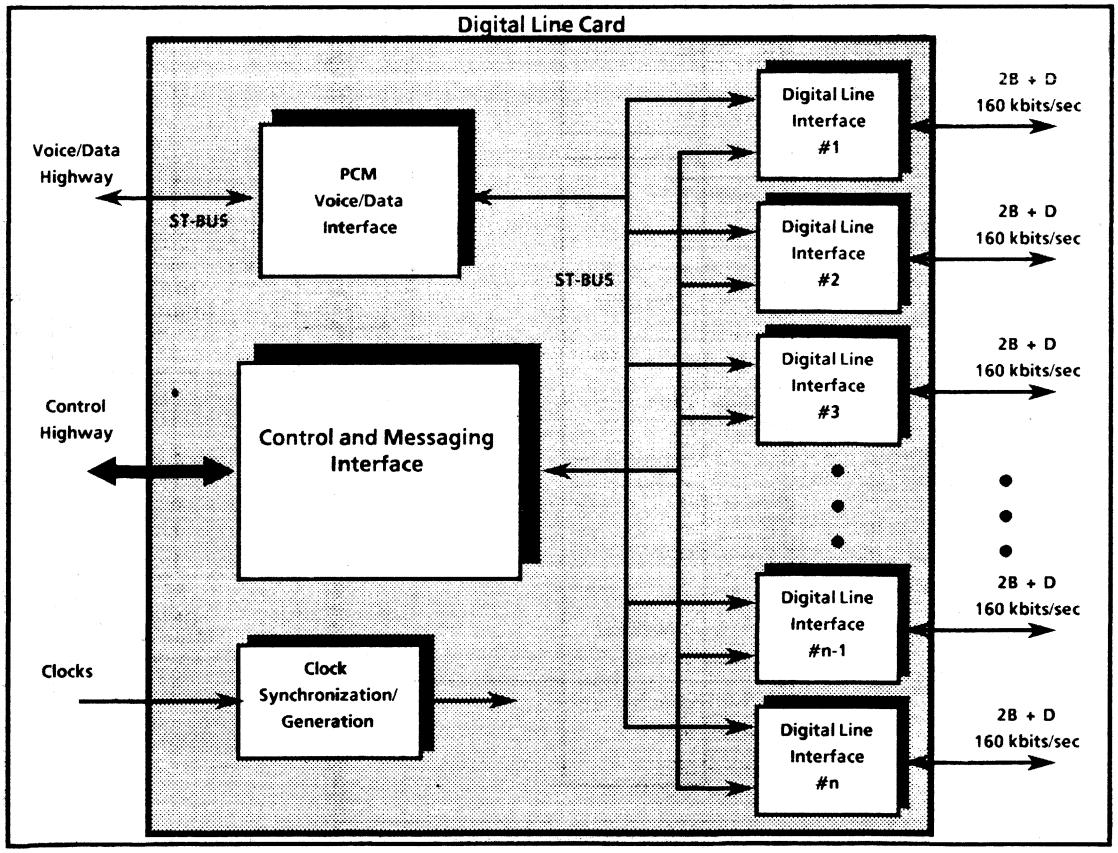

Figure 6. Line Card Functional Block Diagram

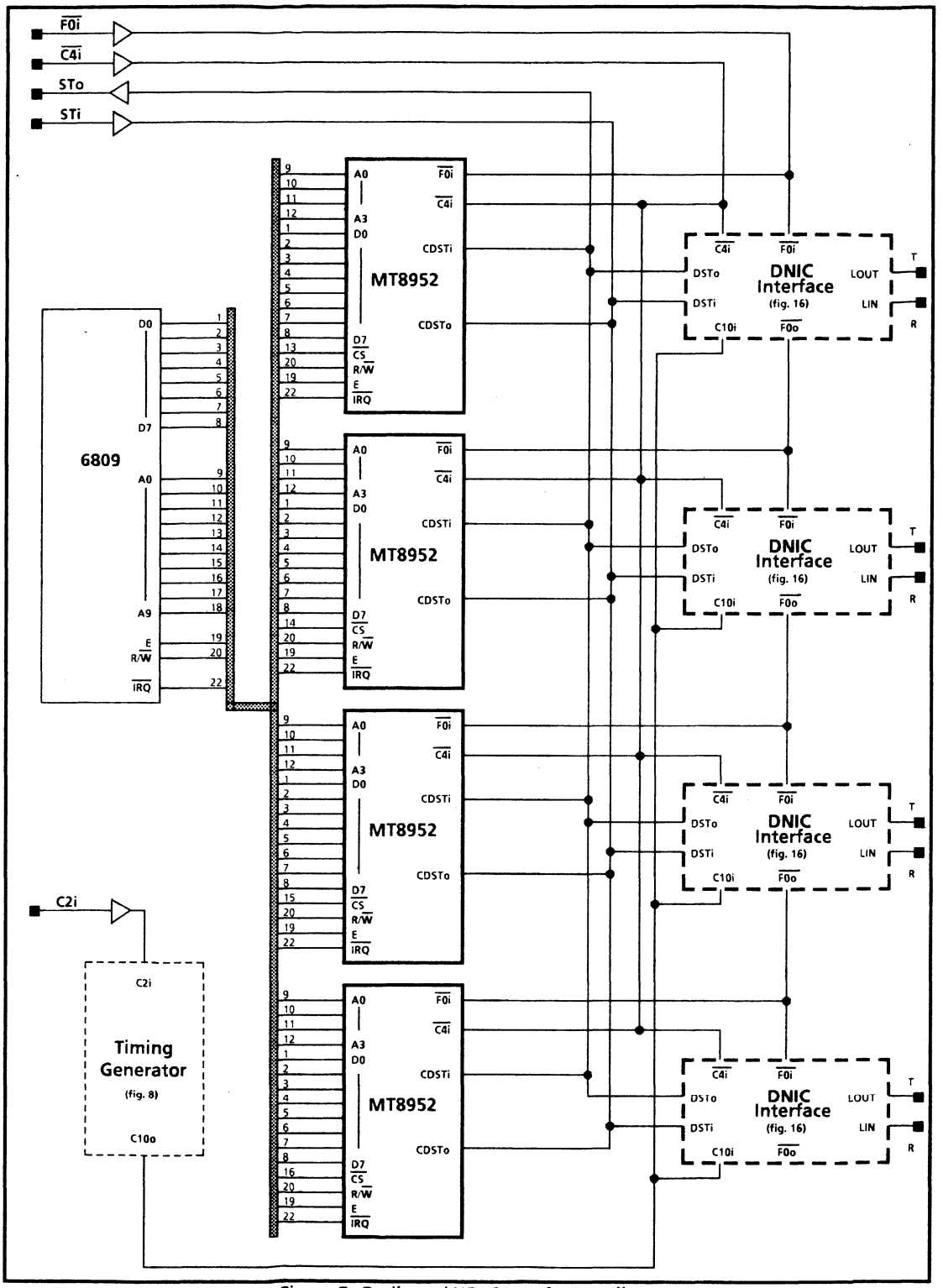

Figure 7. Dedicated HDLC Interface per line

corresponding dedicated MT8952s may be supported by one ST-BUS link. The resulting composition of the link is shown in Figure 9.

It is important to note that the HDLC device, while not transmitting, is in a high impedance state allowing a different source to drive the B1 and B2 channels. Likewise, in this application, it is imperative that the source of the B1 and B2 composite stream also go into a high impedance state whenever one of the MT8952s is active on the ST-BUS. If the B1 and B2 channels are driven directly from a MT8980 Digital Crosspoint Switch this task is made easy since the MT8980 can be programmed to go into high impedance during selected channels. If buffer circuits are driving the ST-BUS at this point, special consideration must be given to disabling these during the appropriate channels.

While this method is the costliest of the three approaches presented in this note, it is by far the fastest in terms of system response time and has the greatest flexibility. In this case, system response time is largely determined by the operating speed of the µP and the software which is driving it since the concentration of information is done at the µP interface. With this setup, full advantage of the MT8952's 19 byte FIFO buffers may be realized since messages may be sent and received without waiting for queued requests and go-aheads as required in a shared resource scheme. The D-channels may be operated in the Asynchronous Balanced mode (ABM) as defined by ISO HDLC. Further savings in speed are possible since response to incoming messages can be interrupt driven.

3.2 Shared HDLC Resource - method #1

In this scheme a single HLDC Protocol Controller is time-shared between up to eight digital line circuits. Figure 10 illustrates a schematic representation of this method. The time sharing is accomplished using the MT8981 Digital Crosspoint Switch (DX).

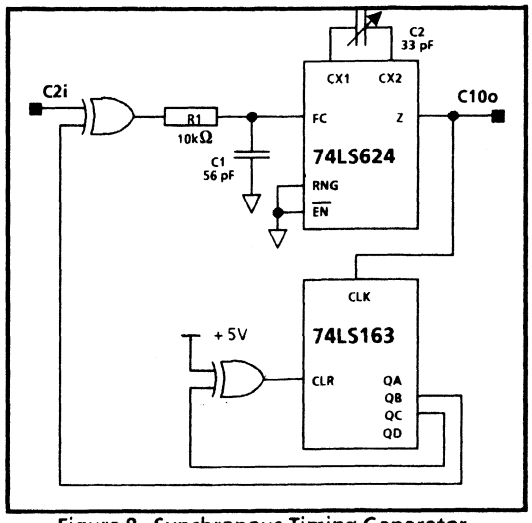

Figure 8. Synchronous Timing Generator

Under control of a µP, the MT8981 is used to connect the MT8952, in succession, to each DNIC's D-channel at a predetermined regular interval. The B1 and B2 channels arrive at the line card at STi1 and terminate at DX link STi1 where they are routed to STo2. Figure 11 shows an arbitrary arrangement of the incoming STi1 stream in which the B1 and B2 channels for each of eight line circuits are packed into the first 16 ST-BUS channels. The D-channel information originating at the MT8952 arrives at DX link STi3 in channel 0. This is also routed to STo2 and into the channel corresponding to the line circuit selected to receive the packet. In Figure 11, the D-channel arriving at STi3 is shown arbitrarily switched to channel 8 which corresponds to line circuit #3. The C-channels used to control the DNICs can be accessed from the parallel port of the DX by putting channels 1, 5, 9, 13, 17, 21, 25, 29 of link STo2 into message mode (see MT8981 Data Sheet). This combines the C-channel information with the B1, B2 and D-channels at the composite STo2 output link. When accessing the DNIC registers from the DX, however, the DNIC register bit assignments are reversed. This is due to the fact that the DX outputs the MSB first while the DNIC expects to receive the LSB first.

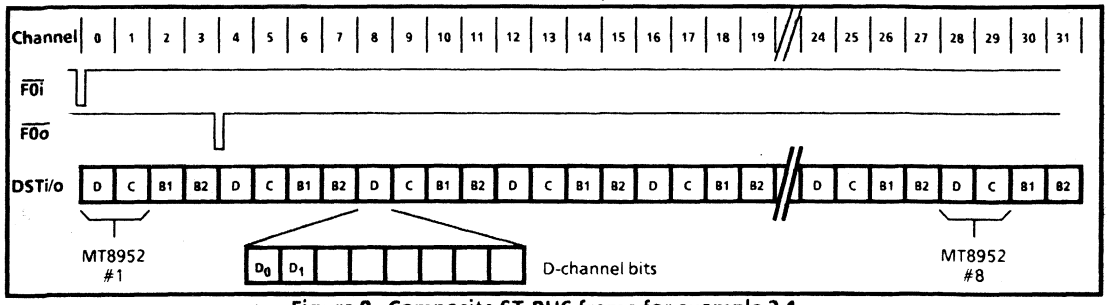

Figure 9. Composite ST-BUS frame for example 3.1

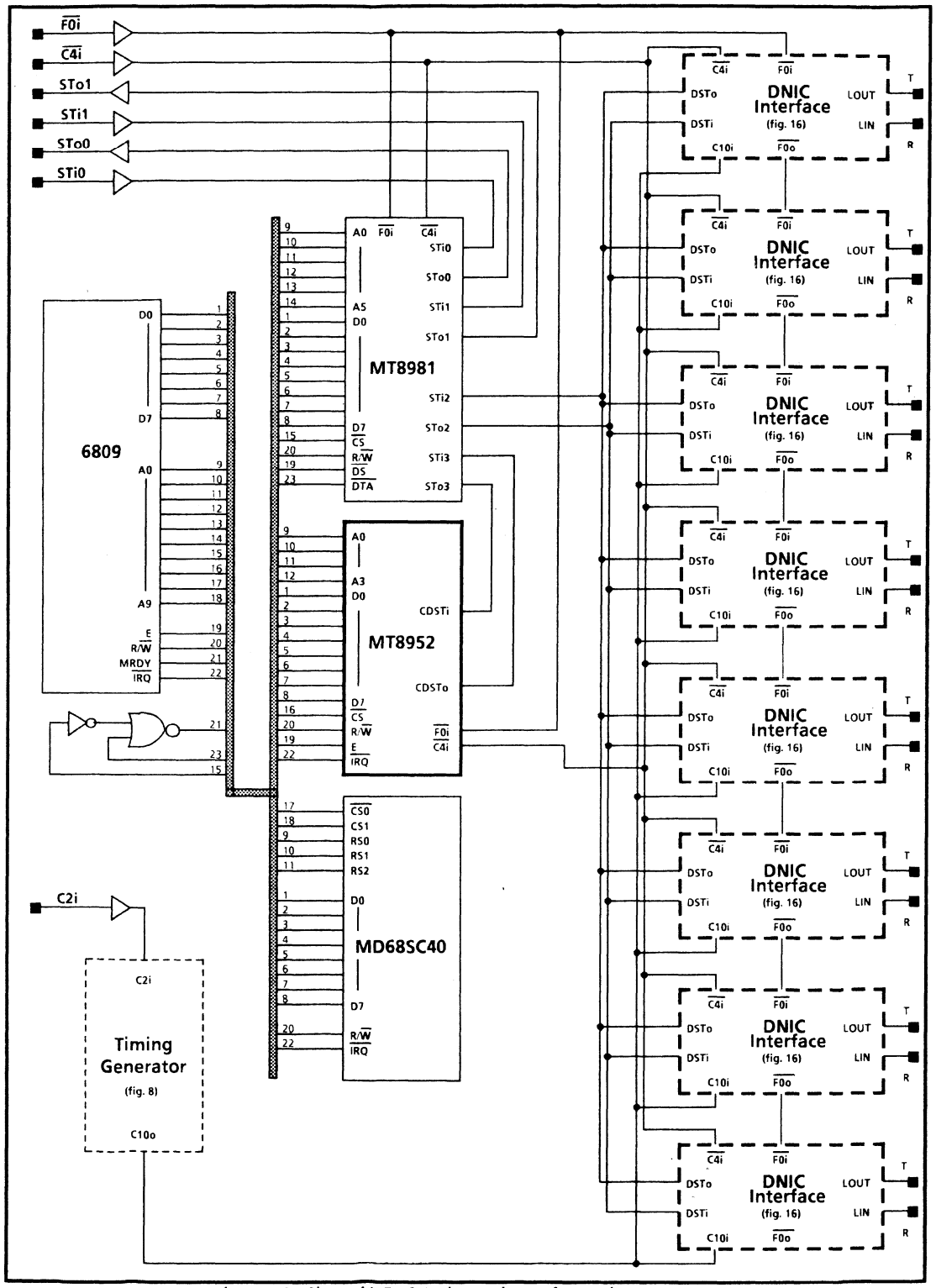

Figure 10. Shared HDLC D-channel Interface using MT8981

On the receive side, the B1 and B2 channels arriving at DX input link STi2 from the line circuits are routed to STo1 and leave the card edge at STo1. The D-channel from the selected receive line circuit is routed to channel 0 of STo3 so that the MT8952 may receive it. The DX's data memory can be used to read the C-channel status from STi2 channels 1, 5, 9, 13, 17, 21, 25, 29.

As in the previous example of 3.1, the HDLC Protocol Controller is used in internal timing mode and the DNIC is used in single port, digital network mode. The MT8952 is programmed to output and accept D-channel information on ST-BUS channel 0 at a rate of 16 kbit/s or 2 bits/frame. Although the MT8952, in this mode, has its C-channel active in timeslot 1 this is ignored since each DNIC C-channel must have a dedicated interface. As mentioned above, these are accessed through the DX.

Each DNIC D-channel is active in the first timeslot relative to its received frame pulse. As in example 3.1, DNICs are 'daisy-chained' together utilizing the $\overline{F0o}$ which, in single port, digital network mode, occurs after completion of channel 3. The composite ST-BUS stream, STo2, sent to all DNIC's is shown in Figure 11 with the D-channel active for DNIC #3. Notice that the 7 remaining inactive DNIC D-channels transmit an 'all-ones' pattern. This is recognized in HDLC as an idle channel state and can be accomplished by connecting the inactive Tx channels via the DX to an 'all ones' pattern originating elsewhere.

This method employs a polling scheme which makes use of the various link states defined in HDLC as well as the GO-AHEAD (GA) sequence incorporated into the MT8952. Normally, incoming and outgoing D-channel links will be in an idle state. If the µP wishes to transmit a packet of information to a peripheral unit it simply connects channel 0 at DX STi3 to the channel at STo2 corresponding to the desired peripheral. The µP then loads it's message into the MT8952 transmit FIFO in the normal manner. When transmission is complete, the channel at STo2 is then returned to an 'all-ones' idle state.

The GA sequence and polling technique are used when receiving messages. Normally all peripheral units will be in idle state. The DX, under µP control, will sequentially connect the HDLC's receiver to each DNIC's incoming D-channel. The HDLC receiver will stay connected to this incoming channel for a specified time 'listening' for a GA sequence which is raised by a peripheral as a request-to-send. Since the GA sequence is nine bits long, including a shared 0 between sequences, the 'listening' time must be at least 16 bits long in order to detect the sequence in a bit oriented protocol. Since two bits are received per frame, this corresponds to eight frames or 1.0 msec which the HDLC must remain connected to the incoming D-channel before proceeding to the next incoming D-channel. This timeout function may be realized with a hardware timer such as the MD68SC40 as shown in Figure 10.

When a peripheral sends a GA sequence and the HDLC Protocol Controller eventually detects this state, it raises the GA flag in the Interrupt Flag register. This may also trigger an interrupt. If this occurs the timeout function is suspended and the DX is programmed to connect the HDLC transmitter to the corresponding peripheral. The HDLC transmitter is then put into GA state signalling back to the peripheral that it may proceed with transmission of its packet. Once the entire packet has been received the timeout function would be enabled and the polling routine restarted.

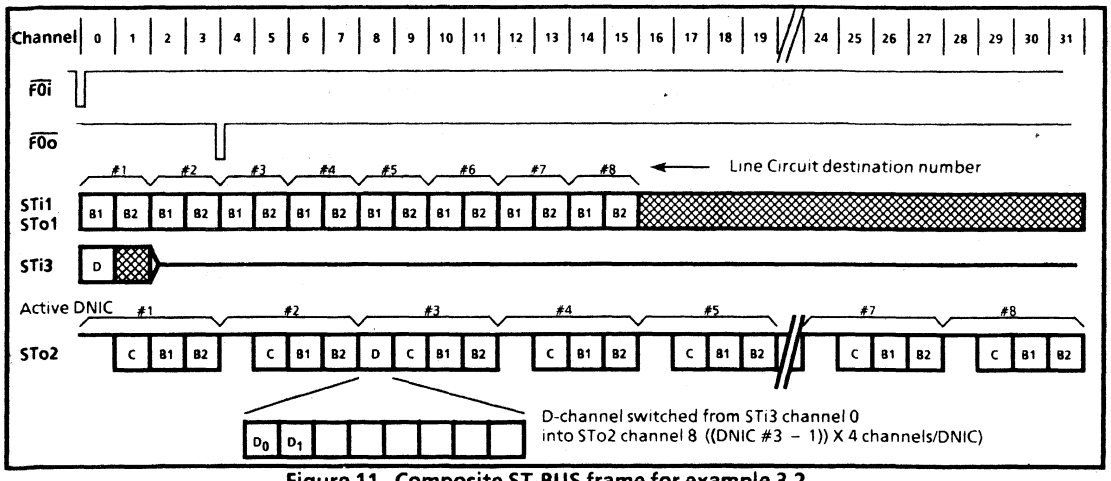

Figure 11. Composite ST-BUS frame for example 3.2

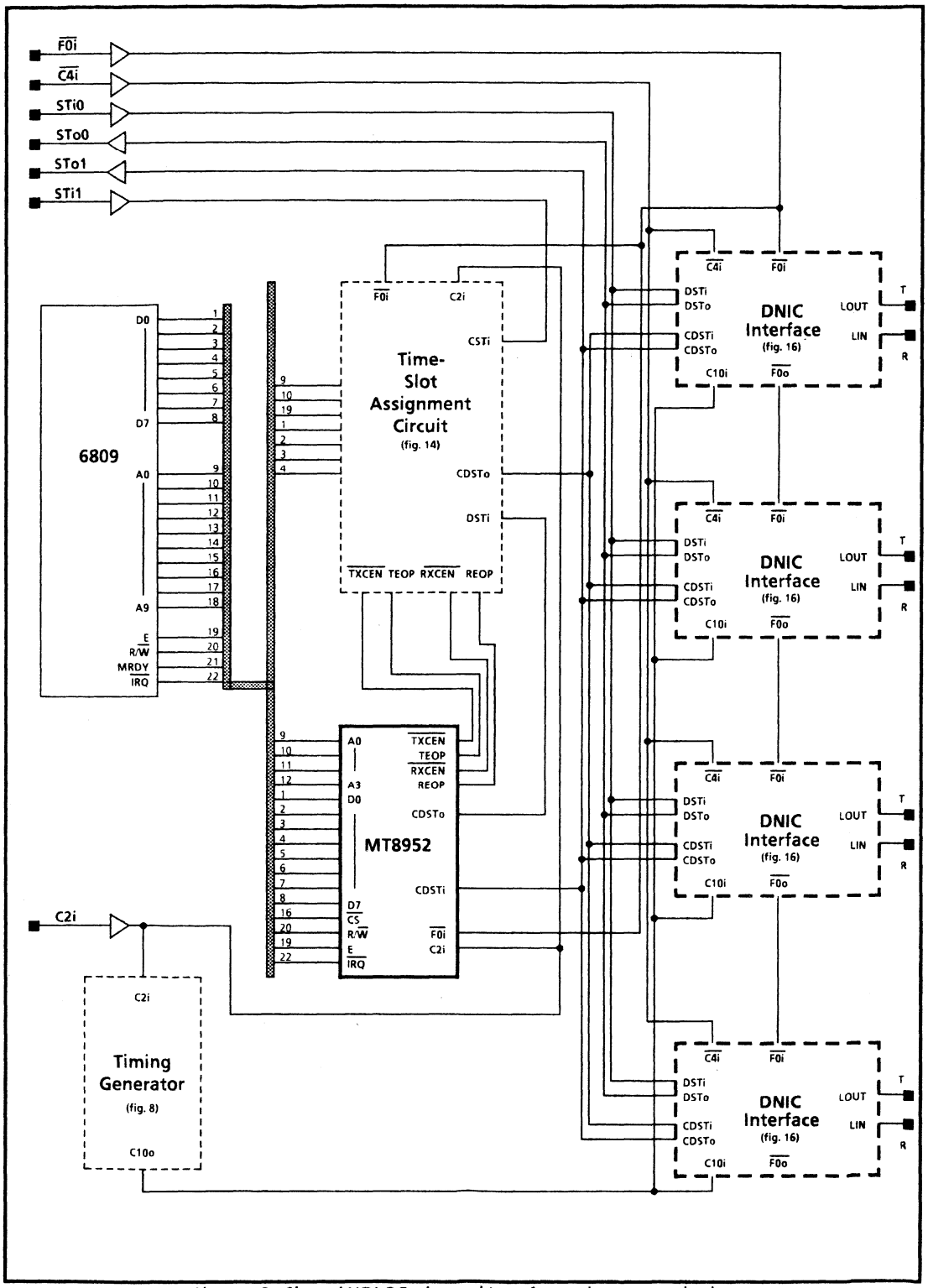

Figure 12. Shared HDLC D-channel Interface using custom logic

This method is more software intensive than the other methods and is better suited to line cards of eight lines or less. System response time becomes primarily a function of the length of the messages and the number of line circuits (up to a max. of eight) the HDLC Protocol Controller must service. In this approach message packets should therefore be limited in size. For example, given eight line circuits and limiting messages to 16 bytes, the worst case system response time would be approximately 100 msec. (Worst case refers to every line requesting to send a maximum length message) This takes into account the time required for polling, the GA response, the actual information transfer and the associated frame structure.

From a hardware standpoint this approach is a simple and relatively inexpensive implementation of the line card function. In cases where the size of the line card is small, the complexity of messages is not too great and/or the system response time is not overly critical this method will provide a suitable solution.

3.3 Shared HDLC Resource - method #2

The significant differences between the previous Shared HDLC Resource method and this method are the operating modes of both the DNIC and the HDLC Protocol Controller and the way in which the timeslot assignment is accomplished. In this method the MT8952 is used in External Timing mode and the DNIC is used in dual-port, digital network mode. The multiplex timing for the HDLC channel is performed by custom circuitry represented by the block labelled 'Timeslot assignment circuit' in Figure 12.

The MT8952 transmit and receive sections, in External Timing mode, are independently controlled by the hardware pins $\overline{TXCEN}$ and $\overline{RXCEN}$ respectively. To assist in multiplexing, the MT8952 outputs TEOP and REOP to indicate when it has finished transmitting or receiving a packet. These four signals make the multiplexing task performed by any custom circuitry relatively simple to implement.

The DNIC, as mentioned earlier, is used in dual-port mode. The B1 and B2 channels are input/output at DNIC port DSTi/DSTo in timeslots 0 (B1) and 16 (B2) relative to $\overline{F0i}$. The D and C information is input/output at port CDSTi/CDSTo on channels 0 (C) and 16 (D). In this application, as in the others presented here, the DNICs are 'daisy-chained' together using the delayed frame pulse output $\overline{F0o}$. In dual-port mode the signal $\overline{F0o}$ comes at the end of channel 0. Supplying this to the next DNIC in the chain skews its active channels by one channel time. Since two ST-BUS links are used to support these 'daisy-chained' DNICs, up to 16 line circuits may be served by one HDLC Protocol Controller with this configuration.

As pointed out previously, the block labelled 'Timeslot assignment circuit' multiplexes the D-channel, originating at the HDLC Protocol Controller, and the C-channels into a common output stream. Figure 14 shows a typical implementation of this circuit. At the microprocessor bus, transmit and receive addresses between 0 and 15 are latched indicating the line circuits to which the HDLC transmitter and receiver are to be connected to respectively. C2i and $\overline{F0i}$ are

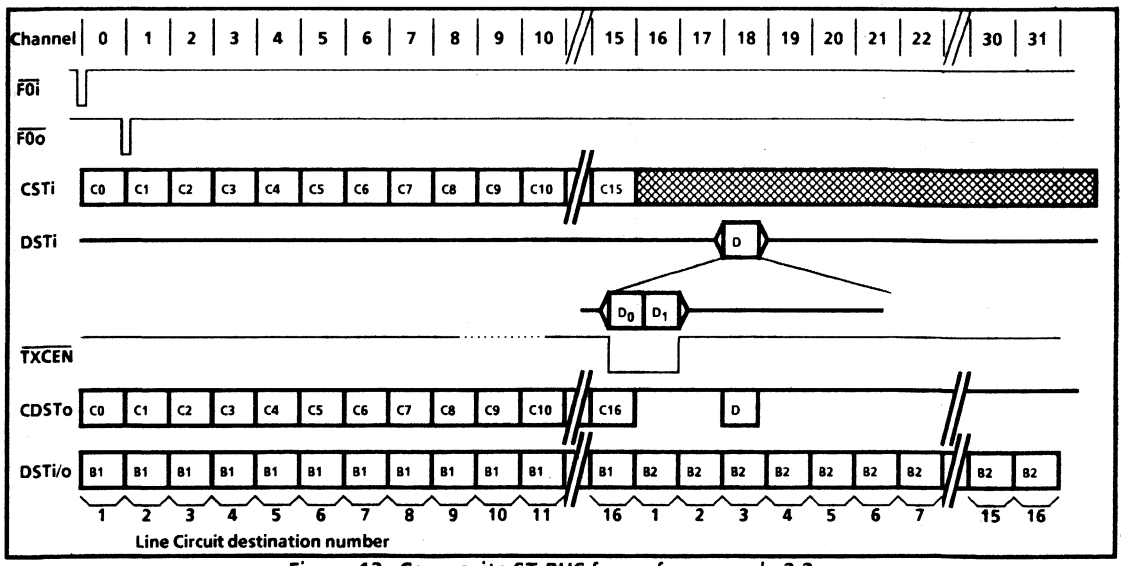

Figure 13. Composite ST-BUS frame for example 3.3

input to a series of counters which in turn supply a two-bit-wide bit count, an incrementing channel count and a half-frame signal used to divide the ST-BUS into two. When the channel count matches the latched Tx or Rx address the comparator output will go active. This signal, gated with the bit count and the half-frame count produces $\overline{TXCEN}$ or $\overline{RXCEN}$ to enable the HDLC transmitter or receiver for precisely two bit periods during the appropriate channel. C-channel and D-channel information destined for the line circuit are also fed through a simple multiplexer controlled by $\overline{TXCEN}$ and the half-frame count. This does the actual merging of the outgoing D and C channel information and can be designed in such a way as to produce a high ('all-ones') pattern on the unused D-channels.

Figure 13 shows the composition of the ST-BUS in the transmit direction. B1 and B2 channels for up to 16 line circuits arrive at the card edge (in Figure 12) at STi0 (and depart at STo0). All DNIC line circuits are connected in parallel to this bus and the channel assignments and line destination addresses are shown as DSTi/o in Figure 13. C-channels for up to 16 circuits originate off card and arrive at STi1. These are input to the timeslot assignment block at CSTi and are assigned to the first 16 channels of the ST-BUS. The D-channel from the MT8952 is input to the Timeslot assignment block at DSTi during the times enable by $\overline{TXCEN}$. These two inputs, CSTi and DSTi, are combined, as shown earlier in Figure 14, to produce CDSTo which is then routed to the DNICs. The composition of CDSTo is shown in Figure 13 with the D-channel enabled for line circuit 3 (channel 18).

In the opposite direction, C-channel information arriving from the line circuits leaves the card edge at STo1 in the first 16 channels. The MT8952, enabled by $\overline{RXCEN}$, receives the active incoming D-channel directly from the same bus.

The protocol used to exchange messages in this method is similar to that used in the previous example 3.2. For messages incoming from the peripheral line circuits the GA sequence and a polling routine are again made use of. If a peripheral requires sending a packet to the system it raises the GA sequence as a request-to-send. The HDLC receiver is switched sequentially among the line circuits listening for the GA sequence. This is done by updating the Rx address in the timeslot assignment circuit Rx latch. When the GA sequence is detected the HDLC transmitter is connected to

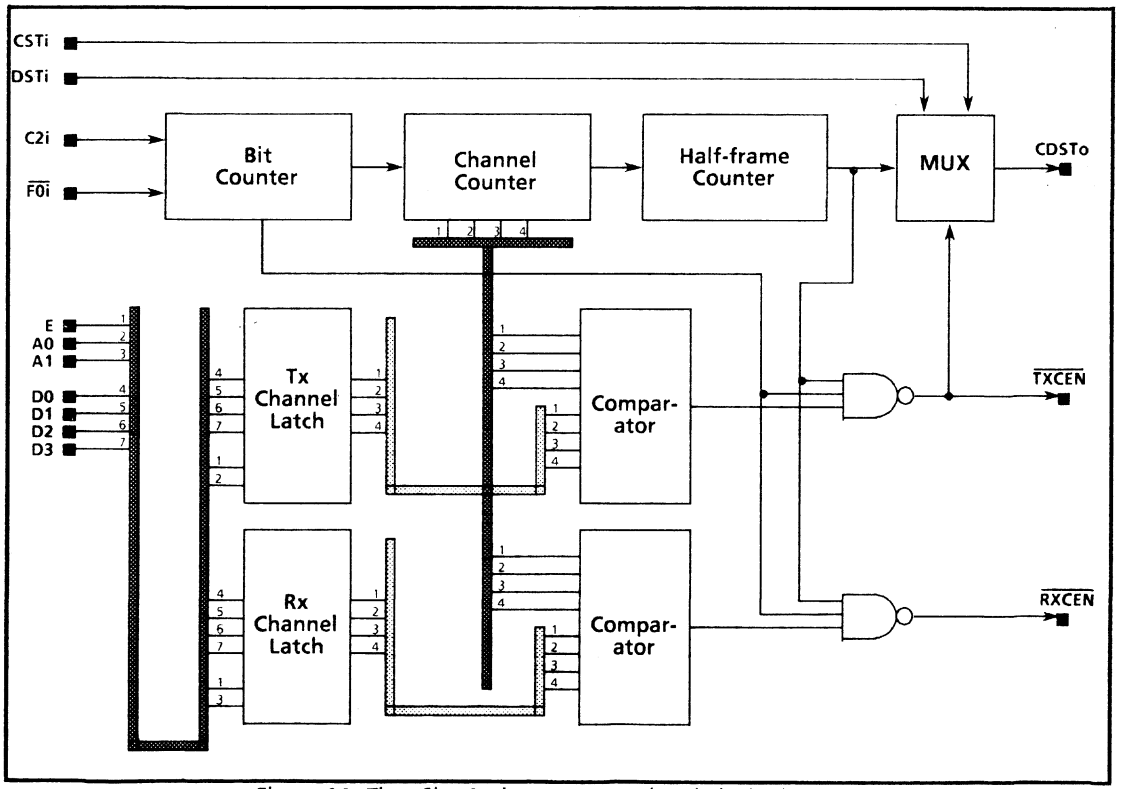

Figure 14. Time Slot Assignment Functional Block Diagram

the corresponding line circuit and acknowledges the request-to-send allowing normal exchange of packets. Outgoing messages, on the other hand, are transmitted directly to the peripheral selected by latching the Tx address in the time-slot assignment circuit and loading the MT8952 Tx FIFO.

While this method appears very similar to the previous method, the advantage lies in the versatility of the custom designed circuit. Shown here is a simple implementation of some basic functions. However, this implementation could be expanded to include a number of timesaving features by further transferring functionality from software to hardware. Possible implementation could include: using a latch/counter to automatically increment the Rx address; independently generating GA acknowledgements in order to relieve the HDLC of this task and; latching the next receive channel address while looking ahead for other Request-To-Send sequences. These functions could easily be implemented using a combination of MSI devices or PALs

In contrast to the previous example, 3.2, this method allows the designer to move some of the functions performed under software control to hardware which results in faster system response time and software reduction. This method still employs a polling technique and uses the GA sequence to request and acknowledge inbound packet transmission as in 3.2. However, this represents a compromise between ease of implementation, cost and system response time. It also allows larger groupings of line circuits on one line card and allows the designer greater flexibilty in designing in other cost/time saving features.

4.0 Digital Telephone/Terminal

This section is intended to briefly introduce the designer to some basic concepts in designing peripheral equipment for use at the far end of the digital link. This equipment may be special feature telephones with RS-232 data ports, terminals/workstations with integrated voice, etc..

The digital link may be terminated and interfaced at the far end using the same two components as

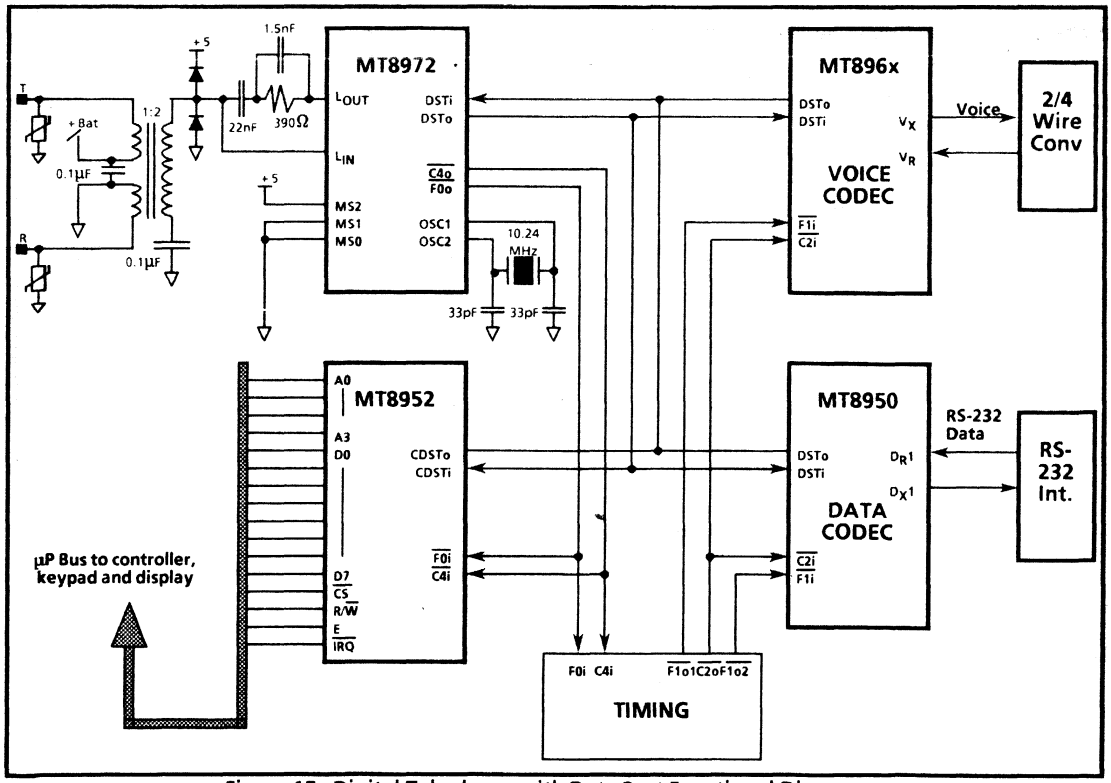

Figure 15. Digital Telephone with Data Port Functional Diagram

are used at the line card. The HDLC Protocol Controller and the Digital Network Interface Circuit are ideal for use in such applications since they are fabricated in low-power CMOS permitting equipment, in many cases, to be line powered.

Figure 15 shows a simplified implementation of a smart telephone set with a data port configured to accept RS-232 type signals. Here the D-channel is used to signal and provide messages between the set and the system, the B1-channel is used to carry voice at 64 kbits/s and the B2-channel is used to carry the data. The RS-232 data port is interfaced to the ST-BUS using the MT8950 Data Codec while the voice is interfaced using the MT896x Voice Codec. The Data Codec uses Transition Encoded Modulation (TEM) to encode the signal transition relative to the ST-BUS $\overline{F1}$ signal and provides the 8 bit data on the ST-BUS in the particular channel to which the device is assigned. The Data Codec will encode signals up to 8 kbits/s, 9.6 and 19.2 kbits/s. The timing circuitry provides $\overline{C2}$ clock for the codecs and generates the appropriate frame pulses to assign the MT8950 to channel 3 and the MT896x to channel 2.

The DNIC is used in Digital Network, single port mode and configured as a slave device. In slave mode the DNIC extracts the timing from the line and provides all ST-BUS clocks to drive the set. The MT8952, acting as the D-channel interface, is operated in Internal Timing mode. In this mode it transmits/receives its D-channel in timeslot 0 and its C-channel registers in timeslot 1. The DNIC, correspondingly, expects its D, C, B1 and B2 channels to be present/active during timeslots 0, 1, 2, 3 respectively.

In order for the set to transmit messages over the D-channel the µP would simply program the MT8952 into GA mode to signal a request-to-send to the DPABX. Upon recognition of the GA sequence the DPABX would reply with a GA sequence back to the set to indicate the system is ready to accept the message. The MT8952 would then be taken out of GA mode and the packet loaded to the FIFO would be sent. When the set transmitter is idle the MT8952 resides in idle fill state.

Incoming messages from the system arrive asynchronously on the D-channel. The MT8952, recognizing the frame structure, indicates to the set µP through an IRQ that an information packet has been received into the Rx FIFO.

As with the line card implementations, digital telephones and special feature terminals can be implemented very easily using the MT8952 HDLC Protocol Controller and the MT8972 Digital Network Interface Circuit.

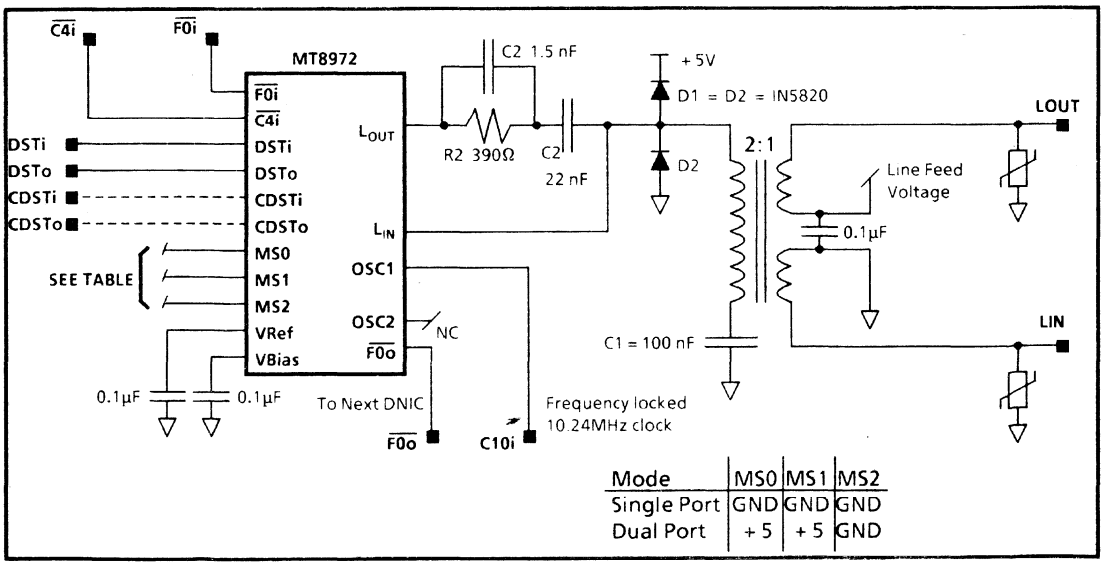

Figure16. DNIC Line Interface - Digital Network Mode, 160 kBit/s (Dual port/Single port)

Application Note MSAN-123
The MT8980 and the MT8981 Digital Crosspoint Switches

9161-001-036 NA ISSUE 1 June 1986

Table of Contents

1.0 Introduction

The MT8980 and the MT8981 are digital crosspoint switches. Any information in an ST-BUS channel (digitized audio, digitized video or data), can be input to the MT8980/81 and then switched to anyone of the its ST-BUS output channels. The MT8980/81 is easily controlled by a microprocessor. The microprocessor can read the contents of all of the input channels and can write information to and read information from all of the output channels.

These capabilities make the MT8980/81 an integral part of a very efficient system of information transport, the ST-BUS. The MT8980/81 provides the ST-BUS system with communication path flexibility.

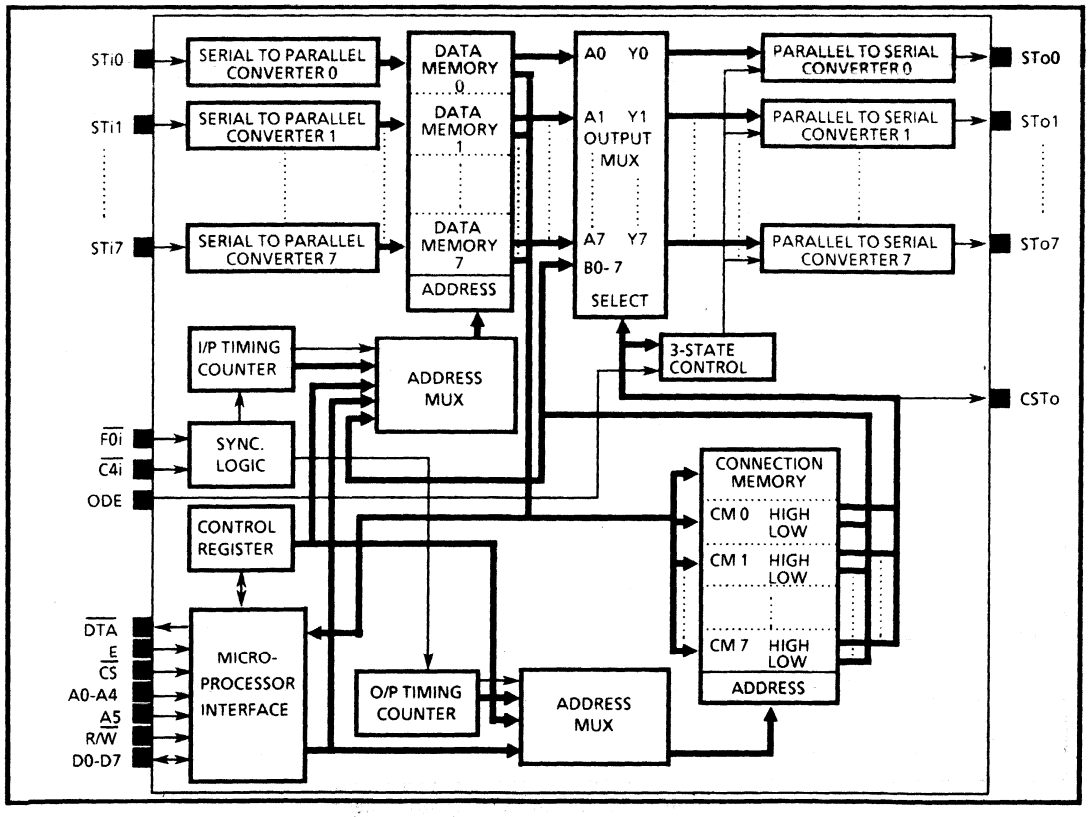

Figure 1 - Block Diagram of the MT8980

This is a prerequisite in today's systems, which emphasize distributed architectures and the integration of voice, video and data.

The principal applications of the MT8980/81 are:

a) **Switching.** The MT8980/81 provides non-blocking switching of information channels (circuit switching). The main difference between the MT8980 and the MT8981 is that the MT8980 has a 256 channel capacity and the MT8981 has a 128 channel capacity. Each channel has a throughput capacity of 64 kbit/s. Channels may carry any form of digitized signal, from encoded voice or data to digitized video.

   The MT8980/81 can provide a communication path between any pair of nodes connected to the MT8980/81 through ST-BUS streams. As well, the MT8980/81 can place its ST-BUS outputs into a high impedance state on a per channel basis, so that larger matrices may be constructed.

b) **ST-BUS Device Control.** When the MT8980/81 is in Message mode, each ST-BUS channel input or output looks like a parallel register to the controlling microprocessor. Each of these input channels or output channels can map directly into the status register, or the control register of a "remote" ST-BUS device connected to the MT8980/81. An individual MT8980 can read up to 256 status registers and write up to 256 control registers.

c) **Interprocessor Communication.** The ability to provide communication paths between microprocessors is a subset of the previous application. In this case, the remote ST-BUS device is another MT8980/81 which is controlled by another microprocessor. This microprocessor is also sending and receiving information on ST-BUS channels in Message mode. The channel that the remote microprocessor is receiving on appears to the "local" microprocessor as a control register of an ST-BUS device appeared in the previous application. The channel that the remote microprocessor is sending on appears to the local microprocessor as a status register of an ST-BUS device appeared in the previous application.

The above applications are discussed in more detail in a subsequent application note.

This application note deals with the relationship between the ST-BUS and the MT8980/81. Other MT8980/81 topics covered are: microprocessor interfacing, the two major modes of the device (Switching mode and Message mode), the delay that the MT8980/81 inserts into end-to-end communication, and miscellaneous details about MT8980/81 operation.

2.0 The ST-BUS

The ST-BUS is a component interface. It minimizes the pin requirements on devices and backplanes by using time division multiplexing to transfer a number of logical data channels through a single wire or pin.

A circuit's ST-BUS interface consists of two control signals and as many input and output streams as are needed to provide the bandwidth required by the circuit to perform its function (usually one input stream and one output stream for information to be processed, and one input and output stream for control and status information).

The standard bit rate of the ST-BUS is 2.048 Mbit/s. The overall bit stream is divided into intervals called frames, yielding a frame rate of approximately 8000 frames/s. Each frame is divided into 256 intervals, each containing one bit of digital information. For most communications applications, the bit stream is also divided into 32 intervals per frame called channels. Each channel is allotted eight bits, for a per channel data rate of :

8000 frames /s x 8 bits/frame = 64 kbit/s.

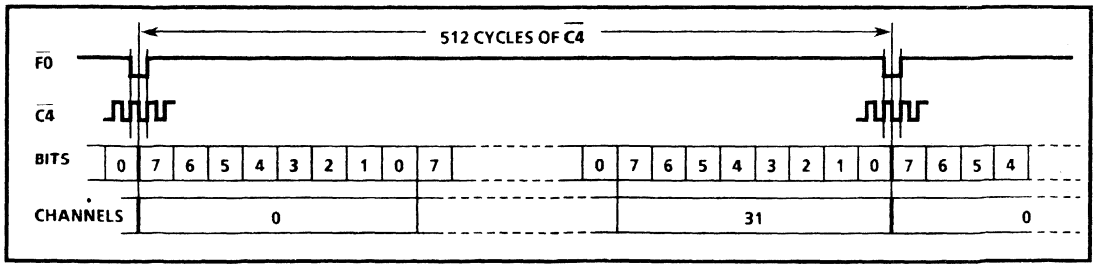

Figure 2 - F0i, C4i and ST-BUS Alignment

Channels are referenced to the start of the frame and are numbered from zero to 31.

Information must be placed on the ST-BUS stream and removed from it synchronously. In most applications, information is placed onto the ST-BUS or received from it in one particular channel time-slot (more than one channel may be used for more bandwidth). Any device interfaced to the ST-BUS must accept a clock signal for bit timing and a framing signal for synchronization with the frame boundaries. There are several types of clock signals and frame synchronization signals (framing pulses) defined for the ST-BUS. These signals are described in the ST-BUS specification in the Mitel Semiconductor Data Book.

3.0 Architecture of MT8980

The MT8980 architecture is illustrated in Figure 1.

3.1 ST-BUS Interface to the MT8980/81

The clock input of the MT8980/81 is called $\overline{C4i}$ and its frequency (4.096 MHz) is twice the data rate. The frame pulse is the $\overline{F0i}$ signal. See Figure 2 for the timing relationship between $\overline{C4i}$, $\overline{F0i}$ and the bits and channels of the ST-BUS.

The ST-BUS outputs of the MT8980/81 derive their output information from two sources: from the ST-BUS streams input to the MT8980/81 and/or from the microprocessor controlling the MT8980/81. The MT8980/81 is also designed to allow the controlling microprocessor to read the information on the input ST-BUS channels.

The MT8980/81 has two modes of operation to accommodate the choice of information sources: Switching mode and Message mode. Switching mode allows the information contained in each output channel to be chosen from any of the input channels in a non-blocking fashion. An advantage of having the output specify the source is that more than one output, all outputs in fact, can have the same source. This is advantageous for broadcasting messages or generating resource channels (eg. dial tone can be input in one channel but output in many). Message mode allows information to be written through the microprocessor port onto the output channels. This information will not change until rewritten. The information on the input channels can be read by the microprocessor no matter what mode the device is in.

The major difference between the MT8980 and the MT8981 is the number of 32 channel streams which each can handle. The MT8980 has eight ST-BUS inputs and eight ST-BUS outputs (256 channels in, 256 channels out). The MT8981 has four ST-BUS inputs and four ST-BUS outputs (128 channels in, 128 channels out). Essentially, the MT8980 is a 256 crosspoint digital switch, and the MT8981 is a 128 crosspoint digital switch. Also, the MT8981 does not have a CSTo output (see Section 6.0). The basic similarities between the two devices allow both to be referred to as the MT8980, unless explicit reference to the MT8981 is needed.

3.2 Microprocessor Interface

The microprocessor port consists of a data bus for information transfer, an address bus, a chip enable, two signals for synchronizing microprocessor bus transfers, and a transfer direction control signal. The data bus is eight bits wide and carries control information for the MT8980 from the microprocessor. The six address bits, A0-A5, help determine which of the individual locations within the MT8980 are accessed.

The Chip Select signal ($\overline{CS}$) is the chip enable. If $\overline{CS}$ is high, no access to the MT8980 is possible. Normally, when DS is brought low, most systems remove the $\overline{CS}$ signal. This is not mandatory, as the MT8980 will not drive the data bus or receive information from the data bus unless DS is high. The Data Strobe signal (DS) and the Data Acknowledge signal ($\overline{DTA}$) perform transfer synchronization. At the rising edge of DS, all other control information must be valid. On the falling edge of DS, data from the microprocessor or data from the MT8980 is valid. DS is usually not brought low until after the MT8980 brings the $\overline{DTA}$ signal low, which occurs when the MT8980 is ready to accept or provide data. Once DS is low, the MT8980 brings $\overline{DTA}$ high, terminating the bus cycle.

The Read/Write signal (R/$\overline{W}$) determines the direction of information flow. When the signal is high, information can be read from the MT8980 by the microprocessor. When R/$\overline{W}$ is low, data from the microprocessor may be written to the MT8980.

3.3 Internal structure

There are four major functional blocks inside the MT8980. These blocks are the Data Memory, the Connection Memory High, the Connection Memory Low and the Control Register. Data Memory is related to the input ST-BUS streams; Connection Memory High and Connection Memory Low are related to the output ST-BUS streams. The Control Register performs block addressing functions and overall mode determination.

The Data Memory is where information is stored as it comes in from the ST-BUS inputs. The loading of information into Data Memory from the inputs is automatic (Data Memory may not be written into from the microprocessor port). Channel information is converted from the serial ST-BUS format into a parallel format and stored in a corresponding byte in the Data Memory in an unchanging sequence. The size of the MT8980s' Data Memory is 256 bytes and the size of the MT8981's Data Memory is 128 bytes (one byte of Data Memory per input channel).

Information may be read from the Data Memory in two ways: through the microprocessor port, or by a sequence that places Data Memory contents into an ST-BUS output channel. For a microprocessor port access, the address of a location in Data Memory is formed by Control Register bits 2, 1 and 0 (CR_b2, CR_b1 and CR_b0) and external address bits A4, A3, A2, A1 and A0. When information in Data Memory is destined for an ST-BUS output channel, the address for Data Memory is formed by the contents of the Connection Memory Low byte associated with the output channel. This latter type of Data

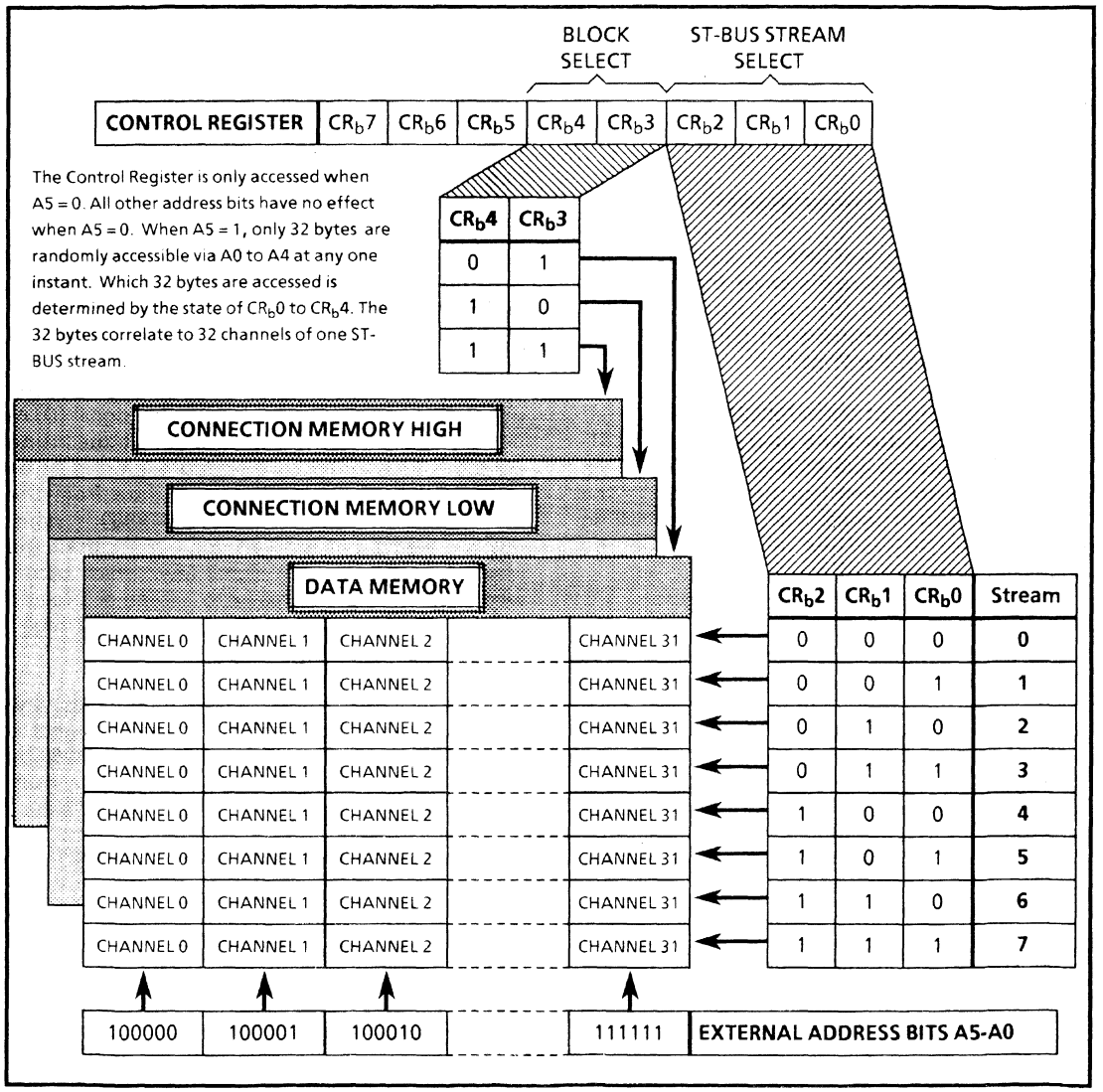

Figure 3 - Relationship Between CR_b4-0, A4-0 and Channel Access for the MT8980

Memory access can only occur when the output channel has been placed into Switching mode.

Connection Memory Low is a block of memory the same size as the Data Memory for the relative device (MT8980 or MT8981). Each byte in Connection Memory Low is associated with an output channel. Information can be placed into Connection Memory Low locations only through the microprocessor port, but it may exit in several directions: the information may be read by the microprocessor, form the address of a location in Data Memory (Switching mode) or be output in the associated ST-BUS output channel (Message mode). When the microprocessor is writing to or reading from Connection Memory Low, the address of the location being written to is formed by CR_b2, CR_b1, CR_b0, A4, A3, A2, A1, and A0. Either the Message mode or Switching mode function of the Connection Memory contents is performed automatically once per frame.

Connection Memory High appears to the microprocessor like Connection Memory Low did, in terms of size of the memory array, method of addressing and being able to be both read from and written to. Each byte of the Connection Memory High is associated with the same output channel as the related byte in the Connection Memory Low.

Only three bits of the Connection Memory High are useful, bits CMH_b2, CMH_b1 and CMH_b0. The other five bits are read as zeroes, and are not changeable. When CMH_b0 is a logical '0' the output channel associated with the Connection Memory High location is placed into a high impedance state. When CMH_b0 is set to a logical '1', the output channel driver is turned on and information from either Data Memory (switched mode) or Connection Memory Low (Message mode) is placed on the output. CMH_b1 controls the state of the bit on the CSTo output that is associated with that particular Connection Memory High location and channel. This bit is not used in the MT8981. CMH_b2 is the channel's mode control bit. When CMH_b2 is a logical '0', the associated output channel is placed into Switching mode and the contents of the Data Memory location addressed by Connection Memory Low are output on the channel. When CMH_b2 is a logical '1', the output channel is in Message mode and the contents of Connection Memory Low are placed on the output channel.

The Control Register is an eight bit register which may be written to or read from the microprocessor port. This register is accessed when A5 is low. When A5 is high, one of the other memory blocks, Data Memory, Connection Memory Low or Connection Memory High, is visible to the microprocessor port. CR_b4 and CR_b3 determine which of the memory blocks is being accessed and CR_b2, CR_b1 and CR_b0 determine which portion of the selected memory block is visible. Each memory block portion selected by CR_b2-0 is 32 bytes long, corresponding to the 32 channels of one of the ST-BUS streams. The state of A4-A0 determines which byte in a 32 byte segment is accessed by the microprocessor at any one time. Figure 3 shows the relationship between CR_b4-0, A5-A0, and channel accesses in the MT8980.

CR_b6 is an overall Message mode bit. This bit can override the setting of the CMH_b2 and the CMH_b0 of an output channel. If CR_b6 is set to a logical '1', all output channels are in Message mode and the CMH_b0 and the CMH_b2 of each channel has no effect. If CR_b6 is low, the Connection Memory High bits determine the mode of their respective channels (Switching or Message) and whether the channel is in a high impedance state or not.

CR_b7 is called the Split Mode bit and is an override of CR_b4 and CR_b3. If CR_b7 is set to a logical '1', the device is in split mode. All microprocessor writes to the MT8980 in Split mode are to the Connection Memory Low. All microprocessor reads of the MT8980 in split mode are from Data Memory. If CR_b7 is a logical '0', memory block selection is determined by CR_b4 and CR_b3.

The last bit in the Control Register, CR_b5, is unused. Also, when using the MT8981, CR_b2 is unused. It is also important to note that CRb4 and CRb3 must never be set to '00'.

3.4 Programming Examples

The way the control register, the memory blocks and the external address bits work together is clarified with several examples.

In the first example, the operation of reading information contained in Channel 5 of Input Stream 2 (STi2) through the microprocessor port is examined. To read ST-BUS input information, the microprocessor must read the Data Memory. Data Memory may be specified in the Control Register by either setting the Split Mode bit, CR_b7, to a logical '1', or by setting CR_b4 and CR_b3 to the binary state '01'. To access the portion of Data Memory corresponding to STi2, CR_b2, CR_b1 and CR_b0 must be set to '010'. CR_b6 and CR_b5 have no effect on this example. Once the Control Register bits are set up in this manner, the microprocessor can read the information contained in any of the channels of

STi2 by keeping A5 high and using A4-A0 to determine which channel is to be read. To access Channel 5, A4-A0 must be set to '00101'.

Example two consists of switching Channel 31 on STi0 to Channel 1 on Output Stream 7 (STo7). In this case, the locations corresponding to Channel 1 on STo7 in the two Connection Memories have to be accessed. Connection Memory Low must contain the Data Memory address of the source channel. Connection Memory High specifies the mode of Channel 1 on STo7 and whether it is in a high impedance state or not. To access Connection Memory Low, CR_b4 and CR_b3 must be set to '10'. To access STo7s' 32 byte segment, CR_b2, CR_b1 and CR_b0 must be set to '111'. CR_b7 may be either a '1' or a '0' for writes (if a '0' then CR_b4 and CR_b3 must have been set properly). For reads, CR_b7 must be a '0'. If it was a '1', then CR_b4 and CR_b3 would have been inconsequential and the read would have been from Data Memory. CR_b6 and CR_b5 do not affect the access of the Connection Memory Low byte. To access Channel 1, A4-A0 must be set to '00001'.

The information that must be written to the Connection Memory Low byte to indicate the source of the information output in STo7 Channel 1 is '00011111'. The three most significant bits of this byte are selecting the input stream and the five least significant bits are accessing the input channel on that stream.

To access Connection Memory High for the same output channel, CR_b4 and CR_b3 must be set to '11' and CR_b7 must be '0'. CR_b2, CR_b1 and CR_b0 need not be changed, and the same setting of A4-A0 must be used. CMH_b0 must be set to a '1' to ensure that the output channel is not in a high impedance state and CMH_b2 must be '0' so the channel is in Switching mode. For the same reason, CR_b6 must be a '0'.

The last example involves writing information from the microprocessor port to output Channel 16 on STo4. The associated bytes for this channel in the Connection Memories may be accessed in the manner described in the last example. The only difference in the procedure is the setting of CR_b2, CR_b1 and CR_b0 ('100'), and the setting of A4-A0 ('10000'). If CR_b6 is set to a '1' (overall Message mode) then the contents of the Connection Memory high are unimportant. If CR_b6 is a logical '0', CMH_b2 must be set to a '1' to specify Message mode, and CMH_b0 must be set to enable the output drivers for STo4 Channel 16. Information desired in

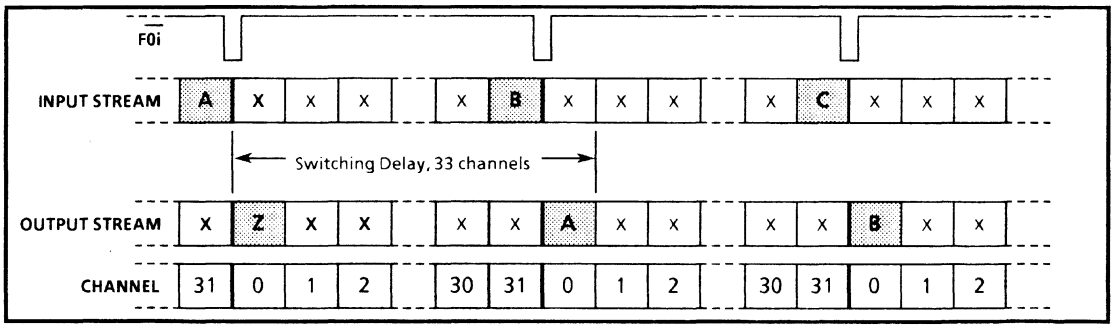

Figure 4 - Delay for Information Switched One Channel Forward, from Channel 31 to Channel Zero

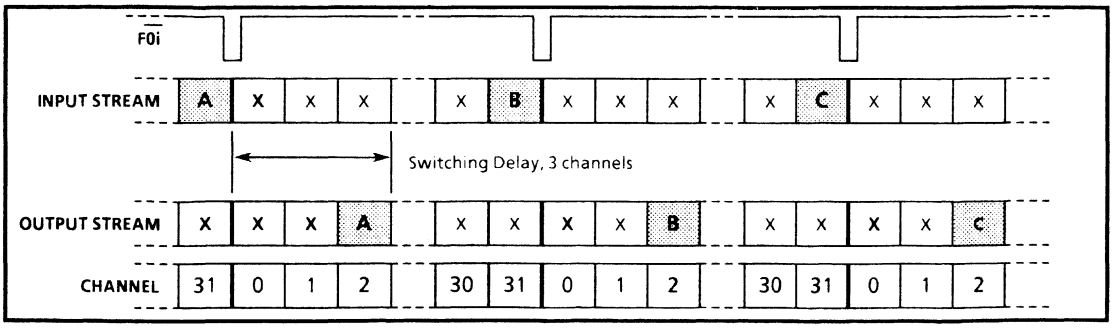

Figure 5 - Delay for Information Switched Three Channels Forward, from Channel 31 to Channel Two

the channel must be written to the associated Connection Memory Low byte.

4.0 Delay through the MT8980

There are standards which dictate the allowable delay that can be tolerated in an end-to-end communication link. When designing a system, the applicable standard or standards must be selected and met. The delay through the MT8980 is described and explained here, so the user may understand how the MT8980 may be used to comply successfully with a particular standard.

4.1 Switching Mode

A delay through the MT8980 results when transferring channel information from an ST-BUS input stream to an output stream. The input information must first be transferred to the Data Memory, where it waits until the next available time-slot allocated to the output channel. Recalling the definition of the ST-BUS, 32 channels arrive at an input and 32 channels leave an output. Each channel is allocated one time-slot per frame, so there are 31 time-slots intervening between each time-slot allocated to a particular channel. If the information has just missed an appropriate time-slot for the output channel, it may have to wait a number of time-slots for the next allocated channel time.

The last bit of a channel is received before the channel information is said to have entered the MT8980 and is sent to the Data Memory. Consequently, a channel's information is sent to Data Memory during the time-slot immediately following a time-slot allocated to the channel. Conversely, channel information is queued for an output channel during the time-slot immediately preceding a time-slot allocated to the channel.

The implication of this ordering of events is that information entering the MT8980 cannot leave it in the same time-slot, or in the time-slot immediately following. Therefore, information that is to be output in the same channel position as the information is input, relative to frame pulse, will be output in the following frame. As well, information switched to the channel immediately following the input channel will not be output in the time-slot immediately following but in the next time-slot allocated to the output channel, one frame later. Examples of channels being switched to the channels immediately following are: switching from Channel 1 to Channel 2, Channel 4 to Channel 5, Channel 30 to Channel 31, Channel 31 to Channel 0 etc. All of the channel changes mentioned above are independent of stream changes.

Input Stream	Output Stream
0	1,2,3,4,5,6,7
1	3,4,5,6,7
2	5,6,7
3	7
4	1,2,3,4,5,6,7
5	3,4,5,6,7
6	5,6,7
7	7

Table 1 - Input Stream to Output Stream Combinations that can Provide the Minimum 2 Channel Delay

Whether the information can be output during the second time-slot after the information entered the MT8980 depends on which ST-BUS stream the channel information enters on and which ST-BUS stream the information leaves on. This situation is caused by the order in which input stream information is placed into Data Memory and the order in which stream information is queued for output. Table 1 shows the input/output stream combinations that would allow information to leave on the second time-slot after the information was received. Information can always leave the MT8980 by the third time-slot after entering the MT8980, independent of which stream it is input on and which stream it is output on. Figure 4 shows the delay of data through the MT8980 for information switched one channel forward. Figure 5 shows the delay of data through the MT8980 for information switched three channels forward. Note that in Figure 4 the input data is not output until one frame later, but in Figure 5 the delay is minimal.

The maximum delay is one frame period (approximately 125 microseconds or 512 $\overline{C4i}$ clock cycles) plus two channels. This is the delay resulting if a switch two channels forward does not meet the input/output stream requirements of Table 1. The minimum delay achievable is two channels. This is the delay resulting if the requirements of Table 1 are met.

Output Stream	Minimum Set Up time
0	$t_{CLK} \times 19$
1	$t_{CLK} \times 19$
2	$t_{CLK} \times 15$
3	$t_{CLK} \times 15$
4	$t_{CLK} \times 11$
5	$t_{CLK} \times 11$
6	$t_{CLK} \times 7$
7	$t_{CLK} \times 7$

Table 2 - Minimum Setup Times for Writing to a Channel in Message Mode (Relative to the Start of the Channel).

Input Stream	Minimum Delays
0	$t_{CLK} \times 1$
1	$t_{CLK} \times 5$
2	$t_{CLK} \times 9$
3	$t_{CLK} \times 13$
4	$t_{CLK} \times 1$
5	$t_{CLK} \times 5$
6	$t_{CLK} \times 9$
7	$t_{CLK} \times 13$

Table 3 - Minimum Delays for Reading Input Channels from Microprocessor Port. Delay is Relative to End of Channel

4.2 Message Mode

In Message mode, there are two delays to contend with. The first delay is the delay between receiving information on the ST-BUS and reading it through the microprocessor port (this delay is not actually constrained to Message mode, as an input channel may be read by the microprocessor independent of any channels being in Switching mode or Message Mode. The other delay is the delay between writing information into Connection Memory Low and transmitting the information on the ST-BUS output.

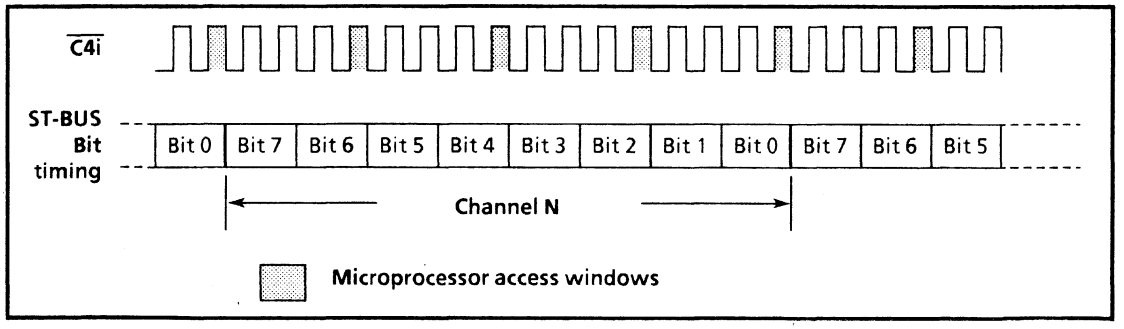

Figure 6 - Position of Microprocessor Access Windows Relative to ST-BUS Channel and C4i Timing

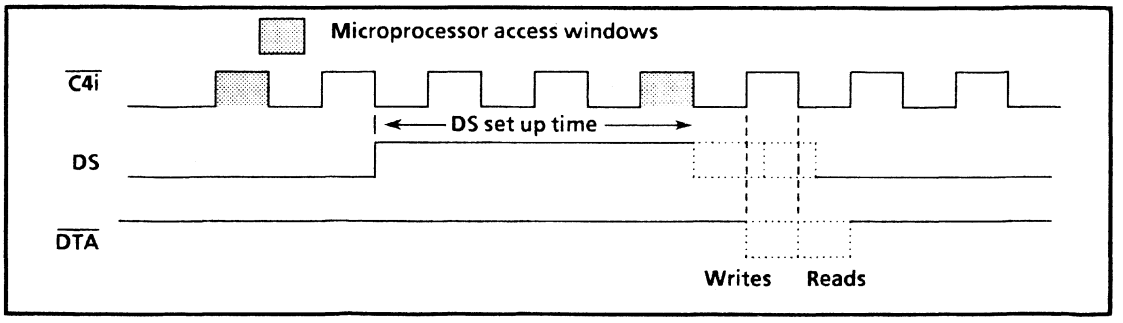

Figure 7 - DS Set Up Time and DTA Return Relative to C4i and Microprocessor Access Window

As with Switching mode, information destined for a particular time-slot on the ST-BUS is sent to the output stream queue during the preceding time-slot. The time during the preceding channel that this occurs is dependent on the stream. The sequence in which the information destined for an output channel is sent to each stream is: STo0, STo1, STo2, STo3, STo4, STo5, STo6, STo7.

To use this information about output sequencing and internal information movement, the microprocessor must synchronize transfers with ST-BUS timing. If the microprocessor transfer is not made before a channel's information is sent to the queue, the newly transferred information will not be output until the next frame.

To ensure that a particular channel on a particular stream may be written to without a one frame delay, a minimum set up time for the write in question must be respected. This set up time is relative to the start of the output channel's time-slot. Table 2 shows the minimum set up times for the different ST-BUS streams (set up times are expressed in multiples of t_{CLK}, the period of the $\overline{C4i}$ clock). There can also be a maximum set up time, if writing information one frame early to a particular channel on a particular stream is undesirable. The maximum set up time is merely the minimum set up time plus one frame.

The minimum delays from the time a channel enters the MT8980 on an ST-BUS input to the time that the information in the channel can be extracted from the Data Memory are given in Table 3. They are measured from the end of the input channel's time-slot to the rising edge of DS. The rising edge of DS corresponds to the earliest point DS may be activated to access the first available microprocessor window from which the information will be visible (see SECTION 5.0).

If the byte of Data Memory that corresponds to the desired channel is accessed earlier than the minimum delay dictates, then the contents of the byte read by the microprocessor will be the information that the channel contained on the previous frame. Conversely, if slightly less than one frame of delay is added to the minimum delay (508 $\overline{C4i}$ clock cycles rather the 512 that make up a frame) the contents of the byte will be the information contained in the channel in the frame following the desired frame.

5.0 Microprocessor Accesses

In the MT8980 data sheet, a parameter is specified (t_{AKD}) for the maximum time taken to return Data Acknowledge after DS goes high. There are two values for this time, one labelled fast, and one labelled slow. The fast t_{AKD} applies to writes to the Control Register. The Control Register can accept data very quickly, and will not cause wait states for most microprocessors. Reading the Control Register and reading or writing to any other part of the MT8980 will receive a slower response (t_{AKD} slow).

Slow microprocessor bus transfers occur because the MT8980 only allocates discrete access windows for the slow transfers. Microprocessor access windows occur every four $\overline{C4i}$ clock cycles during a frame, relative to the frame boundary. Figure 6 and Figure 7 show the relationship between microprocessor access windows, $\overline{C4i}$, DS and the return of $\overline{DTA}$.

$\overline{DTA}$ goes low one half $\overline{C4i}$ cycle after a microprocessor access window in which the set up requirements for DS are met and the operation is a write. If the operation is a read and DS set up is met, $\overline{DTA}$ goes low one $\overline{C4i}$ clock cycle after the access window. DS must be set up three $\overline{C4i}$ cycles ahead of the falling edge of every microprocessor window cycle to meet minimum set up requirements for accessing a window.

If the controlling microprocessor can determine where the falling edge of every fourth $\overline{C4i}$ cycle in a frame occurs, it may use this as a signal to continue on to the next bus cycle rather than wait for $\overline{DTA}$ to go low. $\overline{DTA}$ is a signal provided only to tell the microprocessor that the MT8980 is ready to finish the current bus cycle. DS could be removed between the end of the microprocessor access window and the point where $\overline{DTA}$ would normally go low and the transfer of information would still complete successfully. In such a situation, $\overline{DTA}$ would not go low for that particular bus cycle. Figure 7 shows the two ways in which $\overline{DTA}$ can be returned in response to a microprocessor access. The possible transitions of $\overline{DTA}$ and DS are dotted lines, not solid, because there are several options. If DS goes low at the first transition point, $\overline{DTA}$ does not go low. If DS is held high, the two places that a transition on $\overline{DTA}$ can occur are shown.

6.0 External Control Using CSTo

CSTo is a 2.048 Mbit/s output which is, like the ST-BUS streams, divided into frames that are 256 bits long. Each bit is controlled by one of the 256 CMH_b1's. If a CMH_b1 is a logical '1', the corresponding bit on CSTo is a high. If the CMH_b1 is a logical '0', the corresponding bit on CSTo is a low.

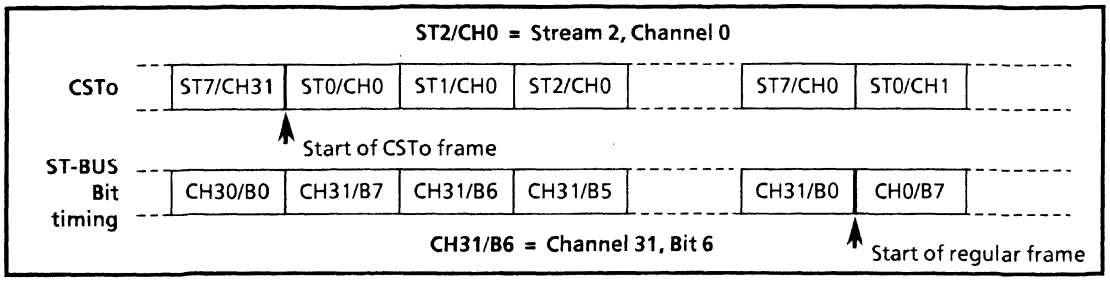

Figure 8 - CSTo Bits Compared to ST-BUS Timing.

Unlike the other ST-BUS outputs, though, CSTo cannot be placed into a high impedance state.

The CMH_b1's of locations that are related by channel time-slot are output sequentially. As an example, there are eight CMH_b1's corresponding to channel zero, one bit for each stream. These bits are output sequentially on CSTo in the following order:

a) CMH_b1 for STo0 Channel 0
b) CMH_b1 for STo1 Channel 0
c) CMH_b1 for STo2 Channel 0
d) CMH_b1 for STo3 Channel 0
e) CMH_b1 for STo4 Channel 0
f) CMH_b1 for STo5 Channel 0
g) CMH_b1 for STo6 Channel 0
h) CMH_b1 for STo7 Channel 0

The eight CSTo bits that correspond to a channel position are output in the timeslot preceding the actual channel position. The reason for this is that CSTo bits are designed to perform external control functions on the individual channels they correspond to.

One control function these bits may perform is to control loop back circuitry for individual channels. If a CSTo bit is set, the loopback circuitry could drive an MT8980 input with the information from the corresponding output channel. This function would be useful for performing system level diagnostics on matrices of MT8980s.

Another use for the CSTo bits is in the sychronization of the microprocessor with ST-BUS timing. CSTo could notify the microprocessor that a predetermined position in the ST-BUS timing has occurred. For example, to mark Channel 7 entering the MT8980, clearing all CSTo bits except the CMH_b1 of STo0 Channel 9 would produce a waveform that had a recurring, high-going, bit-wide pulse immediately following the last bit of Channel 7.

Figure 8 shows the relationship between CSTo bits, ST-BUS timing and the Connection Memory High bytes producing the bits.

7.0 High Impedance Capability

The MT8980 has the capability to put individual channels into a high impedance state, so large switching matrices may be constructed with multiple MT8980's. The ODE input, when it is low, forces all ST-BUS channels into the high impedance condition. When it is high, each channel is controlled by its individual CMH_b0. When the CMH_b0 is logical '1', the channel is driving the ST-BUS. When the CMH_b0 is logical low, the ST-BUS is in the high impedance state during the channel's time-slot.

7.1 Initialization of the MT8980

On initialization or power up, the contents of the Connection Memory High can be in any state. This is a potentially hazardous condition when multiple MT8980 ST-BUS outputs are tied together to form matrices, as these outputs may conflict. The ODE pin should be held low on power up to keep all outputs in the high impedance condition.

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the matrices, and put all other channels into the high impedance state. Care should be taken that no two connected ST-BUS outputs drive the bus simultaneously. When this process is complete, the microprocessor controlling the matrices can bring the ODE signal high to relinquish high impedance state control to the CMH_b0s.

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Connection to Line

Transformer Selection

The major criterion for the selection of a transformer is that it should not significantly attenuate or distort the signals travelling between MT8972's.

Figure 1 gives the specification for a transformer which can be used with the MT8972. A center-tap to ground on the secondary will probably be necessary to ensure good longitudinal balance. The effect of the variations from the specification can be checked with a spectrum analyser.

Protection Circuit for the LIN Pin

In a typical application, the LIN pin of the MT8972 will be connected to a line through a transformer. This means that voltage spikes on the line could cause the voltage at LIN to exceed its Absolute Maximum Rating and damage the device. The circuit shown in Figure 1 is designed to prevent this.

The Schottky diodes, D1 and D2 clamp the voltage received from the line. Further protection is provided by R1 which limits the current at LIN. The diodes will handle several amps of current from the line before the Absolute Maximum Ratings on LIN are exceeded.

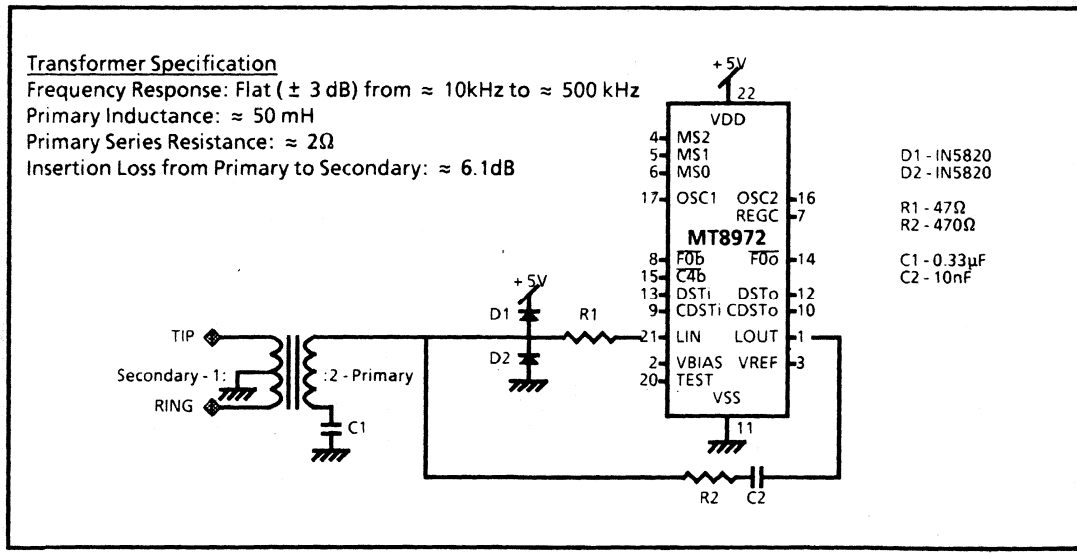


Figure 1 - Connection to Line

Generation of ST-BUS Timing Signals for MT8972 in Master Mode

The circuit shown in Figure 2 generates the ST-BUS framing and clock signals for the MT8972 in Master Mode.

The basic clock source is a 16.384 MHz oscillator. This is used as an input to the MT8940 which generates all the ST-BUS timing signals except C10. C10 is generated by the phase-locked loop formed by the remaining components.

The C10 clock is the output of the 74LS624 Voltage Controlled Oscillator. This is input to the 74LS163 counter which is synchronously reset to 0 after it reaches a count of 4, giving an output which is the 10.24 MHz input divided by 5. This 2.048 MHz output is compared to the C2 clock generated by the MT8940 using the 74LS86 exclusive-or chip.

As C2 slows down, the overlap between the two signals increases causing the output of the exclusive-or to spend more time low. This reduces the input voltage on the 74LS624 and so causes C10 to slow down. The phase-locked loop was found to lock when the period of C2 was between 400 ns and 600 ns.

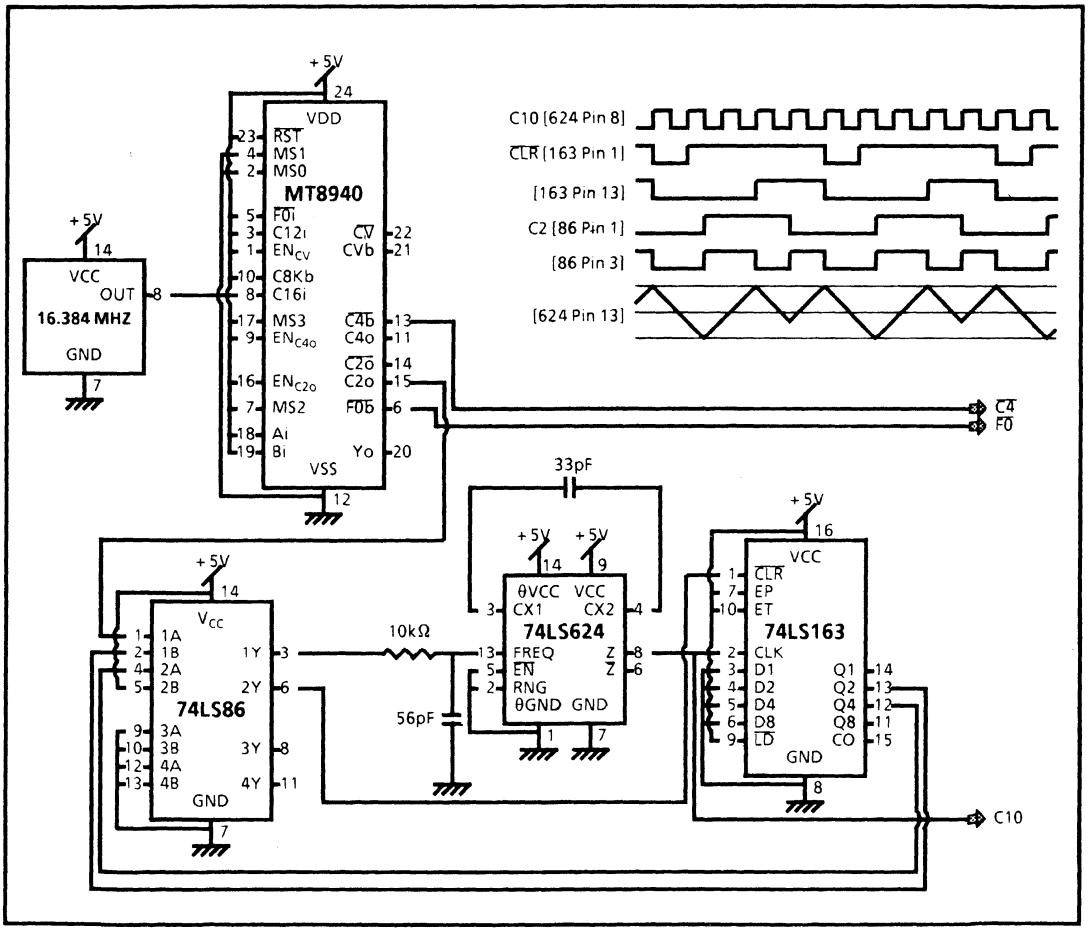


Figure 2 - Generation of ST-BUS Timing Signals for MT8972 in Master Mode

Integrated Voice and RS232 Data Capability for a Personal Computer

Figure 3 shows how an integrated voice and data capability can be added to a Personal Computer.

Data is transmitted and received on the ISDN - compatible digital line using an MT8972. If the MT8972 acts as master on the line then timing is provided by an MT8940. If the MT8972 acts as a slave then it extracts timing from the line and passes it on to the rest of the circuit.

The basic schematic diagram for the handset and RS232 interface is shown in Figure 4. Level shifters (typically an MC1488 and an MC1489) for the RS232 interface and a suitable transducer interface for the handset complete the design.

This particular approach could be used with any Personal Computer which can handle an RS232 link. No additional software is required and there is no microprocessor to be programmed.

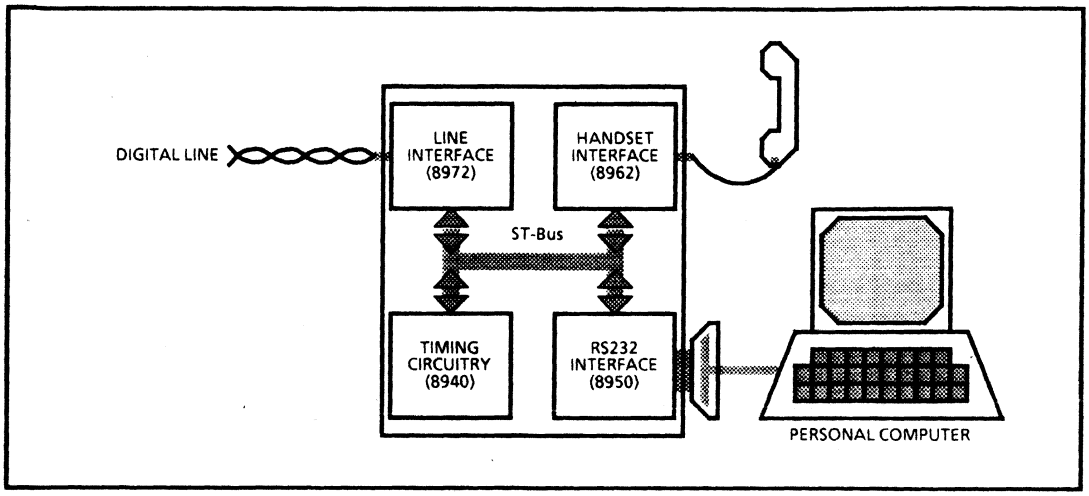


Figure 3 - Integrated Voice and RS232 Data Capability for a Personal Computer

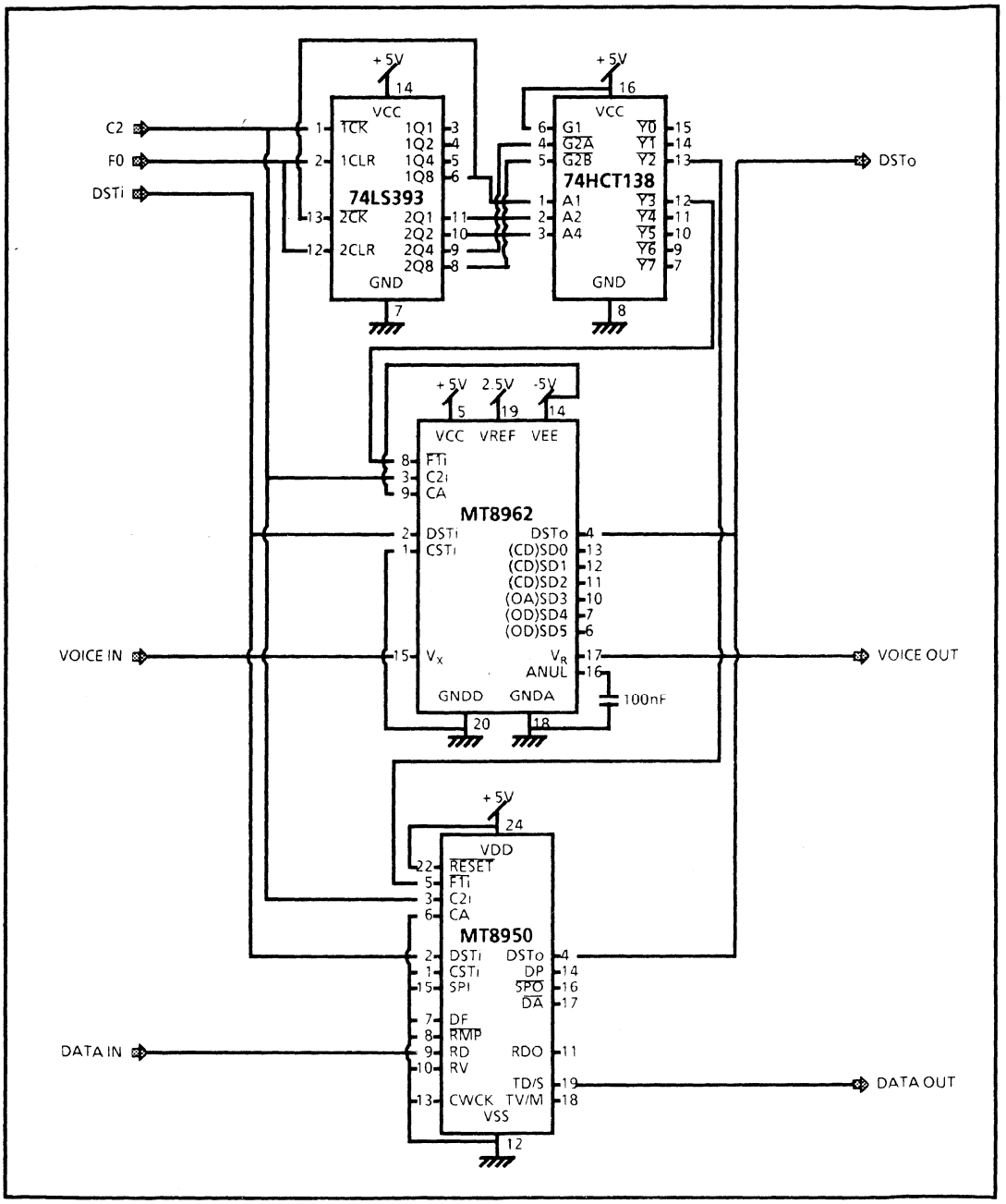


Figure 4 - Handset and RS232 Interface Circuit

Microprocessor Interface to MT8972

Figure 5 shows a simple microprocessor interface to a MT8972 in Slave Mode. A similar approach can be used for Master Mode.

The MT8972 in Slave Mode generates the ST-BUS frame and clock signals needed for the MT8981. As only channels 0 and 16 are used on the ST-BUS streams in this configuration, the A0 to A3 address lines on the MT8981 can be strapped to ground. This reduces the number of address lines needed for the microprocessor interface.

The status of the MT8972 and data received from the line can be read through the MT8981 by selecting the appropriate input stream and reading the appropriate channel. The MT8972 can be controlled and data transmitted on LOUT by selecting the appropriate memory on the MT8981 and writing to the appropriate channel. The MT8981 is used in its Message Mode here.

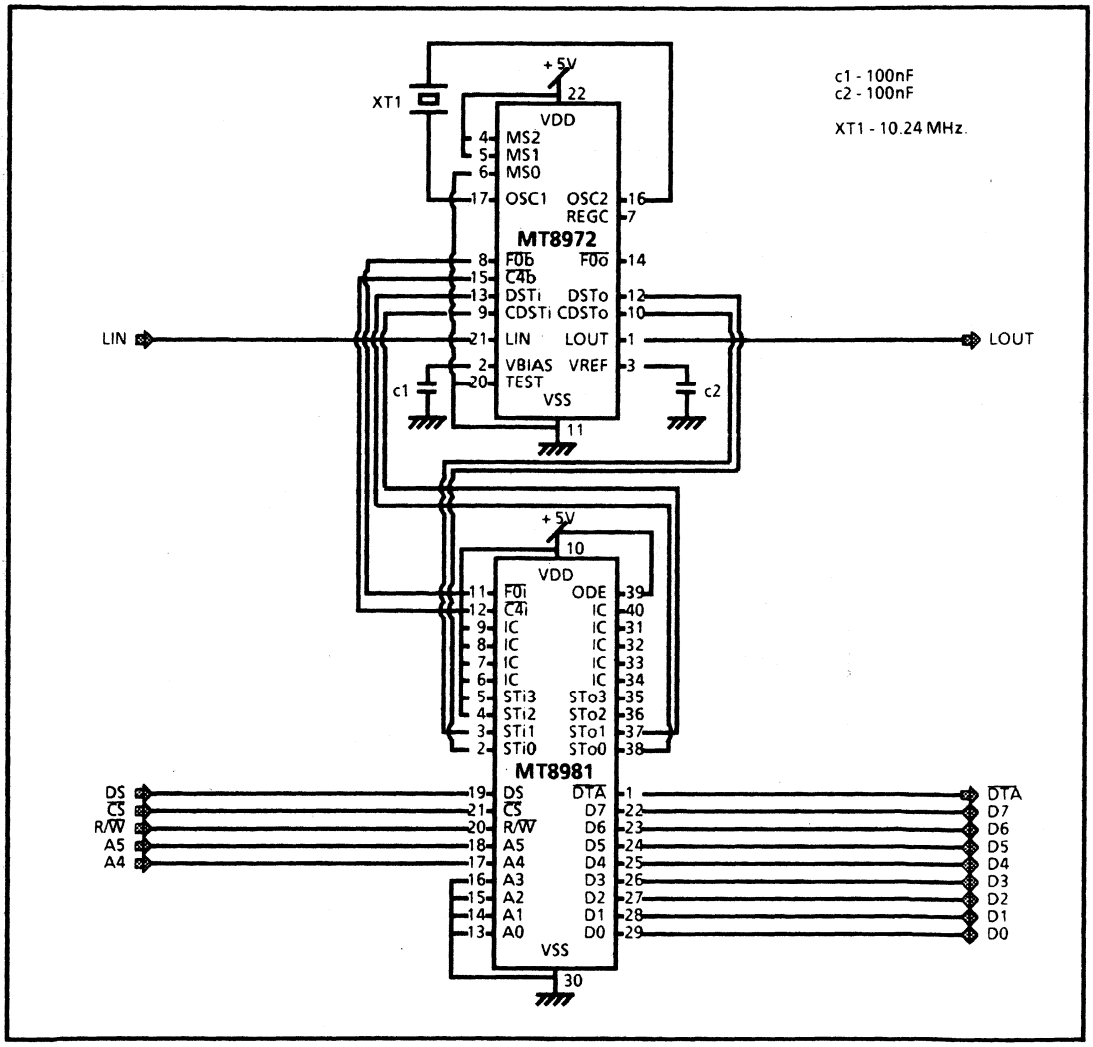


Figure 5 - Microprocessor Interface to MT8972

Digital Line Card

A digital line card can be built by chaining MT8972's together (see Figure 6).

The first MT8972 in the chain receives a framing signal from the system and generates a delayed framing signal for the second MT8972. Each subsequent MT8972 in the chain accepts the framing signal output by the previous MT8972 and generates a delayed signal from it. This eliminates the need for a timeslot assignment circuit for the MT8972's on the digital line card.

In this example data is transmitted down the lines from channels on the DSTi input stream and data from the lines is output on channels on the DSTo output stream. The MT8972's are controlled and monitored on the channels on the CSTi and CSTo streams.

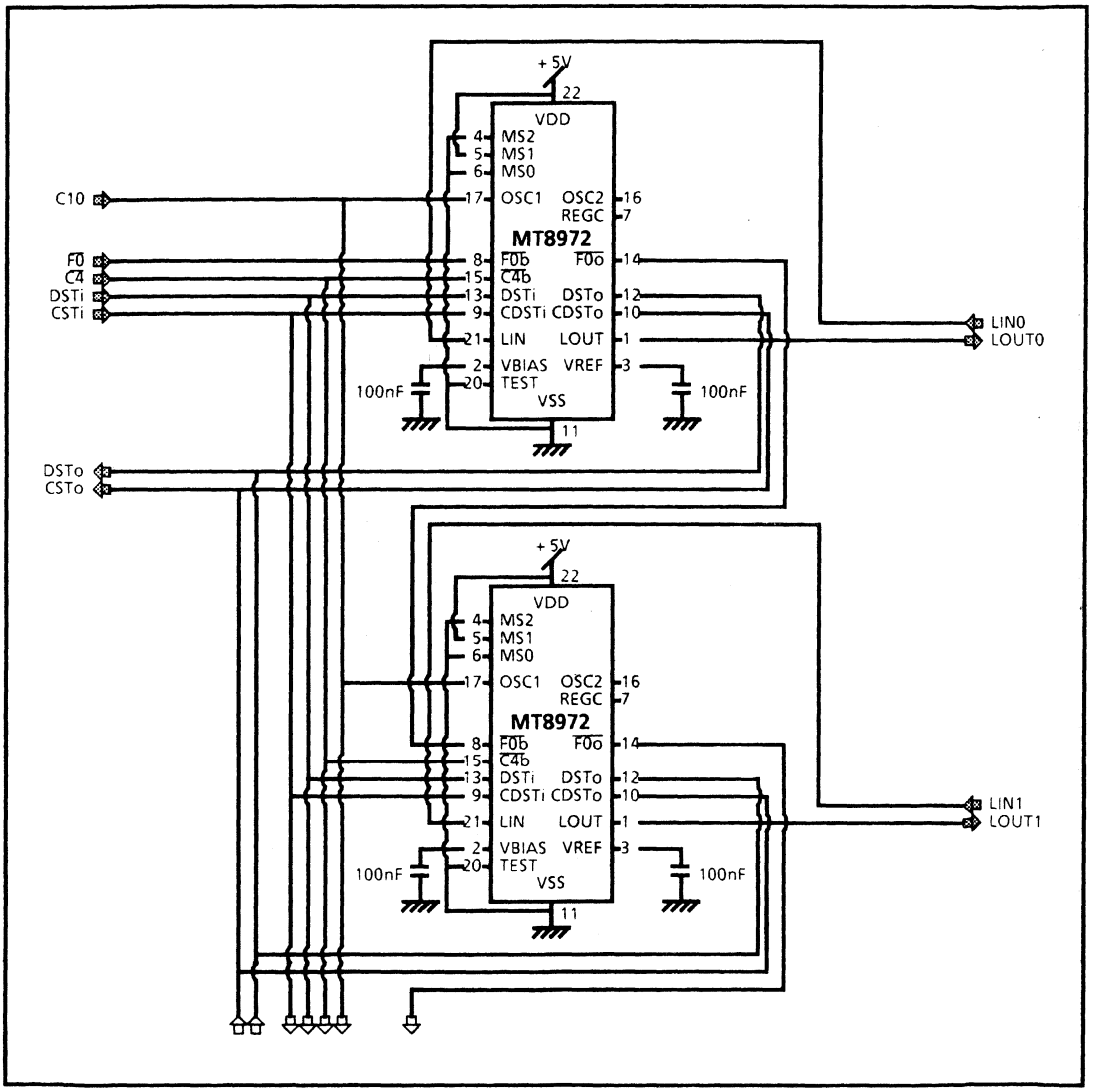


Figure 6 - Digital Line Card

MITEL

Application Note MSAN-125
Introduction to Software Complimenting the ST-BUS Family

9161-001-038 NA ISSUE 1 JUNE 1986

Table Of Contents

1.0 Abstract

Until recently, hardware costs represented the bulk of project development expenses. However, in the span of the last decade software costs exploded, in some cases accounting for over 80% of the total project development cost. Various software design methodologies have evolved which attempt to minimize the time - and thus cost - spent on developing software. Although no single technique is universally accepted, the "structured design" methodology is widely practised. The aspects common to the variations on the structured design technique include: top-down system specification, hierarchical and modular architecture, singularity of module functionality, and precisely defined module interfaces. Implicit in these principles are the concepts of information hiding and reusability of a module's functionality.

We will explain this terminology and apply the principles to an example of PABX software system design. In the course of this study, we will see how the application of the structured design principles promotes reduction of software development costs. In particular, we will focus on the application of these techniques in the design of software modules which support system hardware interfaces.

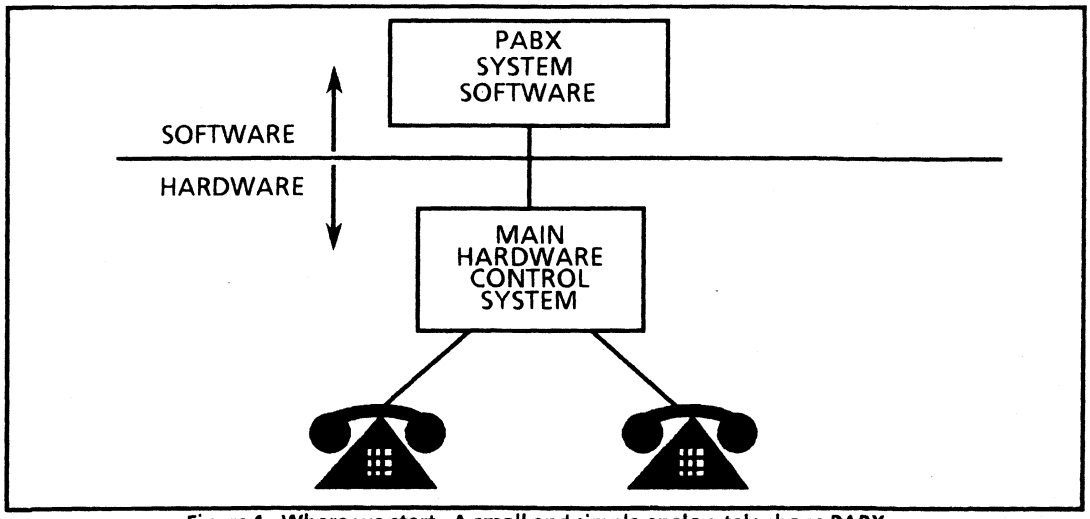


Figure 1 - Where we start - A small and simple analog telephone PABX

2.0 Overview

Once a small fraction of product development costs, software development can now dwarf other cost components. The emphasis shifted largely because, compared to hardware, software is modified or created with relative ease. As more effort was directed towards software creation, the cost of software development rose in relation to other product development costs. It was not until recently that structured software design techniques which harness these costs formally evolved.

Although structured design techniques vary in some respects, they do share a widely accepted set of underlying principles. Borrowing from the better understood discipline of hardware design, these principles parallel hardware design using integrated circuits (ICs). They advocate software systems composed of discrete, independent modules. These modules are rigorously defined in terms of their inputs, their outputs, and their functionality. Furthermore, the software module's functionality is singular.

Structured software design produces modules which are highly reusable over a number and variety of applications in a system, as well as across numerous systems. The amount of development time saved is directly proportional the number of reusable modules which exist and how frequently they are reused. Whether internal to one system, or across many systems, the net result is the same: the more often a software module is reused, the greater the reduction in the overall software development costs.

In hierarchical modular software systems, the lowest level modules are normally the most frequently reused. They provide very specific functionality required by a large percentage of the higher level modules. This is particularly true for software modules which support interaction with hardware (which we call "hardware coupled" software).

Consider, for example, a personal computer with one disk drive. In all likelihood, some software resides in the computer's operating system to interact with the disk drive. At its most basic level, this disk controller module (DCM) may physically control the motion of the read/write heads and order data transfer. At a higher level, it may logically organize the data for transmission between the disk drive and a higher level software module. Some software applications created to run on the computer will require disk input and output (I/O). Every such application will, barring an extraordinary reason, use the DCM for disk I/O. Furthermore, the DCM is readily usable in any other system which uses the same disk drive.

Hardware devices naturally request the existence of closely coupled software. After all, if a system uses particular hardware, software modules must exist to interact with it - assuming, of course, that the hardware is programmable. These hardware coupled software modules are useful in other systems which utilize the hardware with which they interact. In every such instance, the reuse of a software module saves the costs of its recreation.

We stated earlier that the number of reusable modules and the how frequently they are used directly affect how much software development time and costs may be saved. Consider hardware coupled software modules in this light. The number of existing programmable hardware devices is inummerable. Any of these devices may be used across a vast number of different systems. Consequently, software modules which couple these devices represents unlimited potential for significant time and cost savings.

The aims of this document, then, are to examine the concepts, purposes and benefits of structured software design, with particular emphasis on applying it to software which is directly coupled to hardware.

We will accomplish this in three steps as follows:

In the first step we will define the terms, philosophies and methodology of structured software design.

Next we apply these concepts to the general design of a PABX system. The aim of this exercise is to highlight the position, structure and function of hardware coupled modules in a software system.

Finally, we will design the specifications of a software module coupled to the pivotal element of the ST-BUS family architecture: the Mitel MT8980 Digital Crosspoint (DX) Switch. Here we endeavour to reveal thoughts and decisions affecting the design of hardware coupled software, as well as to illustrate how naturally these modules evolve from the hardware.

3.0 Structured Software Design Philosophy

In this section, we will review a top down, iterative approach to modular software design, paying particular attention to a specialized application of this technique: object coupled design. Object coupled modular software is software which is closely coupled to a logical or physical structure.

3.1 Modular Software

When we speak of modular software design we refer to the generally accepted software development methodology which promotes a top down, iterative design approach. The technique is summarized by the following algorithm:

Specify a module
REPEAT
    Refine the module
UNTIL (All modules are completely refined)

Underlying this apparently simple algorithm, of course, is the complexity of the design process. Although a detailed discussion is beyond the scope of this document, let us nonetheless expand on some of the main implications of this highly abstracted algorithm.

A "module" is the abstraction of a function. It is defined by the inputs it expects, the outputs it will generate, and the function it performs. A module may itself consist of zero or more subordinate modules. Each subordinate module has its own input and output specifications, some of which may be included in the definition of superior modules.

The hierarchy of subordinate modules is related by virtue of their inputs, outputs, and function. Either directly or indirectly, these attributes contribute to the operative definition of their superior modules.

One or more modules may be considered equivalent if the specification of their inputs, outputs, and functions is identical. This remains true even if they vary in ultimate implementation details. We will enforce this definition for the purposes of this document since we are primarily concerned with the design, rather than programming, aspect of software development.

To start the design process, a single system module - the "main" program - is specified. The process of designing a module involves specifying its inputs, its intended function, and its outputs. The process of defining the function which a module is to perform - "refining" the module - may spawn subordinate modules. If so, each newly generated module, in it's turn, is refined. As might be expected, the lower a module is in the system design hierarchy, the more specific and singular its functionality. The algorithm terminates when each module has been refined such that it requires no further creation of subordinates.

3.2 Object Coupled Software

An integral part of structured design strategy is to surround a logical data structure with a module of software which performs operations on that structure. No other module may (legitimately) operate on the data structure if not by way of the surrounding module. This practice is called "information hiding". We will say that a module which hides information about a structure is "coupled" to that structure.

Information hiding is based on the premise that the effect of a change to the underlying data structure is limited to the modules which operate on it. For our purposes, the greatest benefit of this strategy is the creation of generalized, highly reusable functionality. If every software module which operates on the structure does so through the interface provided by the module coupled to the object, then that functionality is reused - rather than replicated - in every instance.

For example, consider a software stack data structure. A stack is a last in, first out data structure normally coupled by a module which provides *PUSH*, *POP*, *IS_EMPTY*, and *IS_FULL* operations on the stack. Other modules may operate on the stack, but only through these stack modules. An item is *PUSH*ed to and *POP*ped from the top of the stack. A call to the module *IS_EMPTY* or *IS_FULL* returns a value to indicate whether all or none of the space on the stack is available respectively. The calling modules have no knowledge of the stack format. Consequently, they cannot create functionality to operate on it. Instead they reuse the functionality provided by the stack's module.

The object coupling strategy is not limited to logical data structures. In fact, it lends itself quite naturally to use with hardware devices. As with the data structures, we surround the hardware in question with a module of software which performs operations on it. Any other module which operates on the hardware does so only through the surrounding module. Consequently, the hardware coupled module is highly reusable. This process will, in fact, be the focus of the following sections.

3.3 Summary of Benefits

We can immediately recognize some of the benefits of object coupled software design. First, if the object is a software data structure, only the immediately coupled layer of software needs alteration should the data structure change. Secondly, if numerous applications require access to the object, each of these applications may rely on the object-coupled software to provide such access. As a result, software to access the object may be reused rather than re-created for all these applications.

The same techniques and benefits, apply quite naturally when coupling a software module to a physical device. Consider the following. Since a hardware device is designed to perform a well specified set of one or more functions, and any software designed to directly interact with the device is designed to effect performance of that set of functions, the software is innately related by overall function. Since our definition of a module includes relationship of function, it is natural to create a software module to couple the hardware.

In either case, the modules generated will be highly reusable. As we will see,this is a major factor in keeping the costs of software development down.

4.0 Application of Design Methodology

In the preceding section, we introduced some of the philosophies and goals of modular and object oriented software design. We saw the potential for large gains in software development productivity. We also saw how many of these gains can be realized in the design of hardware coupled software, and how naturally hardware components lend themselves to the design of such software.

In this section, we will embody these concepts through an example. We will apply the structured design principles to design system software modules for a private automated branch exchange (PABX). Naturally, we cannot examine the design of all aspects of such a complex system. In keeping with the emphasis of our discussion thus far, we will concentrate on those modules which ultimately spawn hardware coupled software modules. These modules will be referred to as Hardware Interface Support (HIS) modules.

Once the position of the HIS modules is revealed, we will apply structured design techniques to define their structure and function in more detail. It will become apparent that the structure of the HIS modules is largely dictated by the system's hardware elements.

To conclude this section, we will describe the typical interactions and types of data flow among the HIS and system level PABX software modules.

4.1 PABX System Functionality

A Private Automated Branch Exchange (PABX), is the center of a network of peripheral telecommunication devices. In its simplest terms, a PABX system allows communication between any two peripheral devices provided that they can sensibly communicate. For example, the PABX software would prohibit communication between a standard telephone and a digital data terminal. Before digital data sets ever came onto the scene, the PABX provided switched communications between two regular telephone sets. This is where we will begin.

Figure 1 (see front page) illustrates a very small and very simple PABX. The PABX software consists of one main module - the PABX system module. The hardware module - which we will refer to as the Main Control Module (MCM) -contains all the components necessary to support switched communications between any two telephones connected to it. The details of both the software and hardware modules will be revealed in the course of our design.

The PABX software module in Figure 1 represents the first iteration through the modular software design algorithm. In the next iteration we refine the module by defining some of its main functions. These include system maintenance (SM), call detail recording (CDR), automatic call routing (ACR), and call processing (CP). Each function is performed by a unique module, as illustrated in Figure 2.

4.2 The Call Processing Module

The call processing module is that body of software in the PABX system which sets up, supervises and terminates a device to device communication session. Let us take this module through some further design iterations, starting with decomposition into a front and back end.

The back end of the call processing module is responsible for tasks involved in supervising a call from inception to termination, but with which the user is not involved. This includes tasks such as characterizing the called device, toll denial, activating route selection (for outgoing calls), and supervising the call for feature activation until termination.

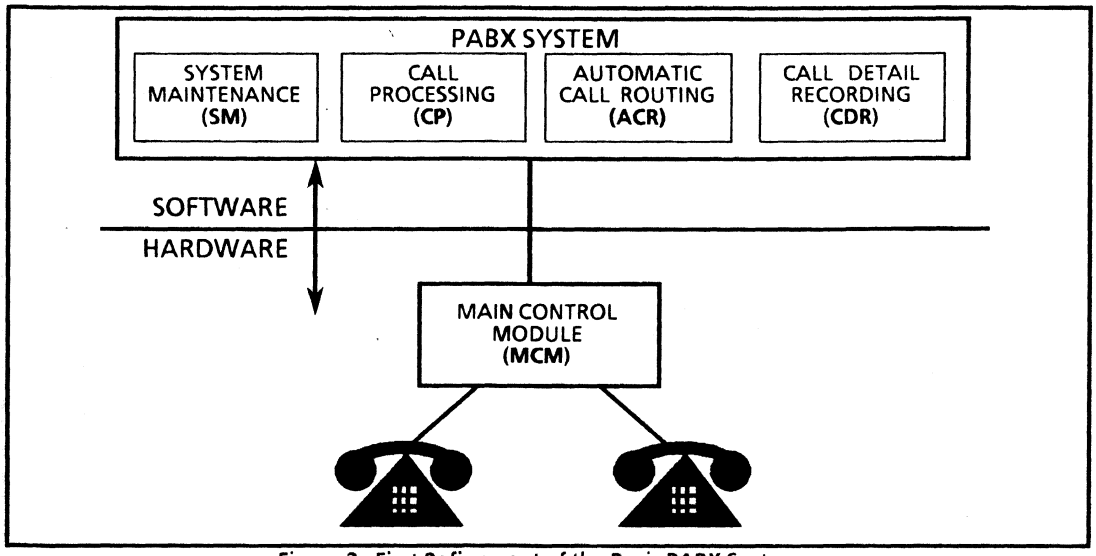


Figure 2 - First Refinement of the Basic PABX System

The front end, which we will henceforth refer to as the User Interface Support (UIS) module, supports the CP module's interaction with the caller. It performs tasks such as detecting and servicing the telephone handset being lifted (going OFFHOOK), collecting the digits being sent by the user (either dial pulse or DTMF), sending back call progress tones to the user (such as dial tone, busy, and ringing) and, ultimately, detecting when the user replaces the handset (goes ONHOOK) to terminate the call.

The UIS module demands direct hardware interaction. To achieve this, we further refine it by creating a separate hardware interface support (HIS) module. The HIS module supports the interaction protocol between the UIS and the hardware and makes the intricacies of this interaction completely transparent to the UIS module.

Although the UIS module's function is singular, it is also restricted in usefulness to the CP module. The particular telephone call interface we described above, though very useful to the CP module, is probably not so useful to any other system module.

On the other hand, the HIS module is quite useful to other modules in the system. In fact, all the modules we first described require interaction of one form or another with various system hardware elements. The hardware invariably demands precisely the same protocol. So, although each system module may use only a subset of the overall HIS module functionality, why recreate any part of it? Instead, we can take advantage of such high reusability by spawning an independent module to service all the other system modules. In so doing, every system module has transparent access to any hardware element and the HIS is created but once.

Transparency is a key consideration. It means that system modules may only communicate with the hardware through parametric messages to and from the HIS module. The intricacies of direct hardware interaction are completely hidden behind the HIS software. This concept is crucial to our definition of hardware coupled software design.

The results of our design so far are illustrated in Figure 3.

4.3 The HIS Module

Having established the position of the HIS module in the software system, let us now consider its structure and function.

The simple two telephone PABX system was adequate for the discussion thus far. However, to better study the HIS module, let us expand the PABX system as illustrated in Figure 4. This new system provides integrated voice and data sevices. Along with the standard telephones, it supports public telephone network trunks, integrated voice and data sets, T1 trunks, packet switching (HDLC) networks, and the emerging technology of the Integrated Services Digital Network (ISDN).

With the additional capabilities come additional hardware modules. The main hardware control module (MCM) of our former system still exists, but

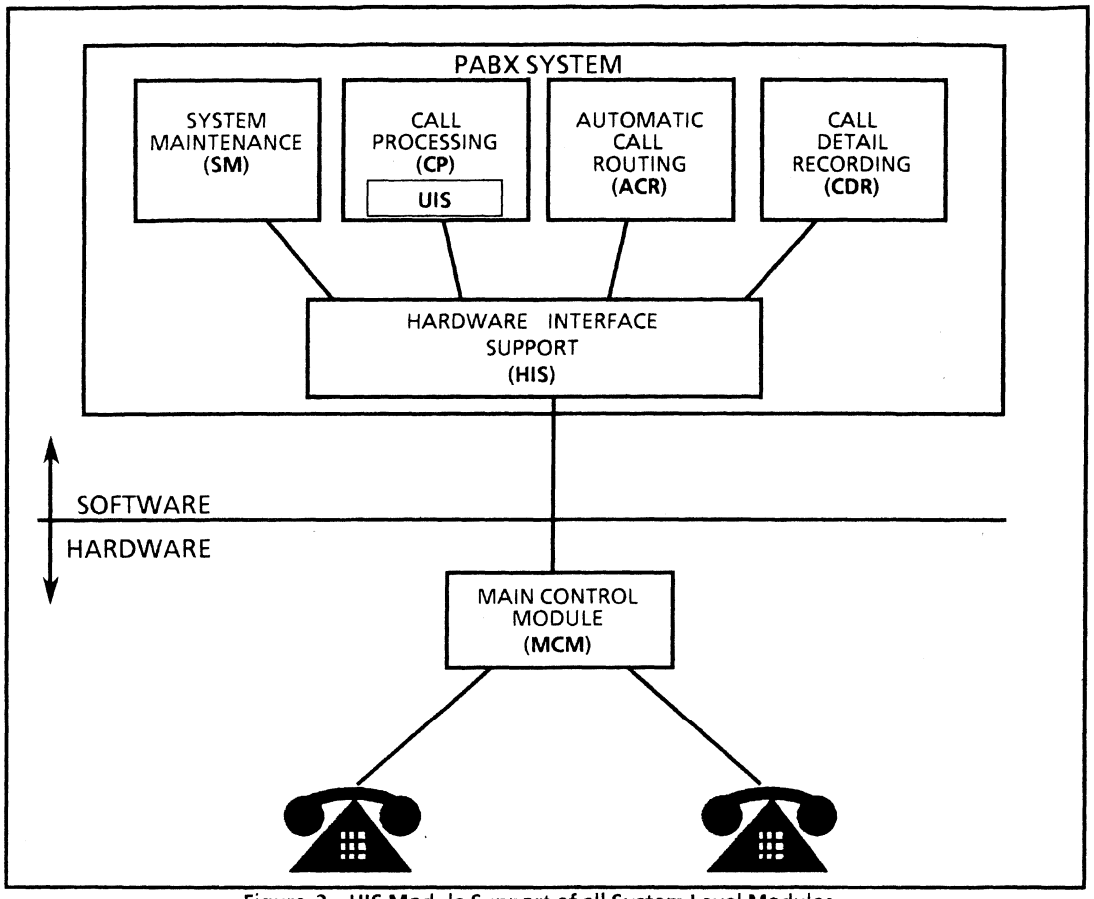


Figure 3 - HIS Module Support of all System Level Modules

has more responsibility. The MCM now controls the group of subordinate hardware modules rather than telephones alone. The MCM directs the flow of information among its subordinates as well as between its subordinates and the PABX system software.

In keeping with our hardware coupled philosophy, we decompose the HIS software module into unique HIS modules to support each different type of hardware module. Furthermore, since the software may communicate with the hardware modules only through the MCM, a unique HIS module supports interaction with the MCM for each other HIS module.

The MCM directs the flow of three types of information: switched data, device control data, and interprocessor messages. We will discuss each of these momentarily.

Since we have been partitioning along functional lines, the main control module is further decomposed into three modules. Each of these modules will service one of the three main types of information flow through the system.

Consistent with the hardware coupling philosophy, the main control HIS is correspondingly decomposed, resulting in the architecture illustrated in Figure 5.

4.4 System Integration of HIS

We have now designed to the lowest level of our HIS module. Along the way, we have seen where the HIS modules reside in the overall PABX software system architecture. We have also seen the structure and functions expected of the HIS modules. What remains is to study the interaction of the various levels of HIS and system modules.

To this end, we will study the three types of information which flows through the MCM: switched data, device control data, and interprocessor messages. We will describe in turn

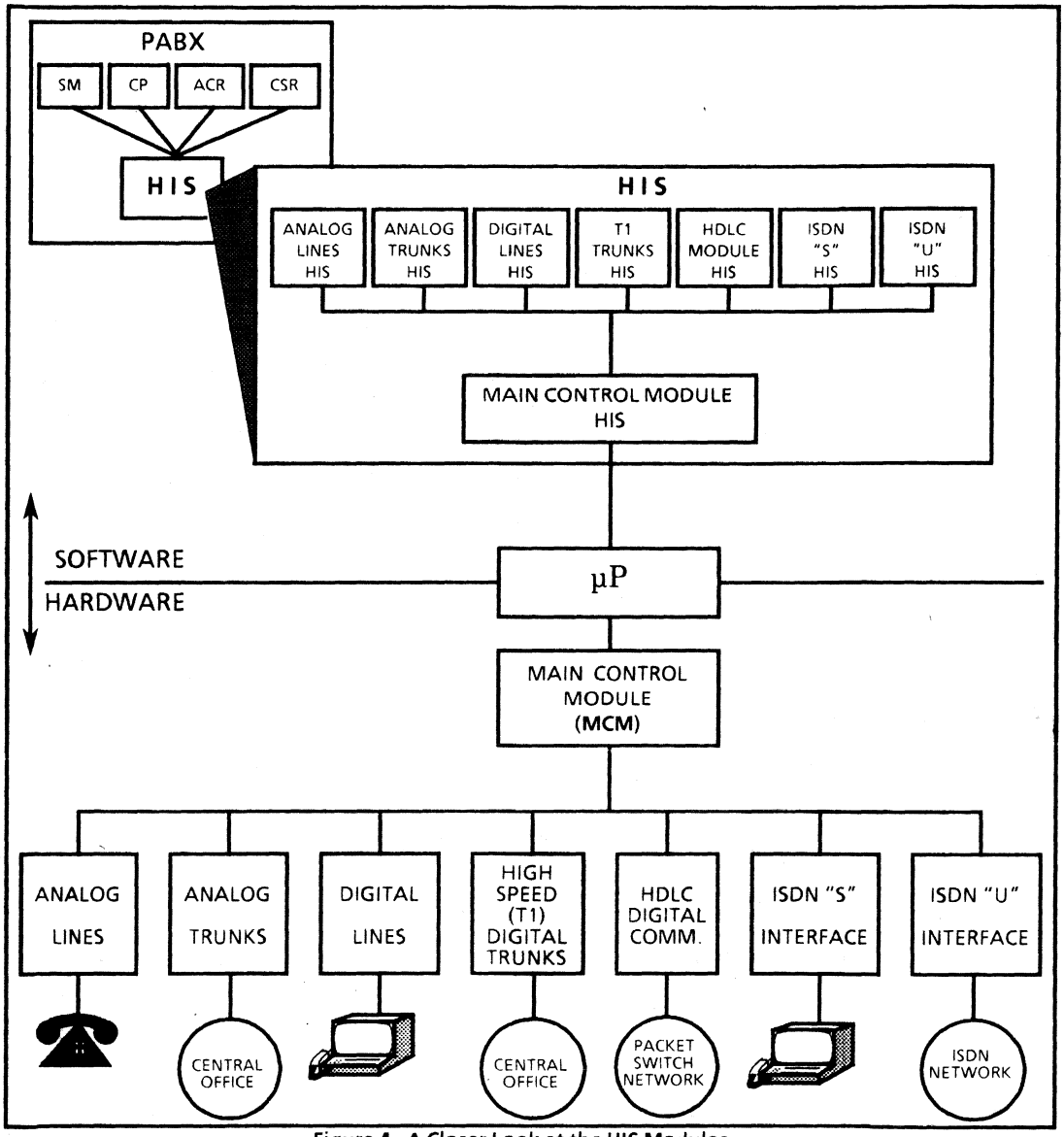


Figure 4 - A Closer Look at the HIS Modules

each type of information and the sequence module interactions which effects its flow through the system.

The discussion is in reference to Figure 6.

4.4.1 Switched Information

Switched data is unformatted raw data transferred between devices. This data includes no device control information.

The switching HIS interfaces directly with system application modules. An appropriate example of this is the CP system module. As we described earlier, the back end of the CP module makes decisions as to which devices may intercommunicate.

Once it decides that communication between devices is allowed, the CP module may use the switching HIS directly to make the necessary connections.

The lines carrying switched data are labelled SwData in Figure 6.

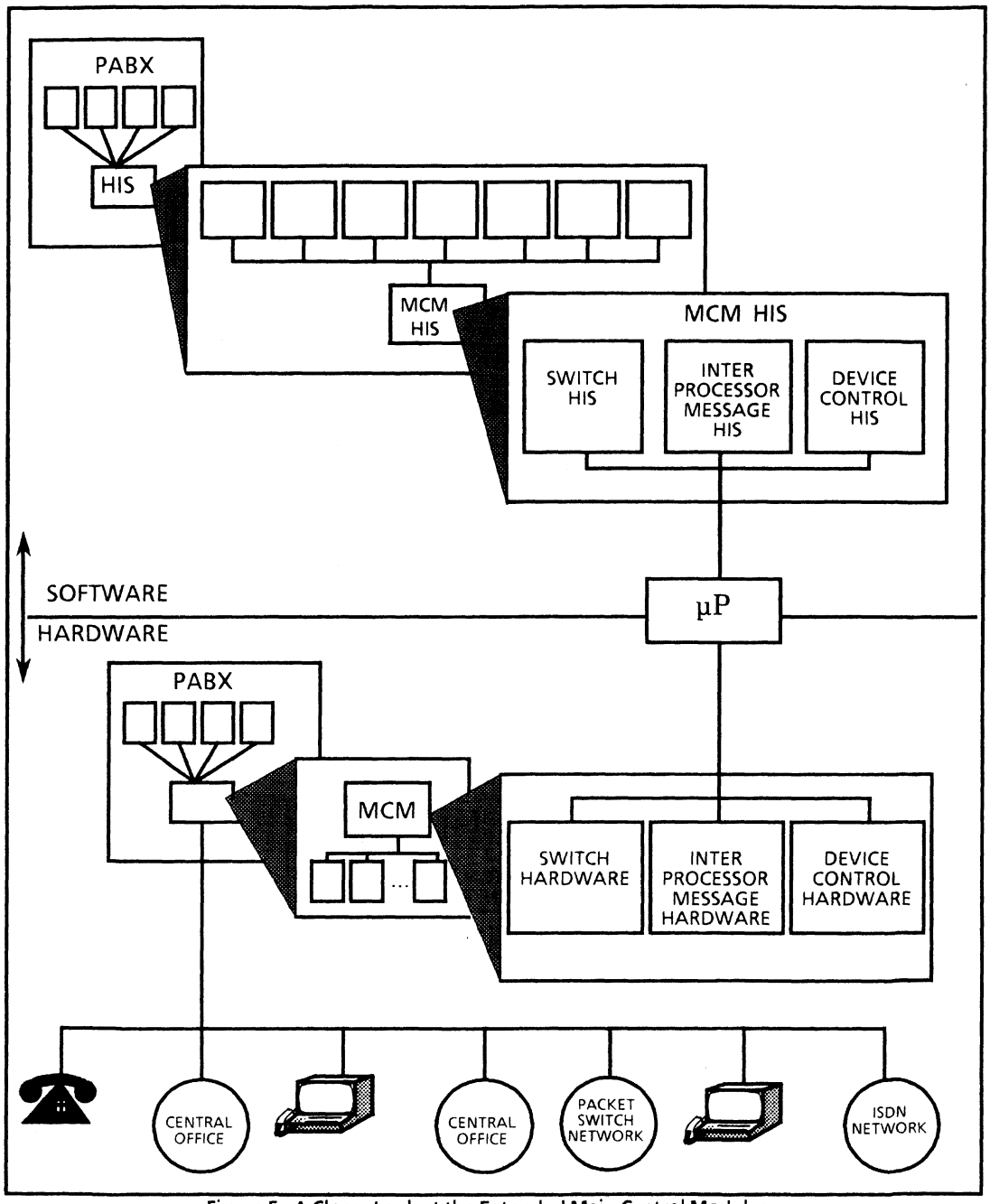


Figure 5 - A Closer Look at the Extended Main Ccntrol Modules

4.4.2 Device Control Information

Device control data includes single byte control and status infomation communicated between a device and its controlling microprocessor. Device control information normally provides interaction with hardware module having no local intelligence (i.e. no resident microprocessor).

Assume the first four lowest level hardware modules of Figure 6 - the Analog Lines, Analog Trunks, Digital Lines, and T1 Trunks modules - have no resident microprocessor.

An HIS module communicates with the hardware module it supports through the STDC module. The

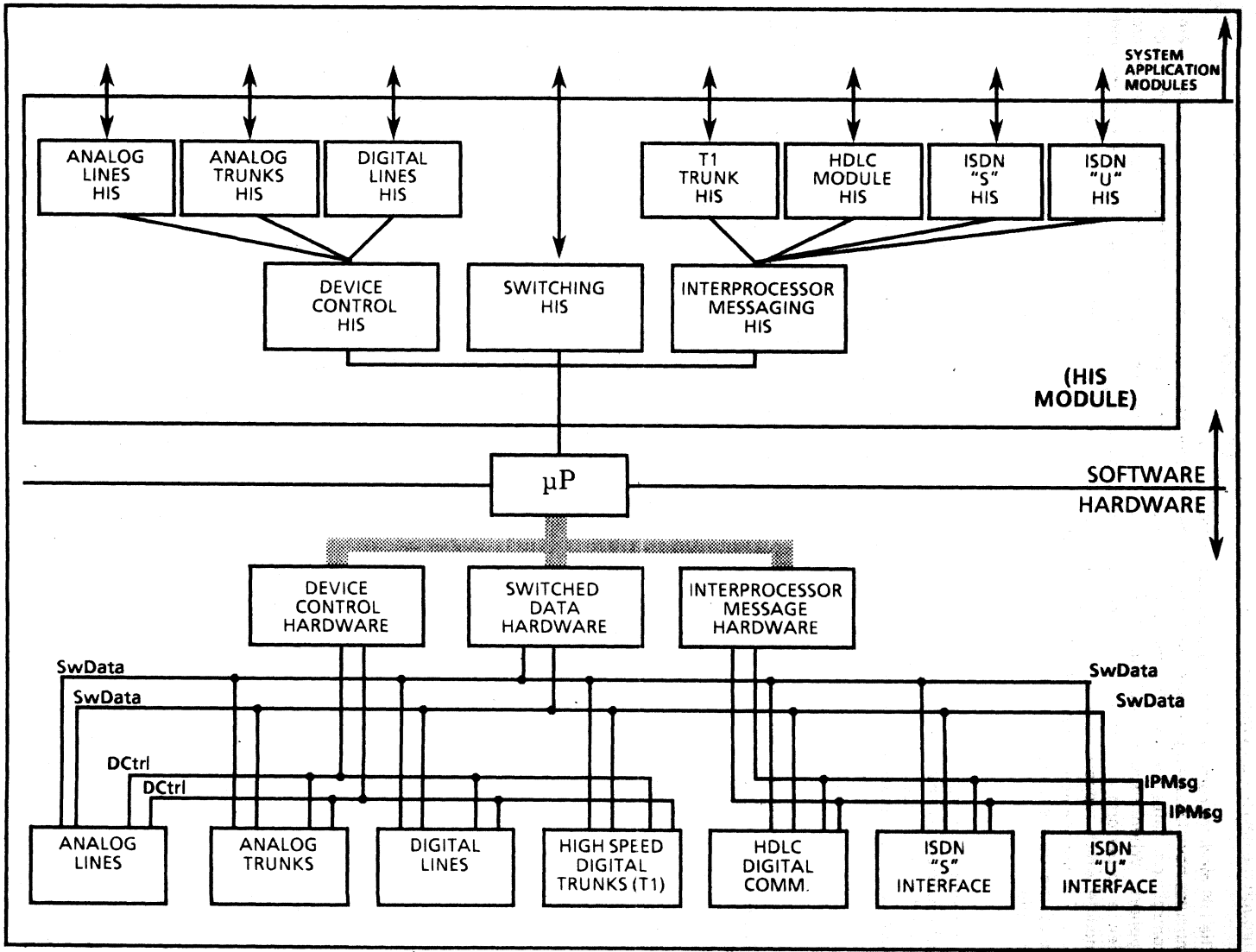


Figure 6- Integration of HIS Modules with System

HIS module sends control information to the device control register and receives status information through the device status register.

The HIS modules corresponding to these hardware modules have knowledge about the format of the control and status registers for the devices they support. When a system level module requires a device to perform a function, it invokes the HIS module which supports that device. The HIS, in turn, formats the appropriate bit pattern and sends it to the device control register via the STDC module.

The system level module requests status information by invoking the appropriate HIS module which supports that device. The HIS module reads the device status register through the use of the STDC module, decodes the appropriate status information, and returns it to the calling system module.

The lines carrying device control information are labelled DCtrl in Figure 6.

4.4.3 Interprocessor Message Information

Interprocessor messages are multiple bytes of information formatted according to some protocol. They are normally used to interact with hardware modules having local intelligence (i.e. a resident microprocessor).

Assume the last three lowest level hardware modules in Figure 6 - HDLC Network, ISDN "S" Interface, and ISDN "U" Interface modules - have resident microprocessors. An HIS module communicates with the hardware module it supports by messages to and form the IPM module.

The HIS module hides the details of the message protocol and format from the system level modules. A higher level module instructs the hardware to perform a function by invoking the corresponding HIS module. The HIS module formats the message appropriately and sends it to the hardware module using the IPM module, adhering to any protocol sequence demanded.

To obtain information from the hardware module a higher level module, once again, invokes the appropriate HIS module. The HIS module, in turn, communicates the appropriate message sequence to the hardware module. When the message with the information arrives, the HIS module extracts the relevant data from the message and communicates it to the calling system module.

The lines carrying interprocessor messages are labelled IPMsg in Figure 6.

4.5 Summary

We have concluded all the general PABX system design required to fullfill the goals of this section. As intended, we have shown where the hardware coupled modules reside, their structure and function, and overall software system module interaction.

Throughout, our design has been such that the software architecture mirrored the hardware architecture. This is an indication of how naturally the hardware demands its closely coupled software counterpart.

Furthermore, the design recalls the resemblance of modular software and hardware ICs. In the same way that a number of discrete hardware components define the individual hardware functionalities, the discrete software modules comprise the support for those functions. As individual ICs are combined and interconnected on a single hardware module, so does each HIS module consist of a hierarchy of subordinate modules.

Above all, as the hardware is designed to be reusable to the greatest extent possible, so is the software. If, for example, the hardware module supporting the ISDN "S" interface were removed and plugged into another system, the corresponding software HIS could appropriately be plugged into the software architecture of the new system. (Of course, this presupposes an appropriate level of compatibility across systems).

5.0 Design of Hardware Coupled Software

In the previous section, we stepped through the general design of a PABX software system architecture. Using structured design techniques, we developed a hierarchical system of software modules, and analysed the time and cost savings benefits of such an architecture. In this section we will design the module specifications for the center of activity in the PABX - the main control module (MCM).

The aim of this exercise is twofold: to reveal the process involved in the design of a hardware coupled module, and to reinforce how naturally the design evolves from the definition of the hardware itself.

In our example PABX system, the software and hardware architectures mirror each other. Both are a hierarchy of functionally partitioned modules. The basis of the architecture's elegance is the single, consistent interface provided by the MCM hardware interface support (HIS) module. The Mitel ST-BUS family of semiconductor components encourages modular, optimally partitioned hardware design. Although some ST-BUS components do have direct microprocessor interfaces, all ST-BUS components may be accessed through a single, consistent interface: the Mitel MT8980 Digital Crosspoint (DX) Switch.

The three main types of information which flow through the main control module (data, device control, and interprocessor messages) are key to the operation of many electronic systems besides the PABX. The DX handles the transmission of each of these types of information. It is the device of choice for each of the three modules which comprise the MCM hardware. Being the pivotal element of the PABX architecture and the ST-BUS family, we will design a hardware coupled module for the DX in this section by the following process:

1. Define the characteristics of the hardware.
2. Define the functions likely to be performed using this hardware.
3. Use the results of (1) and (2) above to specify procedural interfaces for the module

5.1 Characterizing the Hardware

Figure 7 illustrates the physical structure of the DX. Data travels in and out of the DX serially at 2.048MBps. This data stream is composed of 32 8-bit data channels on 8 input and 8 output data streams. The 8-bit data for each of the incoming streams is stored in the 32 byte Data Memory (DM) associated with each stream.

Also associated with each stream is a Connection Memory (CM). The connection memory for a stream consists of 32 11-bit words - one for each

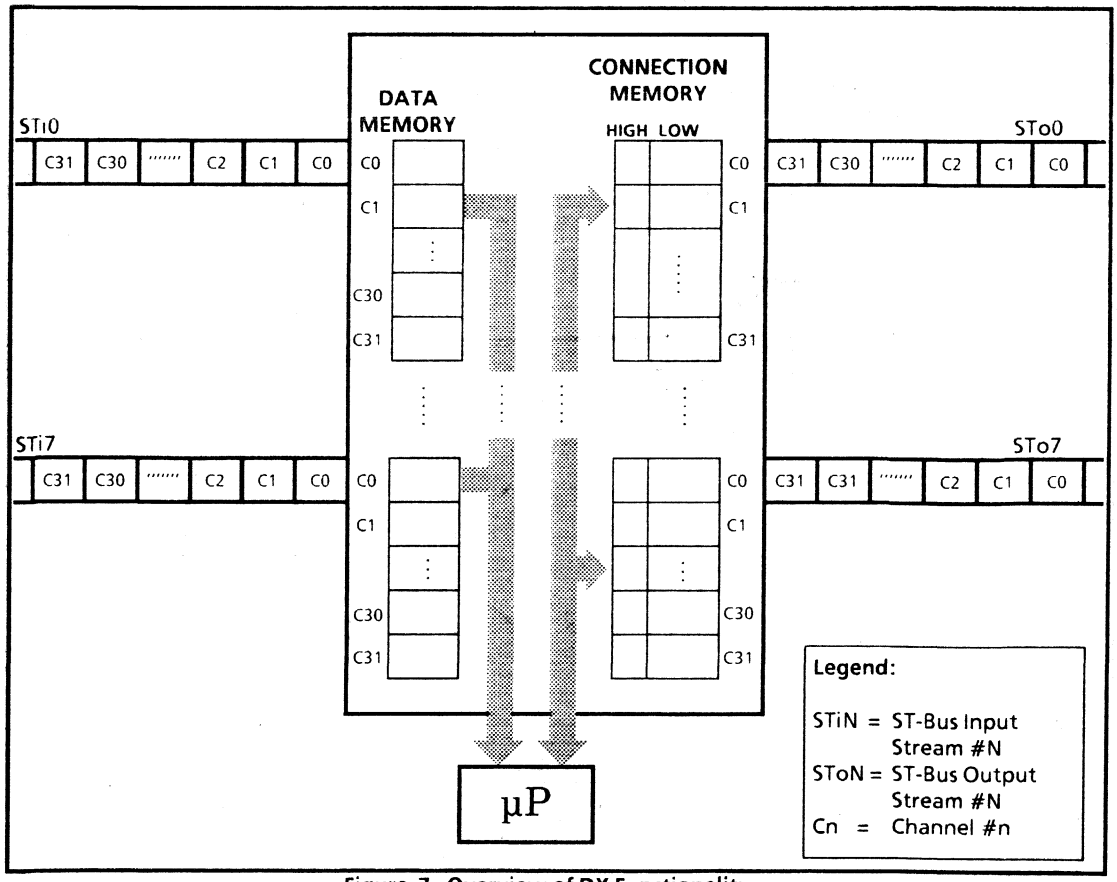


Figure 7 - Overview of DX Functionality

channel. The three high order bits of connection memory - "connection memory (CM) high" - are control bits for the channel. The low order byte - "connection memory (CM) low" - has variable meaning depending on the channel's mode.

A DX channel may be in one of two operating modes: switch and message. In switch mode, the value of CM low is used as a pointer to a data memory address for some incoming channel. In this configuration, the DX automatically switches input data from the specified channel to the output channel associated with the CM low.

In message mode, the value of the CM low byte is sent uninterpreted to the corresponding channel on the output stream. Conversely, incoming data is stored in DM and read by the microprocessor.

The controlling microprocessor may access the data and connection memories through a parallel port. The data memory may only be read. The connection memories may be read and written. These concepts are illustrated in Figures 8 and 9.

The DX also provides a control register through which the microprocessor selects stream number and memory type (data or connection) for ensuing channel read and write operations, and the device level DX mode. The device level mode is established by two bits: the message mode bit and the split memory mode bit. When the message mode bit is set, every channel of every stream is in message mode. When it is not set, the mode of each channel is determined by the CM high for that channel. The split memory mode bit, when set, places the DX in split memory mode. In this mode, all subsequent microprocessor input/output operations read from the data memory and write to the connection memory low. When not set, memory is selected by the control register's memory type field.

Any more detailed account of the MT8980 hardware is beyond the scope of this application note. For more detailed information, please refer to the MT8980 data sheet and application note MSAN-123.

5.2 Defining Software Functionality

As we have seen, the DX hardware can be in one of two modes: switching or messaging. These two modes provide three types of software functionality. In switching mode, we can provide a raw data switching function. With the DX in message mode, we can define two unique software functions: microprocessor control of ST-BUS devices, and interprocessor communications.

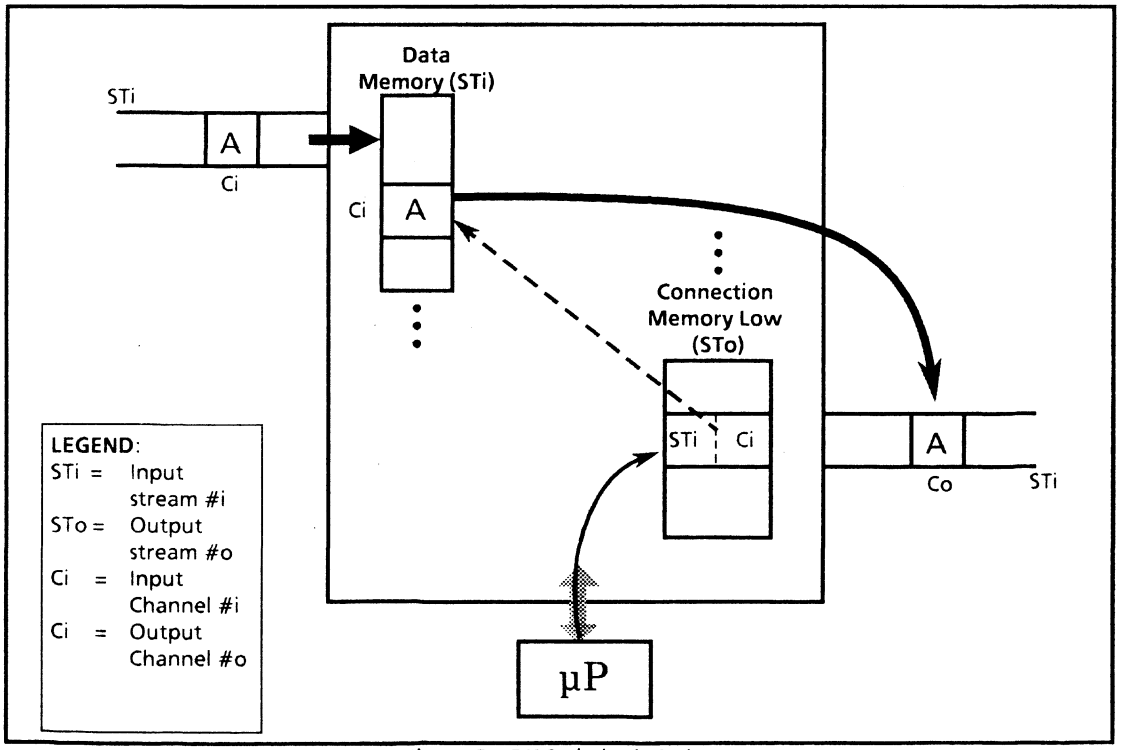


Figure 8 - DX Switched Mode

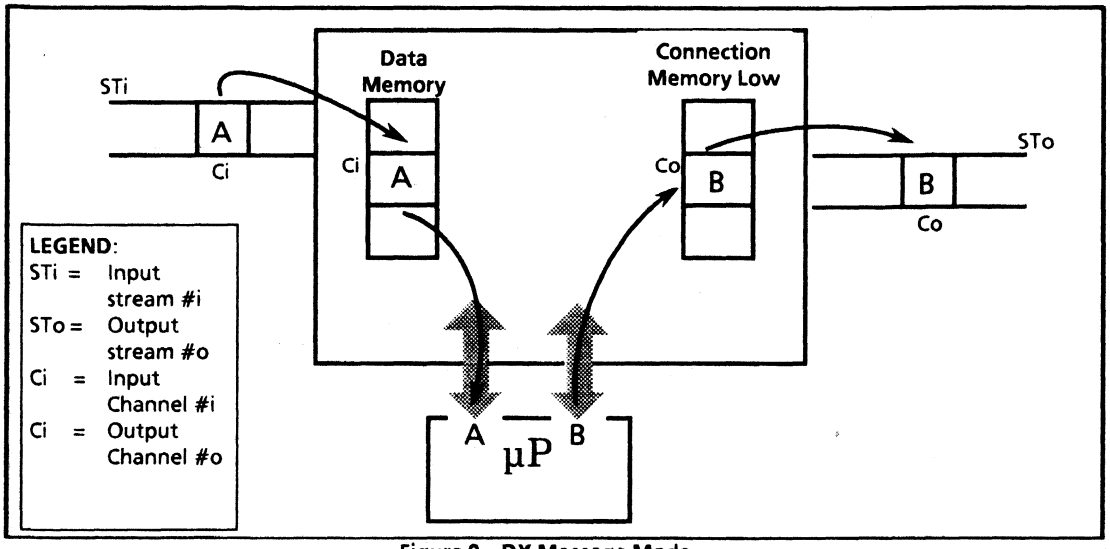


Figure 9 - DX Message Mode

To perform the data switching function, the software places the DX in switched mode and specifies the data switch paths in connection memory low. As a result, incoming serial data is automatically switched to the outgoing stream and channel specified in connection memory low.

The microprocessor ST-BUS device control (STDC) and interprocessor messaging (IPM) software functions both require the DX in message mode. They are distinguished by application rather than hardware. Whereas IPM is peer level communication, STDC is hierarchical. While IPM involves multiple byte, byte encoded messages, STDC uses single byte, bit encoded information.

Let us study Figures 10 and 11 to reinforce the distinction. Note that both diagrams refer to an "ST-BUS connection" between two devices. This connection is not necessarily a direct point to point

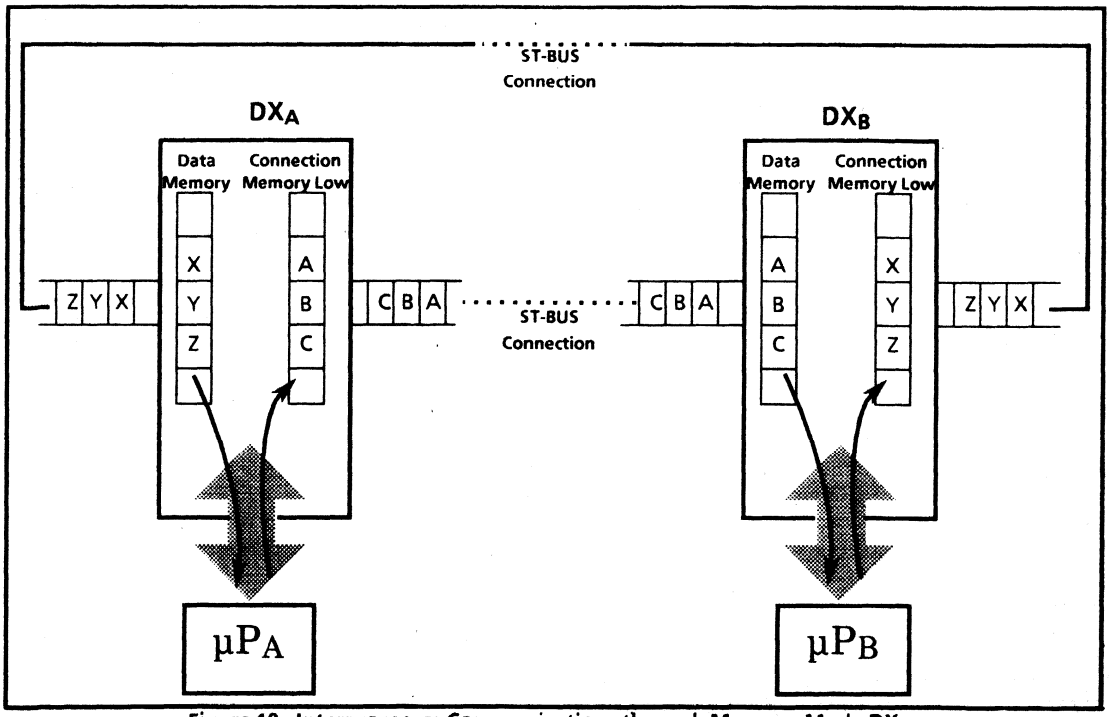


Figure 10 - Interprocessor Communications through Message Mode DX

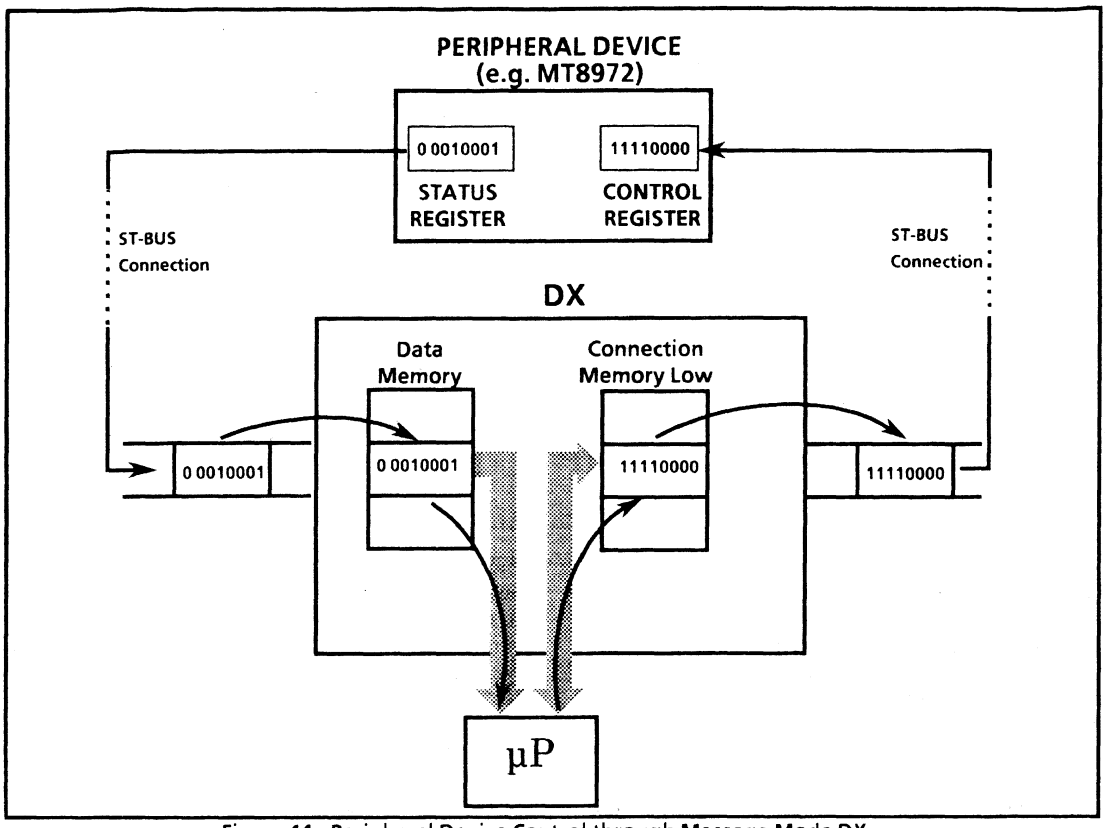


Figure 11 - Peripheral Device Control through Message Mode DX

connection. It may, in fact, represent connection through a network of local ST-BUS devices. To reflect this, we will say that the connection medium "ultimately connects" two devices.

An IPM message is represented on the DX as a block of consecutive channels. The data in the message adheres to a protocol defined between processors. Figure 10 exemplifies a configuration which provides IPM capability between microprocessors uP_A and uP_B which control DX_A and DX_B respectively. Typically, messages are up to 32 bytes long - the full length of a single ST-BUS stream. For the purposes of illustration, microprocessors uP_A and uP_B communicate by way of a three byte message protocol.

To begin the communication cycle, uP_A sends the message "ABC" into the connection memory low of DX_A. Since DX_A is in message mode, this data is output directly onto a block of output channels. These channels are ultimately connected to the incoming serial stream of uP_B. uP_B reads the message "ABC" from data memory of DX_B, and responds by storing the message "XYZ" in the CM low of DX_B. Again, since DX_B is in message mode, "XYZ" is sent directly to a block of output channels. These channels are ultimately connected to the input stream of DX_A. uP_A reads the message "XYZ" from the DM of DX_A to complete the first IPC cycle.

STDC functionality is characterized by single byte information exchange between microprocessor and peripheral device. That single byte contains either control or status information for the peripheral device. Figure 11 exemplifies a typical STDC configuration. The device illustrated is controlled by a control register and returns status information in a status register. In the configuration illustrated, data from a DX output channel is mapped onto the device control register. Similarly, the device status register data is mapped onto a DX input channel. The microprocessor sends a control byte to the peripheral by writing that byte to the DX connection memory low. Since the DX is in message mode, the control byte is sent directly to an output channel, and ultimately to the peripheral's control register. Conversely, the peripheral's status register data is sent on a line which is ultimately connected to an incoming DX channel. The microprocessor reads the peripheral's status from the data memory location corresponding to that channel.

Note the elegance of this functionality. To the microprocessor, the existence and complexity of the ST-BUS connection is completely transparent. It need only ever be concerned with the simple control/status register interface.

5.3 Module Design Specifications

Having characterized some of the physical and functional aspects of the DX, we are now ready to write the design specifications for the DX HIS module.

We will specify the modules along much the same lines as we characterized the DX. We will begin by specifying the modules that pertain directly to interaction with the hardware, followed by those that support the DX's software application characteristics.

The format of the design specification is according to the following template:

> *FUNCTION Module_Name (DX, Parameter_List)*
>
> *Description text*

The elements of the template are defined as follows:

FUNCTION -
is an optional keyword which indicates that the module name is a function. A function module assumes a value upon return from being called.

Module_Name -
is the name of the module - ostensibly as it would appear upon its invocation in software.

DX -
is a parameter sent to the module describing the DX on which the module's function is carried out. This is mandatory information, since a system could conceivably comprise a great many DX ICs.

(Parameter_List) -
is a list of zero or more parameters which define the software interface to the module. The parameters are individually separated by commas. Each parameters may either hold a valid value prior to invocation of the module or upon its return. Prior to invocation, the parameter represents information written to it by the calling software for use by the module. Upon its return, the module will communicate results or data by writing to the appropriate parameter.

Whether the parameter is communicating information to the module, from the module, or both, should be obvious from the module description.

Description text -
is a description of the function which the module performs. Where *italicized* text appears in the description text, it represents a reference to one of the module's parameters.

There are a few other intracies of the DX which are not covered by the following modules - it is not intended to be an exhaustive list. However, it is very representative of the bulk of the reusable functionality of the DX and illustrates how naturally hardware interface support modules can be defined by understanding the physical and functional capabilities of a hardware component.

5.4 Modules Based on Hardware Characteristics

The following set of routines are based on the characterization of the DX hardware. As such they provide direct hardware interaction support with the DX.

The routines fall into the following categories:

1. Control register
2. Connection memory high
3. Connection memory low
4. Data memory

These modules represent a base of software which directly interacts with the DX hardware. They are reusable by all three modules which currently comprise the MCM HIS module. As such, our MCM HIS module would be modified to reflect the fact that all interaction with the DX is done exclusively through these direct DX support modules.

Following is the specification of these modules.

5.4.1 Control Register Modules

FUNCTION IsChipInMsgMode(DX)
Queries whether or not chip level message mode is set on *DX*. Returns TRUE if set, FALSE if not.

SetChipMsgMode (DX, OnOrOff)
Sets or resets chip level message mode on *DX* according to whether *OnOrOff* has value TRUE or FALSE respectively.

FUNCTION IsSplitMemSet (DX)
Queries whether or not *DX* in split memory mode. Returns TRUE if set,FALSE if not.

SetSplitMem (DX, OnOrOff)
Sets or resets split memory mode on *DX* according to whether value of *OnOrOff* is TRUE or FALSE respectively.

SelectStream (DX, Stream)
Selects *Stream* for subsequent read/write operations on *DX*.

GetStream (DX, Stream)
Returns the number of the stream currently specified for subsequent operations in *Stream*.

SelectMem (DX, MemType)
Selects memory *MemType* for subsequent read/write operations. *MemType* indicates either DM, CM high, or CM low.

GetMemSelected (DX, MemType)
Queries which memory is selected for subsequent read/write operations. Returns coded value of memory type (DM, CM low, CM high) in *MemType*.

5.4.2 Connection Memory High Modules

FUNCTION IsChanInMsgMode (DX, Stream, Channel)
Returns TRUE if *Channel* on *Stream* is in message mode, FALSE if not.

SetChanMsgMode (DX, Stream, VChannel, Num, OnOrOff)
Sets or resets message mode on *Num* channels starting on *Channel* of *Stream* on *DX* according to whether value of *OnOrOff* is TRUE or FALSE respectively.

FUNCTION IsODEnabled (DX, Stream, Channel)
Queries whether the output driver of *Channel* on *Stream* is enabled. Returns a value TRUE if it is, FALSE if not.

ODEnable (DX, Stream, Channel, Num, OnOrOff)
Enables or disables output drivers for a block of *Num DX* channels starting with *Channel* of *Stream* according to whether the value of *OnOrOff* is TRUE or FALSE respectively.

RdConnMemHigh (DX, Stream, Channel, Num, Data)
Reads a block of *Num* bytes from *DX* connection memory high starting with *Channel* on *Stream* and store in first *Num* bytes of *Data*.

WrConnMemHigh (DX, Stream, Channel, Num, Data)
Writes the first *Num* bytes of *Data* to *DX* connection memory high for block of channels starting with *Channel* on *Stream*.

5.4.3 Connection Memory Low Modules

RdConnMemLo (DX, Stream, Channel, Num, Data)
Reads a block of *Num* bytes from *DX* connection memory low starting with *Channel* on *Stream* and stores in first *Num* bytes of *Data*.

WrConnMemLo (DX, Stream, Channel, Num, Data)
Writes the first *Num* bytes of *Data* to *DX* connection memory low for block of channels starting with *Channel* on *Stream*.

SetSwitch (DX, InStream,InChannel, OutStream, OutChannel)
Encodes the values of *InStream* and *InChannel* and stores it in the connection memory low of *Outchannel* on *OutStream* on *DX*.

GetSwitch (DX, Stream, Channel, InStream, InChannel)
Decodes the value in connection memory low of *Channel* on *Stream* of *DX* into a stream and channel number and returns decoded values in *InStream* and *InChannel*.

5.4.4 Data Memory Modules

RdDataMem (DX, Stream, Channel, Num, Data)
Reads a block of *Num* bytes from *DX* data memory starting with *Channel* on *Stream* and store in first *Num* bytes of *Data*.

5.5 Modules to Support Software Functionality

The following modules support the applications of switching, microprocessor peripheral control, and interprocessor communications described earlier. Unlike the modules described above, these modules do not interact physically with the DX. They are nonetheless part of the DX HIS module because the functions they perform directly depends upon the DX.

As with the characterization of this level of functionality, the module constituents are categorized by the functional group which they

support, namely:

1. Switching
2. Interprocessor communications
3. Microprocessor control of ST-BUS devices

The design specification for each follows:

5.5.1 Switching

Connect (DX, InStream, InChannel, OutStream, OutChannel, Num)
Creates a switched data path connection for *Num* consecutive channels on *DX* starting from *InChannel* of *InStream* connecting to *OutChan* of *OutStream*. All outgoing channels are set to message mode.

Disconnect (DX, InStream, InChannel, OutStream, OutChan, Num)
Disconnects a block of consecutive switched data path connections on *DX* starting from *InChannel* of *Instream* connected to *OutChannel* of *OutStream*.

GetConnection (DX, Stream, Channel, InStream, InChannel)
Returns the *InChannel* of *InStream* from which incoming data is switched out to *Channel* of *Stream* on *DX*.

5.5.2 Interprocessor Communications

SendMsg (DX, Message, Stream, Channel)
Sends *Message* out on block of channels starting at *Channel* on *Stream*. It is assumed that the length of the message is included as a field in the *Message* data structure.

RcvMsg (DX, Stream, Channel, Message)
Receive message from *DX* starting at *Channel* on *Stream* and return data and length of data in *Message*. It is assumed that the length of the message is a field in the *Message* data structure.

5.5.3 Microprocessor Control of ST-BUS Devices

RdDvcStat (DX, Stream, Chan, Status)
Read the Status register of the ST-BUS device connected to *Channel* of *Stream* on *DX*.

WrDvcCtrl (DX, OutStream, OutChan, CtrlByte)
Write a control byte to ST-BUS control register connected to *Channel* of *Stream* on *DX*.

5.6 Summary

As we mentioned in the preceding sections, two levels of HIS functionality reside in the DX HIS module. The lower level modules represent software which interacts directly with the hardware. The higher level does not interact directly with the hardware, but is still included in the DX HIS because its functions directly depend on the DX. In fact, the algorithms for the higher level modules, include combinations of calls to the lower level modules (see Figure 12).

6.0 CONCLUSION

Some interesting observations are to be made regarding the art of structured and object coupled design:

1. The architecture of the system reflects the algorithm for system design we presented early in our discussion. Beginning with one module - the PABX system module - the architecture ultimately is a recursive series of successive module refinements. Each module refinement of spawns a hierarchy of subordinate modules which, in turn, are either the final leaf in that branch of the

```
SendMsg( DX, Message, Stream, Channel )
{       :
        :
        SelectMem( DX, CM_LOW );
        SelectStream( DX, Stream );
        SetChanMsgMode( DX, Stream, Channel, Message.Length, TRUE );
        WrConnMemLo( DX, Stream, Channel, Message.Length, Message.Data);
        ODEnable( DX, Stream, Channel, Message.Length, TRUE );
        :
        :
}
```

Figure 12 - Sample of Psuedo Code for an HIS Module

hierarchical tree, or the root of their own subordinate hierarchies.

2. Each group of modules subordinate to a parent module are related by a common goal: to effect the overall functionality of the parent module. This recalls the analogy between software and hardware architecture wherein a series of ICs - each with its own specific functionality - is glued somehow on a hardware module for the sake of performing a higher level function.

3. This hierarchy of modules evolves naturally from the definition of the intended functionality of a module, particularly in regards to hardware coupled software. Other software modules are thus provided a transparent interface to the system's hardware modules.

4. Most importantly, since each module is created for the purpose of performing an expressed functionality, it is potentially reusable. Thus, reduction of software development time and costs is an innate part of the structured design methodology.

We have seen some software design ideas that have the potential to drastically reduce the time required to develop software.

Modular and object coupled software design produce highly reusable modules of software. These modules can be designed to function in much the same way as hardware ICs do. They are independent modules with precisely specified inputs, functions and outputs. These can be used in conjunction with other similarly designed modules to produce systems of various applications. A software systems designer may, therefore, reuse existing functionality rather than unneccessarily recreating it.

We have also mentioned that the amount of software development time saved is directly proportional to the amount of widely reusable software. In the case of hardware components, which are highly utilized, the existence of object oriented software modules for the components results in a time saving proportional to the number of such devices being used.

Future application notes will address the detailed design and implementation of object oriented software for specific Mitel Semiconductor devices. Our aim in this effort is to provide the Mitel Semiconductor customer with a practical, highly reusable library of tried and proven functionality. This will further enhance the simplicity of system design offered by the optimally partitioned digital communications devices of the ST-BUS family.

Application Note MSAN-126
ST-BUS™
Generic Device Specification (Rev. A)

9161-001-032 NA ISSUE 1 AUGUST 1986

Table of Contents

1.0 Introduction

As systems become more complex, the trend in system design has been to partition circuitry into well defined functional blocks. Such partitioning localizes circuitry performing a particular function to a specific location in a system, thus promoting modularity. Modularity is an important consideration, particularly for flexibility in system configuration. Systems with unique configurations for different situations or uses are economical to design as well as being attractive to the customer. Modularity is also a good defence against obsolescence. The amount of investment in a system design makes it expensive to throw away, especially when only portions may be outdated. This is avoided by improving the outdated portions and keeping the rest of the system. Both of these design philosophies can only be implemented if the system is designed modularly from the beginning.

It is necessary to have a well defined, effective means of communication and information transfer between modules (the term information is used here because it can apply equally to audio, video, control information or data - modern systems are increasingly integrating all three). The definition of a common interface between functional blocks eases the addition of new circuitry to a design. Such an interface should be simple, to allow modules to have a wide range of complexity. The interface should be capable of being overlayed by higher levels of communication protocol such as High Level Data Link Control (HDLC), for instances where communication needs are more demanding. There is no need to constrain module design where such a protocol is not needed.

Mitel Semiconductor has defined the ST-BUS (Serial Telecom Bus) with the above requirements in mind. It is simple to interface to, and can handle all four

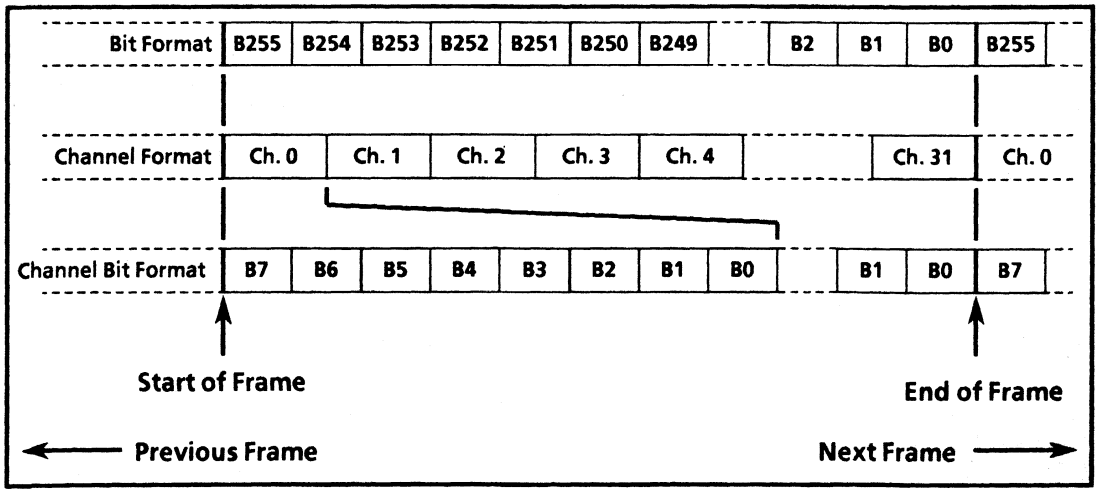


Figure 1 - Frame and Channel timing for ST-BUS, including eight bit Telecom partitioning

types of information mentioned, when the information is digitized. The ST-BUS Generic Device Specification presented in Table 1 of this document encompasses the "worst case" timing parameters of existing ST-BUS components. New ST-BUS compatible components or circuits must conform to these minimum and maximum timing specifications, or be better, to ensure compatibility with all components and systems that already exist. A system designer may use these overall component timing specifications to aid in the interconnection of ST-BUS devices.

2.0 ST-BUS Form and Signals

The ST-BUS is a high speed, synchronous serial bus for transporting information in a digital format. The use of serial streams minimizes the printed circuit board area needed for information transfer between functional modules. Fewer tracks, backplane connections, and intra-shelf cables are needed compared to systems that use parallel paths. These considerations become critical in systems that have a high information flow density, with many simultaneous communications occuring between functional modules. At the integrated circuit level, the benefits of using a serial interface on an IC are reduced pin count, improved reliability and decreased power dissipation.

The signals required to interface to the ST-BUS are:

i) A framing signal for frame alignment
ii) A clock signal for bit timing
iii) Serial information streams

The aggregate rate of the ST-BUS information stream is 2.048 Mbit/s. This stream is divided into frames, each frame having a period of 125 μs, for a frame rate of 8000 frames/s. The start of each ST-BUS frame is indicated by the framing signal (frame pulse). Each frame is divided into 256 bit periods, with bit timing provided by the clock signal (Figure 1). This information stream could be considered a single 2.048 Mbit/s communication channel between two points, however, the full 2.048 MBit/s digital bandwidth is not needed for many applications. It is therefore useful to divide this 2.048 Mbit/s channel into multiple, lower bandwidth channels. This makes it possible to share the capacity of one serial ST-BUS stream among several channels, referenced to the frame pulse, to improve system efficiency and economy. This technique is called Time Division Multiplexing (TDM).

As an example of a lower bandwidth requirement, transferring voice down a digital channel in a telecommunications application requires a digital bandwidth of 64 kbit/s. This value is obtained from the following facts about digitizing voice:

a/ The normal voice band has an upper frequency bound of 3.5 kHz to 4 kHz, through the telephone network.
b/ Voice may be translated to digital format by taking a sample of the analog voice signal and producing an eight bit code from the sample. One type of encoding is called Pulse Code Modulation (PCM). An eight bit PCM sample contains polarity and amplitude information.
c/ All the information in the original analog signal can be replicated from the digital information if enough samples are taken. To retain all of the information, sampling must be performed at twice the highest frequency contained in the signal being digitized. In this case sampling must be performed at 8 kHz. 8000 samples of eight bits each, per second, is 64 kbit/s; the digital bandwidth of normal voice transmitted through the public telephone network.

Note that the sampling rate for voice is equivalent to the frame rate of the ST-BUS. If an ST-BUS frame were divided into eight bit bytes, one ST-BUS frame could contain 32 of these portions, equivalent to 32 PCM encoded voice samples. This translates into 32 channels with a 64 kbit/s digital bandwidth, enough for 32 simultaneous digitized voice channels. See Figure 1 for a typical representation of an ST-BUS frame and how it may be divided into sub-channels (in this instance 64 kbit/s channels).

A convenient method of constructing sub-channels of various sizes is to select a minimum channel size and create larger channels using increments of the minimum channel size. With 64 Kbit/s channels being used as the basic building block, paths of from 64 kbit/s to the full 2.048 Mbits/s can be constructed, in 64 kbit/s increments. It should be remembered, however, that a channel can have a bandwidth as low as 8 kbit/s (1 bit/frame). One frame can carry 256 of these 8 Kbit/s channels.

For a number of different nodes to source information onto a single ST-BUS stream, three-state buffers must be used. All outputs but one must be in the high impedance state, so that no more than one device drives the bus at a time. The upper bound on the number of sources is determined by definition of the number of channels, the output drive of the source node with

the least current driving capability, and the capacitance of the track and/or wire on which the stream is carried. In the example of voice transmission, the definition of the number of channels per stream is 32, allowing a maximum of 32 channel sources.

The number of receivers on one ST-BUS stream is also limited by the source node with the least output drive capability, and by the capacitance of the wire and/or track carrying the stream. Access to a particular channel or channels is achieved by referencing the frame pulse and using the clock signal to position the access.

3.0 Clocking Signals

The ST-BUS defines two standard clock frequencies. Either one is used for supplying ST-BUS components' internal timing needs, but only one is required at any one time by a particular component (some components are designed to select either clock speed). The currently defined clock frequencies are 4.096 MHz and 2.048 MHz. These clocks have a specified relationship with frame timing and bit timing. This relationship is shown in Figures 2, 3, 4, 5 and 6.

4.0 Alignment Signals

There are two main types of alignment signals (also called Frame Pulses). One type is a pulse that always occurs at the start of a frame (Type 0). ST-BUS components that use this signal use it as a reference and then use the clock input to determine when to receive or transmit information on the serial stream.

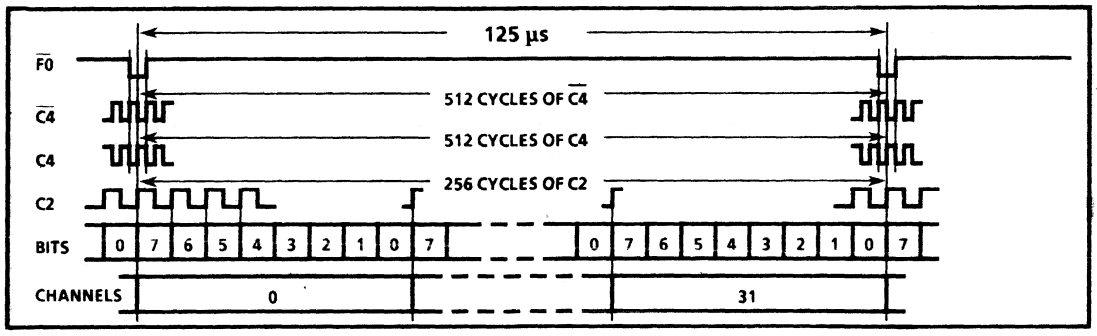


Figure 2 - F0 and Clock Alignment

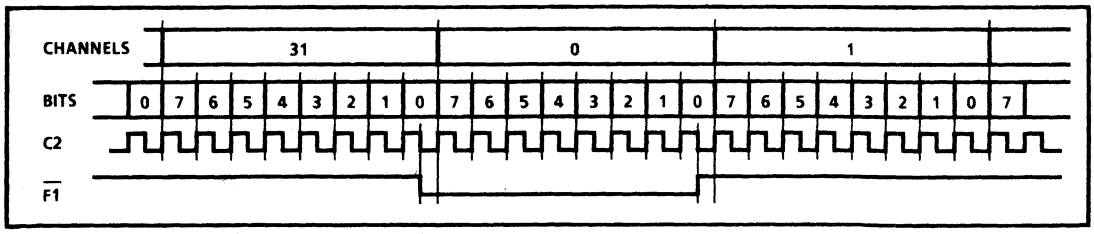


Figure 3 - F1 Alignment

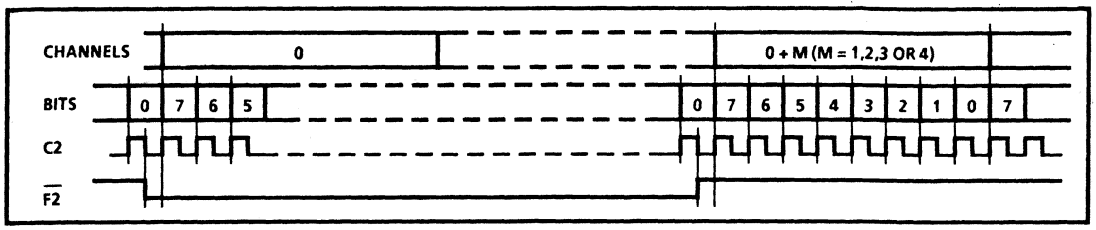


Figure 4 - F2 Alignment

The other type of Frame Pulse (Type 1) is similar to a chip enable (Figures 3 and 6). This pulse must span the entire ST-BUS channel time in which an ST-BUS component is to receive or transmit serial information. A variation of the Type 1 frame pulse (Type 2) is required for some components that need more than one channel time slot per frame (Figures 4 and 6). Type 1 and Type 2 frame pulses are usually generated by external time slot allocation circuitry that has a Type 0 Frame Pulse and a clock signal as its input.

5.0 Information Streams

The information stream is the serial stream on which information is carried between ST-BUS components. An information stream can be output entirely from one device (an MT8980 output), or

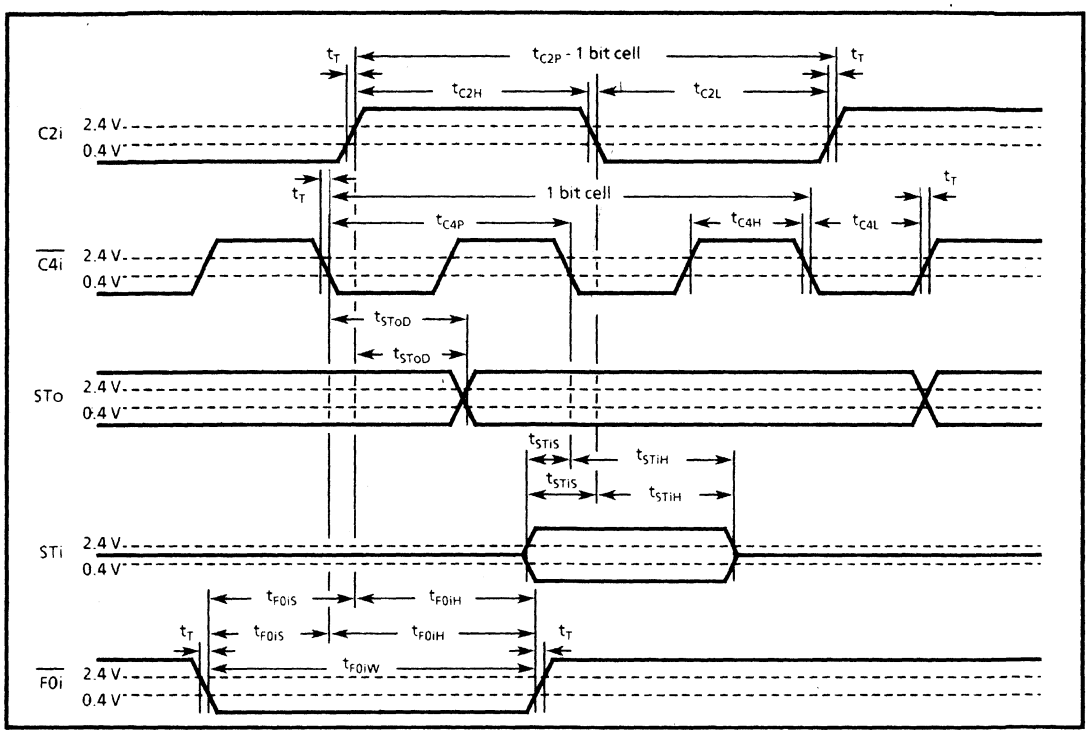


Figure 5 - ST-BUS Component Timing

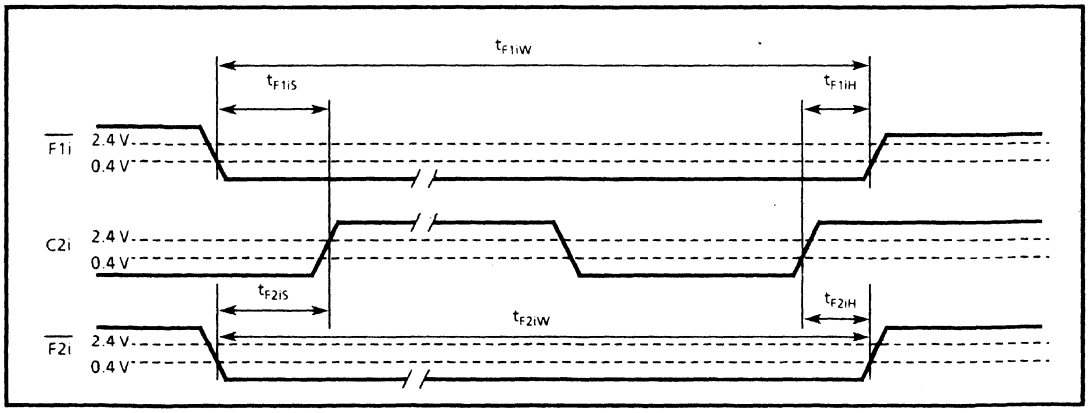


Figure 6 - Other types of Frame Pulses

Table 1 - Worst Case Component Timing† Specification

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
1	Clock C4 /$\overline{C4}$ period*	t_{C4P}	243.9	244.1	244.4	ns	
2	Clock C4 /$\overline{C4}$ High width	t_{C4H}	110	122	134	ns	
3	Clock C4 /$\overline{C4}$ Low width	t_{C4L}	110	122	134	ns	
4	Clock C2 period*	t_{C2P}	487.8	488.3	488.8	ns	
5	Clock C2 High width	t_{C2H}	220	244	268	ns	
6	Clock C2 Low width	t_{C2L}	220	244	268	ns	
7	$\overline{F0i}$ Set Up Time	t_{F0iS}	50		150	ns	
8	$\overline{F0i}$ Hold Time	t_{F0iH}	50		150	ns	
9	$\overline{F1i}$ Set Up Time	t_{F1iS}	50		150	ns	
10	$\overline{F1i}$ Hold Time	t_{F1iH}	50		150	ns	
11	$\overline{F2i}$ Set Up Time	t_{F2iS}	50		150	ns	
12	$\overline{F2i}$ Hold Time	t_{F2iH}	50		150	ns	
13	$\overline{F0i}$ width	t_{F0iW}	200		300	ns	
14	$\overline{F1i}$ width	t_{F1iW}	3.903		3.910	μs	
15	$\overline{F2i}$ width	t_{F2iW}	3.903		15.64	μs	
16	STo Delay Level 1 Output	t_{SToD}	20	90	125	ns	C_L = 50 pF
17	STo Delay Level 2 Output	t_{SToD}	20	90	125	ns	C_L = 150 pF
18	STo Delay Level 3 Output	t_{SToD}	20	90	125	ns	C_L = 350 pF
19	STi Set Up Time	t_{STiS}	30			ns	
20	STi Hold Time	t_{STiH}	224			ns	
21	Transition Time	t_T			11	ns	

†Timing is over recommended temperature range (0 °C and 70 °C) and recommended voltage range (5 V ± 5%)

*These tolerances are required by voice codecs to meet CCITT G.712 Method 2. Other devices have less stringent requirements.

built up from the individual channel outputs of multiple devices (for example: a number of MT8960 Voice Codecs, or multiple MT8980 Digital Time Space Switches). Most ST-BUS components transmit status information and receive control information, as well as information for processing, on ST-BUS information streams.

6.0 Worst Case Timing Parameters

Table 1 contains the worst case timing parameters that must be met by any ST-BUS device. Devices may be better than this specification, but they may be no worse. The definition of what is better or worse is dependent on the perspective taken, so several typical examples shall be described to clarify this.

The typical C4 clock period is 244.1 ns. The smallest range about this typical value that can be tolerated by any of the existing ST-BUS devices is from a minimum of 243.9 ns to a maximum of 244.4 ns. No ST-BUS device can have a narrower range than this, however, a wider range is acceptable (eg. minimum 240 ns to maximum 250 ns). A system designer can be sure that if a clock is provided with a tolerance that is within the worst case tolerances in Table 1 for C4, it will be good enough for all ST-BUS devices.

The perspective is similar for other parameters with both a minimum and a maximum specified, except for the STo Delay (Parameters 16, 17 and 18 in Table 1). For STo Delay, there is an acceptable window that no device may be outside of. There are three values of STo Delay, distinguished by load capacitance. This reflects the varying drive requirements of ST-BUS devices. Almost all ST-BUS devices available from Mitel Semiconductor at present have Level 2 STo outputs. An example of a device that does not require greater drive capability is the MT8994/5 Digital Phone chip, which is

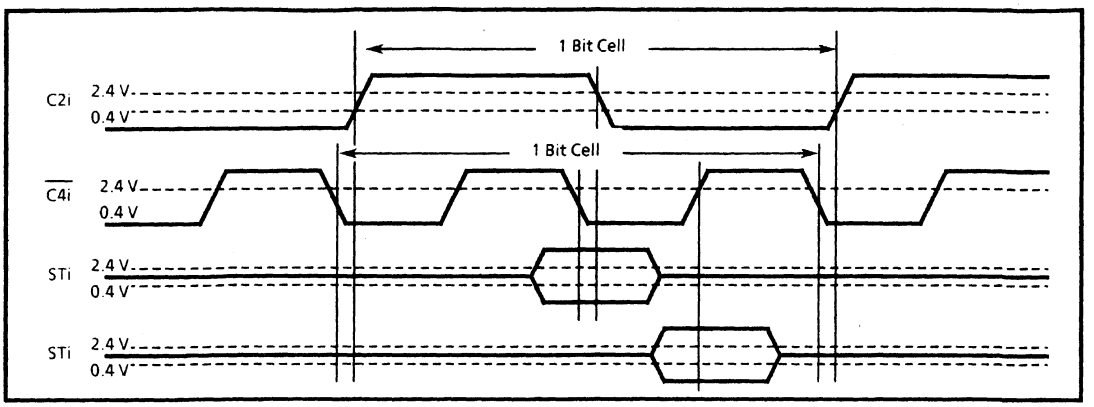


Figure 7 - Mitel ST-BUS Component Sampling Points

designed for an isolated environment. Because this device does not need to support many channels, there is no need to provide high current output drivers.

For the next two parameters in the table (STi Set Up Time and STi Hold Time), it is acceptable for a device to have smaller minimums, but not to have larger minimums. It is interesting to note that all ST-BUS devices provided by Mitel have either better STi Set Up Times or better STi Hold Times than are shown here. This is because ST-BUS device inputs are either sampled at the halfway point in a bit cell or at the three quarter point in a bit cell (Figure 7). The STi Set Up and Hold times in Table 1 are with respect to the halfway point in the bit cell, and are defined to accommodate both sampling points.

Devices that are sampled at the half way point will generally have better STi Hold Times (smaller than 224 ns) and devices sampled at the three quarter point will have better STi Set Up Times (less than 30 ns; usually negative). This negative set up time attribute can be useful in meeting overall system timing requirements when using ST-BUS devices in particular system architectures. As such, future Mitel ST-BUS devices are likely to have a negative set up time, with respect to the halfway point of the bit cell.

The maximum transition time between logic levels of a signal input as a clock or frame pulse, t_T (Parameter 21), can be no less than the maximum time specified in Table 1. The transition time on an STi input is included in set up time or hold time specifications, because the information on this input is sampled.

7.0 Nomenclature

A nomenclature has been created to quickly identify ST-BUS signals

7.1 Clock Signals

A bar above a clock name means that the clock has a falling edge at the frame boundary. Examples of clock signals are C4i, C2i, E8Ko etc. The meaning of each letter or digit in the clock name is as follows:

1) Clock Type
   C - ST-BUS system clock.
   E - extracted or derived clock associated in some way with a received digital trunk or line.
2) Frequency
   Approximate frequency in megahertz (kilohertz if K added).
3) I/O Type
   i - Input.
   o - Output.
   b - Bidirectional.

Example: E 1.5 i

Extracted 1.544 MHz Input

7.2 Framing Signals

A bar above a signal name means that the signal is active low. Some examples of Framing Pulse names are F0i, F1o, F2b etc. The meaning of each letter or digit in the name is as follows:

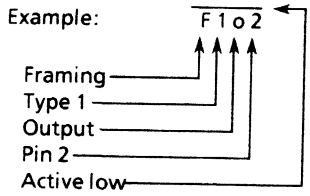
1) First Letter
F - denotes a framing signal.

2) Framing Type Number
0,1,2,... - There is a variety of these signals, each with distinctive properties, conforming to no simple pattern.

3) I/O Type
i - Input.
o - Output.
b - Bidirectional.

4) Optional Suffix
d - Delayed

5) Pin Number
0,1,2,... - distinguishes between different device ports for similar signals.



7.3 ST-BUS Streams

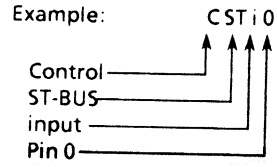
Some examples of ST-BUS stream names are STi0, STo1, CSTo, etc. The meaning of each letter or digit in the name is as follows:

1) Optional Prefix
C - control.
D - data or PCM encoded voice.
NB: No prefix if stream function not pre-assigned.

2) Type Letters
ST - denotes ST-BUS information stream.

3) I/O Type
i - Input.
o - Output.
b - Bidirectional.

4) Pin Number
0,1,2 - distinguishes between different logical ports for similar signals.



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